Integrated Circuit Systems, Inc.

# ICS843-75
## 75MHz, LVCMOS, LVPECL
## DUAL OUTPUT OSCILLATOR

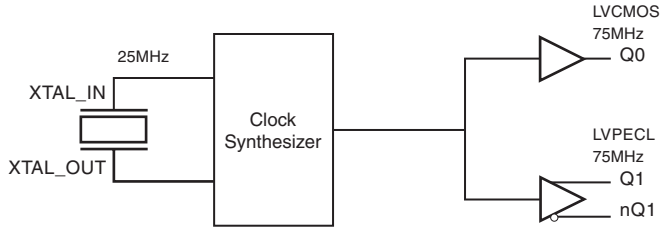
## GENERAL DESCRIPTION

The ICS843-75 is a SAS/SATA Dual Output Oscillator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS843-75 uses a 25MHz crystal to synthesize 75MHz. The ICS843-75 has excellent jitter performance. The ICS843-75 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

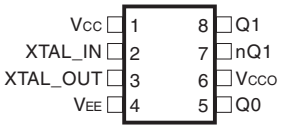
## FEATURES

- One LVCMOS/LVTTL output, 15Ω output impedence
  One LVPECL output pair
- Crystal oscillator interface designed for 25MHz, 18pF parallel resonant crystal
- Output frequency: 75MHz
- Random jitter: 3.07ps (maximum)
- Deterministic jitter: 0.13ps (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

## BLOCK DIAGRAM




## PIN ASSIGNMENT




**ICS843-75**
**8-Lead TSSOP**
4.40mm x 3.0mm x 0.925mm package body
**G Package**
Top View

**ICS843-75**
**8-Lead SOIC**
3.90mm x 4.92mm x 1.37mm body package
**M Package**
Top View

**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | $V_{CC}$ | Power | | Positive supply pin. |
| 2, 3 | XTAL_IN, XTAL_OUT | Input | | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. |
| 4 | $V_{EE}$ | Power | | Negative supply pin. |
| 5 | Q0 | Output | | Single-ended clock output. LVCMOS/LVTTL interface levels. 15Ω output impedence. |
| 6 | $V_{CCO}$ | Power | | Output supply pin. |
| 7, 8 | nQ1, Q1 | Output | | Differential LVPECL output pair. |

**TABLE 2. PIN CHARACTERISTICS**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | | 4 | | pF |
| $R_{OUT}$ | Output Impedance | Q0 | | | 15 | | Ω |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5 V |
| Outputs, $V_O$ (LVCMOS) | -0.5V to $V_{CCO}$ + 0.5V |
| Outputs, $I_O$ (LVPECL) | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, $\theta_{JA}$ | |
| 8 Lead TSSOP | 101.7°C/W (0 mps) |
| 8 Lead SOIC | 112.7°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,** $V_{CC} = V_{CCO} = 3.3V \pm 0.3V$, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Positive Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{CCO}$ | Output Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| $I_{EE}$ | Power Supply Current | | | | 110 | mA |
| $I_{CC}$ | Power Supply Current | | | | 100 | mA |
| $I_{CCO}$ | Output Supply Current | | | | 12 | mA |

**TABLE 3B. LVCMOS/LVTTL DC CHARACTERISTICS,** $V_{CC} = V_{CCO} = 3.3V \pm 0.3V$, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | 2.6 | | | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | | | 0.5 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO}/2$. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit".

**TABLE 3C. LVPECL DC CHARACTERISTICS,** $V_{CC} = V_{CCO} = 3.3V \pm 0.3V$, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CCO}$ - 1.4 | | $V_{CCO}$ - 0.9 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CCO}$ - 2.0 | | $V_{CCO}$ - 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO}$ - 2V.

**TABLE 4. CRYSTAL CHARACTERISTICS (NOTE 1)**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | | Fundamental | | |
| Frequency | | | 25 | | MHz |
| Frequency Tolerance | | | ±30 | | ppm |
| Frequency Stability Over Operating Temperature Range | | | ±30 | | ppm |
| Load Capacitance ($C_L$); NOTE 2 | | | 18 | | pF |
| Aging for 10 Years | | | ±15 | | ppm |
| Drive Level | | | | 1 | mW |

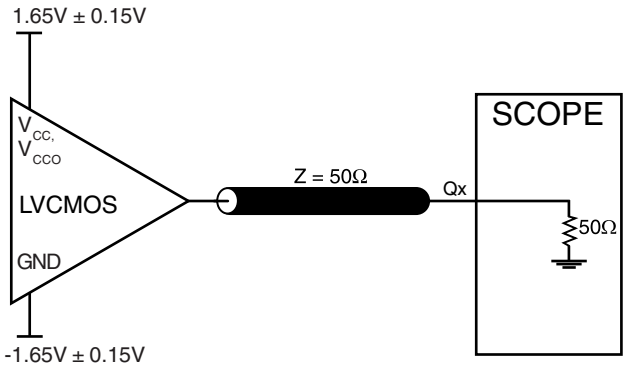
NOTE 1: Using an HC49/US SMD package, the parameters shown above target ±100ppm accuracy.
NOTE 2: See *Crystal Input Interface* in the Application Information Section.

**TABLE 5. AC CHARACTERISTICS,** $V_{CC} = V_{CCO} = 3.3V \pm 0.3V$, $T_A = 0°C$ TO $70°C$

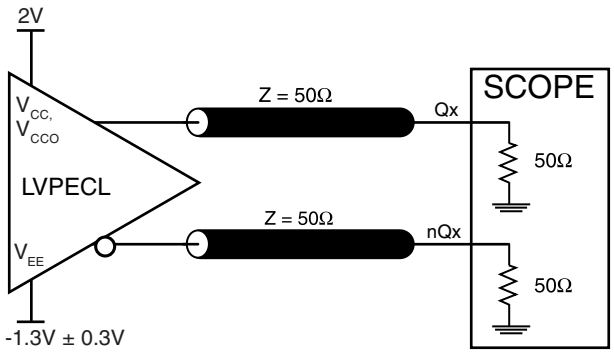
| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | | | | 75 | | MHz |
| $t_{DJ}$ | Deterministic Jitter; NOTE 1 | | | | | 0.13 | ps |
| $t_{RJ}$ | Random Jitter; NOTE 1 | | | | | 3.07 | ps |
| $t_{RMS}$ | RMS of Total Distribution (σ); NOTE 2 | | | | | 3.08 | ps |
| $t_{p-p}$ | Peak-to-Peak Jitter; NOTE 1 | | | | | 25 | ps |
| $t_{OSC}$ | Oscillation Start Up Time | | | | | 10 | ms |
| $t_R$ / $t_F$ | Output Rise/Fall Time | Q0 | 20% to 80% | 100 | | 500 | ps |
| | | Q1/nQ1 | | 250 | | 800 | ps |
| odc | Output Duty Cycle | Q0 | | 48 | | 52 | % |
| | | Q1, nQ1 | | 49 | | 51 | % |

NOTE 1: Measured using Wavecrest SIA-3000.
NOTE 2: Measured using Wavecrest SIA-3000, Tj @ 10e-12BER result divided by 14.

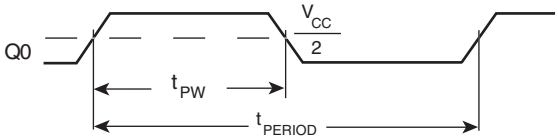
# PARAMETER MEASUREMENT INFORMATION




**3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT**

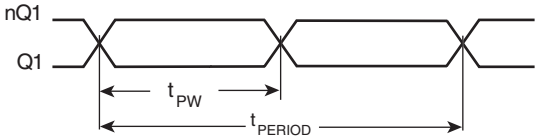



**3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT**



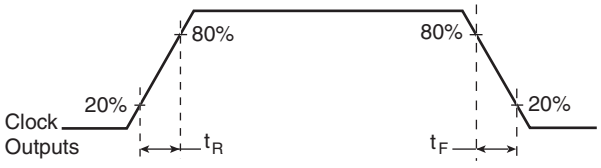

$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

**LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

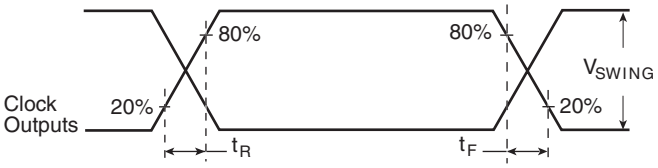



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

**LVPECL OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**




**LVCMOS OUTPUT RISE/FALL TIME**




**LVPECL OUTPUT RISE/FALL TIME**

# APPLICATION INFORMATION

## RECOMMENDATIONS FOR UNUSED OUTPUT PINS

**LVCMOS OUTPUT:**
An unused LVCMOS output should be terminated with 100Ω to ground as close as possible to the device.

**LVPECL OUTPUT**
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## CRYSTAL INPUT INTERFACE

The ICS843-75 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

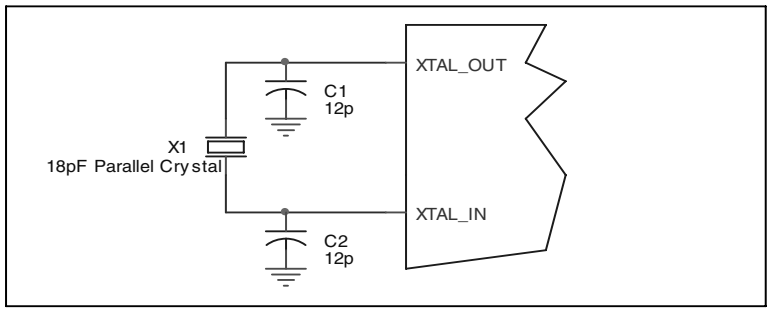



**Figure 1. CRYSTAL INPUT INTERFACE**

## FREQUENCY STABILITY

The table shown below provides a basic guideline in selecting the proper quartz crystal that meets a timing budget of ±100ppm. For more information on selecting the proper crystal, see the application note, *Crystal Timing Budget and Accuracy for FemtoClock™* .

| Parameter | Typical | Units |
|---|---|---|
| Frequency Tolerance | ±30 | ppm |
| Frequency Stability | ±30 | ppm |
| Aging for 10 Years | ±15 | ppm |
| Accuracy of ICS Oscillator | ±10 | ppm |
| Load Capacitance Accuracy | ±3 | ppm |
| **Total Overall Timing Error** | ±88 | ppm |

## TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines.Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

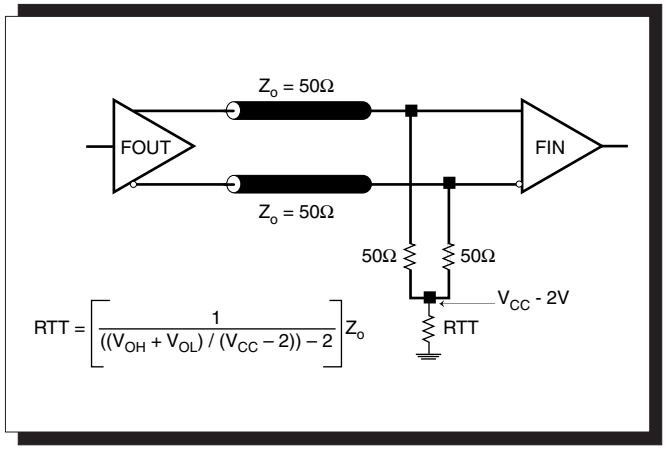



FIGURE 2A. LVPECL OUTPUT TERMINATION

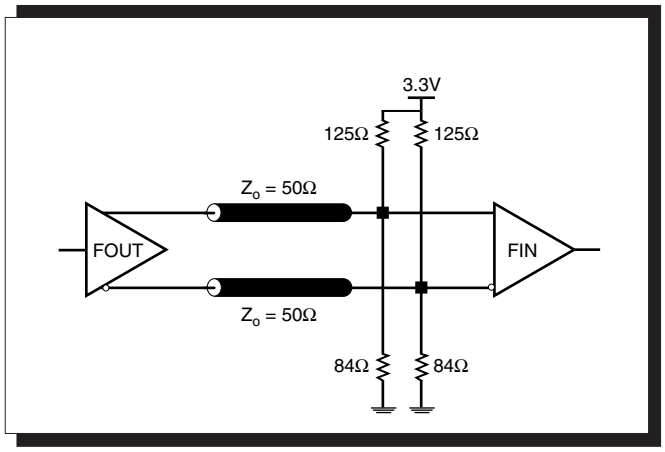



FIGURE 2B. LVPECL OUTPUT TERMINATION

# POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843-75. Equations and example calculations are also provided.

*1. Power Dissipation.*
The total power dissipation for the ICS843-75 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC}$ = 3.3V + 0.3V = 3.6V, which gives worst case results.
**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = $V_{CC_MAX}$ * $I_{EE_MAX}$ = 3.6V * 110mA = **396mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

**Total Power$_{_MAX}$** (3.465V, with all outputs switching) = 396mW + 30mW = **426mW**

*2. Junction Temperature.*
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 6A below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.426W * 90.5°C/W = 108.6°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6A. THERMAL RESISTANCE $\theta_{JA}$ FOR 8-PIN TSSOP, FORCED CONVECTION**

| $\theta_{JA}$ by Velocity (Meters per Second) | 0 | 1 | 2.5 |
|---|---|---|---|
| Multi-Layer PCB, JEDEC Standard Test Boards | 101.7°C/W | 90.5°C/W | 89.8°C/W |

**TABLE 6B. THERMAL RESISTANCE $\theta_{JA}$ FOR 8 LEAD SOIC FORCED CONVECTION**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | 0 | 200 | 500 |
|---|---|---|---|
| Single-Layer PCB, JEDEC Standard Test Boards | 153.3°C/W | 128.5°C/W | 115.5°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 112.7°C/W | 103.3°C/W | 97.1°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

*3. Calculations and Equations.*
The purpose of this section is to derive the power dissipated into the load.
LVPECL output driver circuit and termination are shown in *Figure 3.*

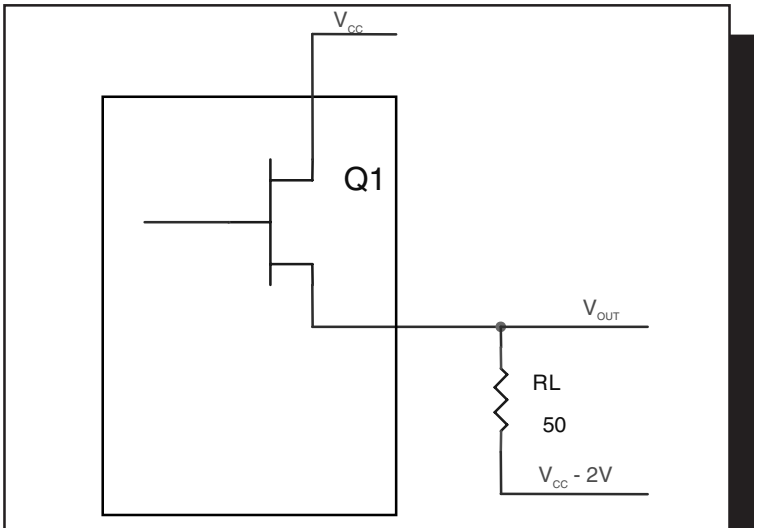



**FIGURE 3. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination
voltage of $V_{CC}$ - 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CC_MAX} – 0.9V}$

  $(V_{CCO_MAX} - V_{OH_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CC_MAX} – 1.7V}$

  $(V_{CCO_MAX} - V_{OL_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd_L = [(V_{OL_MAX} – (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

# RELIABILITY INFORMATION

**TABLE 7A. $\theta_{JA}$ VS. AIR FLOW TABLE FOR 8 LEAD TSSOP**

| $\theta_{JA}$ by Velocity (Meters per Second) | | | |
|---|---|---|---|
| | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 101.7°C/W | 90.5°C/W | 89.8°C/W |

**TABLE 7B. $\theta_{JA}$ VS. AIR FLOW TABLE 8 LEAD SOIC**

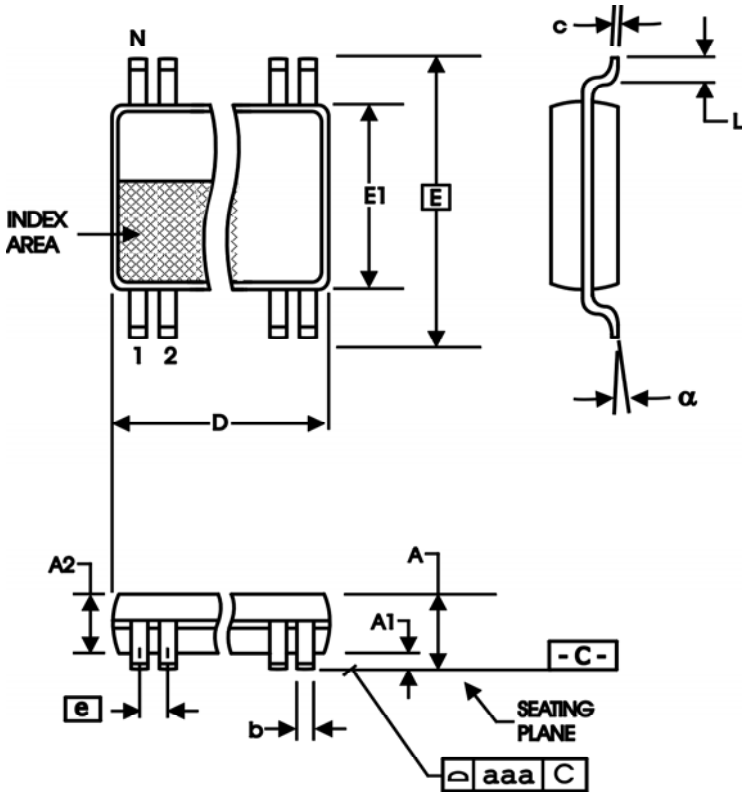
| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 153.3°C/W | 128.5°C/W | 115.5°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 112.7°C/W | 103.3°C/W | 97.1°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

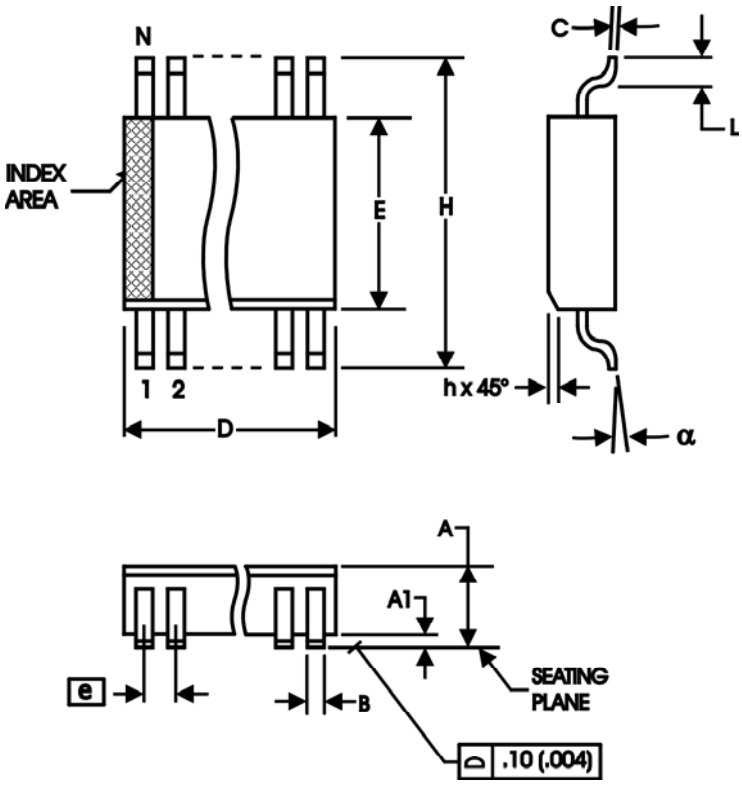
### TRANSISTOR COUNT

The transistor count for ICS843-75 is: 2376

## PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP




## PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC




### TABLE 8A. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|---|---|---|
| | Minimum | Maximum |
| N | 8 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 2.90 | 3.10 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

### TABLE 8B. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|---|---|---|
| | MINIMUM | MAXIMUM |
| N | 8 | |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BASIC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| α | 0° | 8° |

Reference Document: JEDEC Publication 95, MS-012

**TABLE 9. ORDERING INFORMATION**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| ICS843AG-75 | 43A75 | 8 lead TSSOP | tube | 0°C to 70°C |
| ICS843AG-75T | 43A75 | 8 lead TSSOP | 2500 tape & reel | 0°C to 70°C |
| ICS843AG-75LF | TBD | 8 lead "Lead-Free" TSSOP | tube | 0°C to 70°C |
| ICS843AG-75LFT | TBD | 8 lead "Lead-Free" TSSOP | 2500 tape & reel | 0°C to 70°C |
| ICS843AM-75 | TBD | 8 lead SOIC | tube | 0°C to 70°C |
| ICS843AM-75T | TBD | 8 lead SOIC | 2500 tape & reel | 0°C to 70°C |
| ICS843AM-75LF | TBD | 8 lead "Lead-Free" SOIC | tube | 0°C to 70°C |
| ICS843AM-75LFT | TBD | 8 lead "Lead-Free" SOIC | 2500 tape & reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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