3.3-V FULL-DUPLEX RS-485 DRIVERS AND RECEIVERS

Check for Samples: SN65HVD30-EP, SN65HVD31-EP, SN65HVD32-EP, SN65HVD33-EP, SN65HVD34-EP, SN65HVD35-EP

FEATURES

- **1/8 Unit-Load Option Available (up to 256 Nodes on the Bus)**
- **Bus-Pin ESD Protection Exceeds 15-kV HBM**
- **Optional Driver Output Transition Times for Signaling Rates (1) of 1 Mbps, 5 Mbps, and 25 Mbps**
- **Low-Current Standby Mode: <1 μA**
- **Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications**
- **5-V-Tolerant Inputs**
- **Bus Idle, Open, and Short-Circuit Fail Safe**
- **Driver Current Limiting and Thermal Shutdown**
- **Meet or Exceed the Requirements of ANSI TIA/EIA-485-A and RS-422 Compatible**

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

APPLICATIONS

- **Utility Meters**
- **DTE/DCE Interfaces**
- **Industrial, Process, and Building Automation**
- **Point-of-Sale (POS) Terminals and Networks**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

DESCRIPTION

The SN65HVD3x devices are 3-state differential line drivers and differential-input line receivers that operate with 3.3-V power supply.

Each driver and receiver has separate input and output pins for full-duplex bus communication designs. They are designed for balanced transmission lines and interoperation with ANSI TIA/EIA-485A, TIA/EIA-422-B, ITU-T v.11, and ISO 8482:1993 standard-compliant devices.

The SN65HVD30, SN65HVD31, and SN65HVD32 are fully enabled with no external enabling pins.

The SN65HVD33, SN65HVD34, and SN65HVD35 have active-high driver enables and active-low receiver enables. A low (less than 1 μA) standby current can be achieved by disabling both the driver and receiver.

All devices are characterized for operation from –55°C to 125°C.

IMPROVED REPLACEMENT FOR:

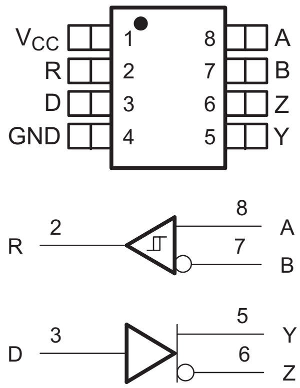
Part Number	Replace With	
xxx3491 xxx3490	SN65HVD33: SN65HVD30:	Better ESD protection (15 kV vs 2 kV or not specified), higher signaling rate (25 Mbps vs 20 Mbps), fractional unit load (64 nodes vs 32)
MAX3491E MAX3490E	SN65HVD33: SN65HVD30:	Higher signaling rate (25 Mbps vs 12 Mbps), fractional unit load (64 nodes vs 32)
MAX3076E MAX3077E	SN65HVD33: SN65HVD30:	Higher signaling rate (25 Mbps vs 16 Mbps), lower standby current (1 μA vs 10 μA)
MAX3073E MAX3074E	SN65HVD34: SN65HVD31:	Higher signaling rate (5 Mbps vs 500 kbps), lower standby current (1 μA vs 10 μA)
MAX3070E MAX3071E	SN65HVD35: SN65HVD32:	Higher signaling rate (1 Mbps vs 250 kbps), lower standby current (1 μA vs 10 μA)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

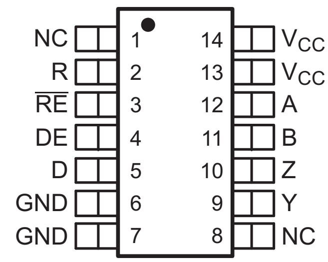
SN65HVD30, SN65HVD31, SN65HVD32

D PACKAGE
(TOP VIEW)

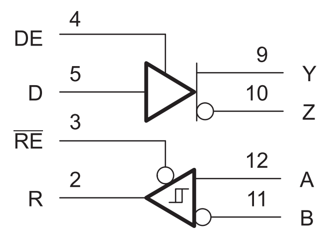


SN65HVD33, SN65HVD34, SN65HVD35

D PACKAGE
(TOP VIEW)



NC - No internal connection



AVAILABLE OPTIONS[1]

BASE PART NUMBER	SIGNALING RATE	UNIT LOADS	RECEIVER EQUALIZATION	ENABLES	SOIC MARKING
SN65HVD30MDREP	25 Mbps	1/2	No	No	HVD30EP
SN65HVD31MDREP[2]	5 Mbps	1/8	No	No	PREVIEW
SN65HVD32MDREP[2]	1 Mbps	1/8	No	No	PREVIEW
SN65HVD33MDREP	25 Mbps	1/2	No	Yes	HVD33EP
SN65HVD34MDREP[2]	5 Mbps	1/8	No	Yes	PREVIEW
SN65HVD35MDREP[2]	1 Mbps	1/8	No	Yes	PREVIEW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Product Preview

Absolute Maximum Ratings[1] [2]

over operating free-air temperature range (unless otherwise noted)

		UNIT
V_{CC}	Supply voltage range	–0.3 V to 6 V
$V_{(A)}$, $V_{(B)}$, $V_{(Y)}$, $V_{(Z)}$	Voltage range at any bus terminal (A, B, Y, Z)	–9 V to 14 V
$V_{(TRANS)}$	Voltage input, transient pulse through 100 Ω (see Figure 12) (A, B, Y, Z)[3]	–50 V to 50 V
V_I	Input voltage range (D, DE, $\overline{RE}$)	–0.5 V to 7 V
$P_{D(cont)}$	Continuous total power dissipation	Internally limited[4]
I_O	Output current (receiver output only, R)	11 mA
T_J	Junction temperature	165°C
T_{STG}	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) This tests survivability only and the output state of the receiver is not specified.
(4) The thermal shutdown protection circuit internally limits the continuous total power dissipation. Thermal shutdown typically occurs when the junction temperature reaches 165°C.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		3.6	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–7[1]		12	V
$1/t_{UI}$	Signaling rate	'HVD30, 'HVD33			25	Mbps
		'HVD31, 'HVD34			5	
		'HVD32, 'HVD35			1	
R_L	Differential load resistance		54	60		Ω
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_{OH}	High-level output current	Driver	–60			mA
		Receiver	–8			
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Ambient still-air temperature		–55		125[2]	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
(2) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

Electrostatic Discharge Protection

PARAMETER	TEST CONDITIONS	TYP[1]	UNIT
Human-Body Model	Bus terminals and GND	±16	kV
Human-Body Model[2]	All pins	±4	
Charged-Device Model[3]	All pins	±1	

(1) All typical values at 25°C with 3.3-V supply
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A
(3) Tested in accordance with JEDEC Standard 22, Test Method C101

Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$V_{I(K)}$	Input clamp voltage		I_I = –18 mA		–1.5			V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage		I_O = 0		2.3		V_{CC} + 0.1	V
			R_L = 54 Ω, See Figure 1 (RS-485)		1.5	2		
			R_L = 100 Ω, See Figure 1 (RS-422)		2	2.3		
			V_{test} = –7 V to 12 V, See Figure 2		1.5			
$\Delta\|V_{OD(SS)}\|$	Change in magnitude of steady-state differential output voltage between states		R_L = 54 Ω, See Figure 1 and Figure 2		–0.2		0.2	V
$V_{OD(RING)}$	Differential output voltage overshoot and undershoot		R_L = 54 Ω, C_L = 50 pF, See Figure 5 and Figure 3				10%(2)	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	'HVD30, 'HVD33	See Figure 4			0.5		V
		'HVD31, 'HVD32, 'HVD34, 'HVD35				0.25		
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 4		1.6		2.3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		See Figure 4		–0.05		0.05	V
$I_{Z(Z)}$ or $I_{Y(Z)}$	High-impedance state output current	'HVD30, 'HVD31, 'HVD32	V_{CC} = 0 V, V_Z or V_Y = 12 V, Other input at 0 V				90	μA
			V_{CC} = 0 V, V_Z or V_Y = –7 V, Other input at 0 V		–10			
		'HVD33, 'HVD34, 'HVD35	V_{CC} = 3 V or 0 V, DE = 0 V, V_Z or V_Y = 12 V	Other input at 0 V			90	
			V_{CC} = 3 V or 0 V, DE = 0 V, V_Z or V_Y = –7 V		–10			
$I_{Z(S)}$ or $I_{Y(S)}$	Short-circuit output current		V_Z or V_Y = –7 V	Other input at 0 V		±250		mA
			V_Z or V_Y = 12 V					
I_I	Input current	D, DE			0		100	μA
$C_{(OD)}$	Differential output capacitance		V_{OD} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			16		pF

(1) All typical values at 25°C with 3.3-V supply
(2) 10% of the peak-to-peak differential output voltage swing, per TIA/EIA-485

Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	'HVD30, 'HVD33	R_L = 54 Ω, C_L = 50 pF, See Figure 5	4	10	23	ns
		'HVD31, 'HVD34		25	38	65	
		'HVD32, 'HVD35		120	175	305	
t_{PHL}	Propagation delay time, high- to low-level output	'HVD30, 'HVD33		4	9	23	ns
		'HVD31, 'HVD34		25	38	65	
		'HVD32, 'HVD35		120	175	305	
t_r	Differential output signal rise time	'HVD30, 'HVD33		2.5	5	18	ns
		'HVD31, 'HVD34		20	37	60	
		'HVD32, 'HVD35		120	185	300	
t_f	Differential output signal fall time	'HVD30, 'HVD33		2.5	5	18	ns
		'HVD31, 'HVD34		20	35	60	
		'HVD32, 'HVD35		120	180	300	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	'HVD30, 'HVD33			0.6		ns
		'HVD31, 'HVD34			2.0		
		'HVD32, 'HVD35			5.1		
t_{PZH1}	Propagation delay time, high-impedance to high-level output	'HVD33	R_L = 110 Ω, $\overline{RE}$ at 0 V, D = 3 V and S1 = Y, or D = 0 V and S1 = Z, See Figure 6			45	ns
		'HVD34				235	
		'HVD35				490	
t_{PHZ}	Propagation delay time, high-level to high-impedance output	'HVD33				25	ns
		'HVD34				65	
		'HVD35				165	
t_{PZL1}	Propagation delay time, high-impedance to low-level output	'HVD33	R_L = 110 Ω, $\overline{RE}$ at 0 V, D = 3 V and S1 = Z, or D = 0 V and S1 = Y, See Figure 7			35	ns
		'HVD34				190	
		'HVD35				490	
t_{PLZ}	Propagation delay time, low-level to high-impedance output	'HVD33				30	ns
		'HVD34				120	
		'HVD35				290	
t_{PZH2}	Propagation delay time, standby to high-level output	'HVD30	R_L = 110 Ω, $\overline{RE}$ at 3 V, D = 3 V and S1 = Y, or D = 0 V and S1 = Z, See Figure 6			4000	ns
		'HVD33				5000	
t_{PZL2}	Propagation delay time, standby to low-level output	'HVD30	R_L = 110 Ω, $\overline{RE}$ at 3 V, D = 3 V and S1 = Z, or D = 0 V and S1 = Y, See Figure 7			4000	ns
		'HVD33				5000	

(1) All typical values at 25°C with 3.3-V supply

Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage		I_O = –8 mA				–0.02	V
V_{IT-}	Negative-going differential input threshold voltage	'HVD30	I_O = 8 mA		–0.15			V
		'HVD33			-0.2			
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})					50		mV
V_{IK}	Enable-input clamp voltage		I_I = –18 mA		–1.5			V
V_O	Output voltage		V_{ID} = 200 mV, I_O = –8 mA, See Figure 8		2.4			V
			V_{ID} = –200 mV, I_O = 8 mA, See Figure 8				0.4	
$I_{O(Z)}$	High-impedance-state output current		V_O = 0 or V_{CC}, $\overline{RE}$ at V_{CC}		–1		1	µA
I_A or I_B	Bus input current	'HVD31, 'HVD32, 'HVD34, 'HVD35	V_A or V_B = 12 V	Other input at 0 V		0.05	0.1	mA
			V_A or V_B = 12 V, V_{CC} = 0 V			0.06	0.1	
			V_A or V_B = –7 V		–0.10	–0.04		
			V_A or V_B = –7 V, V_{CC} = 0 V		–0.10	–0.03		
		'HVD30, 'HVD33	V_A or V_B = 12 V	Other input at 0 V		0.20	0.35	
			V_A or V_B = 12 V, V_{CC} = 0 V			0.24	0.4	
			V_A or V_B = –7 V		–0.35	–0.18		
			V_A or V_B = –7 V, V_{CC} = 0 V		–0.25	–0.13		
I_{IH}	Input current, $\overline{RE}$		V_{IH} = 0.8 V or 2 V		–60			µA
C_{ID}	Differential input capacitance		V_{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			15		pF
Supply Current								
I_{CC}	Supply current	'HVD30	D at 0 V or V_{CC} and no load				2.1	mA
		'HVD31, 'HVD32					6.4	
		'HVD33	$\overline{RE}$ at 0 V, D at 0 V or V_{CC}, DE at 0 V, No load (receiver enabled and driver disabled)				1.8	
		'HVD34, 'HVD35					2.2	
		'HVD33, 'HVD34, 'HVD35	$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, No load (receiver disabled and driver disabled)			0.022	1.5	µA
		'HVD33	$\overline{RE}$ at 0 V, D at 0 V or V_{CC}, DE at V_{CC}, No load (receiver enabled and driver enabled)				2.1	mA
		'HVD34, 'HVD35					6.5	
		'HVD33	$\overline{RE}$ at V_{CC}, D at 0 V or V_{CC}, DE at V_{CC} No load (receiver disabled and driver enabled)				1.8	
		'HVD34, 'HVD35					6.2	

(1) All typical values at 25°C with 3.3-V supply

Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	'HVD30, 'HVD33	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF, See Figure 9		26	60	ns
		'HVD31, 'HVD32, 'HVD34, 'HVD35			47	70	
t_{PHL}	Propagation delay time, high- to low-level output	'HVD30, 'HVD33			29	60	ns
		'HVD31, 'HVD32, 'HVD34, 'HVD35			49	70	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)	'HVD30, 'HVD33				12	ns
		'HVD31, 'HVD34, 'HVD32, 'HVD35				10	
t_r	Output signal rise time	'HVD30				10	ns
		'HVD33				18	
t_f	Output signal fall time					12.5	ns

(1) All typical values 25°C with 3.3-V supply

Receiver Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PHZ}	Output disable time from high level		DE at 3 V	C_L = 15 pF, See Figure 10			20	ns
t_{PZH1}	Output enable time to high level						20	ns
t_{PZH2}	Propagation delay time, standby to high-level output	'HVD30	DE at 0 V				4000	ns
		'HVD33					5000	
t_{PLZ}	Output disable time from low level		DE at 3 V	C_L = 15 pF, See Figure 11			20	ns
t_{PZL1}	Output enable time to low level						20	ns
t_{PZL2}	Propagation delay time, standby to low-level output	'HVD30	DE at 0 V				4000	ns
		'HVD33					5000	

Receiver Equalization Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			DEVICE	MIN TYP(1) MAX	UNIT
$t_{j(pp)}$	Peak-to-peak eye-pattern jitter	Pseudo-random NRZ code with a bit pattern length of 2^{16} – 1, Belden 3105A cable	25 Mbps	100 m	'HVD33(2)	PREVIEW	ns
				150 m	'HVD33(2)	PREVIEW	
				200 m	'HVD33(2)	PREVIEW	
			10 Mbps	200 m	'HVD33(2)	PREVIEW	
				250 m	'HVD33(2)	PREVIEW	
				300 m	'HVD33(2)	PREVIEW	
			5 Mbps	500 m	'HVD34(2)	PREVIEW	
			3 Mbps	500 m	'HVD33(2)	PREVIEW	
					'HVD34(2)	PREVIEW	
			1 Mbps	1000 m	'HVD34(2)	PREVIEW	

(1) All typical values are at V_{CC} = 5 V and temperature = 25°C.
(2) The SN65HVD33 and the SN65HVD34 do not have receiver equalization, but are specified for comparison.

Device Power Dissipation – P_D

DEVICE	TEST CONDITIONS	MIN	MAX	UNIT
'HVD30 (25 Mbps)	R_L = 60 Ω, C_L = 50 pF, Input to D a 50% duty cycle square wave at indicated signaling rate, T_A = 85°C		197	mW
'HVD31 (5 Mbps)			213	
'HVD32 (1 Mbps)			193	
'HVD33 (25 Mbps)	R_L = 60 Ω, C_L = 50 pF, DE at V_{CC}, $\overline{RE}$ at 0 V, Input to D a 50% duty cycle square wave at indicated signaling rate, T_A = 85°C		197	mW
'HVD34 (5 Mbps)			193	
'HVD35 (1 Mbps)			248	

PARAMETER MEASUREMENT INFORMATION

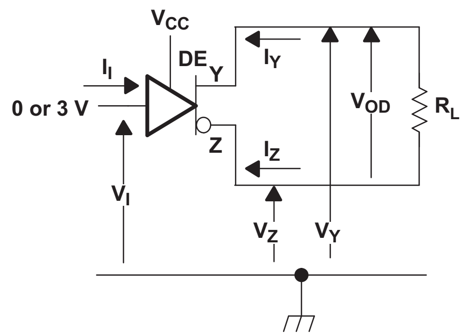


Figure 1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

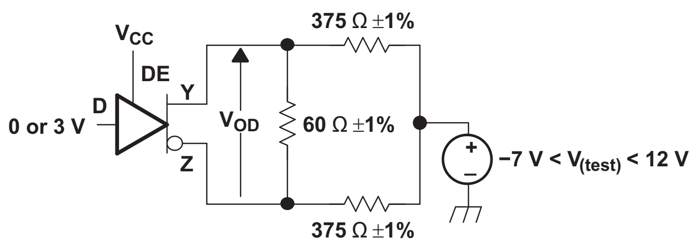


Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit

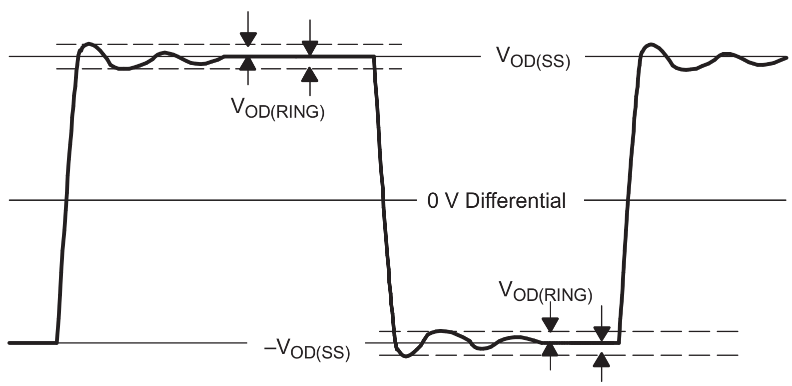
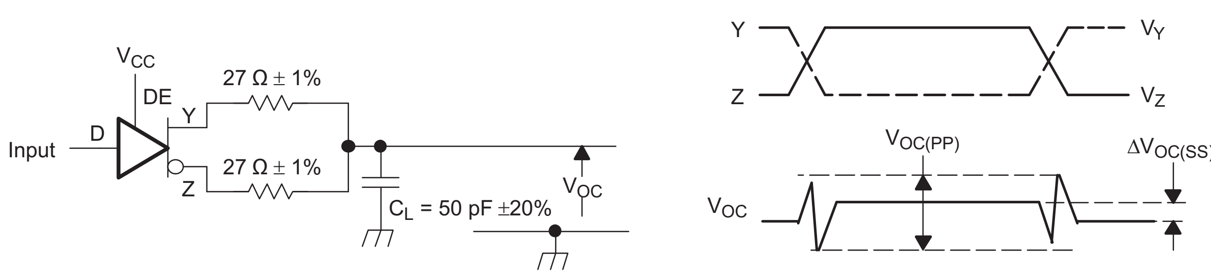


Figure 3. $V_{OD(RING)}$ Waveform and Definitions

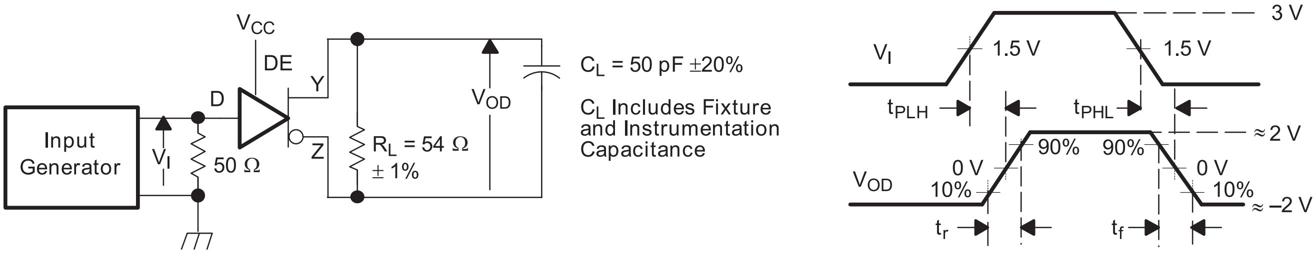
$V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.



Input: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

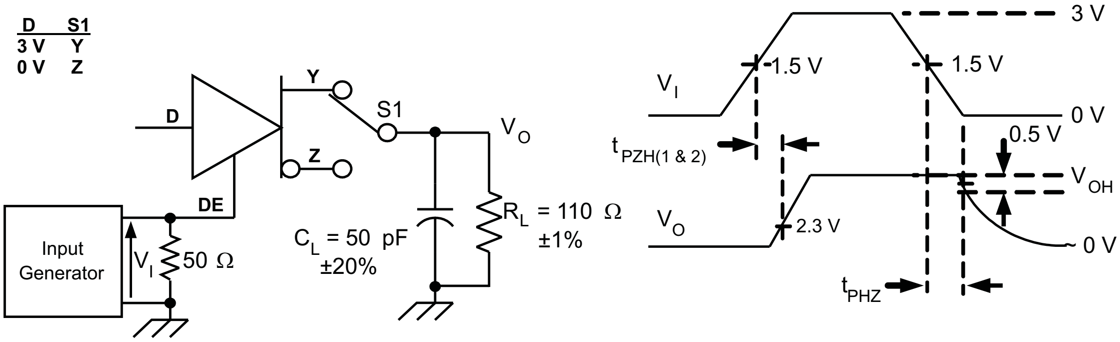
Figure 4. Test Circuit and Definitions for Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)



A. Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

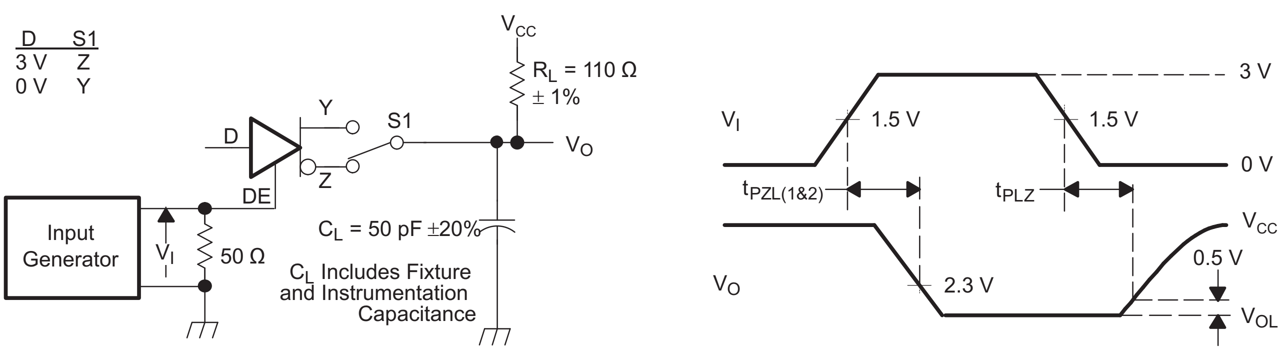
Figure 5. Driver Switching Test Circuit and Voltage Waveforms



A. Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

B. C_L Includes Fixture and Instrumentation Capacitance

Figure 6. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



A. Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

Figure 7. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

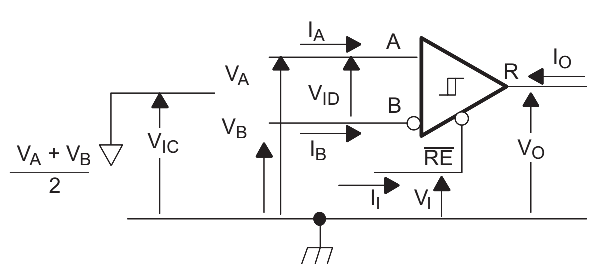
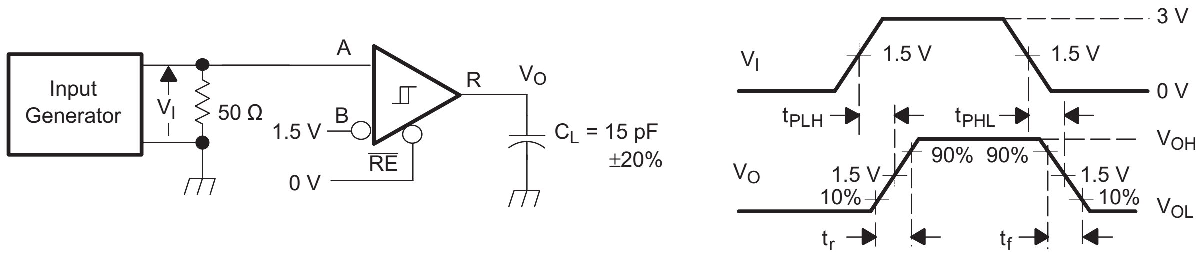


Figure 8. Receiver Voltage and Current Definitions

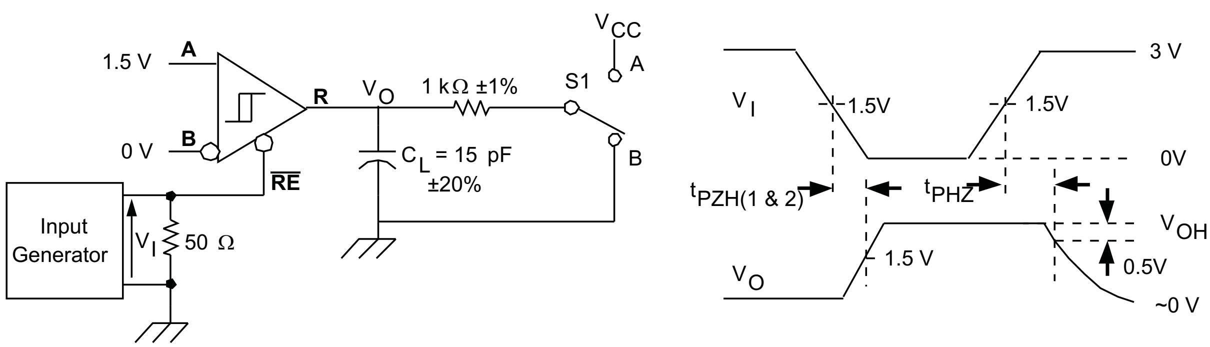
PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L Includes Fixture and Instrumentation Capacitance

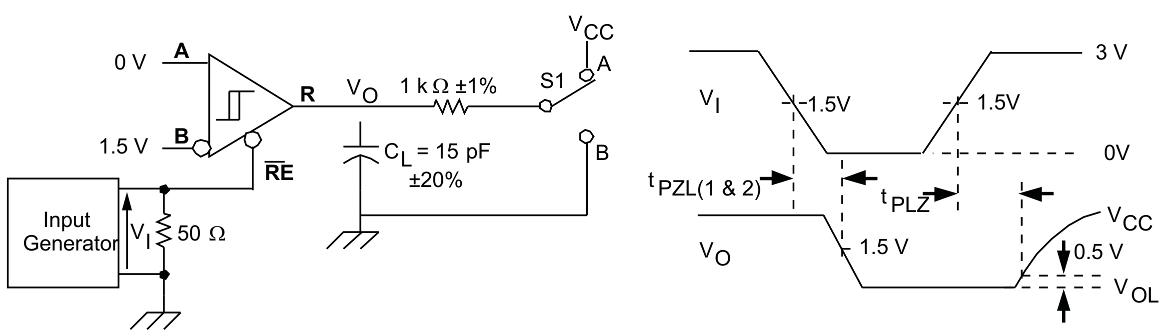
B. Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

Figure 9. Receiver Switching Test Circuit and Voltage Waveforms



A. Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

Figure 10. Receiver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



A. Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

Figure 11. Receiver Enable Time From Standby (Driver Disabled)

PARAMETER MEASUREMENT INFORMATION (continued)

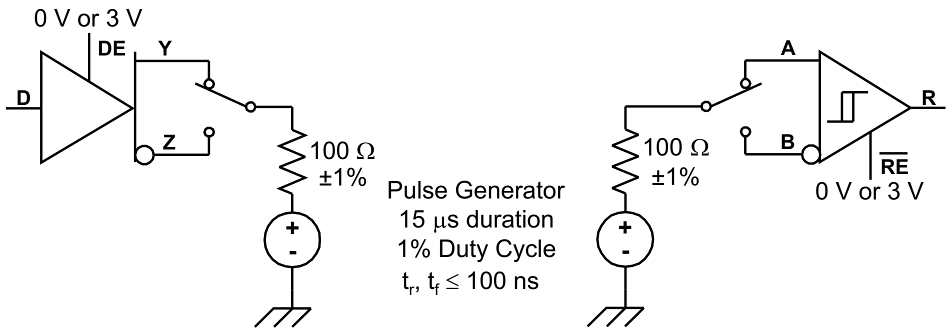


Figure 12. Test Circuit, Transient Over Voltage Test

DEVICE INFORMATION

Low-Power Standby Mode

When both the driver and receiver are disabled (DE low and $\overline{RE}$ high), the device is in standby mode. If the enable inputs are in this state for less than 60 ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

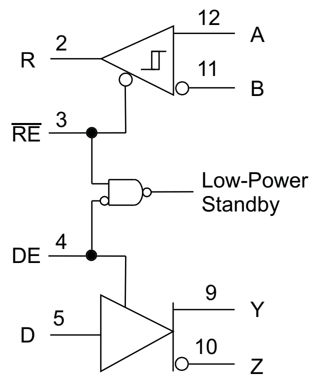


Figure 13. Low-Power Standby Logic Diagram

If only the driver is re-enabled (DE transitions to high), the driver outputs are driven according to the D input after the enable times given by t_{PZH2} and t_{PZL2} in the driver switching characteristics. If the D input is open when the driver is enabled, the driver outputs defaults to A high and B low, in accordance with the driver fail-safe feature.

If only the receiver is re-enabled ($\overline{RE}$ transitions to low), the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by t_{PZH2} and t_{PZL2} in the receiver switching characteristics. If there is no valid state on the bus, the receiver responds as described in the fail-safe operation section.

If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input. Note that the state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

FUNCTION TABLES

Table 1. SN65HVD33, SN65HVD34, SN65HVD35 DRIVER(1)

INPUTS		OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L or open	Z	Z
Open	H	L	H

(1) H = high level, L = low level, Z = high impedance, X = irrelevant

Table 2. SN65HVD33, SN65HVD34, SN65HVD35 RECEIVER(1)

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \leq -0.2$ V	L	L
-0.2 V < V_{ID} < -0.02 V	L	?
-0.02 V ≤ V_{ID}	L	H
X	H or open	Z
Open circuit	L	H
Idle circuit	L	H
Short circuit, $V_{(A)} = V_{(B)}$	L	H

(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

Table 3. SN65HVD30, SN65HVD31, SN65HVD32 DRIVER(1)

INPUT D	OUTPUTS	
	Y	Z
H	H	L
L	L	H
Open	L	H

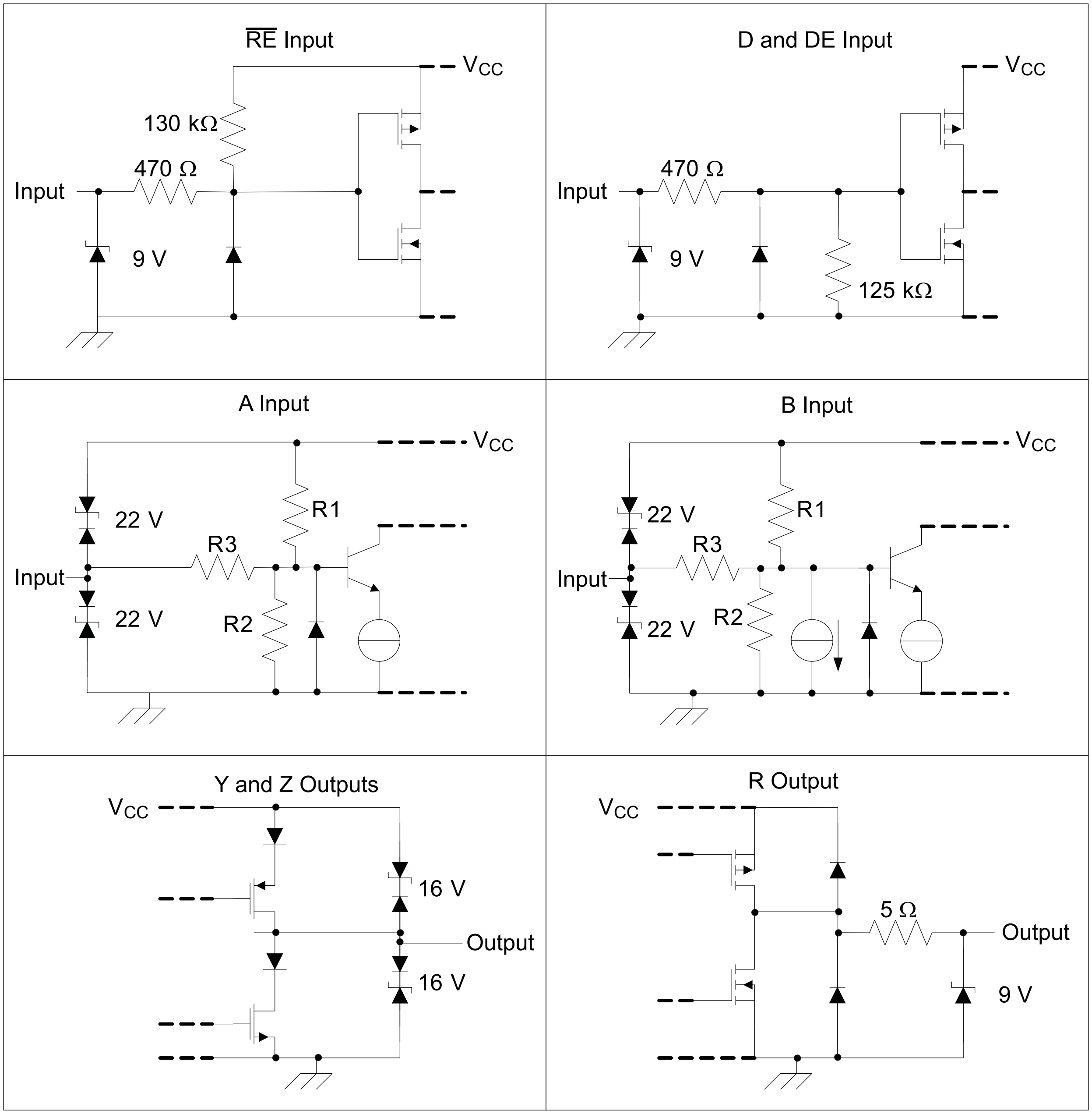
(1) H = high level, L = low level

Table 4. SN65HVD30, SN65HVD31, SN65HVD32 RECEIVER(1)

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	OUTPUT R
$V_{ID} \leq -0.15$ V	L
-0.15 V < V_{ID} < -0.02 V	?
-0.02 V ≤ V_{ID}	H
Open circuit	H
Idle circuit	H
Short circuit, $V_{(A)} = V_{(B)}$	H

(1) H = high level, L = low level, ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
SN65HVD30, SN65HVD33	9 kΩ	45 kΩ
SN65HVD31, SN65HVD32, SN65HVD34, SN65HVD35	36 kΩ	180 kΩ

TYPICAL CHARACTERISTICS

**'HVD30, 'HVD33
RMS SUPPLY CURRENT
vs
SIGNALING RATE**

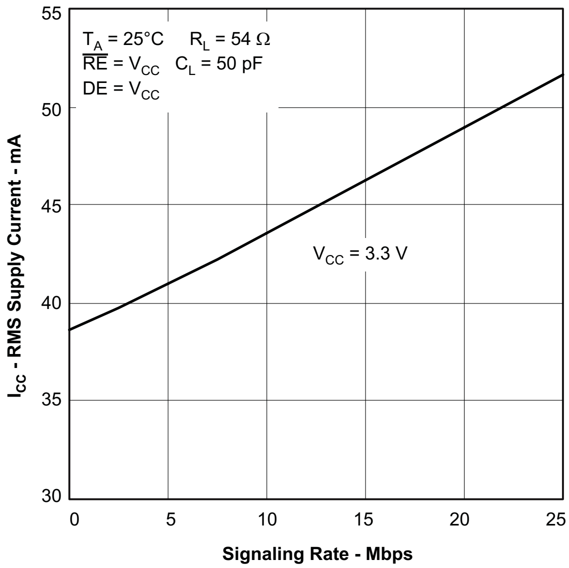


Figure 14.

**'HVD31, 'HVD34
RMS SUPPLY CURRENT
vs
SIGNALING RATE**

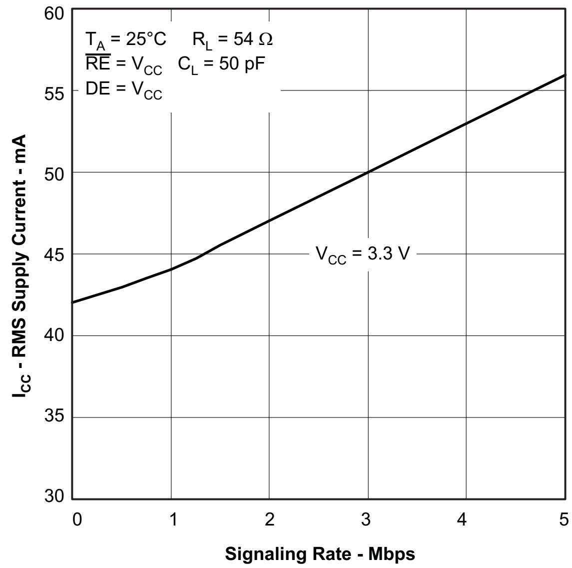


Figure 15.

**'HVD32, 'HVD35
RMS SUPPLY CURRENT
vs
SIGNALING RATE**

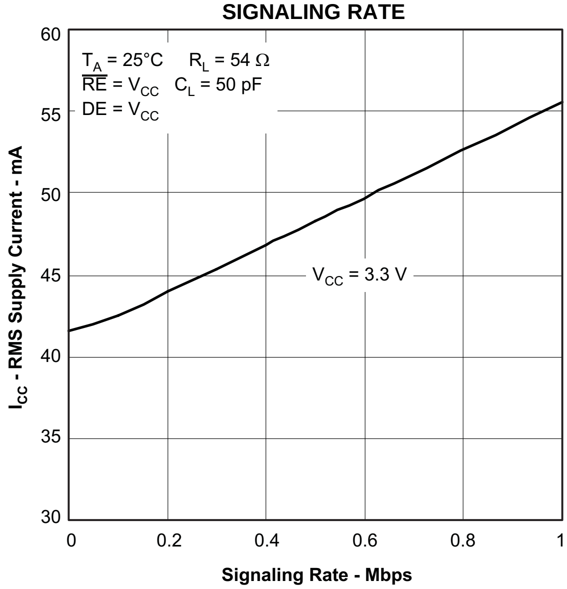


Figure 16.

TYPICAL CHARACTERISTICS (continued)

'HVD30, 'HVD33
BUS INPUT CURRENT
vs
INPUT VOLTAGE

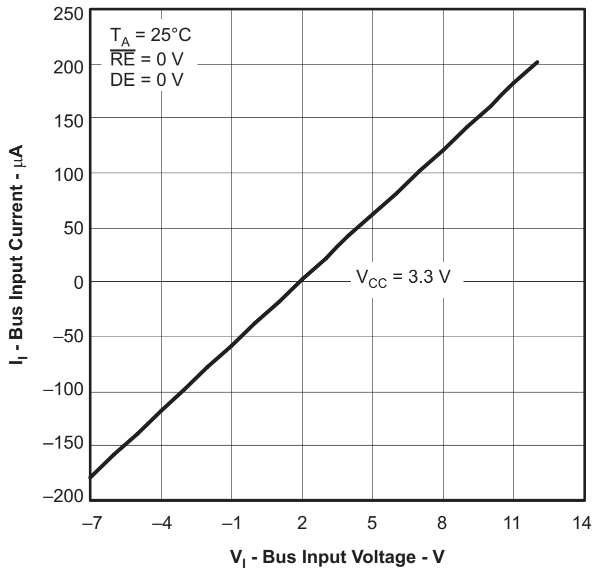


Figure 17.

'HVD31, 'HVD32, 'HVD34, 'HVD35
BUS INPUT CURRENT
vs
INPUT VOLTAGE

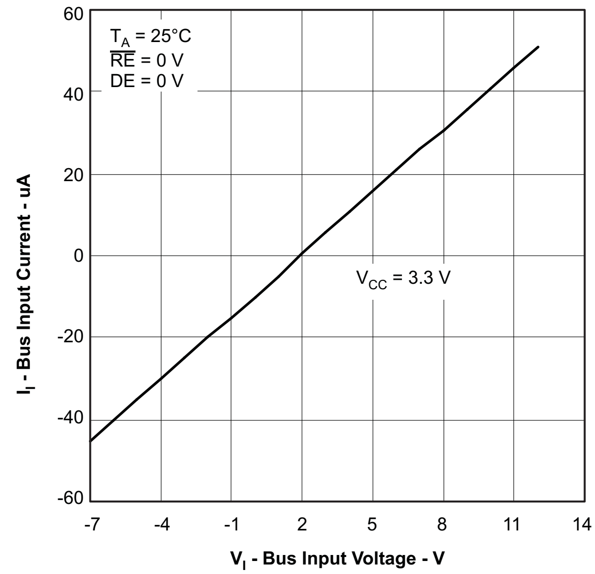


Figure 18.

DRIVER LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

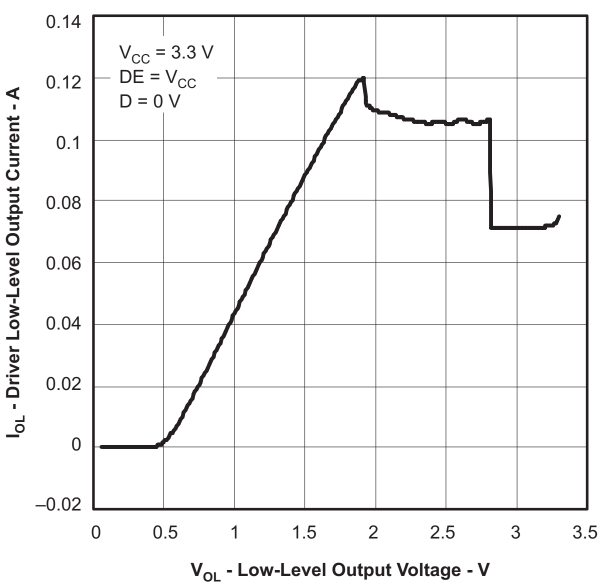


Figure 19.

DRIVER HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

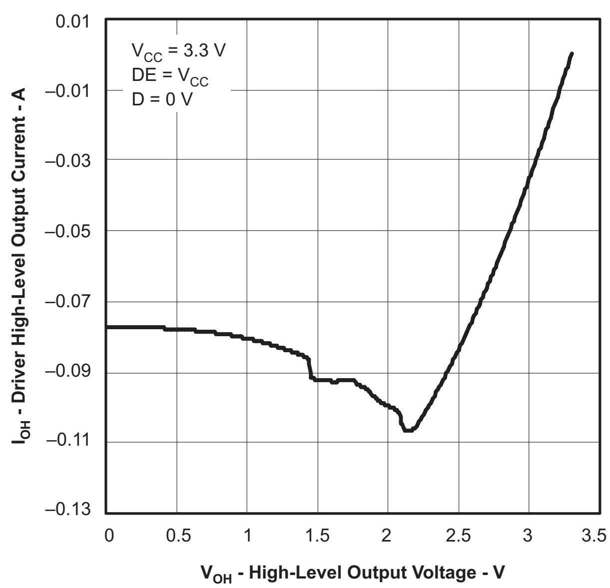


Figure 20.

TYPICAL CHARACTERISTICS (continued)

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

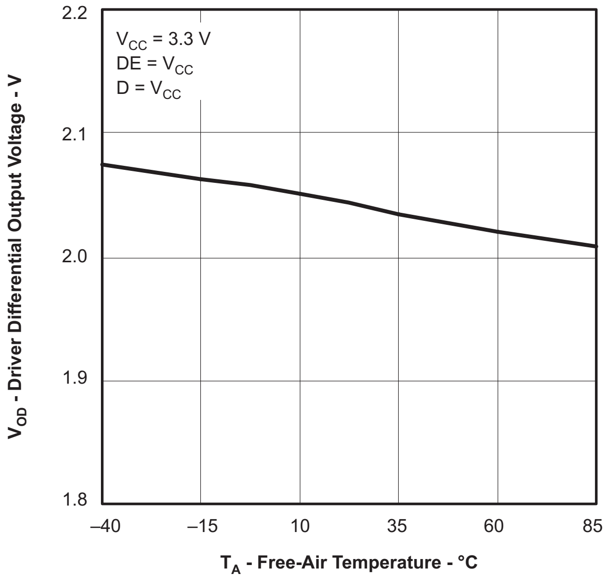


Figure 21.

DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE

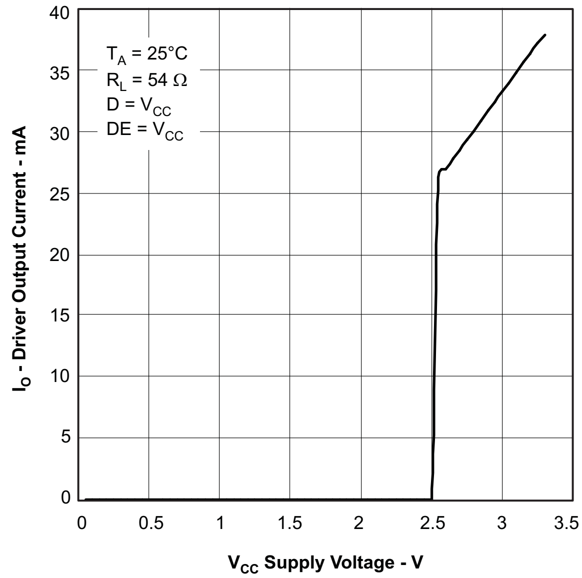


Figure 22.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN65HVD30MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD30MDREPG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD33MDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD33MDREPG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06634-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06634-04YE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN65HVD30-EP, SN65HVD33-EP :

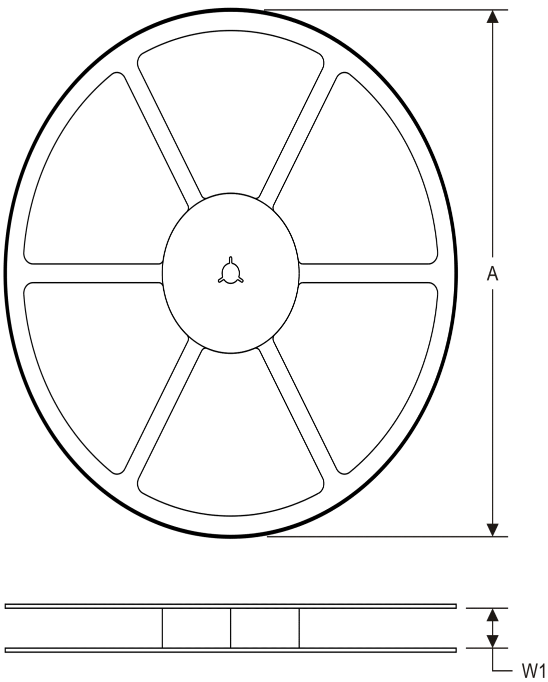
- Catalog: SN65HVD30, SN65HVD33

NOTE: Qualified Version Definitions:

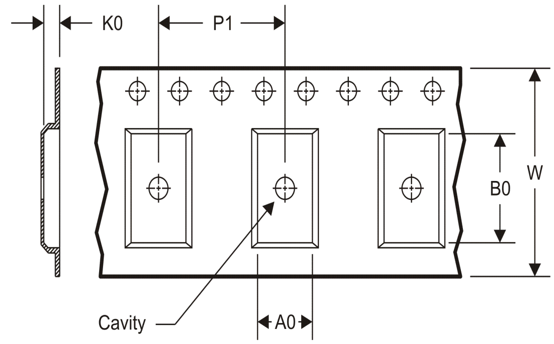
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



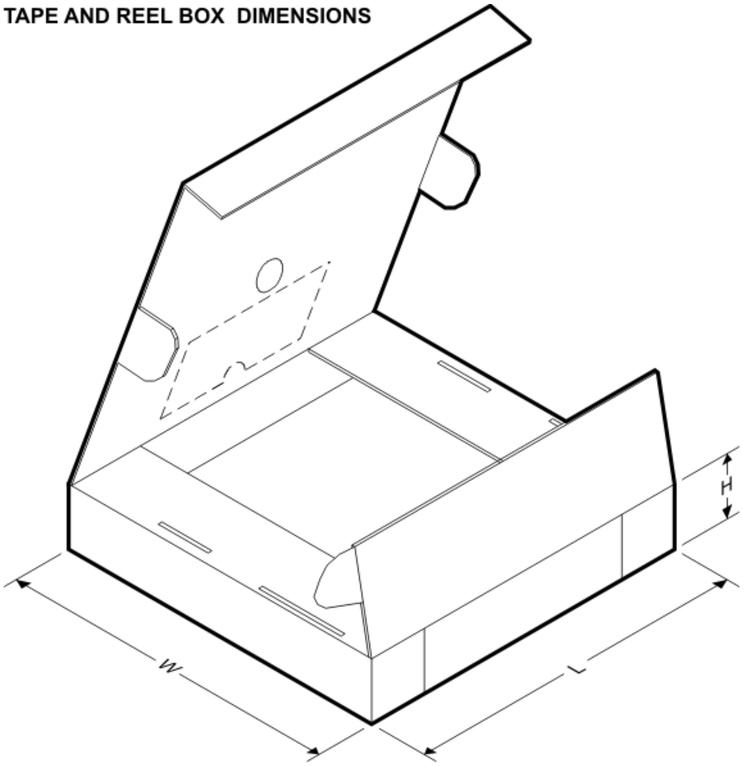
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD30MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD33MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

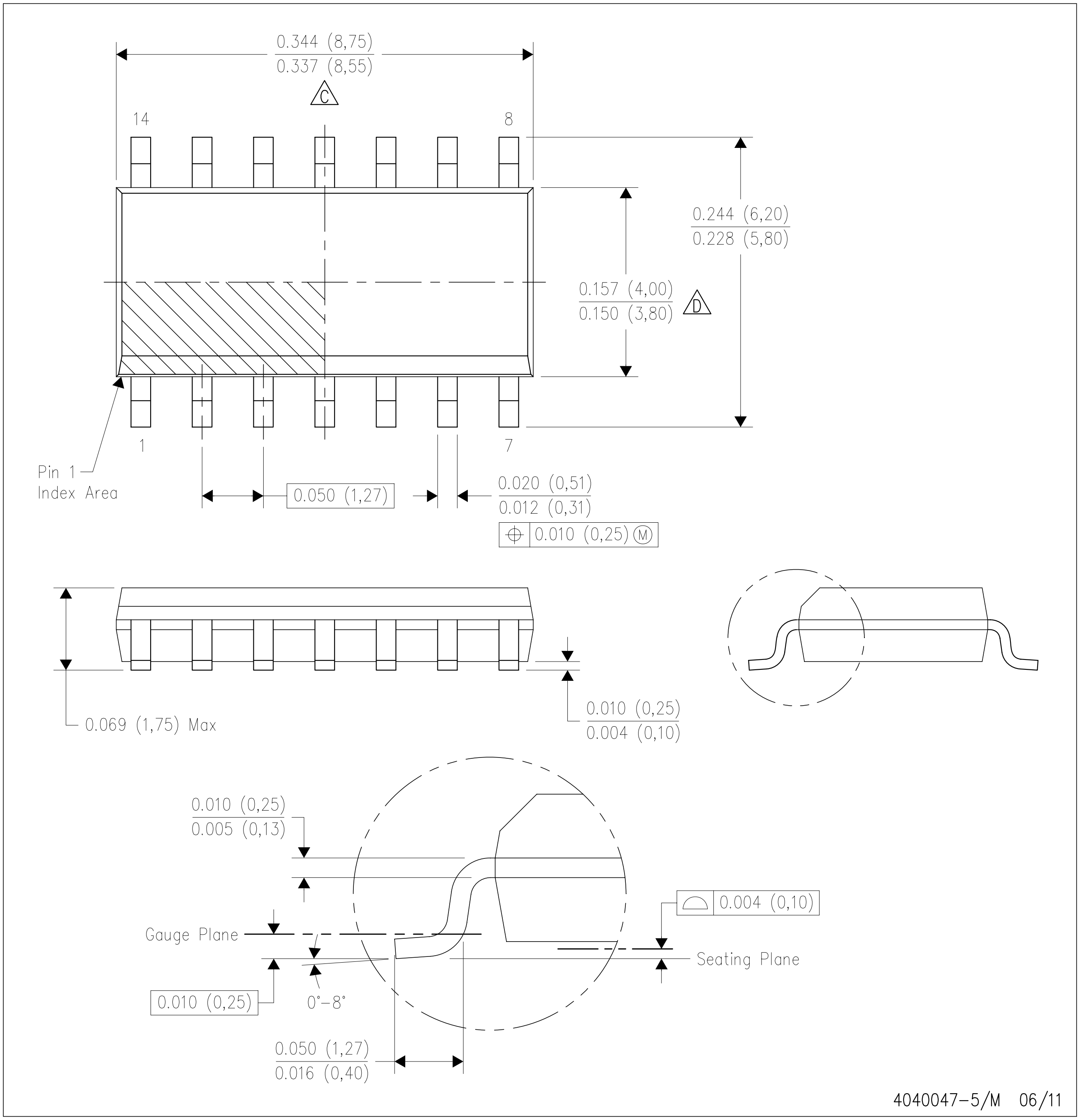
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

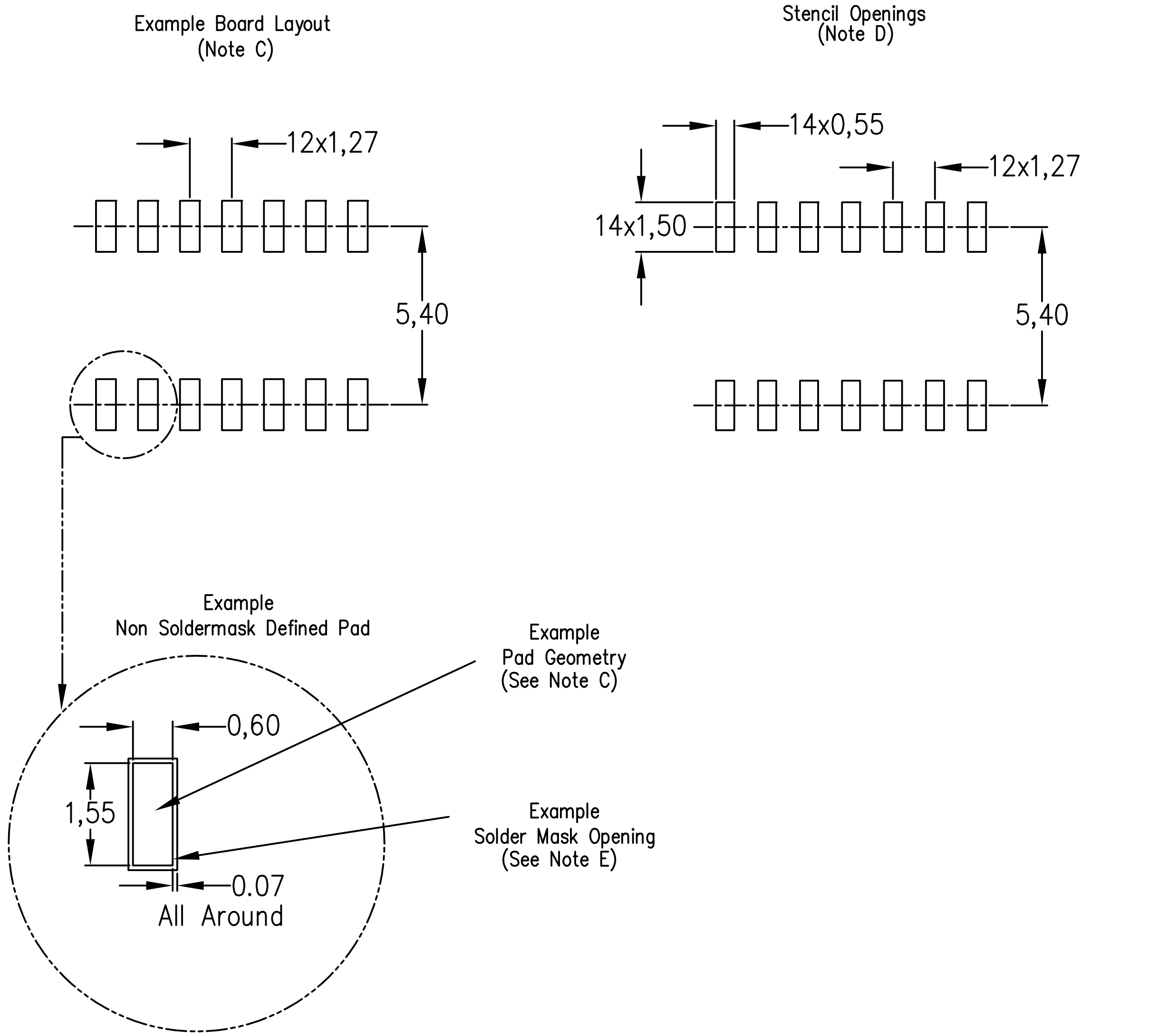
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD30MDREP	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD33MDREP	SOIC	D	14	2500	333.2	345.9	28.6

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

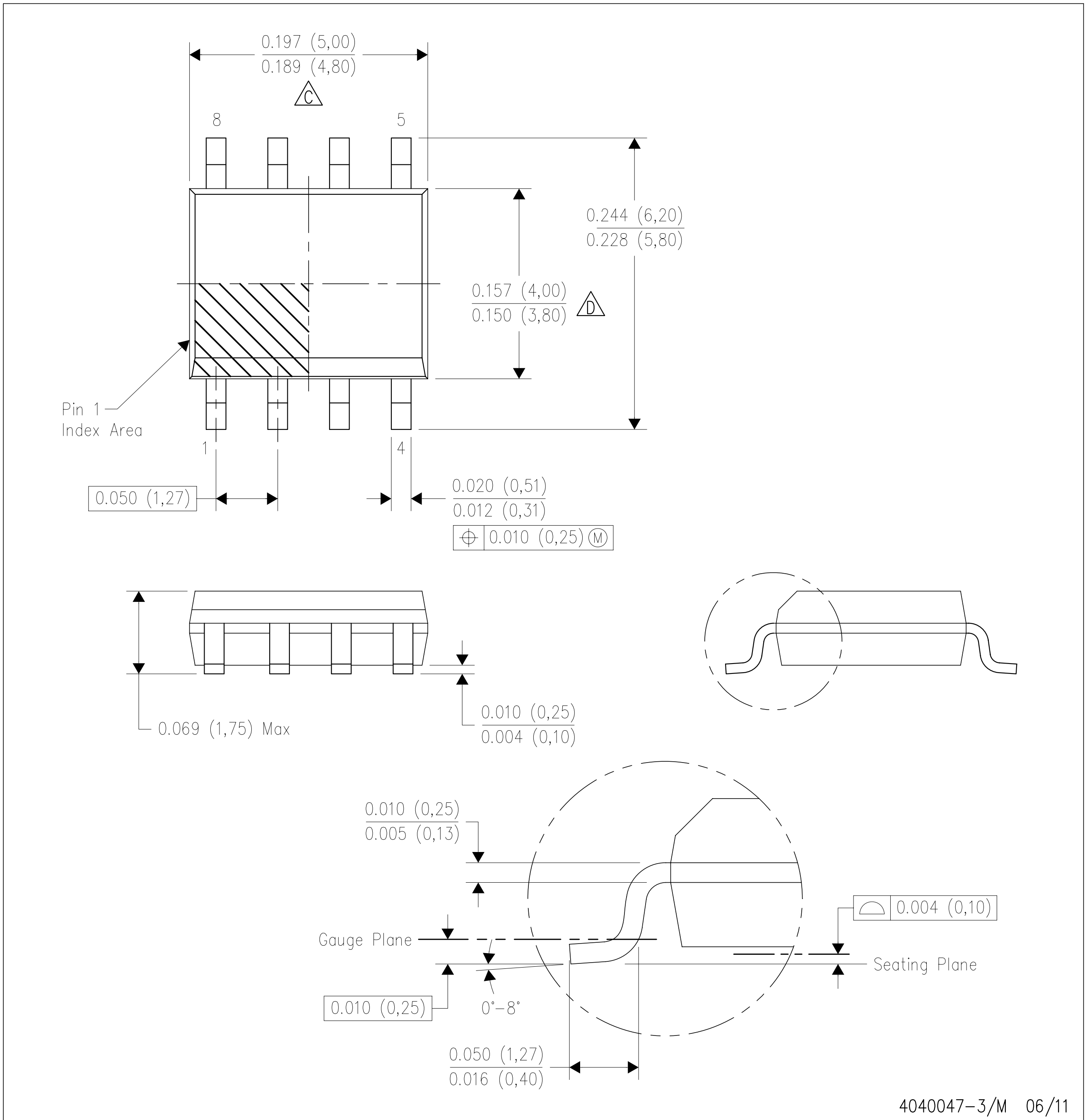
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4211283–3/E 08/12

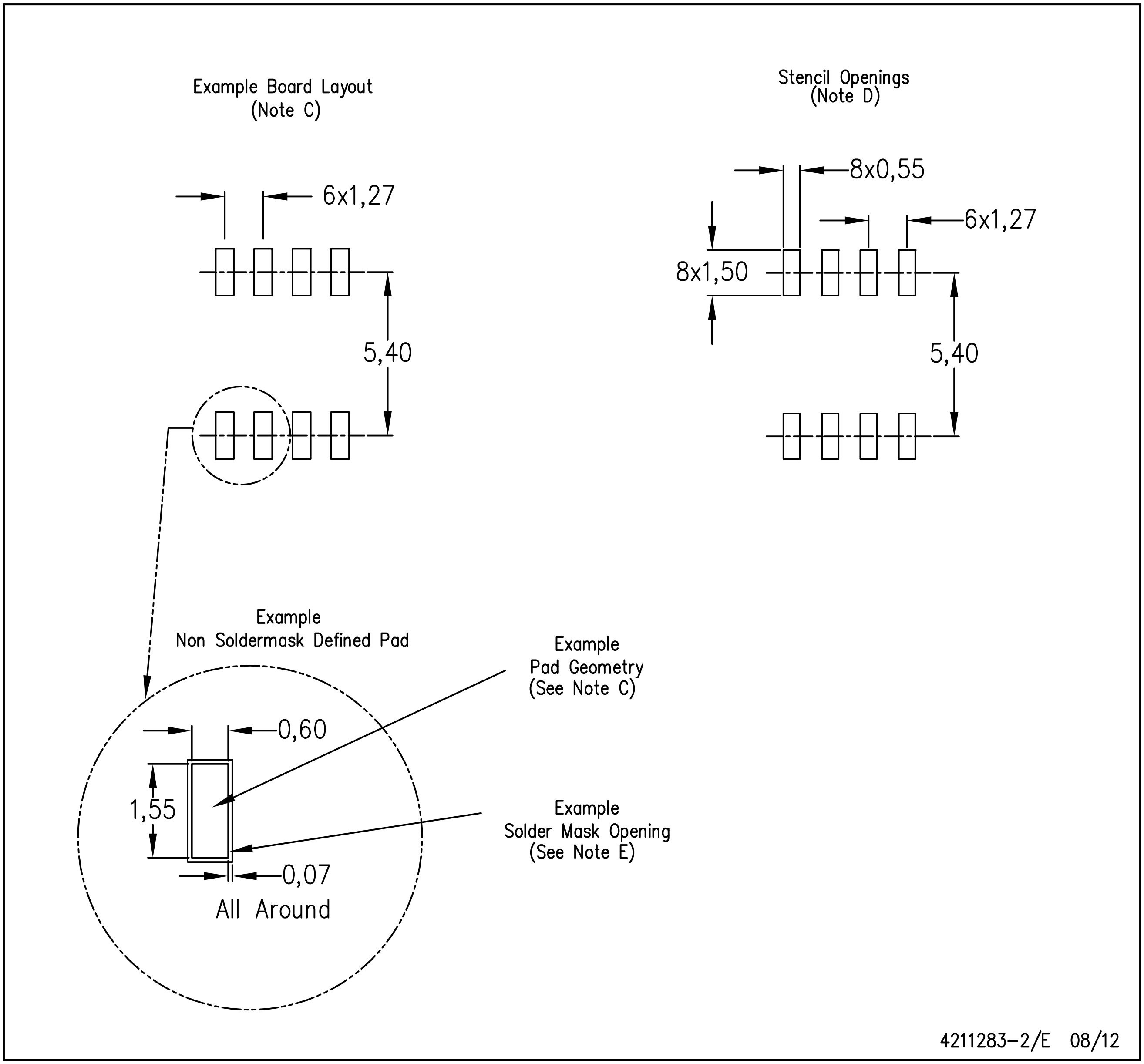
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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