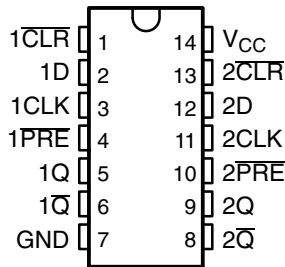


SN54LV74A, SN74LV74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

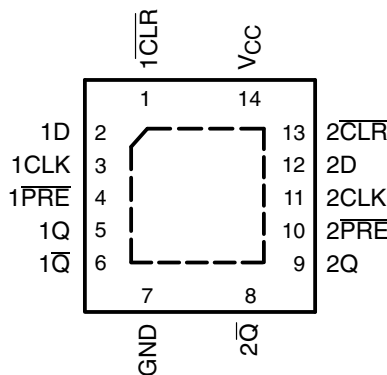
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- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 8.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

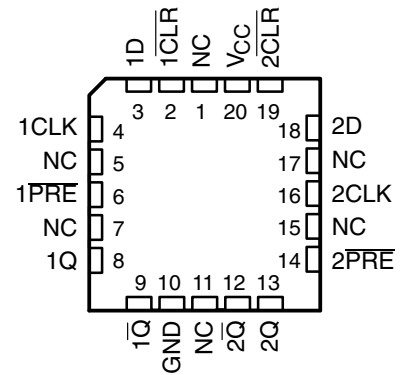
SN54LV74A . . . J OR W PACKAGE
SN74LV74A . . . D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LV74A . . . RGY PACKAGE
(TOP VIEW)



SN54LV74A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These dual positive-edge-triggered D-type flip-flops are designed for 2-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|--------------|---------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RGY | Reel of 1000 | SN74LV74ARGYR | LV74A |
| | SOIC – D | Tube of 50 | SN74LV74AD | LV74A |
| | | Reel of 2500 | SN74LV74ADR | |
| | SOP – NS | Reel of 2000 | SN74LV74ANSR | 74LV74A |
| | SSOP – DB | Reel of 2000 | SN74LV74ADBR | LV74A |
| | TSSOP – PW | Tube of 90 | SN74LV74APW | LV74A |
| | | Reel of 2000 | SN74LV74APWR | |
| Reel of 250 | | SN74LV74APWT | | |
| TVSOP – DGV | Reel of 2000 | SN74LV74ADGVR | LV74A | |
| –55°C to 125°C | CDIP – J | Tube of 25 | SNJ54LV74AJ | SNJ54LV74AJ |
| | CFP – W | Tube of 150 | SNJ54LV74AW | SNJ54LV74AW |
| | LCCC – FK | Tube of 55 | SNJ54LV74AFK | SNJ54LV74AFK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN54LV74A, SN74LV74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

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description/ordering information (continued)

A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

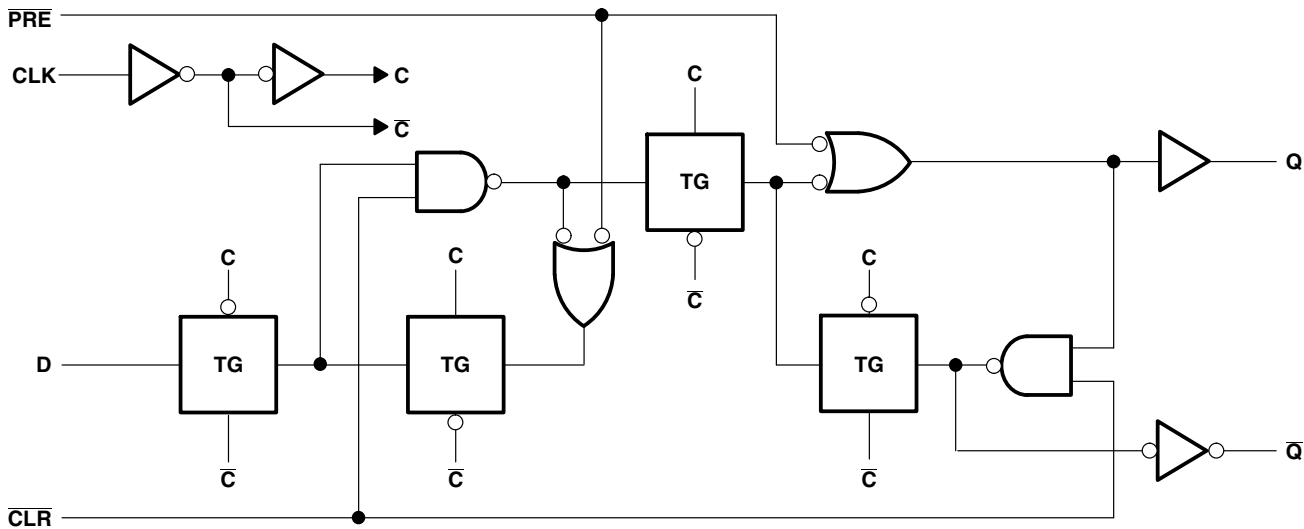
These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|--------|-----|-----|---|----------------|------------------|
| PRE | CLR | CLK | D | Q | \overline{Q} |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H [†] | H [†] |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | Q ₀ | \overline{Q}_0 |

[†] This configuration is nonstable; that is, it does not persist when \overline{PRE} or \overline{CLR} returns to its inactive (high) level.

logic diagram, each flip-flop (positive logic)



SN54LV74A, SN74LV74A

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | –0.5 V to 7 V |
| Output voltage range, V_O (see Notes 1 and 2) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | –20 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through V_{CC} or GND | ±50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): D package | 86°C/W |
| (see Note 3): DB package | 96°C/W |
| (see Note 3): DGV package | 127°C/W |
| (see Note 3): NS package | 76°C/W |
| (see Note 3): PW package | 113°C/W |
| (see Note 4): RGY package | 47°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.



SN54LV74A, SN74LV74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

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recommended operating conditions (see Note 5)

| | | SN54LV74A | | SN74LV74A | | UNIT |
|---------------------|------------------------------------|---|---------------------|---------------------|---------------------|--------------------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 2 | 5.5 | 2 | 5.5 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2\text{ V}$ | 1.5 | 1.5 | | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | $V_{CC} \times 0.7$ | $V_{CC} \times 0.7$ | | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | $V_{CC} \times 0.7$ | $V_{CC} \times 0.7$ | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $V_{CC} \times 0.7$ | $V_{CC} \times 0.7$ | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2\text{ V}$ | | 0.5 | 0.5 | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | | $V_{CC} \times 0.3$ | $V_{CC} \times 0.3$ | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | | $V_{CC} \times 0.3$ | $V_{CC} \times 0.3$ | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | $V_{CC} \times 0.3$ | $V_{CC} \times 0.3$ | |
| V_I | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V_O | Output voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 2\text{ V}$ | | -50 | -50 | μA |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | | -2 | -2 | mA |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | | -6 | -6 | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | -12 | -12 | |
| I_{OL} | Low-level output current | $V_{CC} = 2\text{ V}$ | | 50 | 50 | μA |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | | 2 | 2 | mA |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | | 6 | 6 | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | 12 | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | | 200 | 200 | ns/V |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | | 100 | 100 | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | 20 | 20 | |
| T_A | Operating free-air temperature | -55 | 125 | -40 | 85 | $^{\circ}\text{C}$ |

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | SN54LV74A | | | SN74LV74A | | | UNIT |
|-----------|---|--------------|--------------|-----|-----|--------------|-----|-----|---------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{OH} | $I_{OH} = -50\ \mu\text{A}$ | 2 V to 5.5 V | $V_{CC}-0.1$ | | | $V_{CC}-0.1$ | | | V |
| | $I_{OH} = -2\ \text{mA}$ | 2.3 V | 2 | | | 2 | | | |
| | $I_{OH} = -6\ \text{mA}$ | 3 V | 2.48 | | | 2.48 | | | |
| | $I_{OH} = -12\ \text{mA}$ | 4.5 V | 3.8 | | | 3.8 | | | |
| V_{OL} | $I_{OL} = 50\ \mu\text{A}$ | 2 V to 5.5 V | 0.1 | | | 0.1 | | | V |
| | $I_{OL} = 2\ \text{mA}$ | 2.3 V | 0.4 | | | 0.4 | | | |
| | $I_{OL} = 6\ \text{mA}$ | 3 V | 0.44 | | | 0.44 | | | |
| | $I_{OL} = 12\ \text{mA}$ | 4.5 V | 0.55 | | | 0.55 | | | |
| I_I | $V_I = 5.5\ \text{V or GND}$ | 0 to 5.5 V | ± 1 | | | ± 1 | | | μA |
| I_{CC} | $V_I = V_{CC}\ \text{or GND, } I_O = 0$ | 5.5 V | 20 | | | 20 | | | μA |
| I_{off} | $V_I\ \text{or } V_O = 0\ \text{to } 5.5\ \text{V}$ | 0 | 5 | | | 5 | | | μA |
| C_i | $V_I = V_{CC}\ \text{or GND}$ | 3.3 V | 2 | | | 2 | | | pF |
| | | 5 V | 2 | | | 2 | | | |

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SN54LV74A, SN74LV74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | | | $T_A = 25^\circ\text{C}$ | | SN54LV74A | | SN74LV74A | | UNIT |
|-----------|--------------------------------------|---------------------|--------------------------|-----|-----------|-----|-----------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration | PRE or CLR low | 8 | | 9 | | 9 | | ns |
| | | CLK | 8 | | 9 | | 9 | | |
| t_{su} | Setup time before CLK \uparrow | Data | 8 | | 9 | | 9 | | ns |
| | | PRE or CLR inactive | 7 | | 7 | | 7 | | |
| t_h | Hold time, data after CLK \uparrow | | 0.5 | | 0.5 | | 0.5 | | ns |

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | | | $T_A = 25^\circ\text{C}$ | | SN54LV74A | | SN74LV74A | | UNIT |
|-----------|--------------------------------------|---------------------|--------------------------|-----|-----------|-----|-----------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration | PRE or CLR low | 6 | | 7 | | 7 | | ns |
| | | CLK | 6 | | 7 | | 7 | | |
| t_{su} | Setup time before CLK \uparrow | Data | 6 | | 7 | | 7 | | ns |
| | | PRE or CLR inactive | 5 | | 5 | | 5 | | |
| t_h | Hold time, data after CLK \uparrow | | 0.5 | | 0.5 | | 0.5 | | ns |

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | | | $T_A = 25^\circ\text{C}$ | | SN54LV74A | | SN74LV74A | | UNIT |
|-----------|--------------------------------------|---------------------|--------------------------|-----|-----------|-----|-----------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration | PRE or CLR low | 5 | | 5 | | 5 | | ns |
| | | CLK | 5 | | 5 | | 5 | | |
| t_{su} | Setup time before CLK \uparrow | Data | 5 | | 5 | | 5 | | ns |
| | | PRE or CLR inactive | 3 | | 3 | | 3 | | |
| t_h | Hold time, data after CLK \uparrow | | 0.5 | | 0.5 | | 0.5 | | ns |

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54LV74A | | SN74LV74A | | UNIT |
|-----------|--------------|----------------|----------------------|--------------------------|-------|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | $C_L = 15\text{ pF}$ | 50* | 100* | | 40* | | 40 | MHz | |
| | | | $C_L = 50\text{ pF}$ | 30 | 70 | | 25 | | 25 | | |
| t_{pd} | PRE or CLR | Q or \bar{Q} | $C_L = 15\text{ pF}$ | 9.8* | 14.8* | | 1* | 17* | 1 | 17 | ns |
| | CLK | | | 11.1* | 16.4* | | 1* | 19* | 1 | 19 | |
| t_{pd} | PRE or CLR | Q or \bar{Q} | $C_L = 50\text{ pF}$ | 13 | 17.4 | | 1 | 20 | 1 | 20 | ns |
| | CLK | | | 14.2 | 20 | | 1 | 23 | 1 | 23 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54LV74A | | SN74LV74A | | UNIT |
|------------------|--------------|----------------|----------------------|--------------------------|------|-------|-----------|-------|-----------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | $C_L = 15\text{ pF}$ | 80* | 140* | | 70* | | 70 | | MHz |
| | | | $C_L = 50\text{ pF}$ | 50 | 90 | | 45 | | 45 | | |
| t_{pd} | PRE or CLR | Q or \bar{Q} | $C_L = 15\text{ pF}$ | | 6.9* | 12.3* | 1* | 14.5* | 1 | 14.5 | ns |
| | CLK | | | | 7.9* | 11.9* | 1* | 14* | 1 | 14 | |
| t_{pd} | PRE or CLR | Q or \bar{Q} | $C_L = 50\text{ pF}$ | | 9.2 | 15.8 | 1 | 18 | 1 | 18 | ns |
| | CLK | | | | 10.2 | 15.4 | 1 | 17.5 | 1 | 17.5 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54LV74A | | SN74LV74A | | UNIT |
|------------------|--------------|----------------|----------------------|--------------------------|------|------|-----------|------|-----------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | $C_L = 15\text{ pF}$ | 130* | 180* | | 110* | | 110 | | MHz |
| | | | $C_L = 50\text{ pF}$ | 90 | 140 | | 75 | | 75 | | |
| t_{pd} | PRE or CLR | Q or \bar{Q} | $C_L = 15\text{ pF}$ | | 5* | 7.7* | 1* | 9* | 1 | 9 | ns |
| | CLK | | | | 5.6* | 7.3* | 1* | 8.5* | 1 | 8.5 | |
| t_{pd} | PRE or CLR | Q or \bar{Q} | $C_L = 50\text{ pF}$ | | 6.6 | 9.7 | 1 | 11 | 1 | 11 | ns |
| | CLK | | | | 7.2 | 9.3 | 1 | 10.5 | 1 | 10.5 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 6)

| PARAMETER | | SN74LV74A | | | UNIT |
|-------------|--|-----------|------|------|------|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic V_{OL} | | 0.1 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V_{OL} | | 0 | -0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | | 3.2 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.99 | | V |

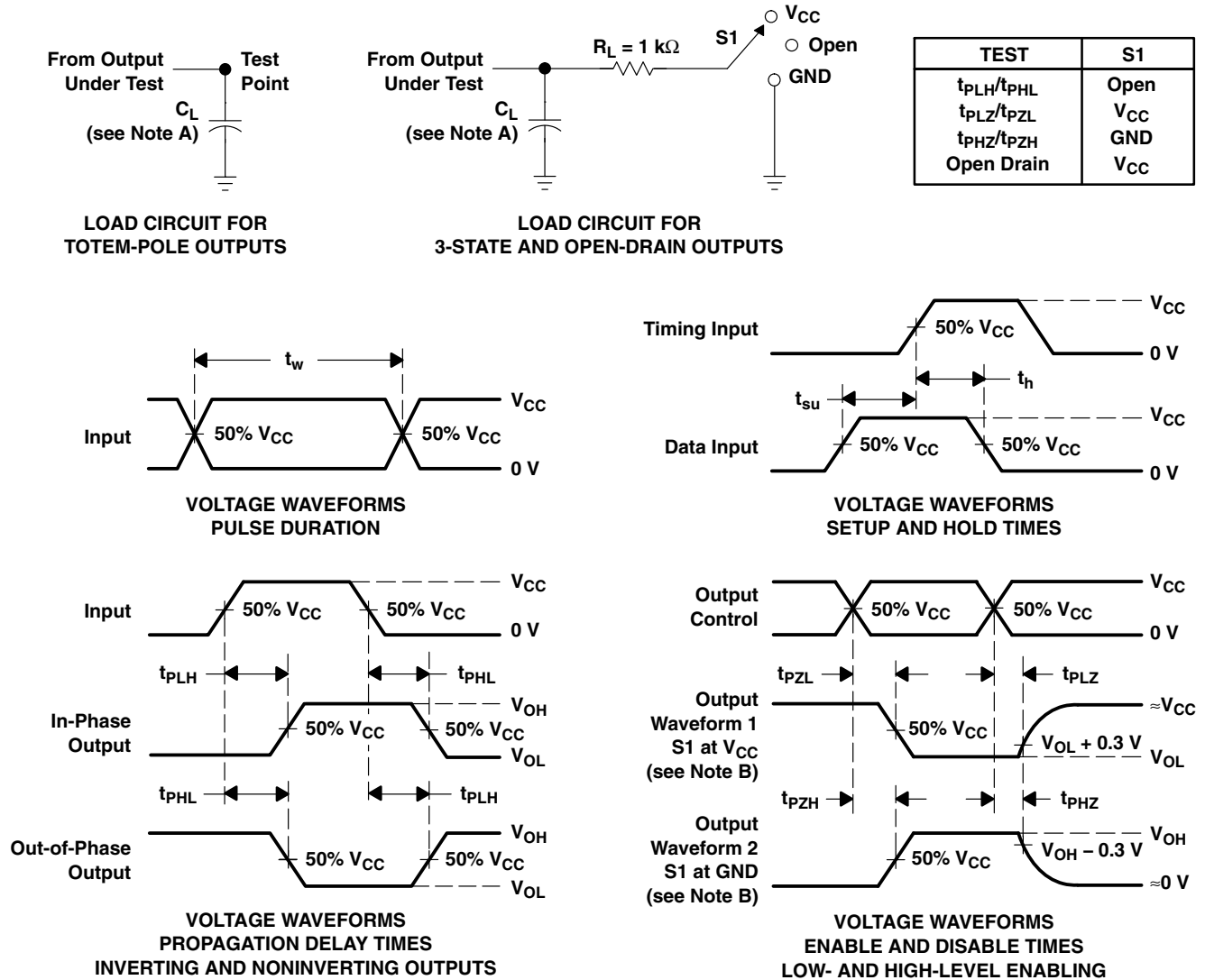
NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | V_{CC} | TYP | UNIT |
|-----------------|-------------------------------|--|----------|-----|------|
| C_{pd} | Power dissipation capacitance | $C_L = 50\text{ pF}$, $f = 10\text{ MHz}$ | 3.3 V | 21 | pF |
| | | | 5 V | 23 | |



PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74LV74AD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74ADBLE | OBSOLETE | SSOP | DB | 14 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74LV74ADBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74ADBRE4 | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74ADBRG4 | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74ADE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74ADG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74ADGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74ADGVRE4 | ACTIVE | TVSOP | DGV | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74ADGVRG4 | ACTIVE | TVSOP | DGV | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74ADR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74ADRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74ADRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74ANSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV74A | Samples |
| SN74LV74ANSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV74A | Samples |
| SN74LV74APW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74APWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74LV74APWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74APWLE | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74LV74APWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74APWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74APWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74APWT | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74APWTE4 | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74APWTG4 | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV74A | Samples |
| SN74LV74ARGYR | ACTIVE | VQFN | RGY | 14 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LV74A | Samples |
| SN74LV74ARGYRG4 | ACTIVE | VQFN | RGY | 14 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LV74A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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OTHER QUALIFIED VERSIONS OF SN74LV74A :

- Automotive: [SN74LV74A-Q1](#)
- Enhanced Product: [SN74LV74A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV74ADBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV74ADGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV74ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV74ANSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV74APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV74APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV74APWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV74APWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV74ARGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV74ADBR | SSOP | DB | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV74ADGVR | TVSOP | DGV | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV74ADR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74LV74ANSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV74APWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV74APWR | TSSOP | PW | 14 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LV74APWRG4 | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV74APWT | TSSOP | PW | 14 | 250 | 367.0 | 367.0 | 35.0 |
| SN74LV74ARGYR | VQFN | RGY | 14 | 3000 | 367.0 | 367.0 | 35.0 |

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

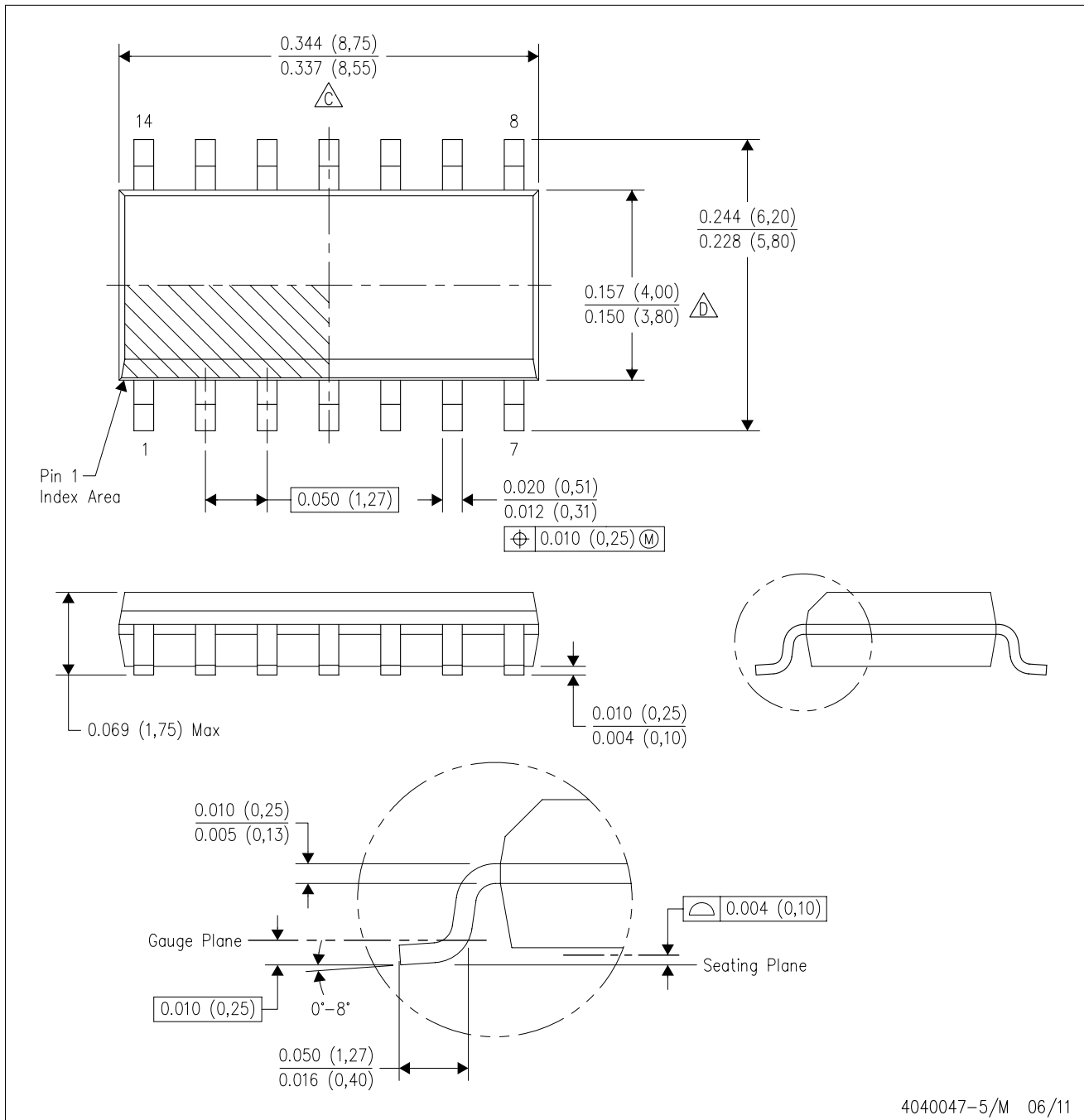
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

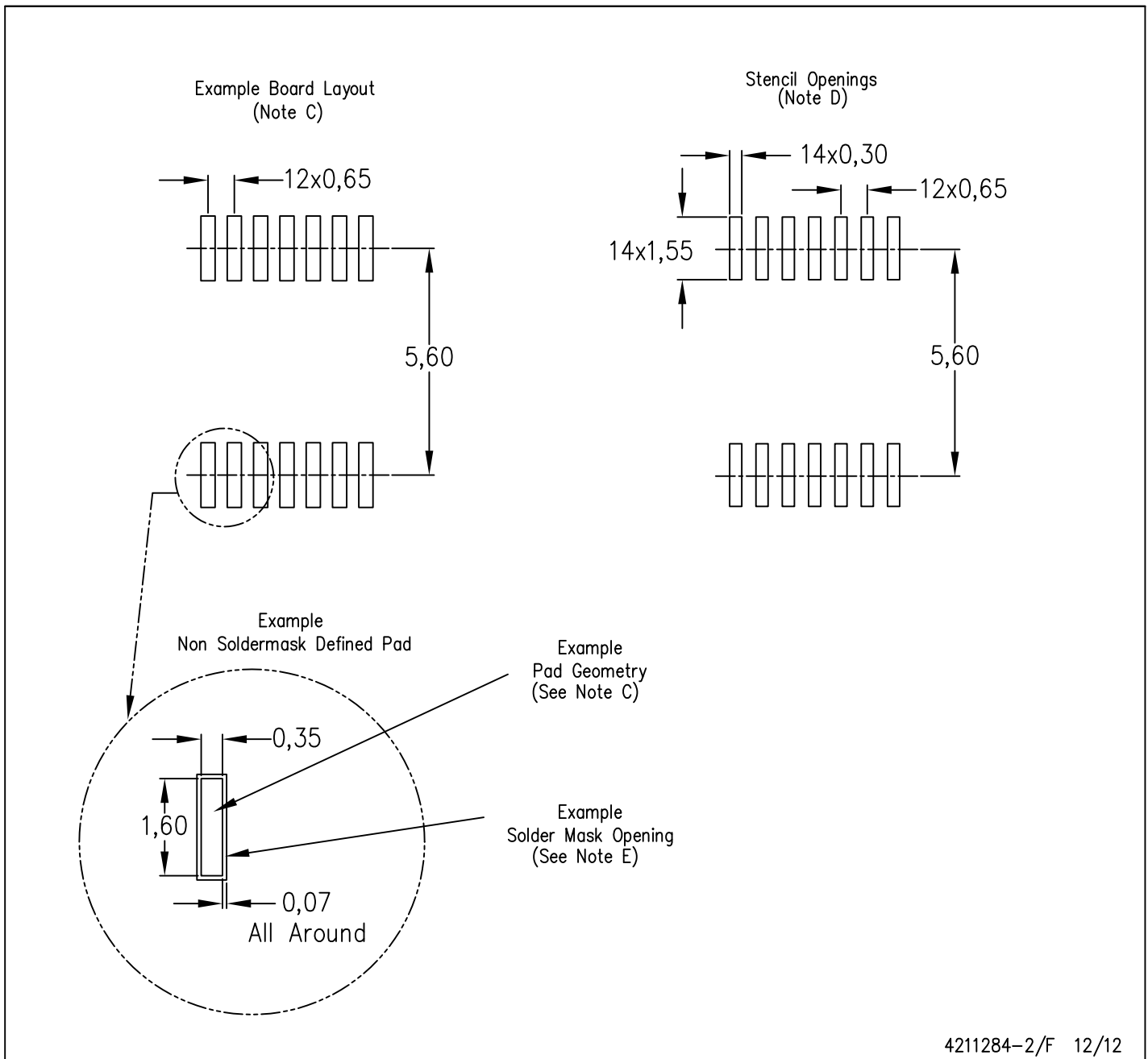
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

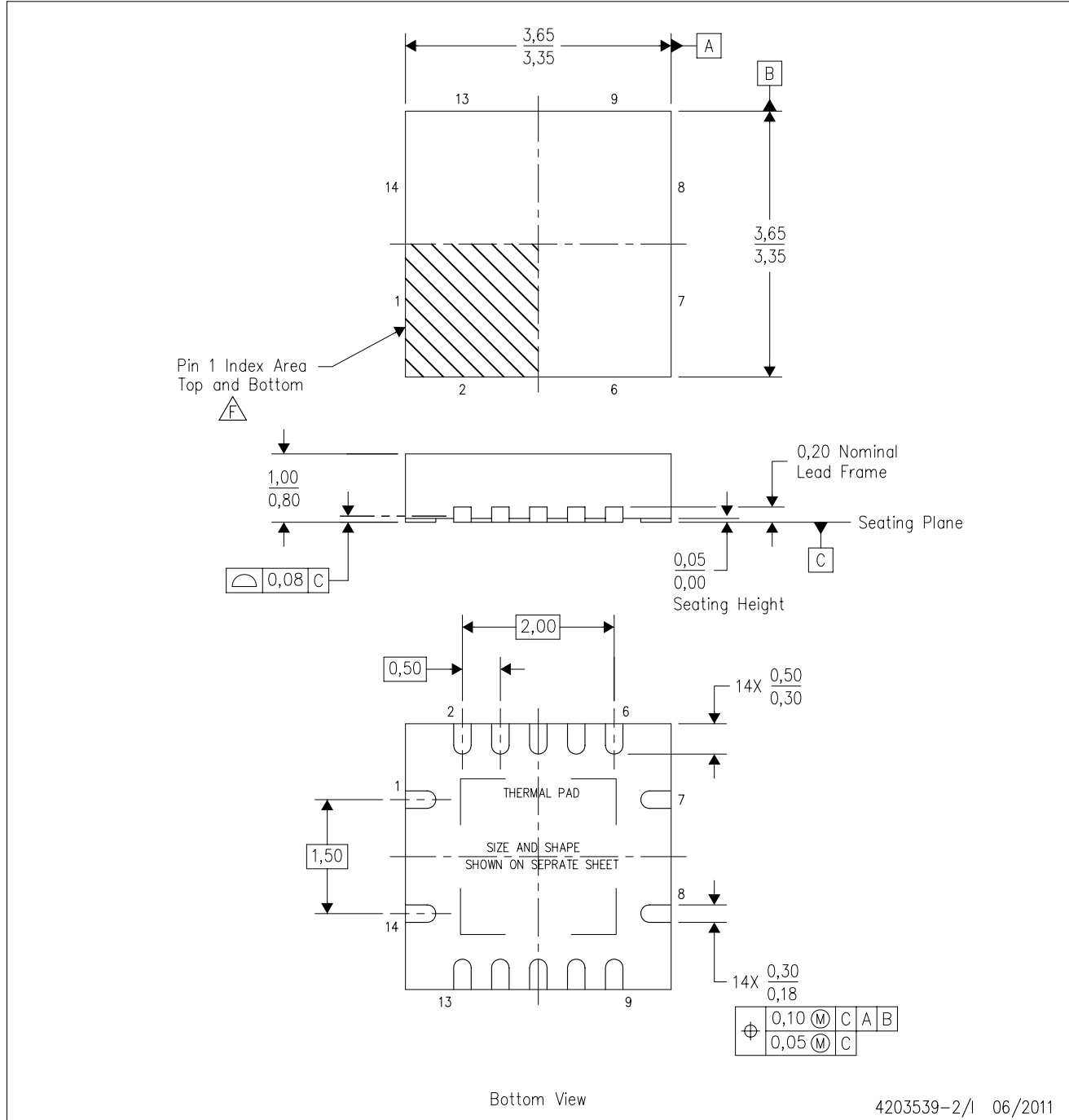
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

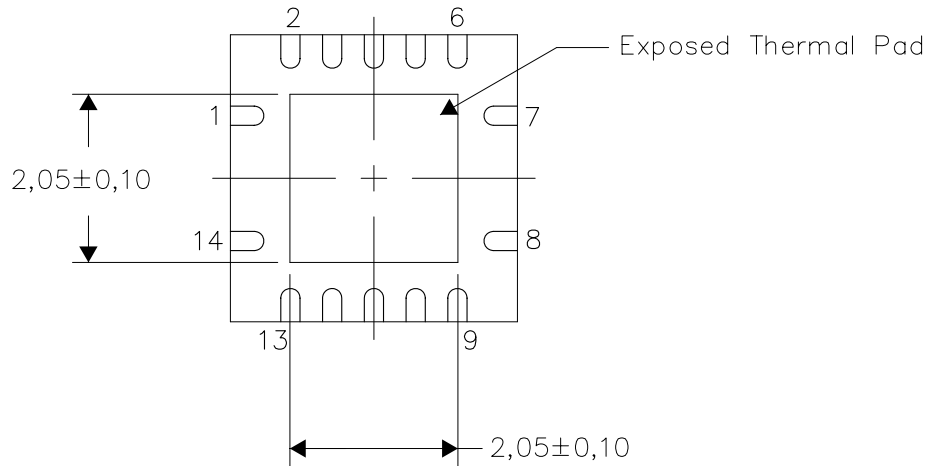
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

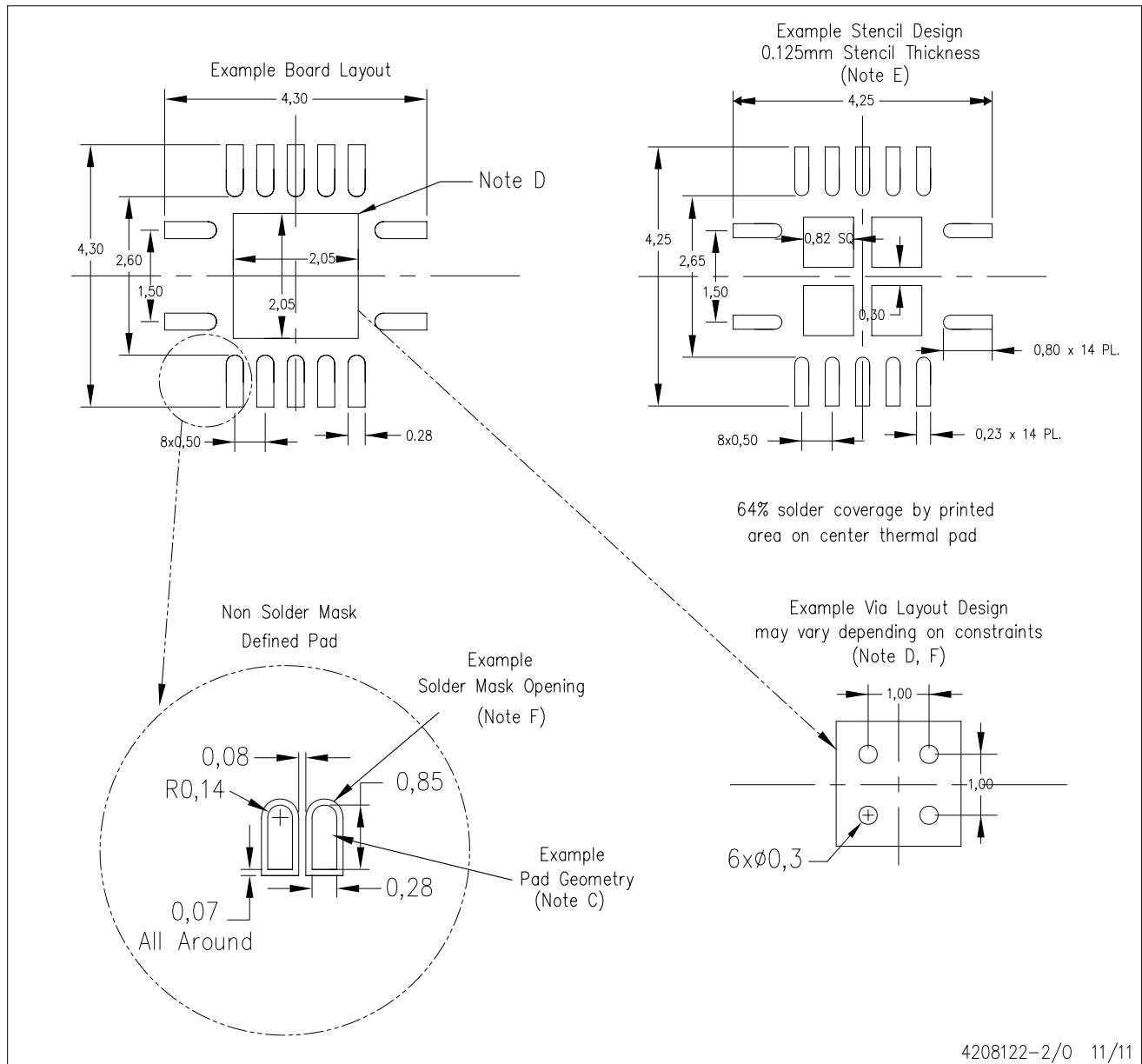
Exposed Thermal Pad Dimensions

4206353-2/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/0 11/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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