



T4 Series

SNUBBERLESSTM & LOGIC LEVEL

4A TRIACs

Table 1: Main Features

Symbol	Value	Unit
$I_{T(RMS)}$	4	A
V_{DRM}/V_{RRM}	600 to 800	V
$I_{GT} (Q_1)$	5 to 35	mA

DESCRIPTION

Based on ST's Snubberless / Logic level technology providing high commutation performances, the **T4** series is suitable for use on AC inductive loads.

They are recommended for applications using universal motors, electrovalves.... such as kitchen aid equipments, power tools, dishwashers,...

Available in a fully insulated package, the T4...-...W version complies with UL standards (ref. E81734).

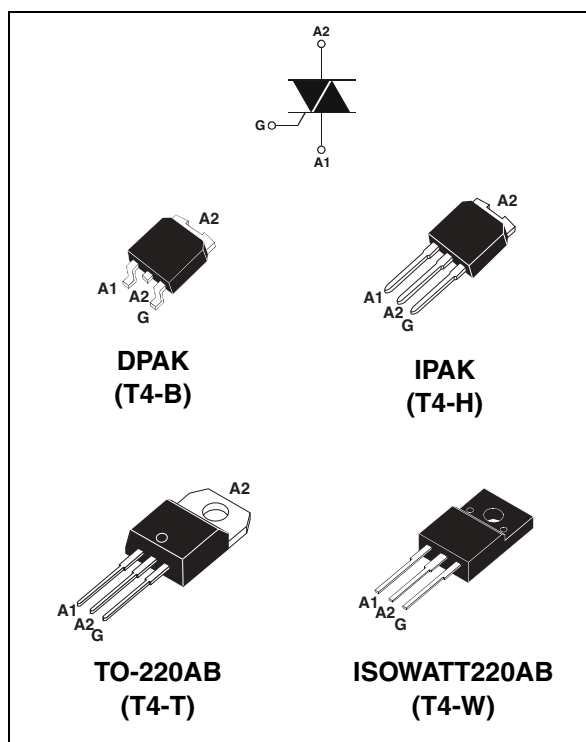


Table 2: Order Codes

Part Number	Marking
T405-xxxB	See page table 8 on page 9
T405-xxxB-TR	
T405-xxxH	
T405-xxxT	
T405-xxxW	
T410-xxxB	
T410-xxxB-TR	
T410-xxxH	
T4105-xxxT	
T410-xxxW	
T435-xxxB	
T435-xxxB-TR	
T435-xxxH	
T435-xxxT	
T435-xxxW	

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Table 3: Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	I _{PAK} /DPAK/ TO-220AB	$T_c = 110^{\circ}\text{C}$	4	A
		ISOWATT220AB	$T_c = 105^{\circ}\text{C}$		
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25°C)	F = 50 Hz	t = 20 ms	30	A
		F = 60 Hz	t = 16.7 ms	31	
I^2t	I^2t Value for fusing	$t_p = 10$ ms		5.1	A ² s
di/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, $t_r \leq 100$ ns	F = 120 Hz	$T_j = 125^{\circ}\text{C}$	50	A/ μ s
I_{GM}	Peak gate current	$t_p = 20$ μ s	$T_j = 125^{\circ}\text{C}$	4	A
$P_{G(AV)}$	Average gate power dissipation		$T_j = 125^{\circ}\text{C}$	1	W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range			- 40 to + 150 - 40 to + 125	$^{\circ}\text{C}$

Tables 4: Electrical Characteristics ($T_j = 25^{\circ}\text{C}$, unless otherwise specified)

Symbol	Test Conditions	Quadrant		T4			Unit
				T405	T410	T435	
I _{GT} (1)	V _D = 12 V R _L = 30 Ω	I - II - III	MAX.	5	10	35	mA
V _{GT}		I - II - III	MAX.	1.3			V
V _{GD}	V _D = V _{DRM} R _L = 3.3 kΩ T _j = 125°C	I - II - III	MIN.	0.2			V
I _H (2)	I _T = 100 mA		MAX.	10	15	35	mA
I _L	I _G = 1.2 I _{GT}	I - III	MAX.	10	25	50	mA
		II		15	30	60	
dV/dt (2)	V _D = 67 %V _{DRM} gate open T _j = 125°C		MIN.	20	40	400	V/μs
(dI/dt)c (2)	(dV/dt)c = 0.1 V/μs T _j = 125°C		MIN.	1.8	2.7	-	A/ms
	(dV/dt)c = 10 V/μs T _j = 125°C			0.9	2.0	-	
	Without snubber T _j = 125°C			-	-	2.5	

Note 1: minimum I_{GT} is guaranteed at 5% of I_{GT} max.

Note 2: for both polarities of A2 referenced to A1.

Table 5: Static Characteristics

Symbol	Test Conditions			Value	Unit	
V _T (2)	I _{TM} = 5.5 A	t _p = 380 μs	T _j = 25°C	MAX.	1.56	V
V _{to} (2)	Threshold voltage		T _j = 125°C	MAX.	0.89	V
R _d (2)	Dynamic resistance		T _j = 125°C	MAX.	120	mΩ
I _{DRM} I _{RRM}	V _{DRM} = V _{RRM}		T _j = 25°C	MAX.	5	μA
			T _j = 125°C		1	mA

Note 1: minimum I_{GT} is guaranteed at 5% of I_{GT} max.

Note 2: for both polarities of A2 referenced to A1.

Table 6: Thermal resistance

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (AC)	IPAK / DPAK / TO-220AB	2.6	$^\circ\text{C/W}$
		ISOWATT220AB	4.0	
$R_{th(j-a)}$	Junction to ambient	$S = 0.5\text{ cm}^2$ DPAK	70	$^\circ\text{C/W}$
		TO-220AB / ISOWATT220AB	60	
		IPAK	100	

S = Copper surface under tab.

Figure 1: Maximum power dissipation versus RMS on-state current (full cycle)

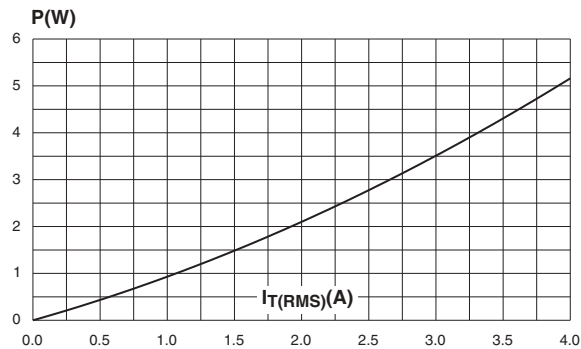


Figure 2: RMS on-state current versus case temperature (full cycle)

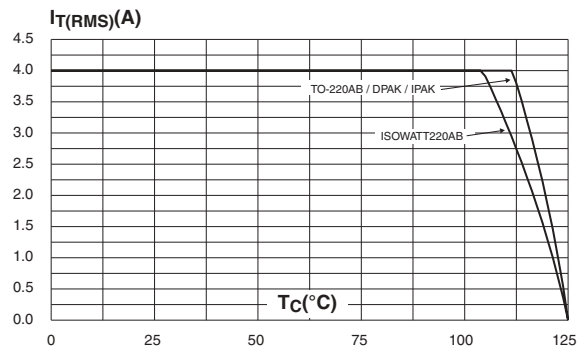


Figure 3: RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35μm) (full cycle)

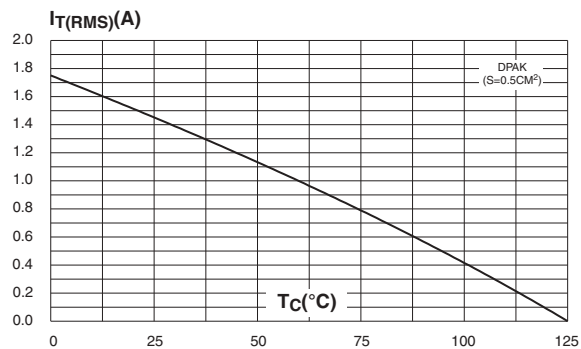


Figure 4: Relative variation of thermal impedance versus pulse duration

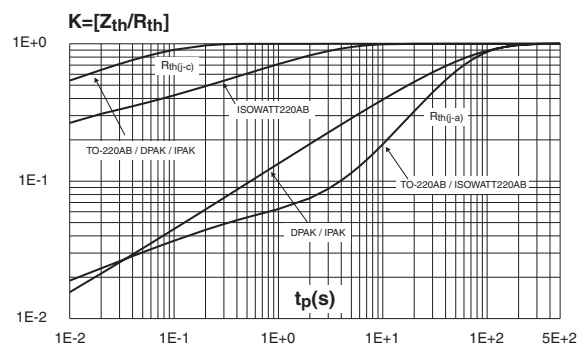


Figure 5: On-state characteristics (maximum values)

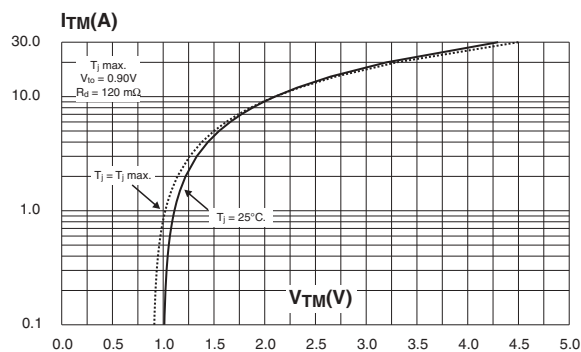


Figure 6: Surge peak on-state current versus number of cycles

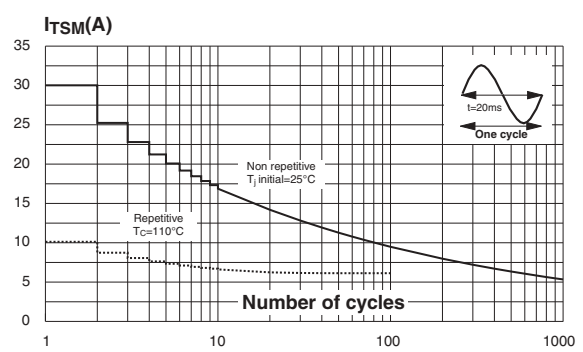


Figure 7: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10$ ms and corresponding value of I^2t

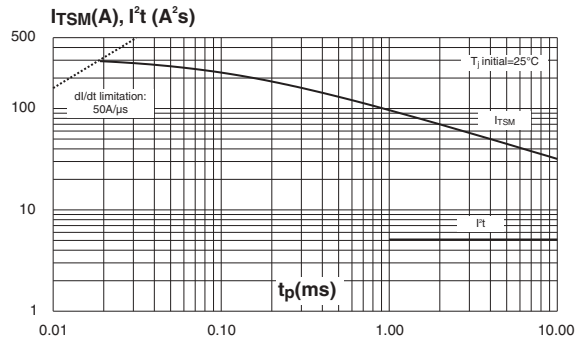


Figure 8: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values)

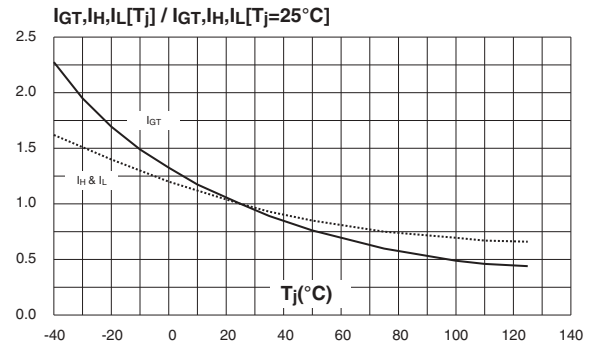


Figure 9: Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values)

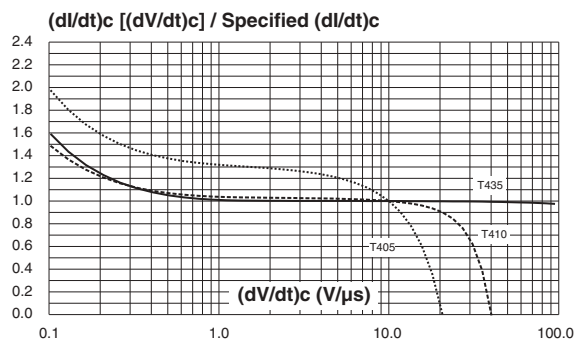


Figure 10: Relative variation of critical rate of decrease of main current versus junction temperature

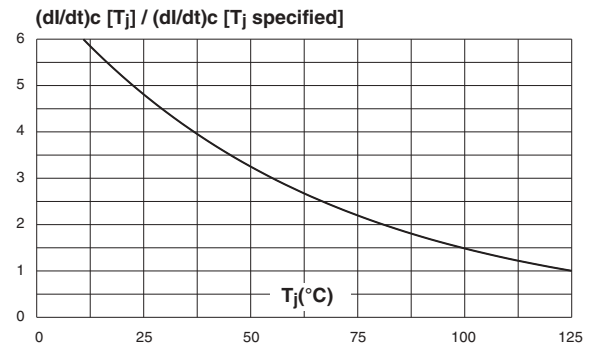
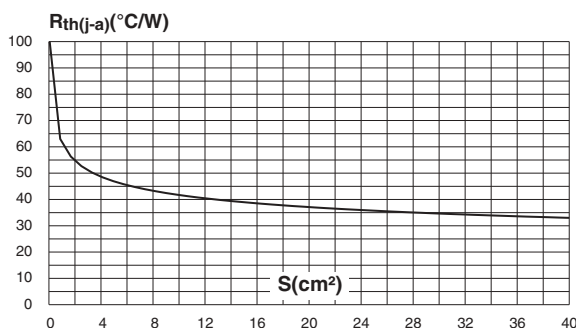


Figure 11: DPAK thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35 μ m)



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Figure 12: Ordering Information Scheme

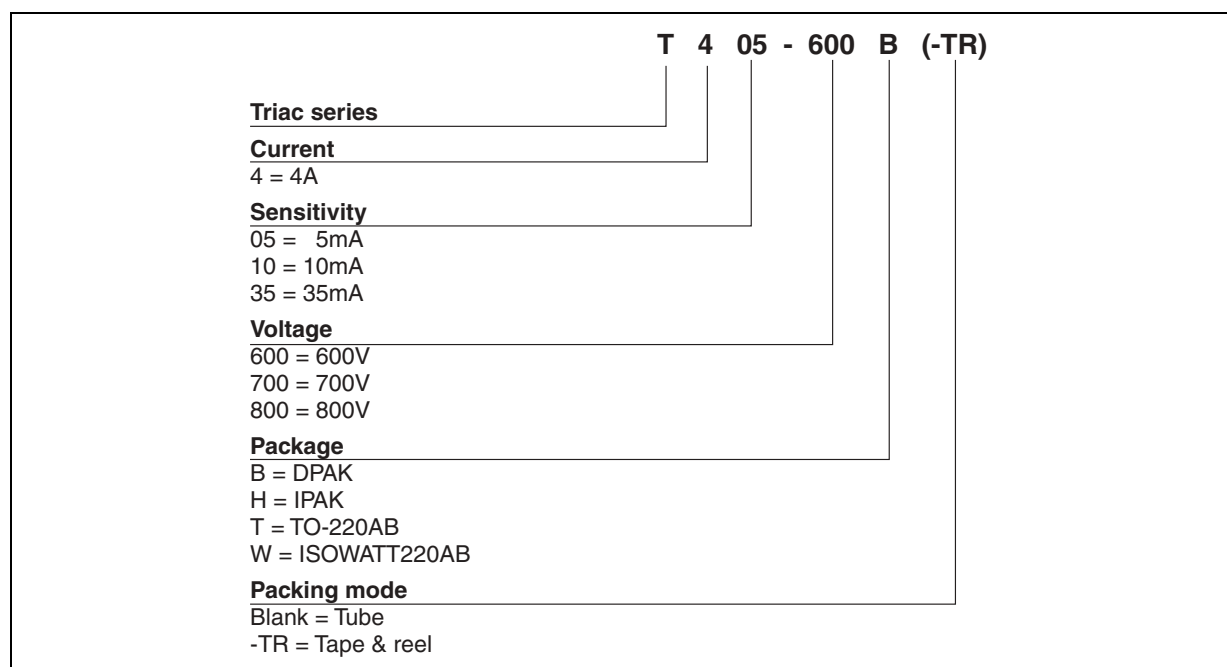


Table 7: Product Selector

Part Number	Voltage (xxx)			Sensitivity	Type	Package
	600 V	700 V	800 V			
T405-xxxB	X	X	X	5 mA	Logic level	DPAK
T405-xxxH	X	X	X	5 mA	Logic level	IPAK
T405-xxxT	X	X	X	5 mA	Logic level	TO-220AB
T405-xxxW	X	X	X	5 mA	Logic level	ISOWATT220AB
T410-xxxB	X	X	X	10 mA	Logic level	DPAK
T410-xxxH	X	X	X	10 mA	Logic Level	IPAK
T410-xxxT	X	X	X	10 mA	Logic Level	TO-220AB
T410-xxxW	X	X	X	10 mA	Logic Level	ISOWATT220AB
T435-xxxB	X	X	X	35 mA	Snubberless	DPAK
T435-xxxH	X	X	X	35 mA	Snubberless	IPAK
T435-xxxT	X	X	X	35 mA	Snubberless	TO-220AB
T435-xxxW	X	X	X	35 mA	Snubberless	ISOWATT220AB

Figure 13: DPAK Package Mechanical Data

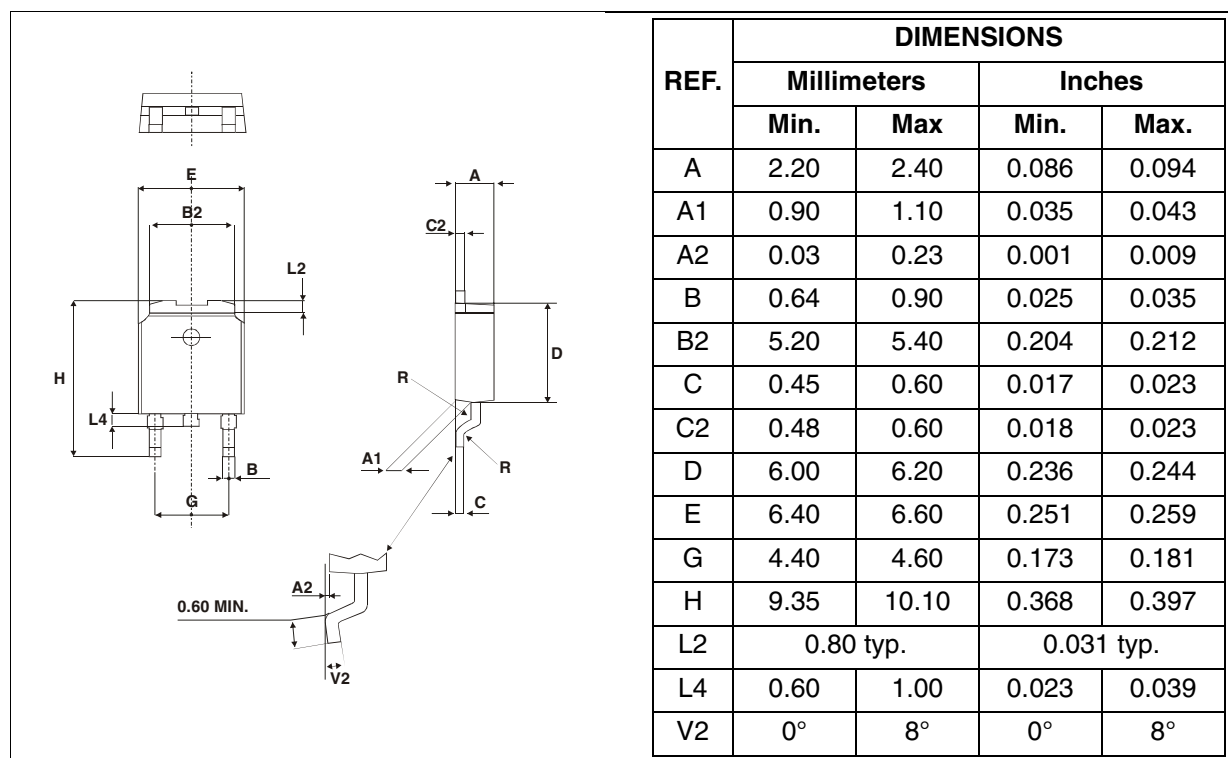
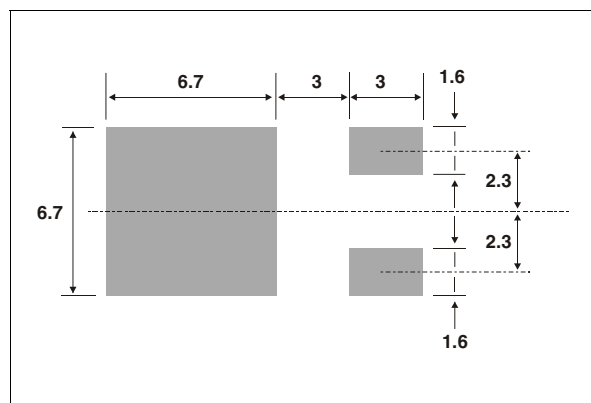
Figure 14: DPAK Foot Print Dimensions
(in millimeters)

Figure 15: ISOWATT220AB Package Mechanical Data

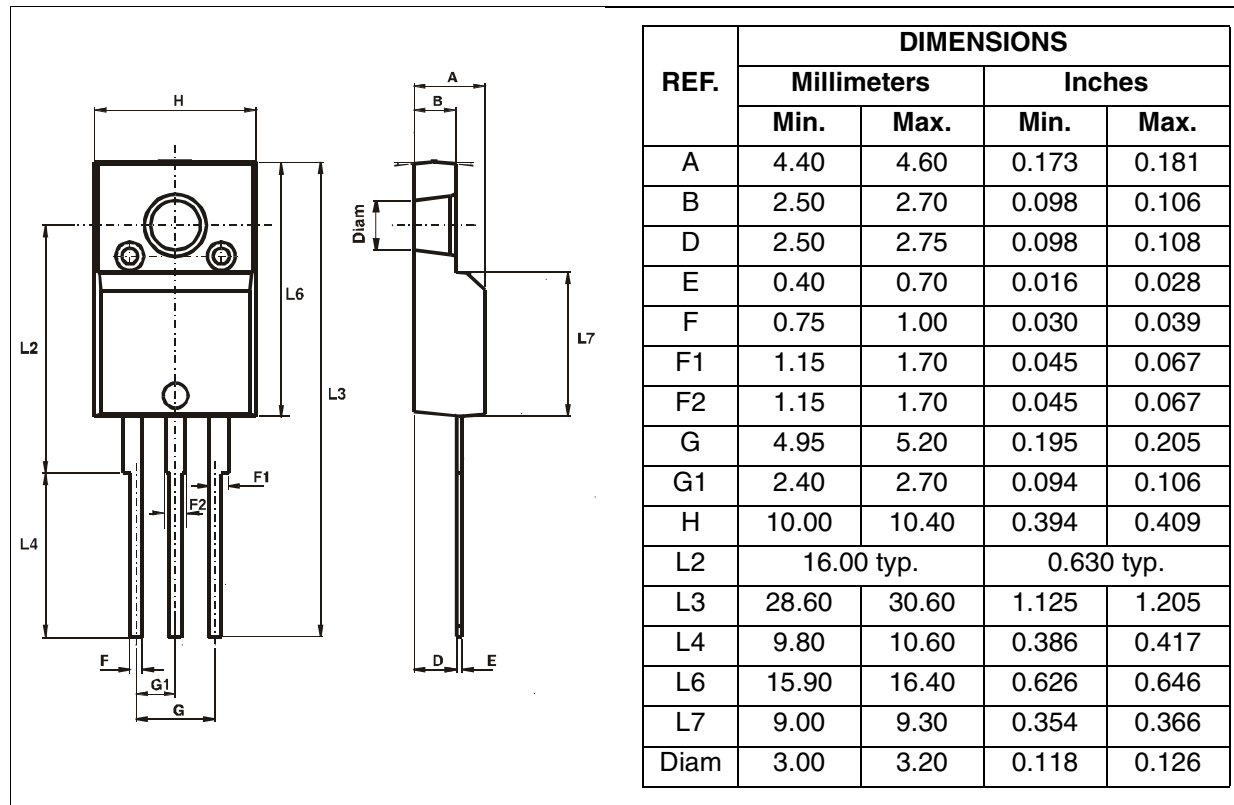


Figure 16: IPAK Package Mechanical Data

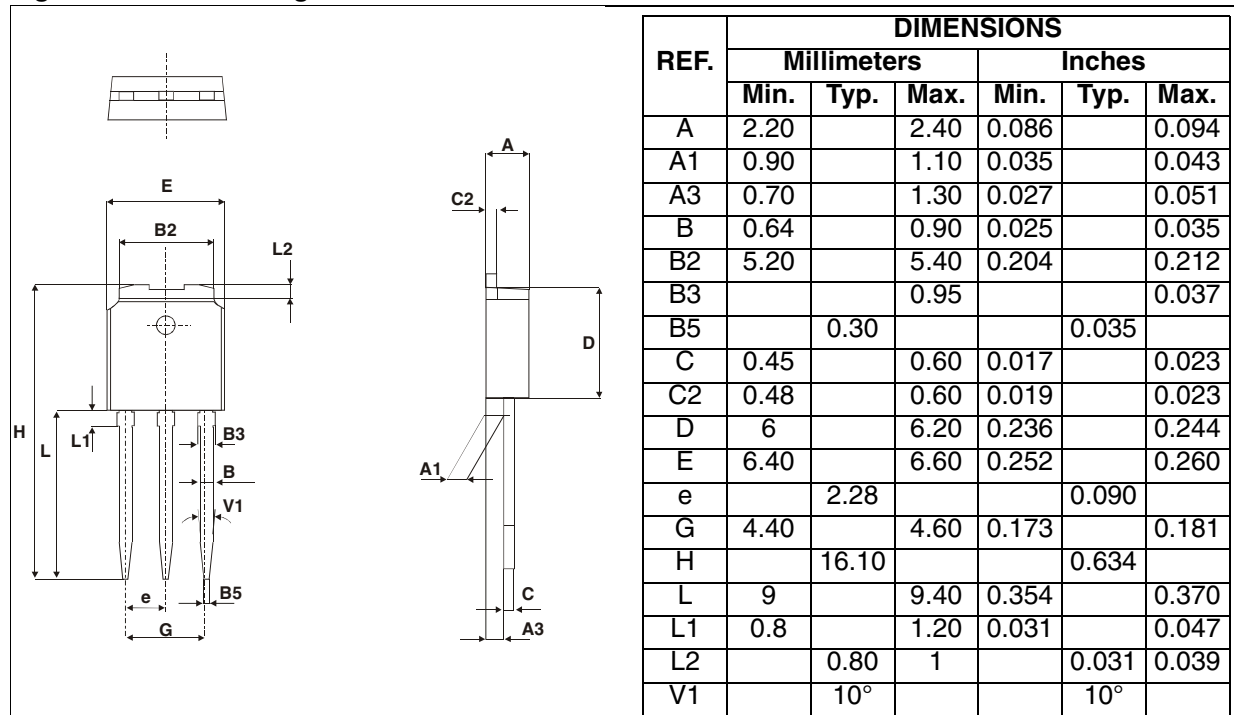


Figure 17: TO-220AB Package Mechanical Data

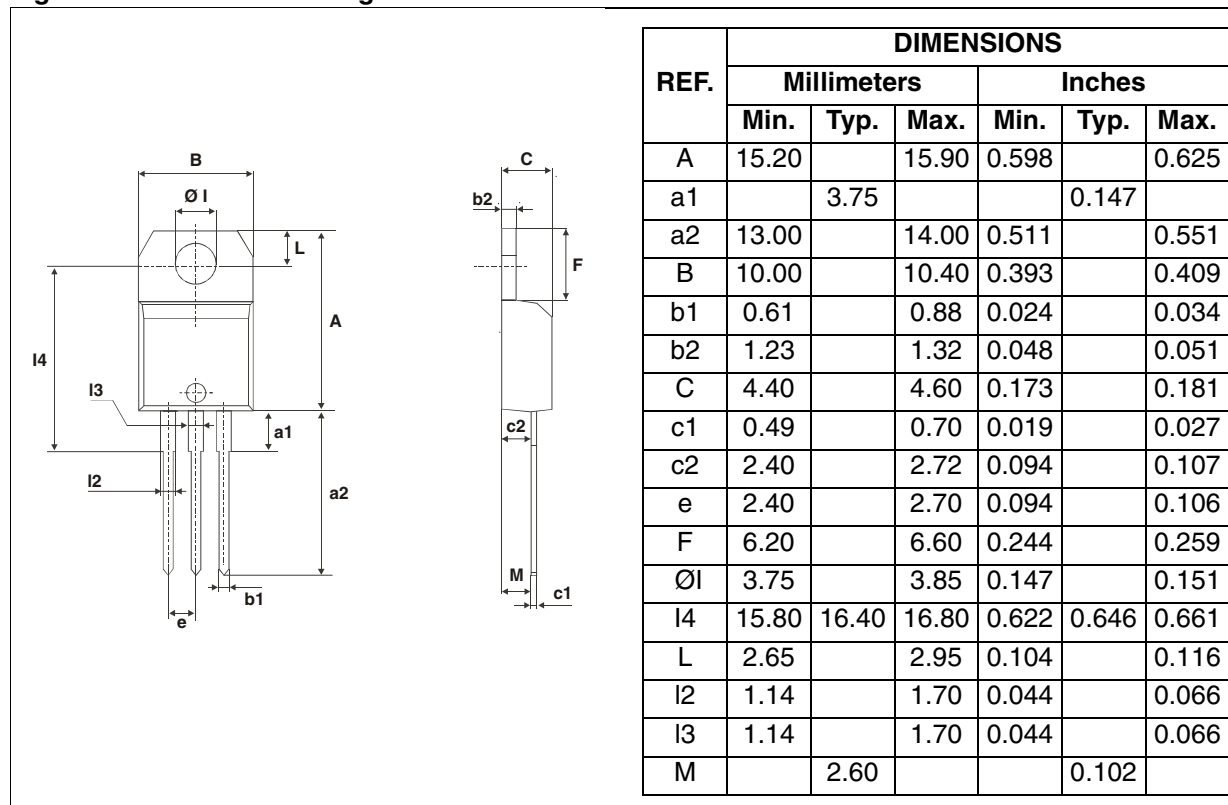


Table 8: Ordering Information

Ordering type	Marking	Package	Weight	Base qty	Delivery mode
T4xx-yyyB	T4 xxyy	DPAK	0.3 g	75	Tube
T4xx-yyyB-TR	T4 xxyy	DPAK	0.3 g	2500	Tape & reel
T4xx-yyyH	T4 xxyy	IPAK	0.4 g	75	Tube
T4xx-yyyT	T4xx yyyT	TO-220AB	2.3 g	50	Tube
T4xx-yyyB	T4xxyyyW	ISOWATT220AB	2.1 g	50	Tube

Note: xxx = voltage, yy = sensitivity

Table 9: Revision History

Date	Revision	Description of Changes
Jun-2003	5	Last update.
25-Mar-2005	6	Layout update. No content change.
25-Jan-2005	7	Markings changed in Table 8

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Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331