Data Sheet July 22, 2005 FN3183.4

Automatic Battery Back-Up Switch

The Intersil ICL7673 is a monolithic CMOS battery backup circuit that offers unique performance advantages over conventional means of switching to a backup supply. The ICL7673 is intended as a low-cost solution for the switching of systems between two power supplies; main and battery backup. The main application is keep-alive-battery power switching for use in volatile CMOS RAM memory systems and real time clocks. In many applications this circuit will represent a low insertion voltage loss between the supplies and load. This circuit features low current consumption, wide operating voltage range, and exceptionally low leakage between inputs. Logic outputs are provided that can be used to indicate which supply is connected and can also be used to increase the power switching capability of the circuit by driving external PNP transistors.

Ordering Information

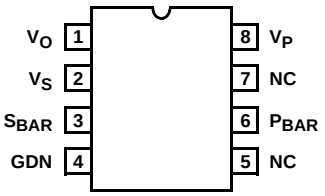
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ICL7673CPA	0 to 70	8 Ld PDIP	E8.3
ICL7673CPAZ (See Note)	0 to 70	8 Ld PDIP* (Pb-free)	E8.3
ICL7673CBA	0 to 70	8 Ld SOIC (N)	M8.15
ICL7673CBA-T	8 Ld SOIC (N) Tape and Reel		M8.15
ICL7673CBAZA (See Note)	0 to 70	8 Ld SOIC (N) (Pb-free)	M8.15
ICL7673CBAZA-T (See Note)	0 to 70	8 Ld SOIC (N) (Pb-free)	M8.15

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

ICL7673 (SOIC, PDIP)
TOP VIEW



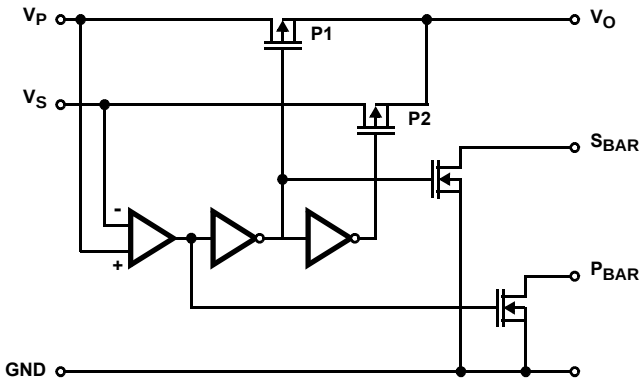
Features

- Automatically Connects Output to the Greater of Either Input Supply Voltage
- If Main Power to External Equipment is Lost, Circuit Will Automatically Connect Battery Backup
- Reconnects Main Power When Restored
- Logic Indicator Signaling Status of Main Power
- Low Impedance Connection Switches
- Low Internal Power Consumption
- Wide Supply Range: . . . . . 2.5V to 15V
- Low Leakage Between Inputs
- External Transistors May Be Added if Very Large Currents Need to Be Switched
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- On Board Battery Backup for Real-Time Clocks, Timers, or Volatile RAMs
- Over/Under Voltage Detector
- Peak Voltage Detector
- Other Uses:
  - Portable Instruments, Portable Telephones, Line Operated Equipment

Functional Block Diagram



$V_P > V_S$, P1 SWITCH ON AND P_{BAR} SWITCH ON
$V_S > V_P$, P2 SWITCH ON AND S_{BAR} SWITCH ON

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Input Supply (V_P or V_S) Voltage . . . . . GND - 0.3V to +18V
Output Voltages P_{BAR} and S_{BAR} . . . . . GND - 0.3V to +18V
Peak Current
Input V_P (at V_P = 5V) (Note 1) 38mA
Input V_S (at V_S = 3V) 30mA
P_{BAR} or S_{BAR} 150mA

Operating Conditions

Temperature Range:
ICL7673C . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package*	150	N/A
Plastic SOIC Package	180	N/A

Maximum Storage Temperature. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering, 10sec). . . . . 300°C
(SOIC - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Derate above 25°C by 0.38mA/°C.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications T_A = 25°C Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_P	V_S = 0V, I_{LOAD} = 0mA	2.5	-	15	V
	V_S	V_P = 0V, I_{LOAD} = 0mA	2.5	-	15	V
Quiescent Supply Current	I+	V_P = 0V, V_S = 3V, I_{LOAD} = 0mA	-	1.5	5	µA
Switch Resistance P1 (Note 1)	$r_{DS(ON)}P1$	V_P = 5V, V_S = 3V, I_{LOAD} = 15mA	-	8	15	Ω
		At T_A = +85°C	-	16	-	Ω
		V_P = 9V, V_S = 3V, I_{LOAD} = 15mA	-	6	-	Ω
		V_P = 12V, V_S = 3V, I_{LOAD} = 15mA	-	5	-	Ω
Temperature Coefficient of Switch Resistance P1	$T_{C(P1)}$	V_P = 5V, V_S = 3v, I_{LOAD} = 15mA	-	0.5	-	%/°C
Switch Resistance P2 (Note 1)	$r_{DS(ON)}P2$	V_P = 0V, V_S = 3V, I_{LOAD} = 1mA	-	40	100	Ω
		At T_A = +85°C	-	60	-	Ω
		V_P = 0V, V_S = 5V, I_{LOAD} = 1mA	-	26	-	Ω
		V_P = 0V, V_S = 9V, I_{LOAD} = 1mA	-	16	-	Ω
Temperature Coefficient of Switch Resistance P2	$T_{C(P2)}$	V_P = 0V, V_S = 3V, I_{LOAD} = 1mA	-	0.7	-	%/°C
Leakage Current (V_P to V_S)	$I_{L(PS)}$	V_P = 5V, V_S = 3V, I_{LOAD} = 10mA	-	0.01	20	nA
		At T_A = +85°C	-	35	-	nA
Leakage Current (V_P to V_S)	$I_{L(SP)}$	V_P = 0V, V_S = 3V, I_{LOAD} = 10mA	-	0.01	50	nA
		at T_A = +85°C	-	120	-	nA
Open Drain Output Saturation Voltages	V_{OPBAR}	V_P = 5V, V_S = 3V, I_{SINK} = 3.2mA, I_{LOAD} = 0mA	-	85	400	mV
		At T_A = 85°C	-	120	-	mV
		V_P = 9V, V_S = 3V, I_{SINK} = 3.2mA, I_{LOAD} = 0mA	-	50	-	mV
		V_P = 12V, V_S = 3V, I_{SINK} = 3.2mA I_{LOAD} = 0mA	-	40	-	mV
Open Drain Output Saturation Voltages	V_{OSBAR}	V_P = 0V, V_S = 3V, I_{SINK} = 3.2mA, I_{LOAD} = 0mA	-	150	400	mV
		at T_A = +85°C	-	210	-	mV
		V_P = 0V, V_S = 5V, I_{SINK} = 3.2mA I_{LOAD} = 0mA	-	85	-	mV
		V_P = 0V, V_S = 9V, I_{SINK} = 3.2mA I_{LOAD} = 0mA	-	50	-	mV

Electrical Specifications T_A = 25°C Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Leakage Currents of P_{BAR} and S_{BAR}	I_{LPBAR}	V_P = 0V, V_S = 15V, I_{LOAD} = 0mA	-	50	500	nA
		at T_A = +85°C	-	900	-	nA
	I_{LSBAR}	V_P = 15V, V_S = 0V, I_{LOAD} = 0mA	-	50	500	nA
		at T_A = +85°C	-	900	-	nA
Switchover Uncertainty for Complete Switching of Inputs and Open Drain Outputs	V_P - V_S	V_S = 3V, I_{SINK} = 3.2mA, I_{LOAD} = 15mA	-	±10	±50	mV

NOTE:

3. The Minimum input to output voltage can be determined by multiplying the load current by the switch resistance.

Typical Performance Curves

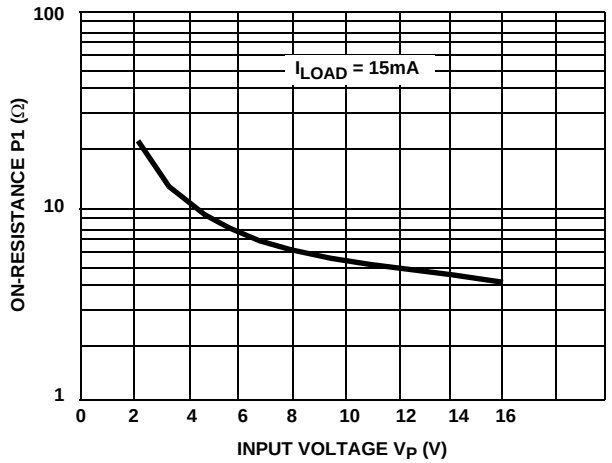

FIGURE 1. ON-RESISTANCE SWITCH P1 AS A FUNCTION OF INPUT VOLTAGE V_P

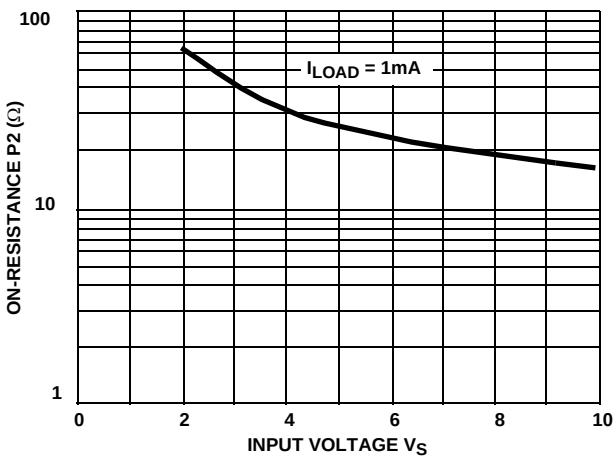

FIGURE 2. ON-RESISTANCE SWITCH P2 AS A FUNCTION OF INPUT VOLTAGE V_S

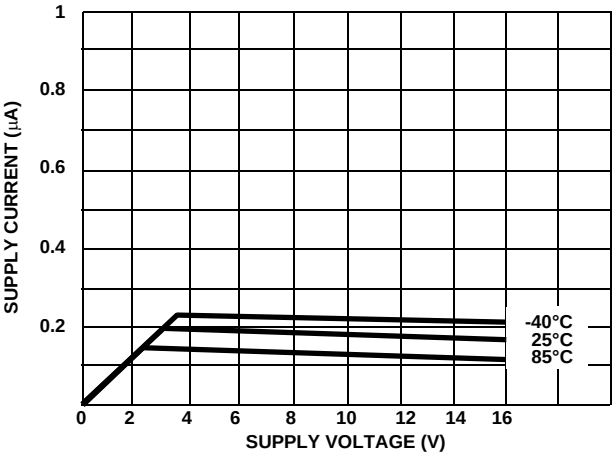

FIGURE 3. SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

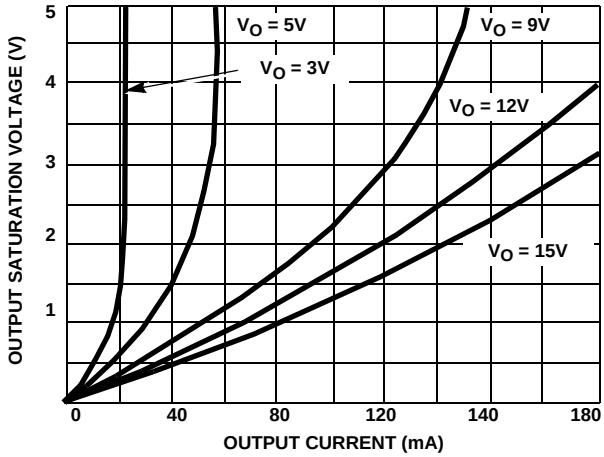

FIGURE 4. P_{BAR} OR S_{BAR} SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

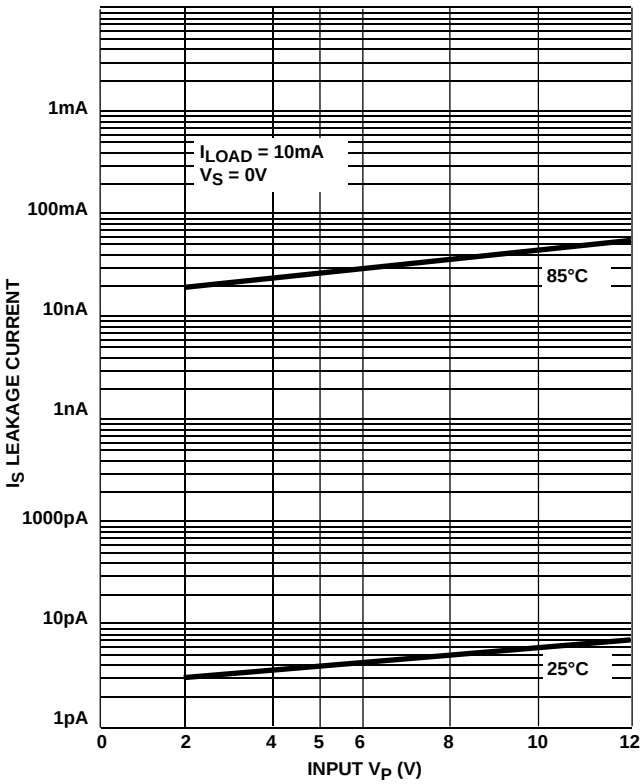

FIGURE 5. I_S LEAKAGE CURRENT V_P TO V_S AS A FUNCTION OF INPUT VOLTAGE

Detailed Description

As shown in the Functional Diagram, the ICL7673 includes a comparator which senses the input voltages V_P and V_S. The output of the comparator drives the first inverter and the open-drain N-Channel transistor P_{BAR}. The first inverter drives a large P-Channel switch, P_1, a second inverter, and another open-drain N-Channel transistor, S_{BAR}. The second inverter drives another large P-Channel switch P_2. The ICL7673, connected to a main and a backup power supply, will connect the supply of greater potential to its output. The circuit provides break-before-make switch action as it switches from main to backup power in the event of a main power supply failure. For proper operation, inputs V_P and V_S must not be allowed to float, and, the difference in the two supplies must be greater than 50mV. The leakage current through the reverse biased parasitic diode of switch P_2 is very low.

Output Voltage

The output operating voltage range is 2.5V to 15V. The insertion loss between either input and the output is a function of load current, input voltage, and temperature. This is due to the P-Channels being operated in their triode region, and, the ON-resistance of the switches is a function of output voltage V_O. The ON-resistance of the P-Channels have positive temperature coefficients, and therefore as temperature increases the insertion loss also increases. At low load currents the output voltage is nearly equal to the greater of the two inputs. The maximum voltage drop across switch P_1 or P_2 is 0.5V, since above this voltage the body-drain parasitic diode will become forward biased. Complete switching of the inputs and open-drain outputs typically occurs in 50µs.

Input Voltage

The input operating voltage range for V_P or V_S is 2.5V to 15V. The input supply voltage (V_P or V_S) slew rate should be limited to 2V per microsecond to avoid potential harm to the circuit. In line-operated systems, the rate-of-rise (or fall) of the supply is a function of power supply design. For battery applications it may be necessary to use a capacitor between the input and ground pins to limit the rate-of-rise of the supply voltage. A low-impedance capacitor such as a 0.047µF disc ceramic can be used to reduce the rate-of-rise.

Status Indicator Outputs

The N-Channel open drain output transistors can be used to indicate which supply is connected, or can be used to drive external PNP transistors to increase the power switching capability of the circuit. When using external PNP power transistors, the output current is limited by the beta and thermal characteristics of the power transistors. The application section details the use of external PNP transistors.

Applications

A typical discrete battery backup circuit is illustrated in Figure 6. This approach requires several components, substantial printed circuit board space, and high labor cost. It also consumes a fairly high quiescent current. The ICL7673 battery backup circuit, illustrated in Figure 7, will often replace such discrete designs and offer much better performance, higher reliability, and lower system manufacturing cost. A trickle charge system could be implemented with an additional resistor and diode as shown in Figure 8. A complete low power AC to regulated DC system can be implemented using the ICL7673 and ICL7663S micropower voltage regulator as shown in Figure 9.

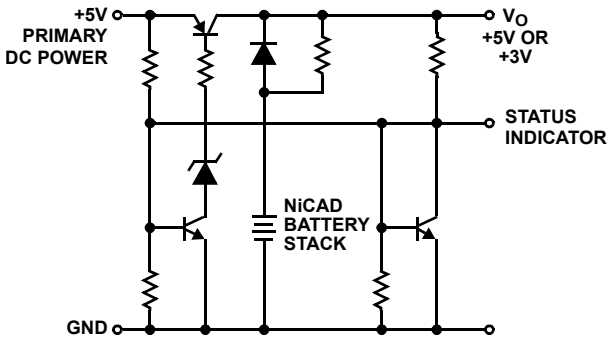

FIGURE 6. DISCRETE BATTERY BACKUP CIRCUIT

Applications for the ICL7673 include volatile semiconductor memory storage systems, real-time clocks, timers, alarm systems, and over/under the voltage detectors. Other systems requiring DC power when the master AC line supply fails can also use the ICL7673.

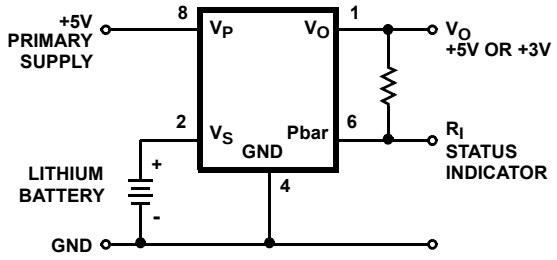

FIGURE 7. ICL7673 BATTERY BACKUP CIRCUIT

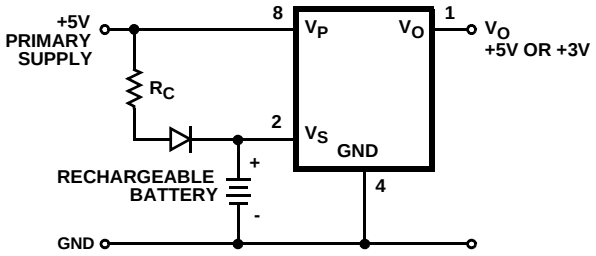

FIGURE 8. APPLICATION REQUIRING RECHARGEABLE BATTERY BACKUP

A typical application, as illustrated in Figure 12, would be a microprocessor system requiring a 5V supply. In the event of primary supply failure, the system is powered down, and a 3V battery is employed to maintain clock or volatile memory data. The main and backup supplies are connected to V_P and V_S, with the circuit output V_O supplying power to the clock or volatile memory. The ICL7673 will sense the main supply, when energized, to be of greater potential than V_S and connect, via its internal MOS switches, V_P to output V_O. The backup input, V_S will be disconnected internally. In the event of main supply failure, the circuit will sense that the backup supply is now the greater potential, disconnect V_P from V_O, and connect V_S.

Figure 11 illustrates the use of external PNP power transistors to increase the power switching capability of the circuit. In this application the output current is limited by the beta and thermal characteristics of the power transistors.

If hysteresis is desired for a particular low power application, positive feedback can be applied between the input V_P and open drain output S_{BAR} through a resistor as illustrated in Figure 12. For high power applications hysteresis can be applied as shown in Figure 13.

The ICL7673 can also be used as a clipping circuit as illustrated in Figure 14. With high impedance loads the circuit output will be nearly equal to the greater of the two input signals.

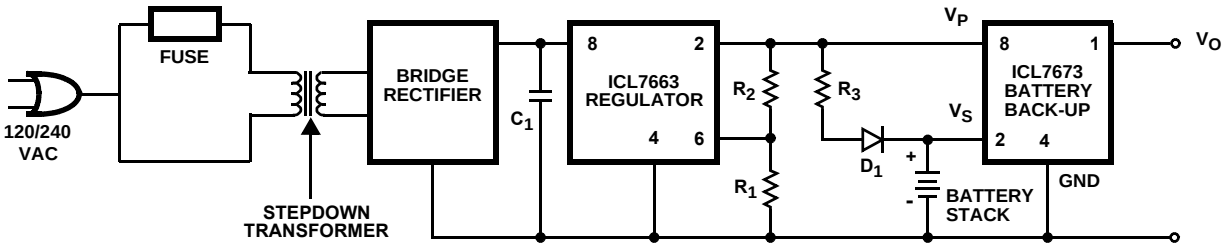

FIGURE 9. POWER SUPPLY FOR LOW POWER PORTABLE AC TO DC SYSTEMS

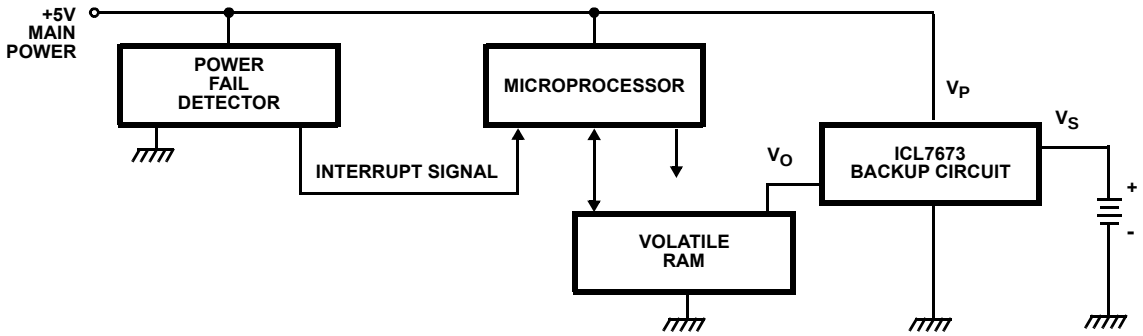

FIGURE 10. TYPICAL MICROPROCESSOR MEMORY APPLICATION

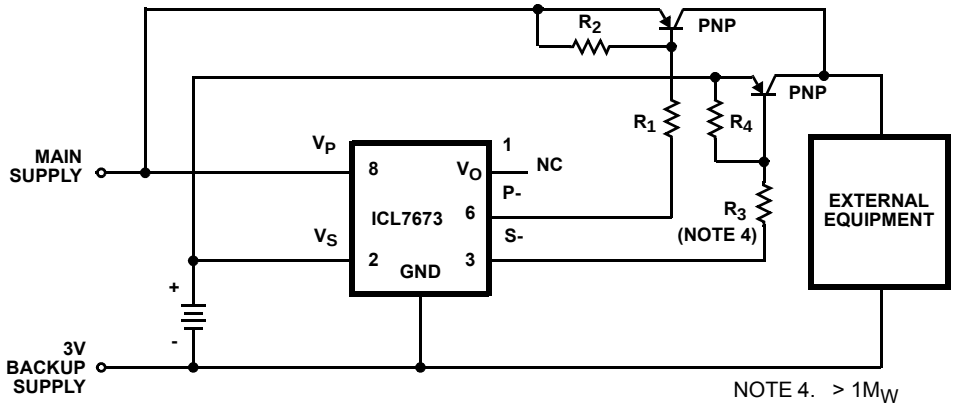

FIGURE 11. HIGH CURRENT BATTERY BACKUP SYSTEM

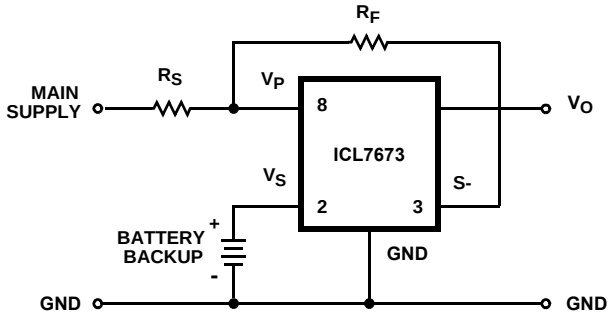

FIGURE 12. LOW CURRENT BATTERY BACKUP SYSTEM WITH HYSTERESIS

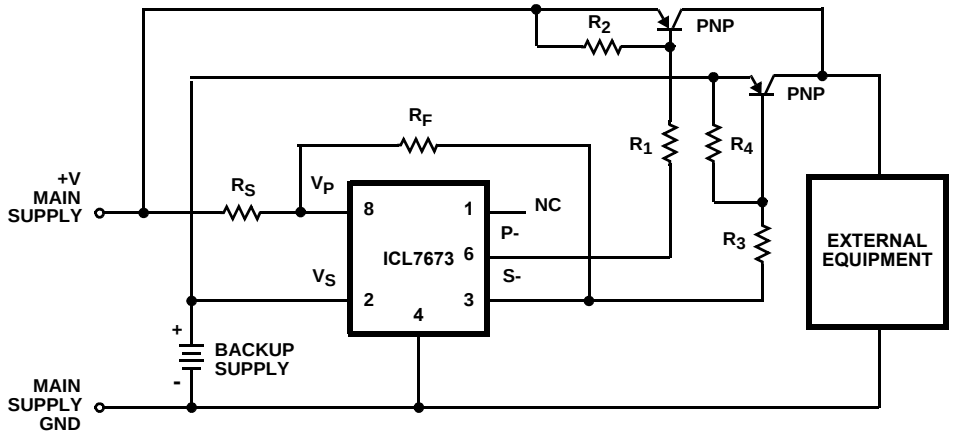

FIGURE 13. HIGH CURRENT BACKUP SYSTEM WITH HYSTERESIS

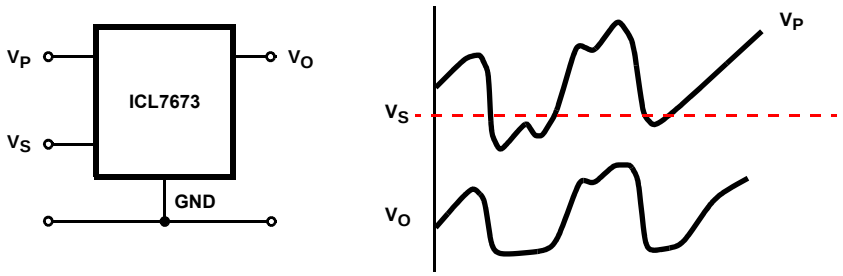

FIGURE 14. CLIPPLING CIRCUITS

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