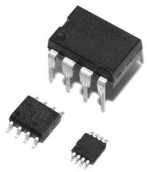


SLUS495H − SEPTEMBER 2001 − REVISED AUGUST 2007

ADVANCED 8-PIN LOAD-SHARE CONTROLLER

FEATURES

- **High Accuracy, Better Than 1% CurrentShare Error at Full Load**
- **High-Side or Low-Side (GND Reference) Current-Sense Capability**
- **Ultra-Low Offset Current Sense Amplifier**
- **Single Wire Load Share Bus**
- **Full Scale Adjustability**
- **Intel® SSI LoadShare Specification Compliant**
- **Disconnect from Load Share Bus at Stand-By**
- **Load Share Bus Protection Against Shorts to GND or to the Supply Rail**
- **8-Pin MSOP Package Minimizes Space**
- **Lead-Free Assembly**

SYSTEM CONFIGURATIONS

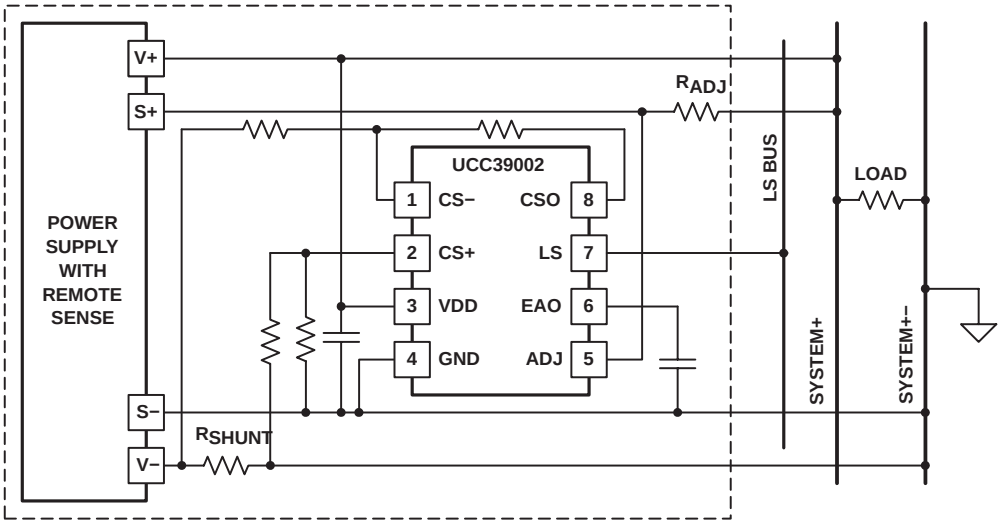
- **Modules With Remote Sense Capability**
- **Modules With Adjust Input**
- **Modules With Both Remote Sense and Adjust Input**
- **In Conjunction With the Internal Feedback E/A of OEM Power Supply Units**

DESCRIPTION

The UCC39002 is an advanced, high performance and low cost loadshare controller that provides all necessary functions to parallel multiple independent power supplies or dc-to-dc modules. Targeted for high reliability applications in server, workstation, telecom and other distributed power systems, the controller is suitable for N+1 redundant systems or high current applications where off-the-shelf power supplies need to be paralleled.

The BiCMOS UCC39002 is based on the automatic master/slave architecture of the UC3902 and UC3907 load share controllers. It provides better than 1% current share error between modules at full load by using a very low offset post-package-trimmed current-sense amplifier and a high-gain negative feedback loop. And with the amplifier's common mode range of 0-V to the supply rail, the current sense resistor, R_{SHUNT}, can be placed in either the GND return path or in the positive output rail of the power supply.

TYPICAL LOW-SIDE CURRENT SENSING APPLICATION



DESCRIPTION (continued)

The functionality of the UCC29002/1 differs slightly compared to the UCC39002. The UCC39002 will force the maximum adjustment range at start up to quickly engage load sharing; the UCC29002/1 ADJ amplifier will operate in a linear mode during start up, resulting in a more gradual load sharing at turn on.

During transient conditions while adding or removing power supplies, the UCC39002 protects the system by keeping the load share bus disconnected from the remaining supplies. By disabling the adjust function in case a short of the load share bus occurs to either GND or the supply rail, it also provides protection for the system against erroneous output voltage adjustment.

The UCC39002 also meets Intel's SSI (Server System Infrastructure) loadshare specifications of a single-line load share bus and scalable load share voltage for any level of output currents.

The UCC39002 family is offered in 8-pin MSOP (DGK), SOIC (D), and PDIP (P) packages.

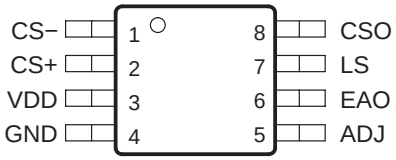
absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡§

Supply voltage, current limited (V_{DD}) . . . . . −0.3 V to 15 V
Supply voltage, voltage source (V_{DD}) . . . . . −0.3 V to 13.5 V
Input voltage, current sense amplifier (V_{CS+}, V_{CS-}) . . . . . −0.3 V to V_{DD} + 0.3 V
Current sense amplifier output voltage (V_{CSO}) . . . . . −0.3 V to V_{DD}
Load share bus voltage (V_{LS}) . . . . . −0.3 V to V_{DD}
Supply current (I_{DD} + I_{ZENER}) . . . . . 10 mA
Adjust pin input voltage (V_{ADJ}) . . . . . V_{EAO} +1 V < V_{ADJ} ≤ V_{DD}
Adjust pin sink current (I_{ADJ}) . . . . . 6 mA
Operating junction temperature range, T_J . . . . . −55°C to 150°C
Storage temperature range T_{stg} . . . . . −65°C to 150°C
Lead Temperature, T_{sol} (Soldering, 10 seconds) . . . . . 300°C

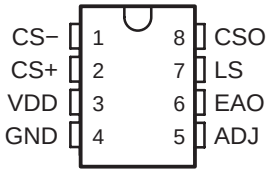
‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

§ All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

SOIC (D) OR MSOP (DGK) PACKAGE
(TOP VIEW)



PDIP (P) PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

$T_A = T_J$	PACKAGED DEVICES		
	SOIC−8 (D)†	**MSOP−8 (DGK)†**	**PDIP−8 (P)**
−40°C to 105°C	UCC29002D	UCC29002DGK	UCC29002P
	UCC29002D/1	UCC29002DGK/1	NA
0°C to 70°C	UCC39002D	UCC39002DGK	UCC39002P

† The D and DGK packages are available taped and reeled. Add R suffix to device type (e.g. UCC39002DR) to order quantities of 2,500 devices per reel.

electrical characteristics V_{DD} = 12 V, 0°C < T_A < 70°C for the UCC39002, −40°C < T_A < 105°C for the UCC29002 and UCC29002/1, T_A = T_J (unless otherwise noted)

general

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply current	LS with no load, ADJ = 5 V		2.5	3.5	mA
VDD clamp voltage	IDD = 6 mA	13.50	14.25	15.00	V

undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Start-up voltage(1)		4.175	4.375	4.575	V
Hysteresis		0.200	0.375	0.550	

current sense amplifier

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IO}	Input offset voltage	T_A = 25°C, V_{IC} = 0.5 V or 11.5 V, V_{CSO} = 5 V	−100		100	µV
		Over-temperature variation		±10		µV/°C
A_V	Gain		75	90		dB
CMRR	Common mode rejection ratio		75	90		
I_{BIAS}	Input bias current (CS+, CS−)		−0.6		0.6	µA
V_{OH}	High-level output voltage (CSO)	0.1 V ≤ ([CS+] − [CS−]) ≤ 0.4 V, I_{OUT_CSO} = 0 mA	10.7	11.0	11.8	V
V_{OL}	Low-level output voltage (CSO)	−0.4 V ≤ ([CS+] − [CS−]) ≤ 0.1 V, I_{OUT_CSO} = 0 mA	0.00	0.10	0.15	
I_{OH}	High-level output current (CSO)	V_{CSO} = 10 V	−1	−1.5		mA
I_{OL}	Low-level output current (CSO)	V_{CSO} = 1 V	1	1.5		
GBW	Gain bandwidth product(2)			2		MHz

load share driver (LS)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{RANGE}	Input voltage range		0		10	V
V_{OUT}	Output voltage	V_{CSO} = 1 V	0.995	1	1.005	
		V_{CSO} = 10 V	9.995	10	10.005	
V_{OL}	Low-level output voltage	V_{CSO} = 0 V, I_{OUT_LS} = 0 mA	0.00	0.10	0.15	
V_{OH}	High-level output voltage(2)		V_{DD}−1.7			
I_{OUT}	Output current	0.5 V ≤ V_{LS} ≤ 10 V	−1	−1.5		mA
I_{SC}	Short circuit current	V_{LS} = 0 V, V_{CSO} = 10 V	−10	−20		
V_{SHTDN}	Driver shutdown threshold	V_{CS-} − V_{CS+}	0.3	0.5	0.7	V

load share bus protection

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{ADJ}	Adjust amplifier current	V_{CSO} = 2 V, V_{LS} = V_{DD}, V_{EAO} = 2 V, V_{ADJ} = 5 V	0	5	10	µA
		V_{CSO} = 2 V, V_{LS} = 0 V, V_{EAO} = 2 V, V_{ADJ} = 5 V	0	5	10	

(1) Enables the load share bus at start-up.
(2) Ensured by design. Not production tested.

electrical characteristics V_{DD} = 12 V, 0°C < T_A < 70°C for the UCC39002, −40°C < T_A < 105°C for the UCC29002 and UCC29002/1, T_A = T_J (unless otherwise noted) (continued)

error amplifier

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{OH}	High-level output voltage	$I_{OUT\ EAO}$ = 0 mA	3.50	3.65	3.80	V
g_M	Transconductance	I_{EAO} = ± 50 µA		14		mS
I_{OH}	High-level output current	V_{LS} − V_{CSO} = 0.4 V R_{EAO} = 2.2 kΩ	0.70	0.85	1.00	mA

ADJ buffer

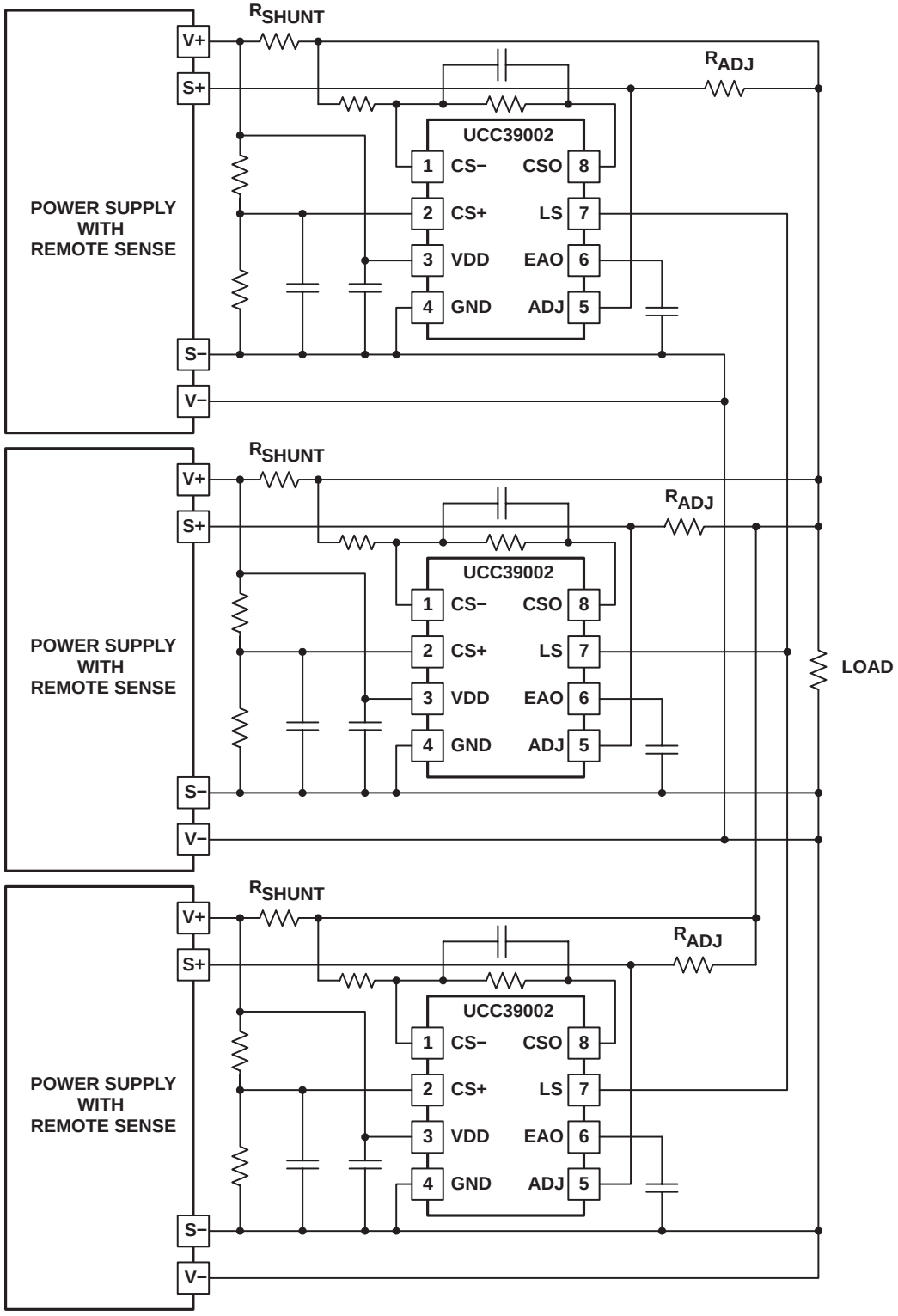
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IO}	Input offset voltage(2)		V_{ADJ} = 1.5 V, V_{EAO} = 0 V,		−60		mV
I_{SINK}	Sink current		V_{ADJ} = 5.0 V, V_{EAO}= 0 V	0	5	10	µA
I_{SINK}	Sink current	T_A = 25°C	V_{ADJ} = 5.0 V, V_{EAO}= 2.0 V LS = floating	3.60	3.95	4.30	mA
		0°C ≤ T_A ≤ 70°C		3.45	3.95	4.45	
		−40°C ≤ T_A ≤ 105°C		3.35	3.95	4.55	

(1) Enables the load share bus at start-up.
(2) Ensured by design. Not production tested.

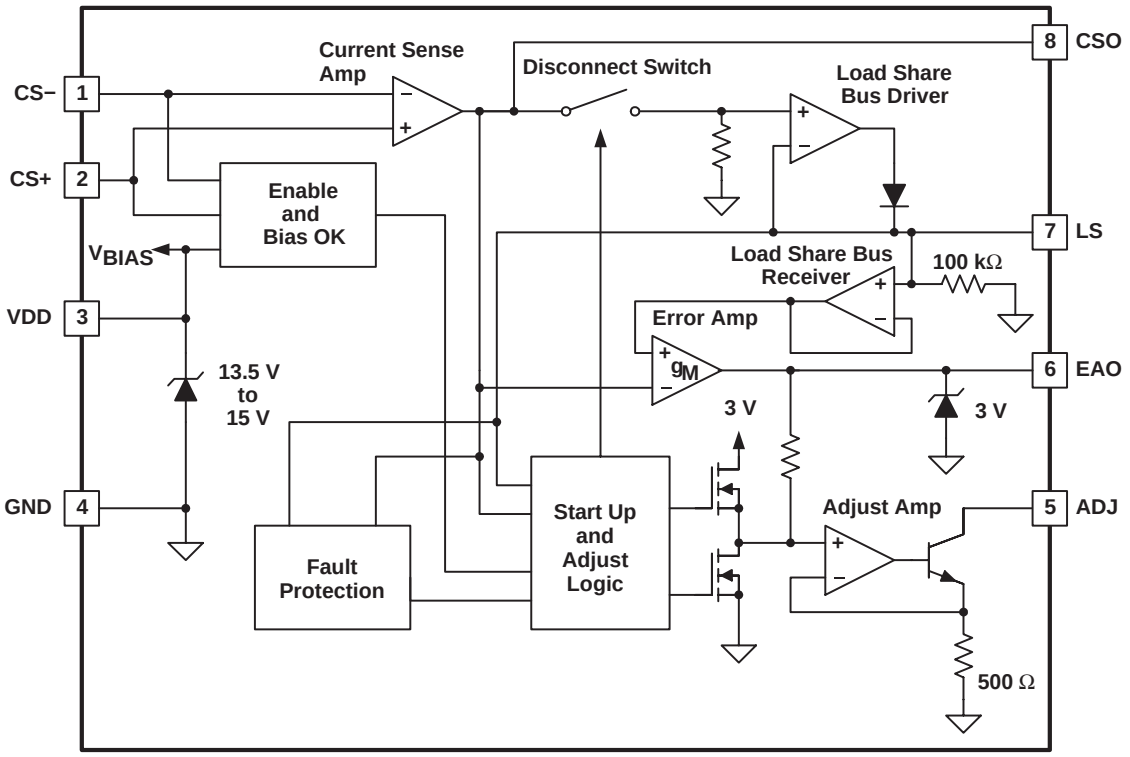
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ADJ	5	O	Adjust amplifier output. This is the buffered output of the error amplifier block to adjust output voltage of the power supply being controlled. This pin must always be connected to a voltage equal to or greater than V_{EAO} + 1 V.
CS−	1	I	Current sense amplifier inverting input.
CS+	2	I	Current sense amplifier non-inverting input.
CSO	8	O	Current sense amplifier output.
EAO	6	O	Output for load share error amplifier. (Transconductance error amplifier.)
GND	4	−	Ground. Reference ground and power ground for all device functions. Return the device to the low current sense− path of the converter.
LS	7	I/O	Load share bus. Output of the load share bus driver amplifier.
VDD	3	I	Power supply providing bias to the device. Bypass with a good quality, low ESL 0.1-µF to 1-µF, maximum, capacitor as close to the VDD pin and GND as possible.

typical high-side current sensing application



functional block diagram



FUNCTIONAL DESCRIPTION

differential current sense amplifier (CS+, CS−, CSO)

The UCC39002 features a high-gain and high-precision amplifier to measure the voltage across a low-value current sense resistor. Since the amplifier is fully uncommitted, the current sense gain is user programmable. The extremely low input offset voltage of the UCC39002 current sense amplifier makes it suitable to measure current information across a low value sense resistor. Furthermore, the input common mode range includes ground and the positive supply rail of the UCC39002 (V_{DD}). Accordingly, the current sense resistor can be placed in the ground return path or in the positive output rail of the power supply V_O as long as $V_O \leq V_{DD}$. The current sense amplifier is not unity gain stable and must have a minimum gain of three.

load share bus driver amplifier (CSO)

This is a unity-gain buffer amplifier to provide separation between the load share bus voltage and the output of the current sense amplifier. The circuit implements an ideal diode with virtually 0 V forward voltage drop by placing the diode inside the feedback loop of the amplifier. The diode function is used to automatically establish the role of the master module in the system. The UCC39002 which is assigned to be the master uses the load share bus driver amplifier to copy its output current information on to the load share bus.

All slave units, with lower output current levels by definition, have this “ideal diode” reversed biased ($V_{CSO} < V_{LS}$). Consequently, the V_{CSO} and V_{LS} signals will be separated. That allows the error amplifier of the UCC39002 to compare its respective module’s output current to the master module’s output current and make the necessary corrections to achieve a balanced current distribution.

Since the bus is always driven by a single load share bus driver amplifier, the number of modules (*n*) are limited by the output current capability of the amplifier according to:

$$n = \frac{100\ k\Omega \times I_{OUT,MIN}}{V_{LS,FULL\_SCALE}} \quad (1)$$

where 100 kΩ is the input impedance of the LS pin as shown in the block diagram, $I_{OUT,MIN}$ is given in the data sheet and $V_{LS,FULL\_SCALE}$ is the maximum voltage on the load share bus at full load.

Note that the number of parallel units can be increased by reducing the full scale bus voltage, i.e. by reducing the current sense gain.

load share bus receiver amplifier (LS)

The load share bus receiver amplifier is a unity gain buffer monitoring the load share bus voltage. Its primary purpose is to ensure that the load share bus is not loaded by the internal impedances of the UCC39002. The LS pin is already internally compensated and has an internal 15-kHz filter. Adding external capacitance, including stray capacitance, should be avoided to maintain stability.

FUNCTIONAL DESCRIPTION

error amplifier (EAO)

As pictured in the block diagram, the UCC39002 employs a transconductance also called g_M type error amplifier. The g_M amplifier was chosen because it requires only one pin, the output to be accessible for compensation.

The purpose of the error amplifier is to compare the average, per module current level to the output current of the respective module controlled by the UCC39002. It is accommodated by connecting the buffered V_{LS} voltage to its non−inverting input and the V_{CSO} signal to its inverting input. If the average per module current, represented by the load share bus is higher than the module's own output current, an error signal will be developed across the compensation components connected between the EAO pin and ground. The error signal is than used by the adjust amplifier to make the necessary output voltage adjustments to ensure equal output currents among the parallel operated power supplies.

In case the UCC39002 assumes the role of the master load share controller in the system or it is used in conjunction with a stand alone power module, the measured current signal on V_{CSO} is approximately equal to the V_{LS} voltage. To avoid erroneous output voltage adjustment, the input of the error amplifier incorporates a typically 25 mV offset to ensure that the inverting input of the error amplifier is biased higher than the non−inverting input. Consequently, when the two signals are equal, there will be no adjustment made and the initial output voltage set point is maintained.

adjust amplifier output (ADJ)

A current proportional to the error voltage V_{EAO} on pin 6 is sunk by the ADJ pin. This current flows through the adjust resistor R_{ADJ} and changes the output voltage of the module controlled by the UCC39002. The amplitude of the current is set by the 500-Ω internal resistor between ground and the emitter of the amplifier's open collector output transistor according to Figure 1. The adjust current value is given as:

$$I_{ADJ} = \frac{V_{EAO}}{500\ \Omega} \tag{2}$$

At the master module V_{EAO} is 0 V, thus the adjust current must be zero as well. This ensures that the output voltage of the master module remains at its initial output voltage set point at all times.

Furthermore, at insufficient bias level, during a fault or when the UCC39002 is disabled, the non-inverting input of the adjust amplifier is pulled to ground to prevent erroneous adjustment of the module's output voltage by the load share controller.

FUNCTIONAL DESCRIPTION

enable function (CS+, CS−)

The two inputs of the current sense amplifier are also used for implementing an ENABLE function. During normal operation CS− = CS+ and the internal offset added between the CS− voltage and the inverting input of the enable comparator ensures that the UCC39002 is always enabled. By forcing the CS− pin approximately 0.5-V above the CS+ pin, the UCC39002 can be forced into a disable mode. While disabled, the UCC39002 disconnects itself from the load share bus and its adjust current is zero.

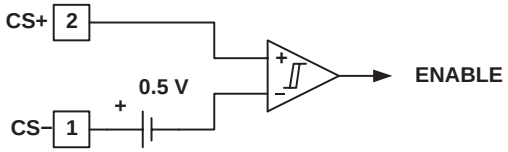


Figure 1. Enable Comparator

fault protection

Accidentally, the load share bus might be shorted to ground or to the positive bias voltage of the UCC39002. These events might result in erroneous output voltage adjustment. For that reason, the load share bus is continuously monitored by a window comparator as shown in Figure 2.

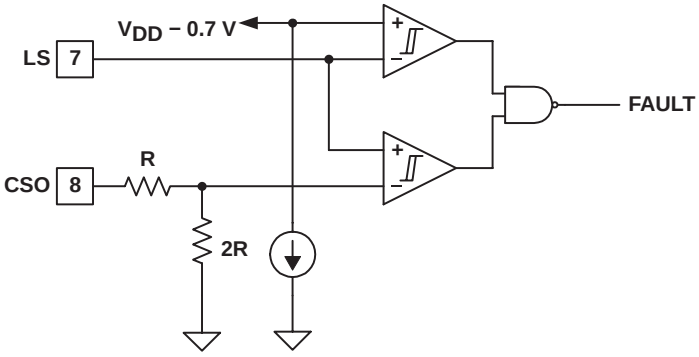


Figure 2. Fault Protection Comparators

The FAULT signal is handled by the start up and adjust logic which pulls the non-inverting input of the adjust amplifier low when the FAULT signal is asserted.

FUNCTIONAL DESCRIPTION

start up and adjust logic

The start up and adjust logic responds to unusual operating conditions during start up, fault and disable. Under these circumstances the information obtainable by the error amplifier of the UCC39002 is not sufficient to make the right output voltage adjustment, therefore the adjust amplifier is forced to certain known states. Similarly, the driver amplifier of UCC39002 is disabled during these conditions.

In the UCC39002/UCC29002, during start up, the load share driver amplifier is disabled by the disconnect switch and the adjust amplifier is forced to sink the maximum current through the adjust resistor. This operating mode ensures that the module controlled by the UCC39002 will be able to quickly engage in sharing the load current since its output will be adjusted to a sufficiently high voltage immediately at turn on. Both the load share driver and the adjust amplifiers revert to normal operation as soon as the measured current exceeds 80% of the average per module current level represented by the LS bus voltage. The UCC29002/1 does not have this logic at start up. In this way, the UCC29002/1 will not adjust the output of the module to its maximum adjustment range at turn on and engages load sharing at more moderate rate.

In case of a fault shorting the load share bus to ground or to the bias of the UCC39002 the load share bus driver and the adjust amplifiers are disabled. The same action takes place when the UCC39002 is disabled using the CS+ and CS− pins or when the bias voltage is below the minimum operating voltage.

bias and bias OK circuit (VDD)

The UCC39002 is built on a 15-V, high performance BiCMOS process. Accordingly the maximum voltage across the V_{DD} and GND pins (pin 3 and 4 respectively) is limited to 15 V. The recommended maximum operating voltage is 13.5 V which corresponds to the tolerance of the on-board 14.2-V Zener clamp circuit. In case the bias voltage could exceed the 13.5-V limit, the UCC39002 should be powered through a current limiting resistor. The current into the V_{DD} pin must be limited to 10 mA as listed in the absolute maximum ratings table.

The bypass capacitor for VDD is also the compensation for the input active clamp of the device and, as such, must be placed as close to the device pins (VDD and GND) as possible, using a good quality low ESL capacitor, including trace length. The device is optimized for a capacitor value of 0.1 μF to 1 μF.

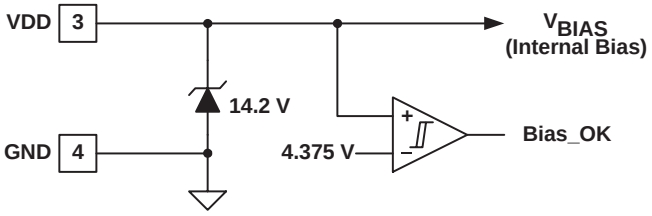


Figure 3. V_{DD} Clamp and Bias Monitor

FUNCTIONAL DESCRIPTION

The UCC39002 does not have an undervoltage lockout circuit. The bias OK comparator works as an enable function with a 4.375-V threshold. While V_{DD} < 4.375 V the load share control functions are disabled. While this might be inconvenient for some low voltage applications it is necessary to ensure high accuracy. The load share accuracy is dependent on working with relatively large signal amplitudes on the load share bus. If the internal offsets, current sense error and ground potential difference between the UCC39002 controllers are comparable in amplitude to the load share bus voltage, they can cause significant current distribution error in the system. The maximum voltage on the load share bus is limited approximately 1.7-V below the bias voltage level (V_{DD}) which would result in an unacceptably low load share bus amplitude therefore poor accuracy at low V_{DD} levels. To circumvent this potential design problem, the UCC39002 won't operate below the above mentioned 4.375-V bias voltage threshold. If the system does not have a suitable bias voltage available to power the UCC39002, it is recommended to use an inexpensive charge pump which can generate the bias voltage for all the UCC39002s in the load share system.

The maximum V_{DD} of the UCC39002 is 15 V. For higher-voltage applications, use the application solution as recommended in Figure 4. A Zener clamp on the VDD pin is provided internally so the device can be powered from higher voltage rails using a minimum number of external components.

The CSA inputs must be adjusted so as to not exceed their absolute maximum voltage ratings.

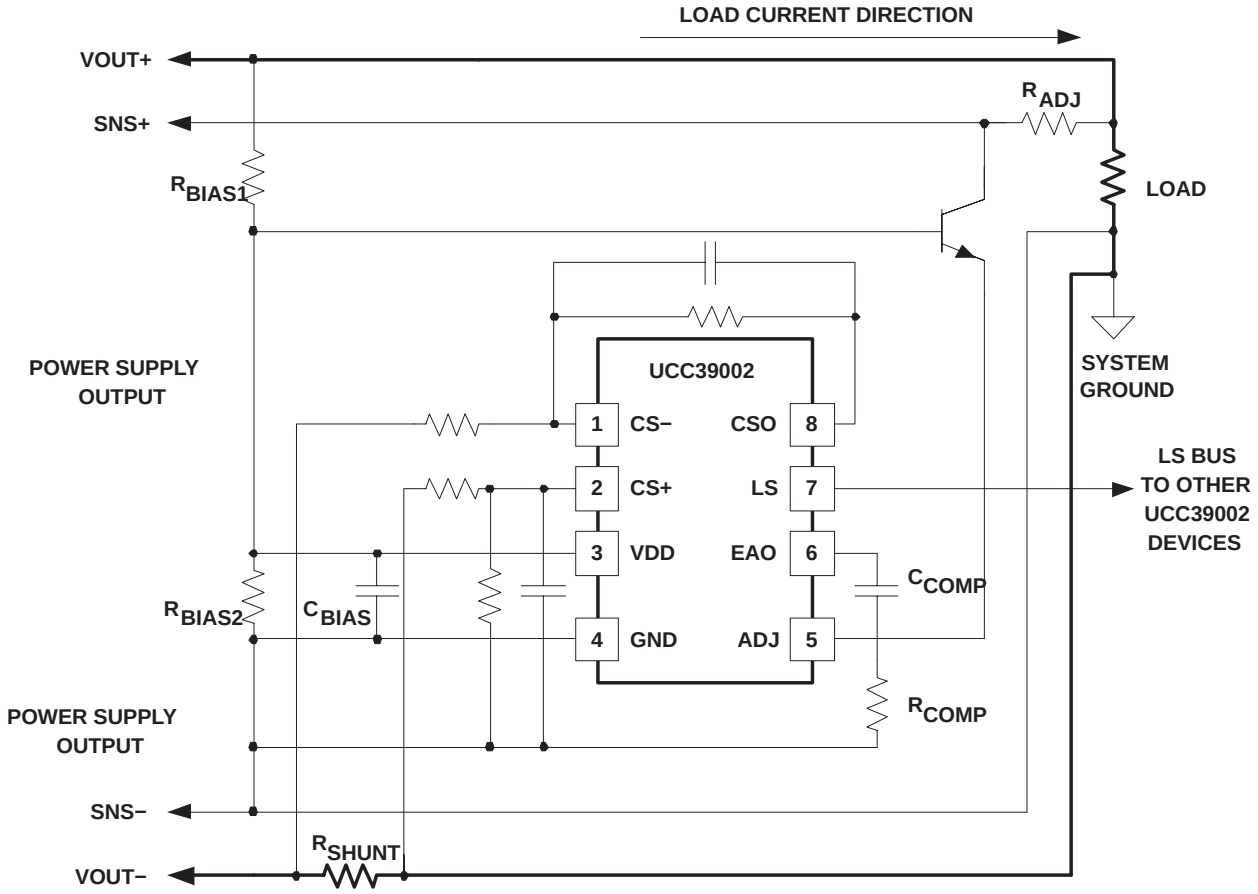


Figure 4. High Voltage Application

DESIGN PROCEDURE

The following is a practical step-by-step design procedure on how to use the UCC39002 to parallel power modules for load sharing.

paralleling the power modules

- V_{OUT} = nominal output voltage of the modules to be paralleled
- $I_{OUT(max)}$ = maximum output current of each module to be paralleled
- ΔV_{ADJ} = maximum output voltage adjustment range of the power modules to be paralleled
- N = number of modules

NOTE: The power modules to be paralleled must be equipped with true remote sense or access to the feedback divider of the module's error amplifier.

A typical high side application for a single module is shown in Figure 5 and is repeated for each module to be paralleled.

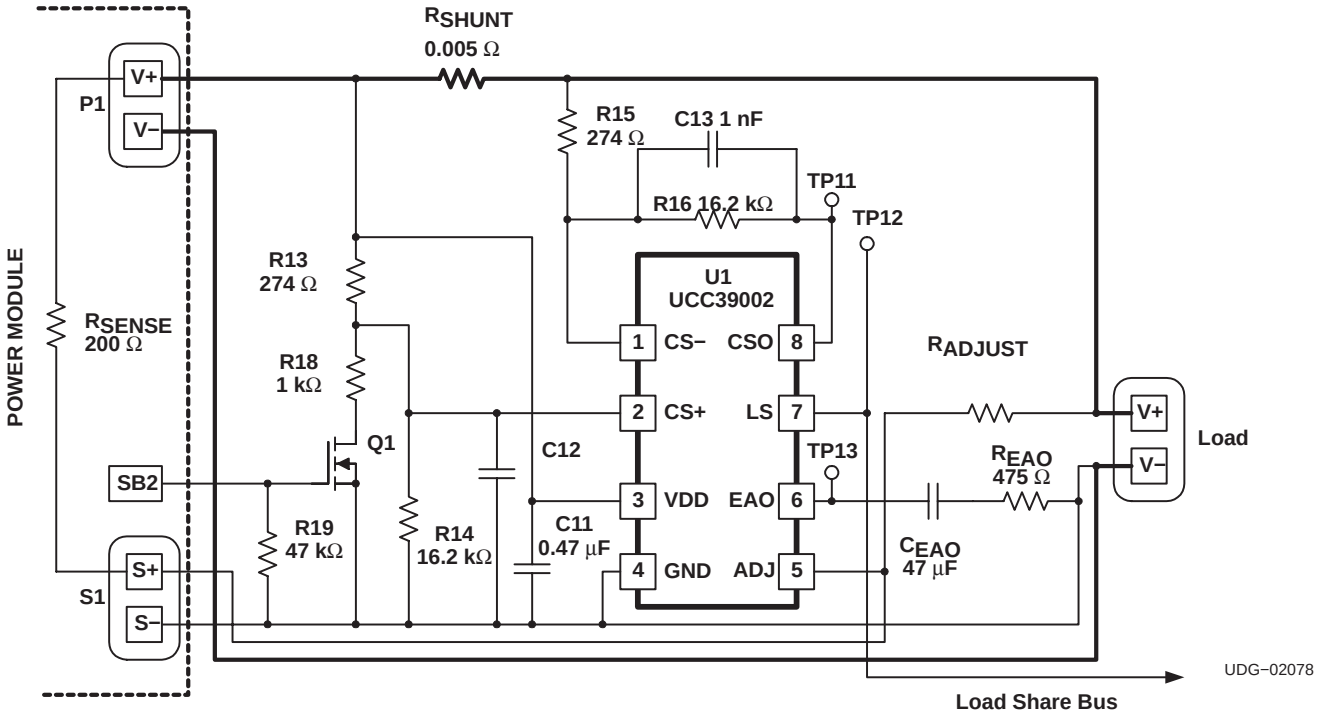


Figure 5. Typical High-Side Application for Single Power Module

In Figure 5, P1 represents the output voltage terminals of the module, S1 represents the remote sense terminals of the module, and a signal on the SB2 terminal will enable the disconnect feature of the device. The load share bus is the common bus between all of the paralleled load share controllers. VDD must be decoupled with a good quality ceramic capacitor returned directly to GND.

DESIGN PROCEDURE

measuring the modules' loop

Using the configuration in Figure 6, measure the unity gain crossover frequency of the power modules to be paralleled. A typical resultant bode plot is shown in Figure 7.

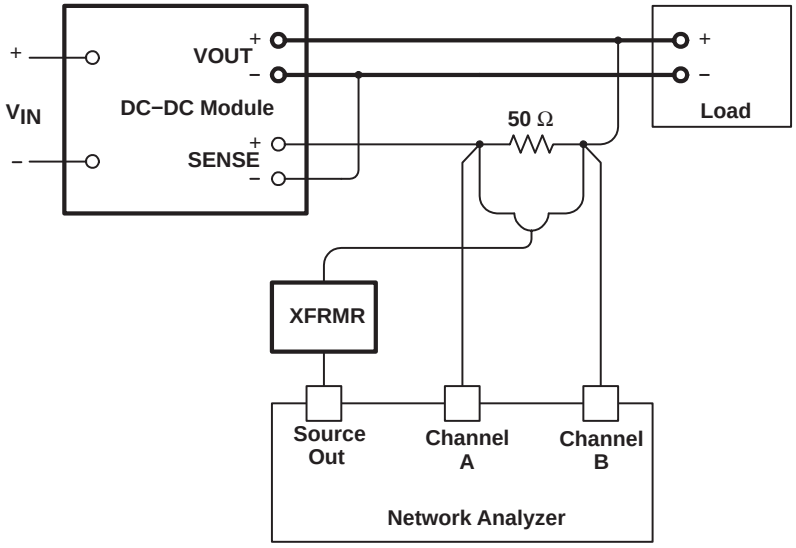


Figure 6. Unity Gain Crossover Frequency Measurement Connection Diagram

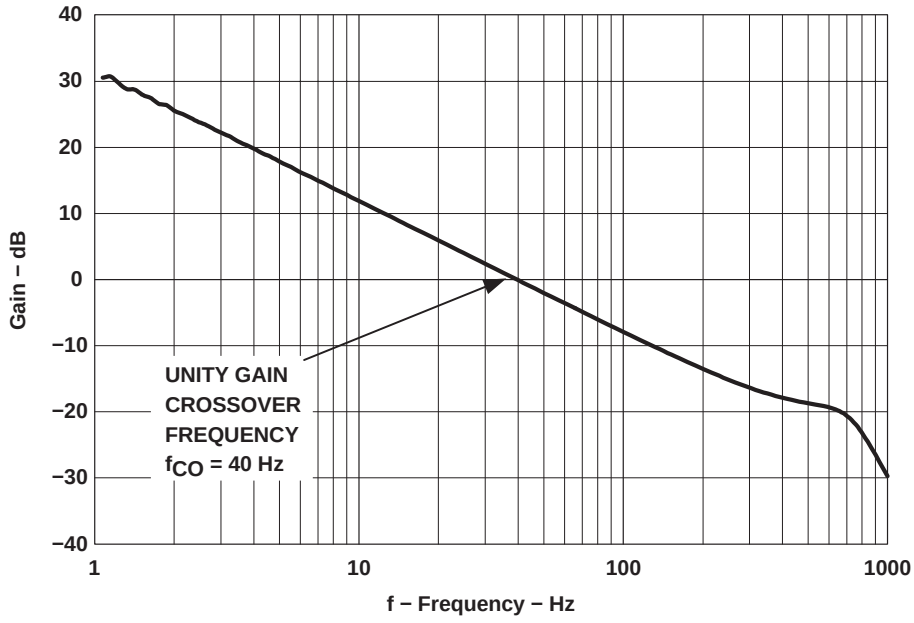


Figure 7. Power Module Bode Plot

DESIGN PROCEDURE

the shunt resistor

Selection of the shunt resistor is limited by its voltage drop at maximum module output current. This voltage drop should be much less than the voltage adjustment range of the module:

$$I_{OUT(max)} \times R_{SHUNT} << \Delta V_{ADJ(max)} \quad (3)$$

Other limitations for the sense resistor are the desired minimum power dissipation and available component ratings.

the CSA gain

The gain of the current sense amplifier is configured by the compensation components between Pin 1, CS−, and Pin 8, CSO, of the load share device. The voltage at the CSO pin is limited by the saturation voltage of the internal current sense amplifier and must be at least two volts less than VDD:

$$V_{CSO(max)} < VDD - 2\ V \quad (4)$$

The maximum current sense amplifier gain is equal to:

$$A_{CSA} = \frac{V_{CSO}}{\left(R_{SHUNT} \times I_{OUT(max)}\right)} \quad (5)$$

Referring to Figure 5, the gain is equal to R16/R15 and a high-frequency pole, configured with C13, is used for noise filtering. This impedance is mirrored at the CS+ pin of the differential amplifier as shown.

The current sense amplifier output voltage, V_{CSO}, serves as the input to the unity gain LS bus driver. The module with the highest output voltage forward biases the internal diode at the output of the LS bus driver and determine the voltage on the load share bus, V_{LS}. The other modules act as slaves and represent a load on the I_{VDD} of the module due to the internal 100-kΩ resistor at the LS pin. This increase in supply current for the master module is equal to N(V_{LS}/100 kΩ).

DESIGN PROCEDURE

determining R_{ADJUST}

The Sense+ terminal of the module is connected to the ADJ pin of the load-share controller. By placing a resistor between this ADJ pin and the load, an artificial Sense+ voltage is created from the voltage drop across R_{ADJUST} due to the current sunk by the internal NPN transistor. The voltage at the ADJ pin must be maintained at approximately 1 V above the voltage at the EAO pin. This is necessary in order to keep the transistor at the output of the internal adjust amplifier from saturating. To fulfill this requirement, R_{ADJUST} is first calculated using the following equation:

$$R_{ADJUST} \geq \frac{\left(\Delta V_{ADJ(max)} - I_{OUT(max)} \times R_{SHUNT}\right) \times 500\ \Omega}{\left[V_{OUT} - \Delta V_{ADJ(max)} - 1\ V - \left(\frac{\Delta V_{ADJ(max)}}{R_{SENSE}} \times 500\ \Omega\right)\right]} \quad (6)$$

Where R_{SHUNT} is the current sense resistor, and R_{SENSE} is the internal resistance between V_{OUT+} and SENSE+ within the module.

Also needed for consideration is the actual adjust pin current. The maximum sink current for the ADJ pin, I_{ADJmax}, is 6 mA as determined by the internal 500-Ω emitter resistor and 3-V clamp. The value of adjust resistor, R_{ADJUST}, is based upon the maximum adjustment range of the module, ΔV_{ADJmax}. This adjust resistor is determined using the following formula:

$$R_{ADJUST} \geq \frac{\left[\Delta V_{ADJ(max)} - I_{OUT(max)} \times R_{SHUNT}\right]}{I_{ADJ(max)} - \frac{\Delta V_{ADJ(max)}}{R_{SENSE}}} \quad (7)$$

By selecting a resistor that meets both of these minimum requirements, the ADJ pin will be at least 1 V greater than the EAO voltage and the adjust pin sink current will not exceed its 6 mA maximum.

DESIGN PROCEDURE

error amplifier compensation

The total load-share loop unity-gain crossover frequency, f_{CO}, should be set at least one decade below the measured crossover frequency of the paralleled modules previously measured, $f_{CO(module)}$. (See Figure 7) Compensation of the transconductance error amplifier is accomplished by placing the compensation resistor, R_{EAO}, and capacitor, C_{EAO}, between EAO and GND. The values of these components is determined using equations (8) and (13).

$$C_{EAO} = \left(\frac{g_M}{2\pi f_{CO}}\right)\left(A_{CSA}\right)\left(A_V\right)\left(A_{ADJ}\right)\left(\left|A_{PWR}\left(f_{CO}\right)\right|\right) \tag{8}$$

Where:

- g_M is the transconductance of the error amplifier, typically 14 mS,
- f_{CO} is equal to the desired crossover frequency in Hz of the load share loop, typically f_{CO} (module)/10,
- A_{CSA} is the CSA gain,
- A_V is the voltage gain,
- A_{ADJ} is the gain associated with the adjust amplifier,
- $|A_{PWR}(f_{CO})|$ is the measured gain of the power module at the desired load share crossover frequency, f_{CO}, converted to V/V from dB

$$A_{CSA} = \frac{R16}{R15} \tag{9}$$

$$A_V = \frac{R_{SHUNT}}{R_{LOAD}},\ R_{LOAD} = \frac{V_{OUT}}{I_{OUT(max)}} \tag{10}$$

$$A_{ADJ} = \frac{R_{ADJUST} \times R_{SENSE}}{\left(R_{ADJUST} + R_{SENSE}\right) \times 500\ \Omega} \tag{11}$$

$$\left|A_{PWR}\left(f_{CO}\right)\right| = 10\left(\frac{G_{MODULE}\left(f_{CO}\right)}{20}\right) \tag{12}$$

Where $G_{MODULE}(f_{co})$ is the measured value of the gain from Figure 7, at the desired crossover frequency.

Once the C_{EAO} capacitor is determined, R_{EAO} is selected to achieve the desired loop response:

$$R_{EAO} = \sqrt{\left(\frac{1}{gm \times \left|A_{PWR}\left(f_{CO}\right)\right| \times A_V \times A_{CSA} \times A_{ADJ}}\right)^2 - \left(\frac{1}{2\pi\left(f_{CO}\right)\left(C_{EAO}\right)}\right)^2} \tag{13}$$

DESIGN PROCEDURE

references

For further details, refer to the following document:

- Reference Design, *48-V_{IN}, 12-V_{OUT} Loadshare System Using UCC39002 with Three DC/DC PH-100S4 Modules*", Texas Instruments Literature No. SLUA270

For a more complete description of general load sharing toics, refer to the following documents.

- Application Note, *The UC3902 Load Share Controller and Its Performance in Distributed Power Systems,* TI Literature No. SLUA128
- Application Note, *UC3907 Load Share IC Simplifies Parallel Power Supply Design*, TI Literature No. SLUA147

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UCC29002D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC29002D/1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC29002D/1G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC29002DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC29002DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC29002DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC29002DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC29002DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC29002DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC29002DR/1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC29002DR/1G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC29002DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC29002P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
UCC29002PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
UCC39002D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC39002DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC39002DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC39002DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UCC39002DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC39002DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC39002DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC39002DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC39002P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
UCC39002PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

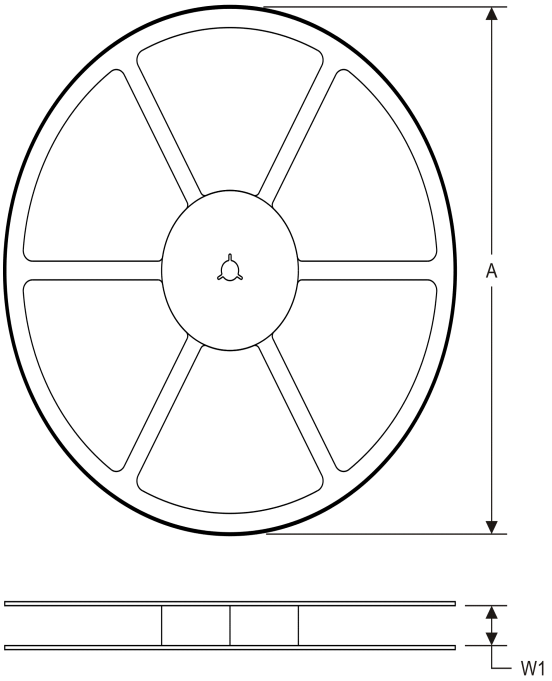
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

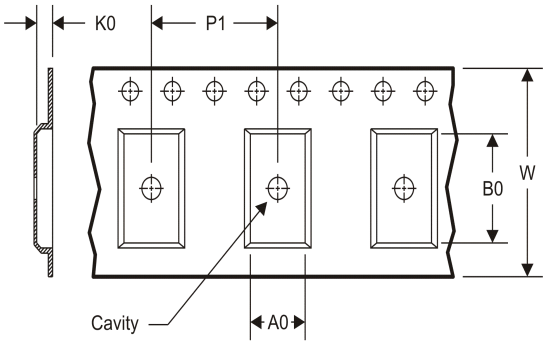
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



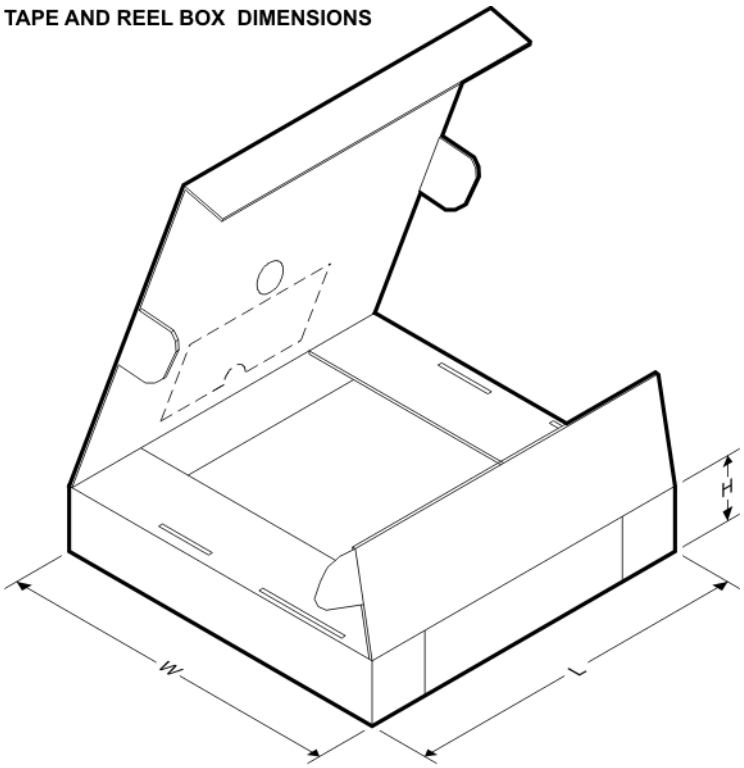
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC29002DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC29002DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC29002DR/1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC39002DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC39002DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

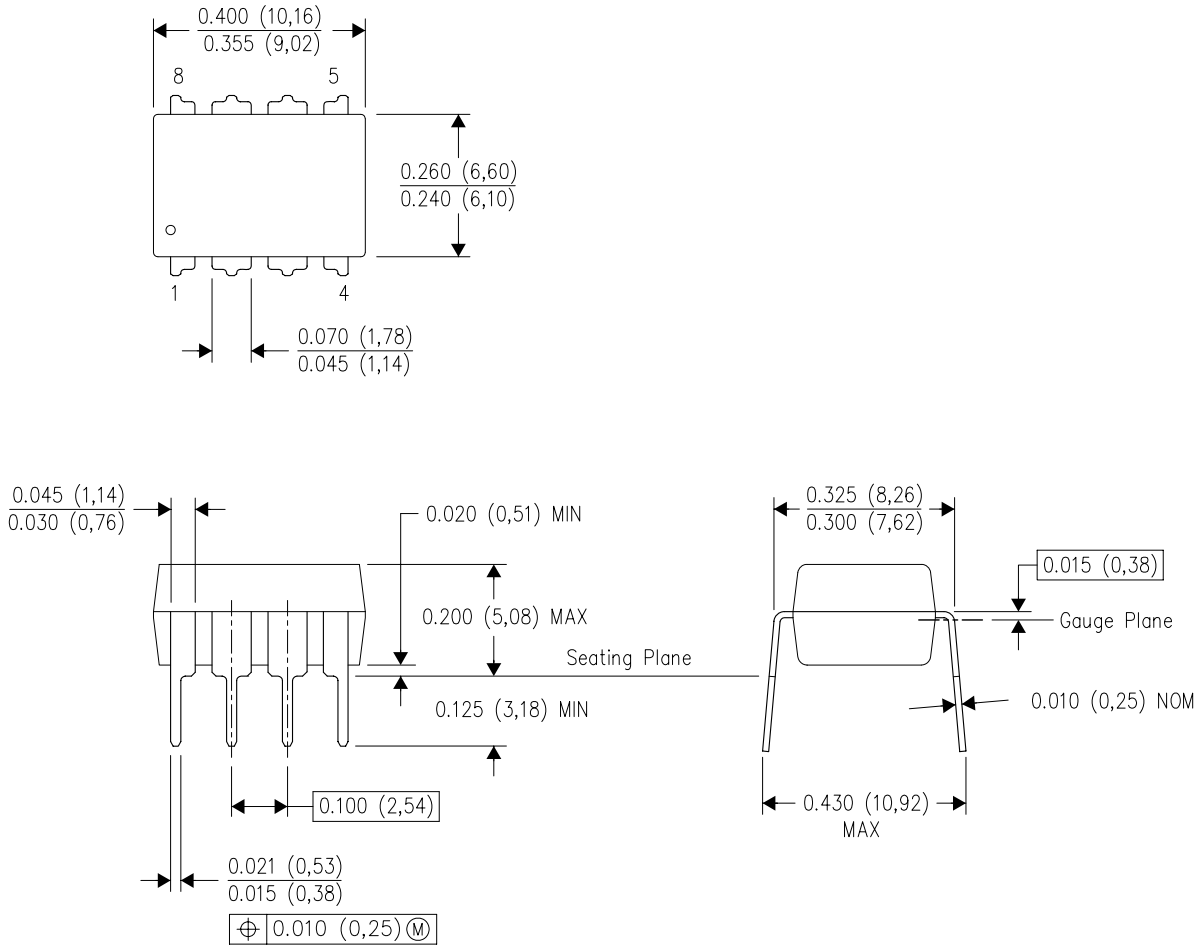
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC29002DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
UCC29002DR	SOIC	D	8	2500	367.0	367.0	35.0
UCC29002DR/1	SOIC	D	8	2500	367.0	367.0	35.0
UCC39002DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
UCC39002DR	SOIC	D	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
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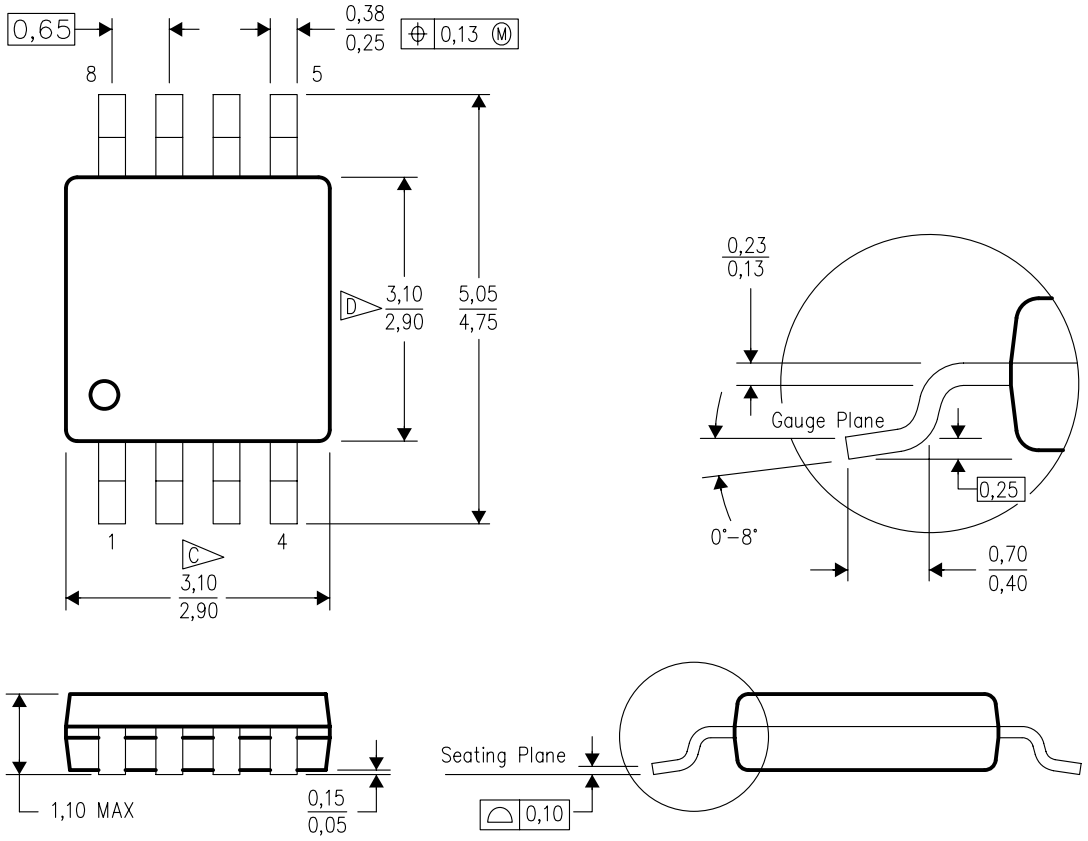
C. Falls within JEDEC MS–001 variation BA.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
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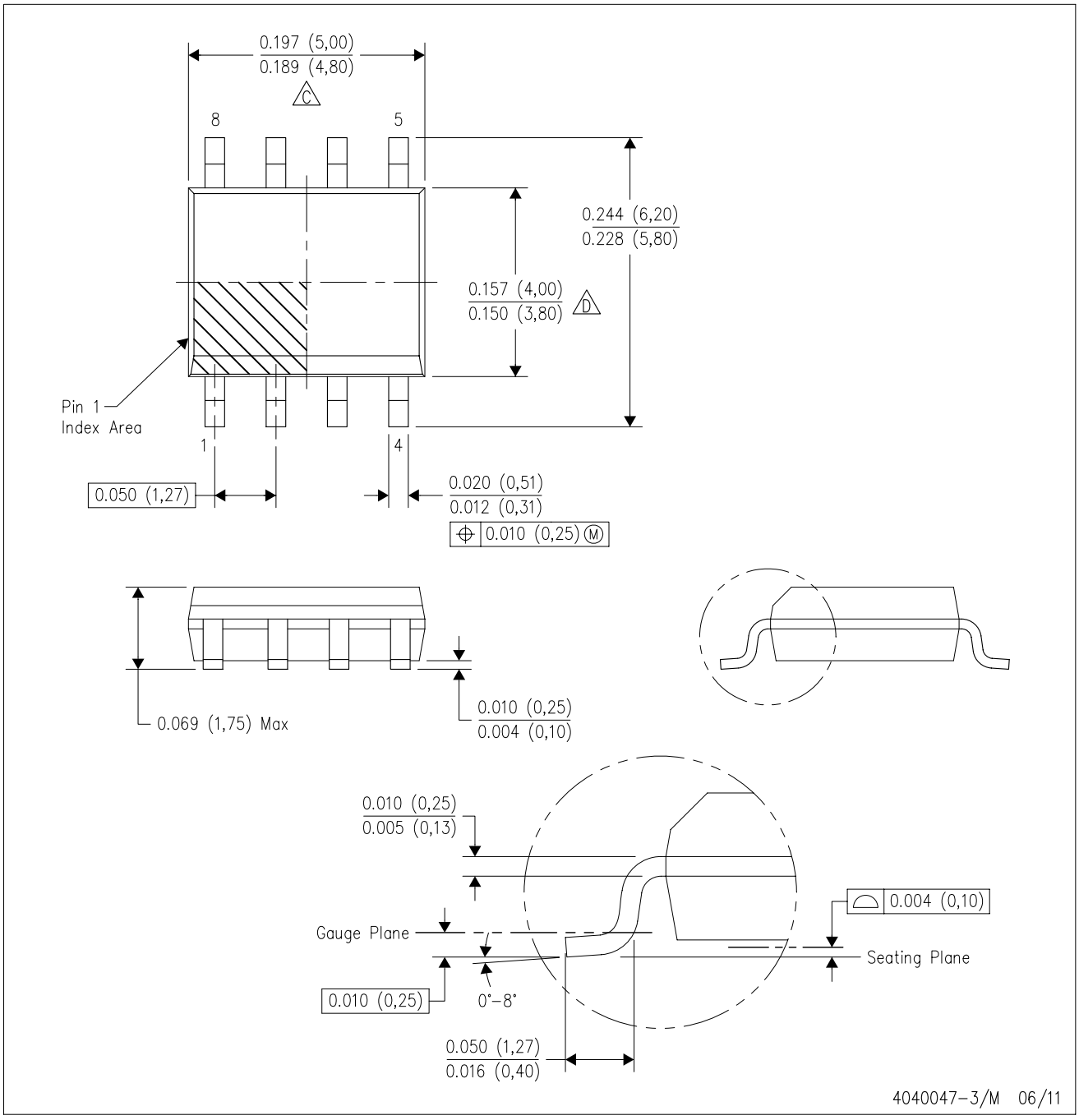
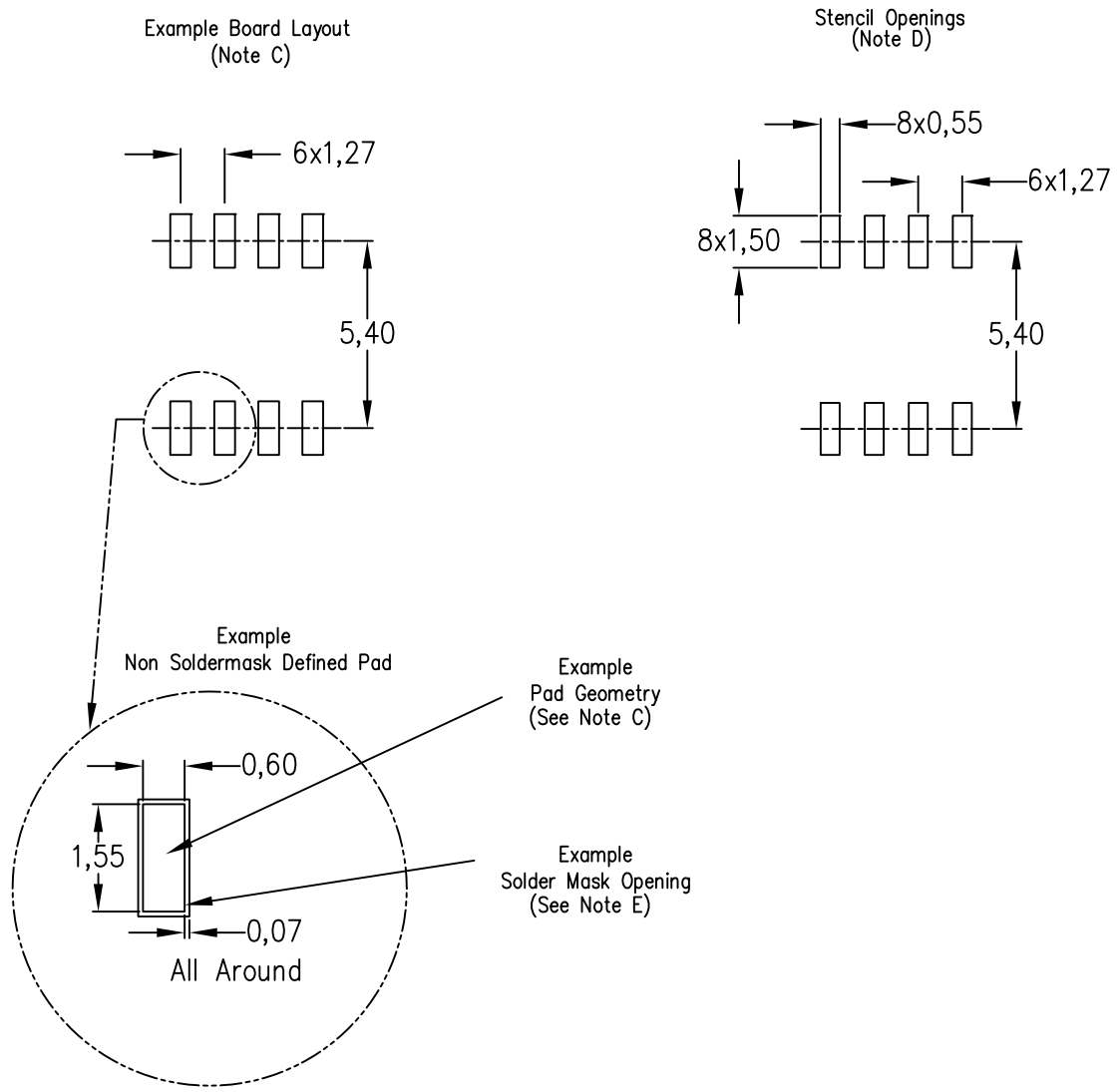
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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