16-BIT DIGITAL-TO-ANALOG CONVERTER with 16-Bit Bus Interface

FEATURES

- **HIGH-SPEED, 16-BIT PARALLEL DOUBLE-BUFFERED INTERFACE**
- **VOLTAGE OUTPUT: ±10V**
- **13-, 14-, AND 15-BIT LINEARITY GRADES**
- **16-BIT MONOTONIC OVER TEMPERATURE (L GRADE)**
- **POWER DISSIPATION: 600mW max**
- **GAIN AND OFFSET ADJUST: Convenient for Auto-Cal D/A Converters**
- **28-LEAD DIP AND SOIC PACKAGES**

DESCRIPTION

The DAC712 is a complete 16-bit resolution digital-to-analog (D/A) converter with 16 bits of monotonicity over temperature.

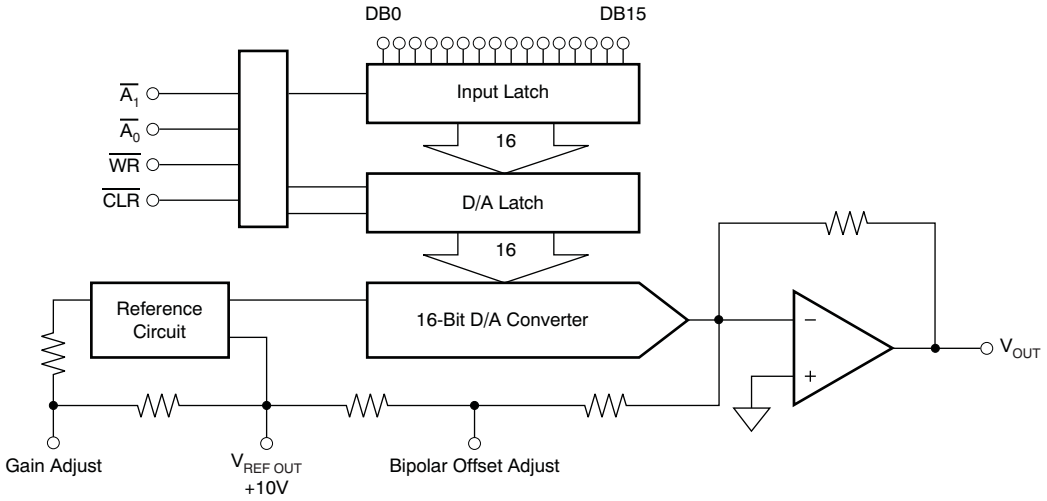
The DAC712 has a precision +10V temperature-compensated voltage reference, ±10V output amplifier, and 16-bit port bus interface.

The digital interface is fast, 60ns minimum write pulse width, double-buffered, and has a CLEAR function that resets the analog output to bipolar zero.

GAIN and OFFSET adjustment inputs are arranged so that they can be easily trimmed by external D/A converters as well as by potentiometers.

The DAC712 is available in two linearity error performance grades: ±4LSB and ±2LSB, and three differential linearity grades: ±4LSB, ±2LSB, and ±1LSB. The DAC712 is specified at power-supply voltages of ±12V and ±15V.

The DAC712 is packaged in a 28-pin, 0.3" wide plastic DIP and in a 28-lead, wide-body plastic SOIC. The DAC712P, U, PB, and UB are specified over the –40°C to +85°C temperature range and the DAC712PK, UK, PL, and UL are specified over the 0°C to +70°C range.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	LINEARITY ERROR MAX AT +25°C	DIFFERENTIAL LINEARITY ERROR MAX AT +25°C	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE
DAC712P	±4LSB	±4LSB	PDIP-28	NT	–40°C to +85°C
DAC712U	±4LSB	±4LSB	SOIC-28	DW	–40°C to +85°C
DAC712PB	±2LSB	±2LSB	PDIP-28	NT	–40°C to +85°C
DAC712UB	±2LSB	±2LSB	SOIC-28	DW	–40°C to +85°C
DAC712PK	±2LSB	±2LSB	PDIP-28	NT	0°C to +70°C
DAC712UK	±2LSB	±2LSB	SOIC-28	DW	0°C to +70°C
DAC712PL	±2LSB	±1LSB	PDIP-28	NT	0°C to +70°C
DAC712UL	±2LSB	±1LSB	SOIC-28	DW	0°C to +70°C

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

	DAC712	UNIT
$+V_{CC}$ to COMMON	0, +17	V
$-V_{CC}$ to COMMON	0, –17	V
$+V_{CC}$ to $-V_{CC}$	34	V
Digital Inputs to COMMON	–1 to $+V_{CC}$ – 0.7	V
External Voltage Applied to BPO and Range Resistors	$\pm V_{CC}$	V
$V_{REF\ OUT}$	Indefinite Short to COMMON	
V_{OUT}	Indefinite Short to COMMON	
Power Dissipation	750	mW
Storage Temperature Range	–60 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

TRUTH TABLE

$\overline{A_0}$	$\overline{A_1}$	$\overline{WR}$	$\overline{CLR}$	DESCRIPTION
0	1	1 → 0 → 1	1	Load Input Latch
1	0	1 → 0 → 1	1	Load D/A Latch
1	1	1 → 0 → 1	1	No Change
0	0	0	1	Latches Transparent
X	X	1	1	No Change
X	X	X	0	Reset D/A Latch

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ELECTRICAL CHARACTERISTICS: DAC712P, U, PB, UB

At T_A = +25°C, $+V_{CC}$ = +12V and +15V, and $-V_{CC}$ = –12V and –15V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DAC712P, U			DAC712PB, UB(1)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
RESOLUTION								
Resolution			16					Bits
DIGITAL INPUTS								
Input Code		Binary Twos Complement						
Logic Levels(2)								
V_{IH}		+2.0		$+V_{CC}$ – 1.4				V
V_{IL}		0		+0.8				V
I_{IH} (V_I = +2.7V)				±10				µA
I_{IL} (V_I = +0.4V)				±10				µA
TRANSFER CHARACTERISTICS								
ACCURACY								
Linearity Error				±4			±2	LSB
T_{MIN} to T_{MAX}				±8			±4	LSB
Differential Linearity Error				±4			±2	LSB
T_{MIN} to T_{MAX}				±8			±4	LSB
Monotonicity Over Temperature		13			14			Bits
Gain Error(3)				±0.1				%
T_{MIN} to T_{MAX}				±0.2			±0.15	%
Bipolar Zero Error(3)				±0.1				% FSR(4)
				±20				mV
T_{MIN} to T_{MAX}				±0.2			±0.15	% FSR
				±40			±30	mV
Power-Supply Sensitivity of Full-Scale				±0.003				% FSR/% V_{CC}
				±30				ppm FSR/% V_{CC}
DYNAMIC PERFORMANCE								
Settling Time (to ±0.003%FSR, 5kΩ || 500pF Load)(5)								
20V Output Step			6				10	µs
1LSB Output Step(6)			4					µs
Output Slew Rate			10					V/µs
Total Harmonic Distortion + Noise								
0dB, 1001Hz, f_S = 100kHz			0.005					%
–20dB, 1001Hz, f_S = 100kHz			0.03					%
–60dB, 1001Hz, f_S = 100kHz			3.0					%
SINAD								
1001Hz, f_S = 100kHz			87					dB
Digital Feedthrough(6)			2					nV-s
Digital-to-Analog Glitch Impulse(6)			15					nV-s
Output Noise Voltage (Includes Reference)			120					nV/√Hz

(1) Shaded cells indicate same specification as the DAC712P, U grade.
(2) Digital inputs are TTL- and +5V CMOS-compatible over the specified temperature range.
(3) Errors externally adjustable to zero.
(4) FSR means Full-Scale Range. For example, for a ±10V output, FSR = 20V.
(5) Maximum represents the 3σ limit. Not 100% tested for this parameter.
(6) For the worst-case code changes: FFFFh to 0000h and 0000h to FFFFh. These are binary twos complement (BTC) codes.

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ELECTRICAL CHARACTERISTICS: DAC712P, U, PB, UB (continued)

At T_A = +25°C, $+V_{CC}$ = +12V and +15V, and $-V_{CC}$ = –12V and –15V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DAC712P, U			DAC712PB, UB(1)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG OUTPUT								
Output Voltage Range								
$+V_{CC}$, $-V_{CC}$ = ±11.4V		±10						V
Output Current		±5						mA
Output Impedance			0.1					Ω
Short-Circuit to ACOM, Duration			Indefinite					
REFERENCE VOLTAGE								
Voltage		+9.975	+10.000	+10.025				V
T_{MIN} to T_{MAX}		+9.960		+10.040				V
Output Resistance			1					Ω
Source Current		2						mA
Short-Circuit to ACOM, Duration			Indefinite					
POWER-SUPPLY REQUIREMENTS								
Voltage								
$+V_{CC}$		+11.4	+15	+16.5				V
$-V_{CC}$		–11.4	–15	–16.5				V
Current (No Load, ±15V Supplies)								
$+V_{CC}$			13	15				mA
$-V_{CC}$			22	25				mA
Power Dissipation(7)			525	600				mW
TEMPERATURE RANGES								
Specified Temperature Range (All Grades)		–40		+85				°C
Storage Temperature Range		–60		+150				°C
Thermal Coefficient, θ_{JA}								
DIP Package			75					°C/W
SOIC Package			75					°C/W

(7) Typical supply voltages times maximum currents.

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ELECTRICAL CHARACTERISTICS: DAC712PK, UK, PL, UL

At T_A = +25°C, $+V_{CC}$ = +12V and +15V, and $-V_{CC}$ = –12V and –15V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DAC712PK, UK			DAC712PL, UL(1)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
RESOLUTION								
Resolution			16					Bits
DIGITAL INPUTS								
Input Code		Binary Twos Complement						
Logic Levels(2)								
V_{IH}		+2.0		$+V_{CC}$ – 1.4				V
V_{IL}		0		+0.8				V
I_{IH} (V_I = +2.7V)				±10				µA
I_{IL} (V_I = +0.4V)				±10				µA
TRANSFER CHARACTERISTICS								
ACCURACY								
Linearity Error				±2				LSB
T_{MIN} to T_{MAX}				±2				LSB
Differential Linearity Error				±2			±1	LSB
T_{MIN} to T_{MAX}				±2			±1	LSB
Monotonicity Over Temperature		15			16			Bits
Gain Error(3)				±0.1				%
T_{MIN} to T_{MAX}				±0.15			±0.2	%
Bipolar Zero Error(3)				±0.1				% FSR(4)
				±20				mV
T_{MIN} to T_{MAX}				±0.15				% FSR
				±30				mV
Power-Supply Sensitivity of Full-Scale				±0.003				% FSR/% V_{CC}
				±30				ppm FSR/% V_{CC}
DYNAMIC PERFORMANCE								
Settling Time (to ±0.003%FSR, 5kΩ || 500pF Load)(5)								
20V Output Step			6	10				µs
1LSB Output Step(6)			4					µs
Output Slew Rate			10					V/µs
Total Harmonic Distortion + Noise								
0dB, 1001Hz, f_S = 100kHz			0.005					%
–20dB, 1001Hz, f_S = 100kHz			0.03					%
–60dB, 1001Hz, f_S = 100kHz			3.0					%
SINAD								
1001Hz, f_S = 100kHz			87					dB
Digital Feedthrough(6)			2					nV-s
Digital-to-Analog Glitch Impulse(6)			15					nV-s
Output Noise Voltage (Includes Reference)			120					nV/$\sqrt{Hz}$

(1) Shaded cells indicate same specification as the DAC712PK, UK grade.
(2) Digital inputs are TTL- and +5V CMOS-compatible over the specified temperature range.
(3) Errors externally adjustable to zero.
(4) FSR means Full-Scale Range. For example, for a ±10V output, FSR = 20V.
(5) Maximum represents the 3σ limit. Not 100% tested for this parameter.
(6) For the worst-case code changes: FFFFh to 0000h and 0000h to FFFFh. These are binary twos complement (BTC) codes.

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ELECTRICAL CHARACTERISTICS: DAC712PK, UK, PL, UL (continued)

At T_A = +25°C, $+V_{CC}$ = +12V and +15V, and $-V_{CC}$ = –12V and –15V, unless otherwise noted.

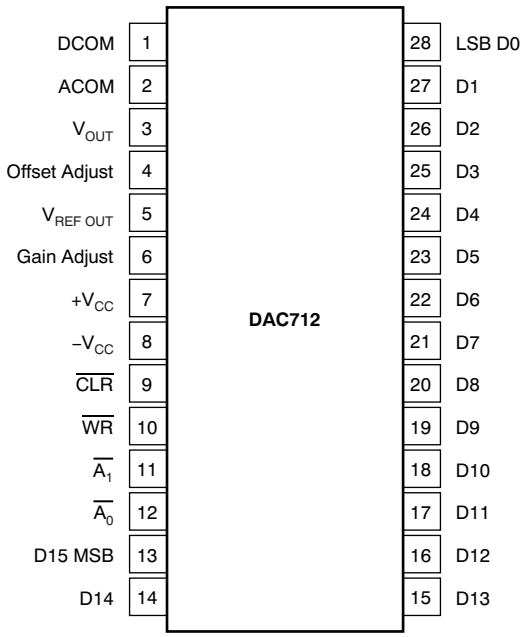
PARAMETER	TEST CONDITIONS	DAC712PK, UK			DAC712PL, UL(1)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG OUTPUT								
Output Voltage Range								
$+V_{CC}$, $-V_{CC}$ = ±11.4V		±10						V
Output Current		±5						mA
Output Impedance			0.1					Ω
Short-Circuit to ACOM, Duration			Indefinite					
REFERENCE VOLTAGE								
Voltage		+9.975	+10.000	+10.025				V
T_{MIN} to T_{MAX}		+9.960		+10.040				V
Output Resistance			1					Ω
Source Current		2						mA
Short-Circuit to ACOM, Duration			Indefinite					
POWER-SUPPLY REQUIREMENTS								
Voltage								
$+V_{CC}$		+11.4	+15	+16.5				V
$-V_{CC}$		–11.4	–15	–16.5				V
Current (No Load, ±15V Supplies)								
$+V_{CC}$			13	15				mA
$-V_{CC}$			22	25				mA
Power Dissipation(7)			525	600				mW
TEMPERATURE RANGES								
Specified Temperature Range (All Grades)		0		+70				°C
Storage Temperature Range		–60		+150				°C
Thermal Coefficient, θ_{JA}								
DIP Package			75					°C/W
SOIC Package			75					°C/W

(7) Typical supply voltages times maximum currents.

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PIN CONFIGURATION

DW AND NT PACKAGES
SOIC-28 AND PDIP-28
(TOP VIEW)



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PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	DCOM	Power-Supply return for digital currents
2	ACOM	Analog Supply Return
3	V_{OUT}	±10V D/A Output
4	Offset Adjust	Offset Adjust (Bipolar)
5	$V_{REF\ OUT}$	Voltage Reference Output
6	Gain Adjust	Gain Adjust
7	$+V_{CC}$	+12V to +15V Supply
8	$-V_{CC}$	–12V to –15V Supply
9	$\overline{CLR}$	CLEAR; Sets D/A output to Bipolar Zero (Active Low)
10	$\overline{WR}$	Write (Active Low)
11	$\overline{A_1}$	Enable for D/A latch (Active Low)
12	$\overline{A_0}$	Enable for Input latch (Active Low)
13	D15	Data Bit 15 (Most Significant Bit)
14	D14	Data Bit 14
15	D13	Data Bit 13
16	D12	Data Bit 12
17	D11	Data Bit 11
18	D10	Data Bit 10
19	D9	Data Bit 9
20	D8	Data Bit 8
21	D7	Data Bit 7
22	D6	Data Bit 6
23	D5	Data Bit 5
24	D4	Data Bit 4
25	D3	Data Bit 3
26	D2	Data Bit 2
27	D1	Data Bit 1
28	D0	Data Bit 0 (Least Significant Bit)

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TIMING CHARACTERISTICS

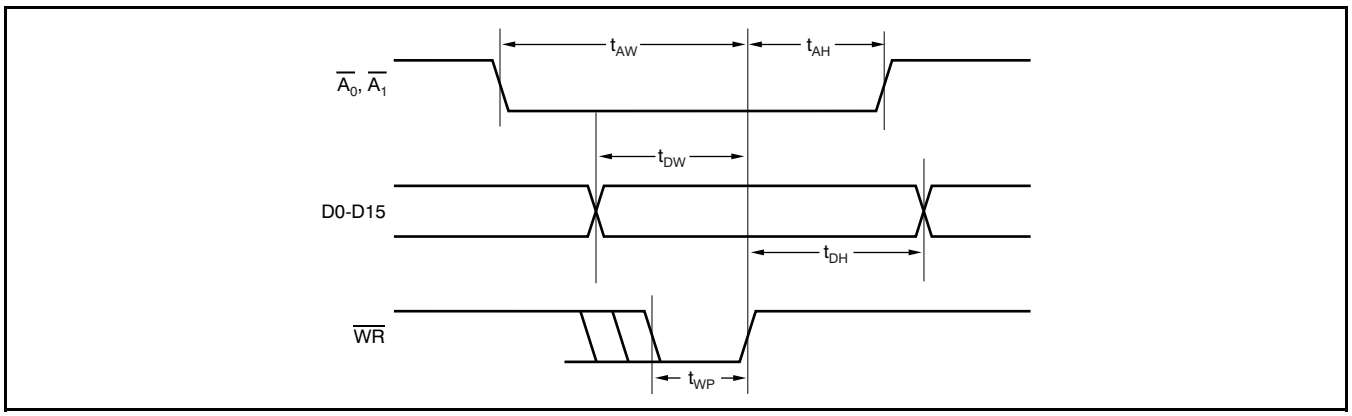


Figure 1. Timing Diagram

TIMING REQUIREMENTS

At T_A = –40°C to +85°C, $+V_{CC}$ = +12V or +15V, and $–V_{CC}$ = –12V or –15V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	DAC712			UNIT
			MIN	TYP	MAX	
t_{DW}	Data Valid to End of $\overline{WR}$		50			ns
t_{AW}	$\overline{A_0}$, $\overline{A_1}$ Valid to End of $\overline{WR}$		50			ns
t_{AH}	$\overline{A_0}$, $\overline{A_1}$ Hold after End of $\overline{WR}$		10			ns
t_{DH}	Data Hold after End of $\overline{WR}$		10			ns
t_{WP} (1)	Write Pulse Width		50			ns
t_{CP}	CLEAR Pulse Width		200			ns

(1) For single-buffered operation, t_{WP} is 80ns minimum; see the *Single-Buffered Operation* section.

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TYPICAL CHARACTERISTICS

At T_A = +25°C and V_{CC} = ±15V, unless otherwise noted.

POWER-SUPPLY REJECTION vs POWER-SUPPLY RIPPLE FREQUENCY

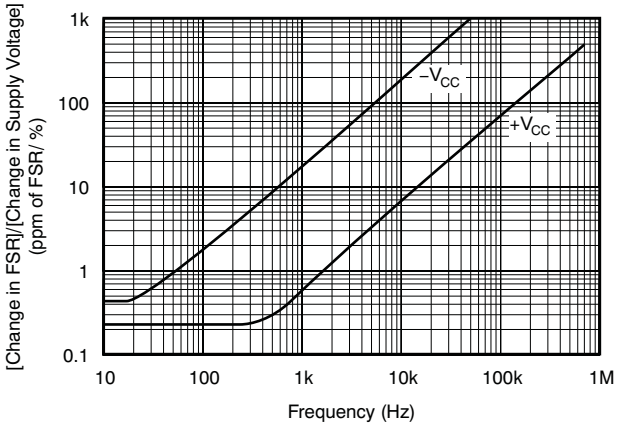


Figure 2.

LOGIC vs V LEVEL

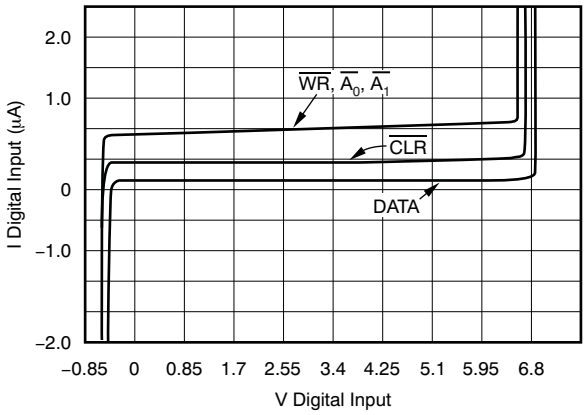


Figure 3.

± FULL-SCALE OUTPUT SWING

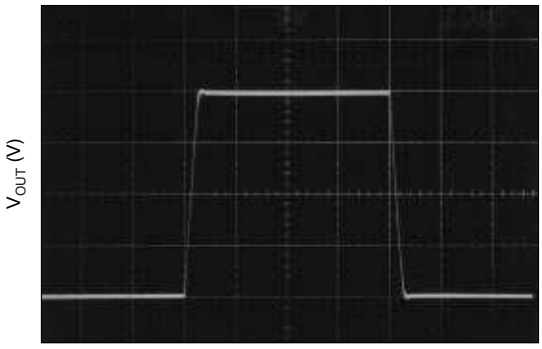


Figure 4.

SETTLING TIME, +10V TO –10V

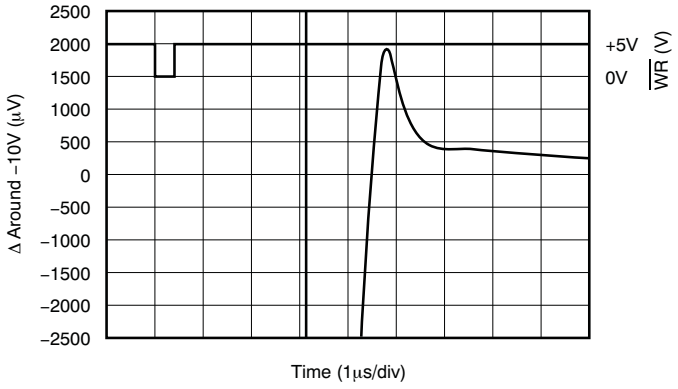


Figure 5.

SETTLING TIME, +10V TO –10V

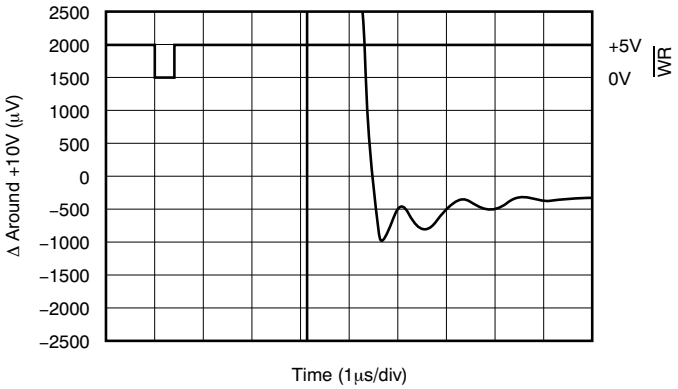


Figure 6.

SPECTRAL NOISE DENSITY

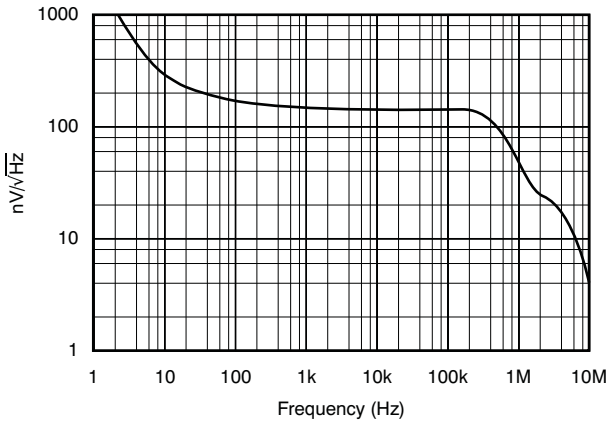


Figure 7.

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DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points of the transfer characteristic.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from 1LSB of an output change from one adjacent state to the next. A DLE specification of ±1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than –1LSB, the D/A converter is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. Monotonicity of the DAC712 is ensured over the specified temperature range to 13, 14, 15, and 16 bits for performance grades DAC712P/U, DAC712PB/UB, DAC712PK/UK, and DAC712PL/UL, respectively.

SETTLING TIME

Settling time is the total time (including slew time) for the D/A output to settle to within an error band around its final value after a change in input. Settling times are specified to within ±0.003% of Full-Scale Range (FSR) for an output step change of 20V and 1LSB. The 1LSB change is measured at the Major Carry (FFFFh to 0000h, and 0000h to FFFFh: BTC codes), the input transition at which worst-case settling time occurs.

TOTAL HARMONIC DISTORTION + NOISE

Total harmonic distortion + noise is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental frequency. It is expressed in % of the fundamental frequency amplitude at sampling rate f_S.

SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing and internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f_S.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected into the analog output from the digital inputs when the inputs change state. It is measured at half-scale at the input codes where as many switches as possible change state—from 7FFFh to 8000h.

DIGITAL FEEDTHROUGH

When the analog-to-digital (A/D) converter is not selected, high-frequency logic activity on the digital inputs is coupled through the device and shows up as output noise. This noise is digital feedthrough.

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OPERATION

The DAC712 is a monolithic integrated-circuit, 16-bit D/A converter complete with 16-bit D/A converter switches and ladder network, voltage reference, output amplifier, and microprocessor bus interface.

INTERFACE LOGIC

The DAC712 has double-buffered data latches. The input data latch holds a 16-bit data word before loading it into the second latch, the D/A latch. This double-buffered organization permits simultaneous update of several D/A converters. All digital control inputs are active low. Refer to the block diagram of Figure 8.

All latches are level-triggered. Data present when the enable inputs are logic '0' enter the latch. When the enable inputs return to logic '1', the data are latched.

The $\overline{CLR}$ input resets both the input latch and the D/A latch to give a bipolar zero output.

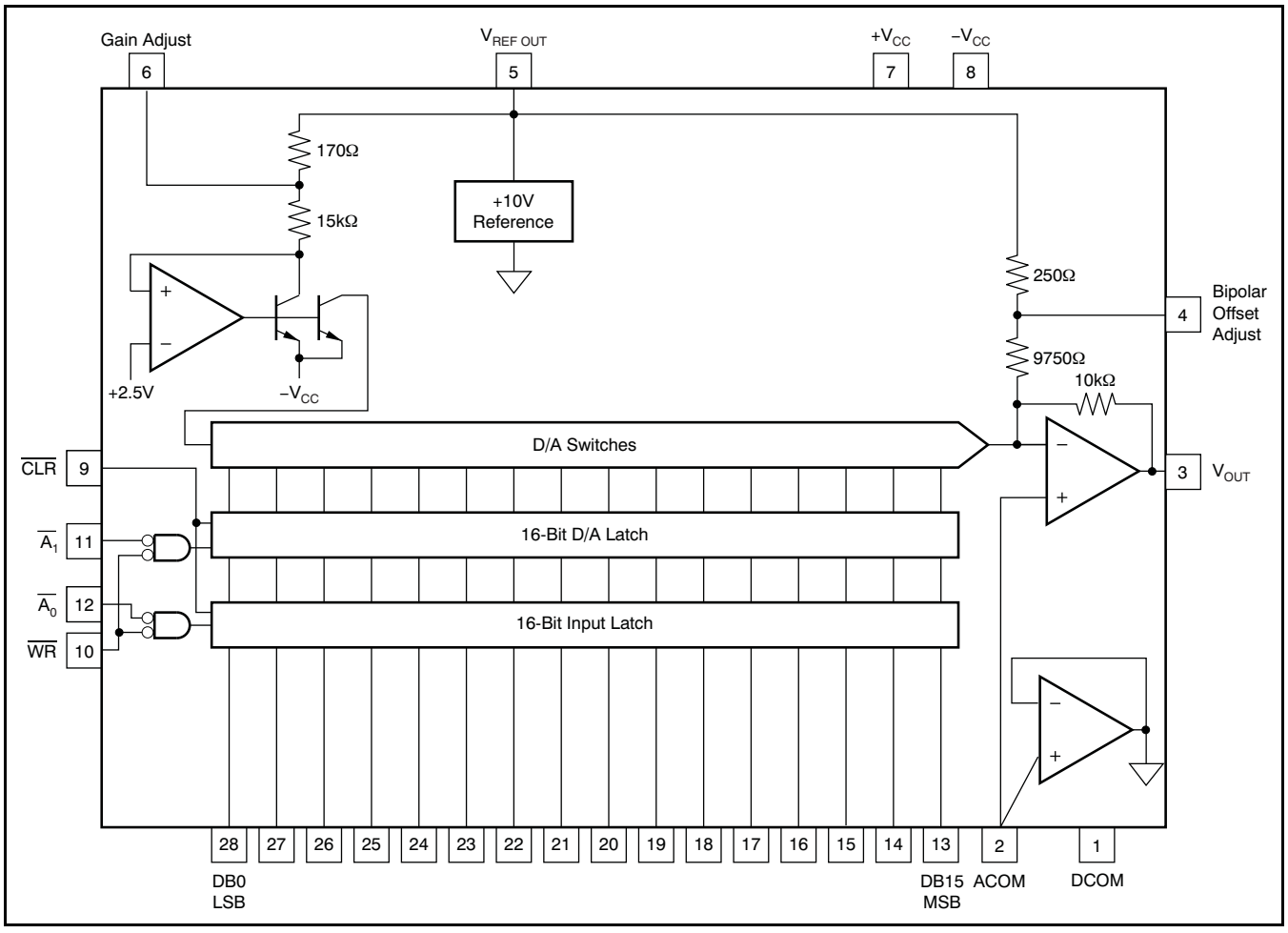


Figure 8. DAC712 Block Diagram

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LOGIC INPUT COMPATIBILITY

The DAC712 digital inputs are TTL-compatible (1.4V switching level) with low-leakage, high-impedance inputs. Thus, the inputs are suitable for being driven by any type of 5V logic such as 5V CMOS logic. An equivalent circuit of a digital input is shown in Figure 9.

Data inputs float to logic '0' and control inputs float to logic '0' if left unconnected. It is recommended that any unused inputs be connected to DCOM to improve noise immunity.

Digital inputs remain high-impedance when power is off.

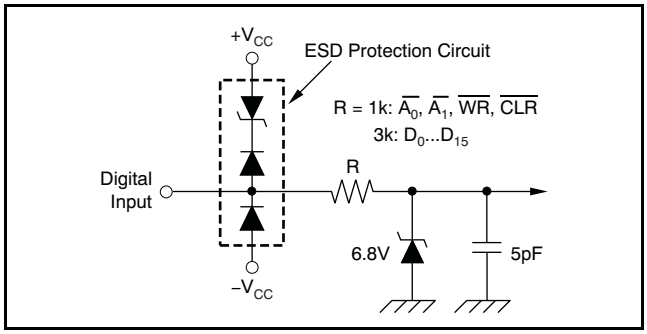


Figure 9. Equivalent Circuit of Digital Inputs

INPUT CODING

The DAC712 is designed to accept positive-true binary twos complement (BTC) input codes that are compatible with bipolar analog output operation. For bipolar analog output configuration, a digital input of 7FFFh gives a positive full-scale output, 8000h gives a negative full-scale output, and 0000h gives bipolar zero output.

INTERNAL REFERENCE

The DAC712 contains a +10V reference.

The reference output may be used to drive external loads, sourcing up to 2mA. The load current should be constant, otherwise the gain and bipolar offset of the converter will vary.

OUTPUT VOLTAGE SWING

The output amplifier of the DAC712 is committed to a ±10V output range. The DAC712 provides a ±10V output swing while operating on ±11.4V or higher voltage supplies.

GAIN AND OFFSET ADJUSTMENTS

Figure 10 illustrates the relationship of offset and gain adjustments for a bipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments. Table 1 shows calibration values and codes. These adjustments have a minimum range of ±0.3%.

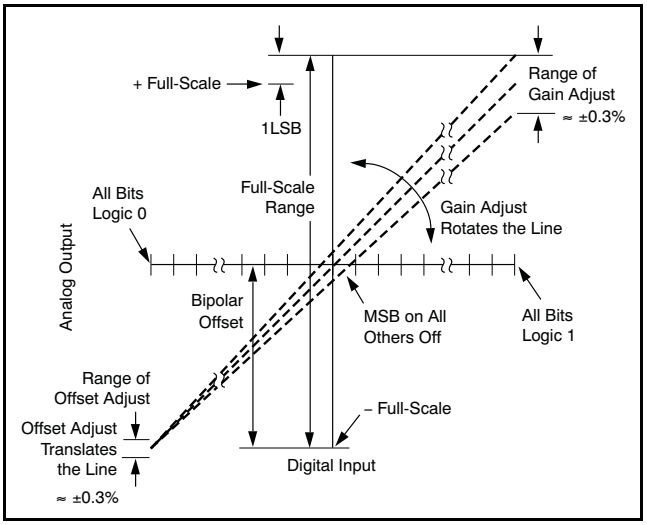


Figure 10. Relationship of Offset and Gain Adjustments

Table 1. Digital Input and Analog Output Voltage Calibration Values

DAC712 CALIBRATION VALUES 1 LEAST SIGNIFICANT BIT = 305μV		
DIGITAL INPUT CODE BINARY TWOS COMPLEMENT, BTC	**ANALOG OUTPUT (V)**	**DESCRIPTION**
7FFFh	+9.999695	Positive Full-Scale – 1LSB
4000h	+5.000000	3/4 Scale
0001h	+0.000305	BPZ + 1LSB
0000h	0.000000	Bipolar Zero (BPZ)
FFFFh	–0.000305	BPZ – 1LSB
C000h	–5.000000	1/4 Scale
8000h	–10.00000	Negative Full-Scale

Offset Adjustment

Apply the digital input code that produces the maximum negative output voltage and adjust the offset potentiometer or the offset adjust D/A converter for –10V.

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Gain Adjustment

Apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer or the gain adjust D/A converter for this positive full-scale voltage.

INSTALLATION

GENERAL CONSIDERATIONS

Because of the high accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 20V full-scale range has a 1LSB value of 305mV. With a load current of 5μA, series wiring and connector resistance of only 60mΩ causes a voltage drop of 300μV. To understand what this means in terms of a system layout, the resistivity of a typical 1-ounce copper-clad printed circuit board (PCB) is 1/2mΩ per square. For a 5mA load, a 10 mil (0.010 inch) wide printed circuit conductor 60 milli-inches long results in a voltage drop of 150μV.

The analog output of the DAC712 has an LSB size of 305μV (–96dB). The noise floor of the D/A converter must remain below this level in the frequency range of interest. The DAC712 noise spectral density (which includes the noise contributed by the internal reference) is shown in the Typical Characteristics section.

Wiring to high-resolution D/A converters should be routed to provide optimum isolation from sources of radio frequency interference (RFI) and electromagnetic interference (EMI). The key to elimination of RF radiation or pickup is a small loop area. Signal leads and the return conductors should be kept close together such that they present a small capture cross-section for any external field. Wire-wrap construction is not recommended.

POWER-SUPPLY AND REFERENCE CONNECTIONS

Power-supply decoupling capacitors should be added as shown in Figure 11. Best performance occurs using a 1μF to 10μF tantalum capacitor at $-V_{CC}$. Applications with less critical settling time may be able to use 0.01μF at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.

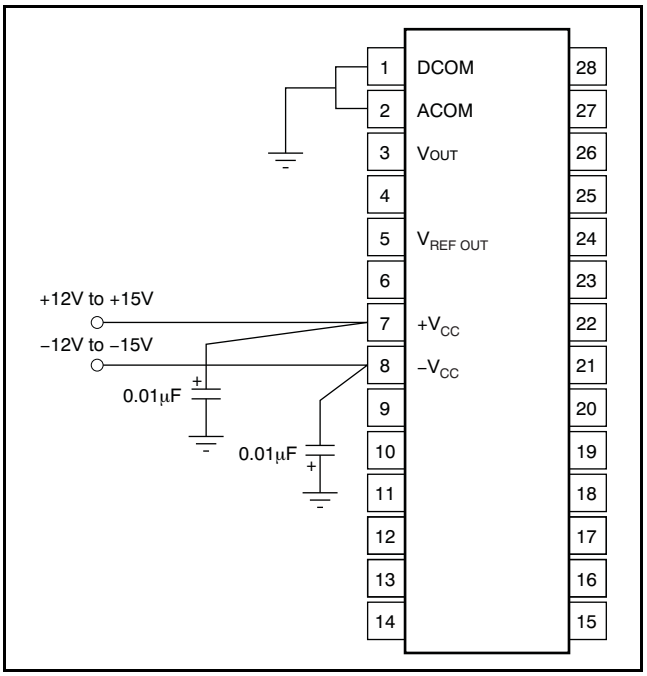


Figure 11. Power-Supply Connections

The DAC712 has separate ANALOG COMMON and DIGITAL COMMON pins. The current through DCOM is mostly switching transients and are up to 1mA peak in amplitude. The current through ACOM is typically 5μA for all codes.

Use separate analog and digital ground planes with a single interconnection point to minimize ground loops. The analog pins are located adjacent to each other to help isolate analog from digital signals. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. A solid analog ground plane around the D/A converter package, as well as under it in the vicinity of the analog and power-supply pins, isolates the D/A converter from switching currents. It is recommended that DCOM and ACOM be connected directly to the ground planes under the package.

If several DAC712s are used, or if the DAC712 shares supplies with other components, connecting the ACOM and DCOM lines together once at the power supplies rather than at each chip may give better results.

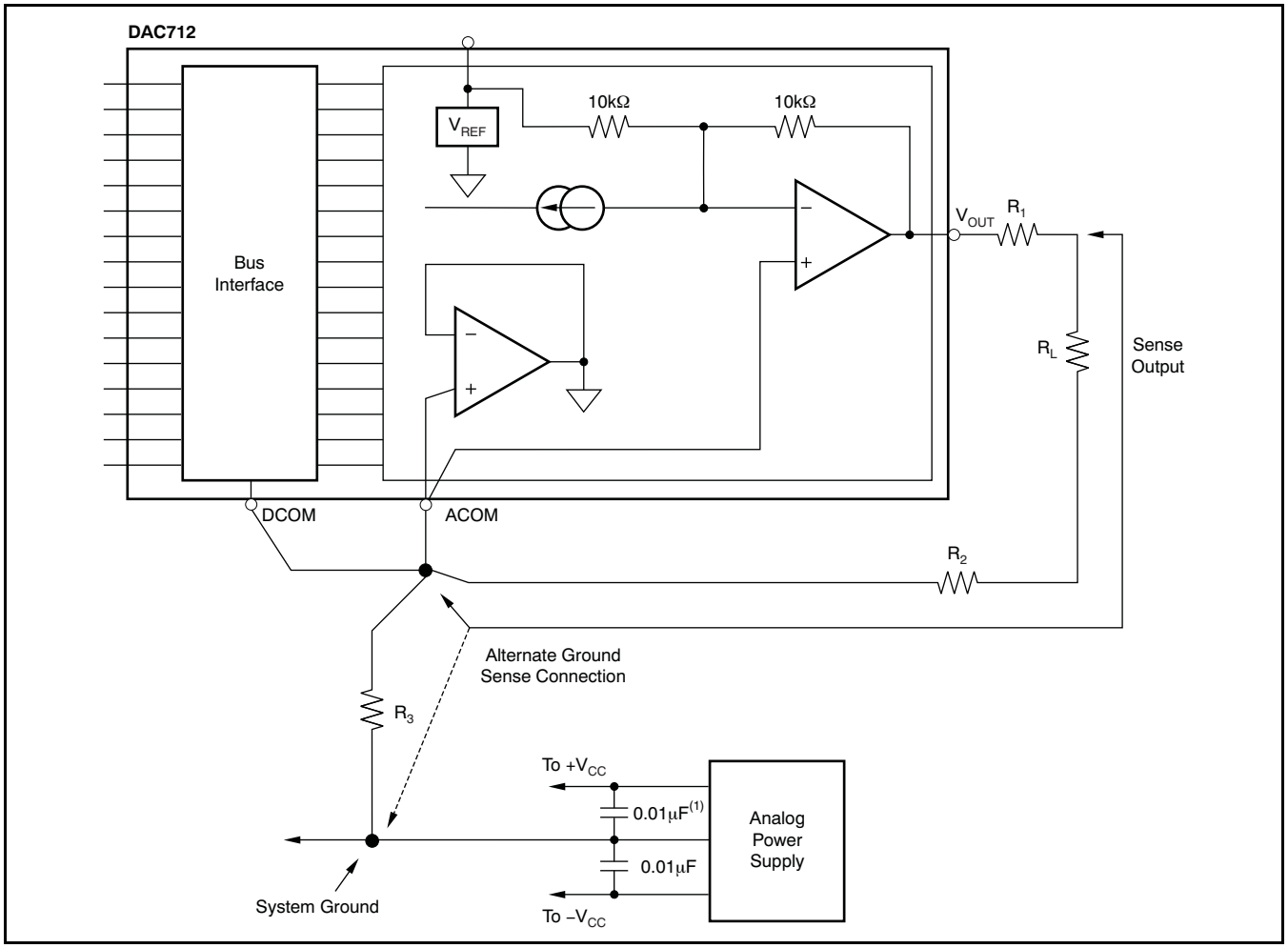
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LOAD CONNECTIONS

Because the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is important to connect the D/A converter load directly to the ACOM pin; see Figure 12.

Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed by gain adjustment of the D/A converter or system-wide gain calibration. R_2 is part of R_L if the output voltage is sensed at ACOM.

In some applications it is impractical to return the load to the ACOM pin of the D/A converter. Sensing the output voltage at the SYSTEM GROUND point is reasonable, because there is no change in the DAC712 ACOM current, provided that R_3 is a low-resistance ground plane or conductor. In this case, DCOM may be connected to SYSTEM GROUND as well.



(1) Locate close to the DAC712 package.

Figure 12. System Ground Considerations for High-Resolution D/A Converters

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GAIN AND OFFSET ADJUST

Connections Using Potentiometers

GAIN and OFFSET adjust pins provide for trim using external potentiometers. 15-turn potentiometers provide sufficient resolution. Range of adjustment of these trims is at least ±0.3% of Full-Scale Range; see Figure 13.

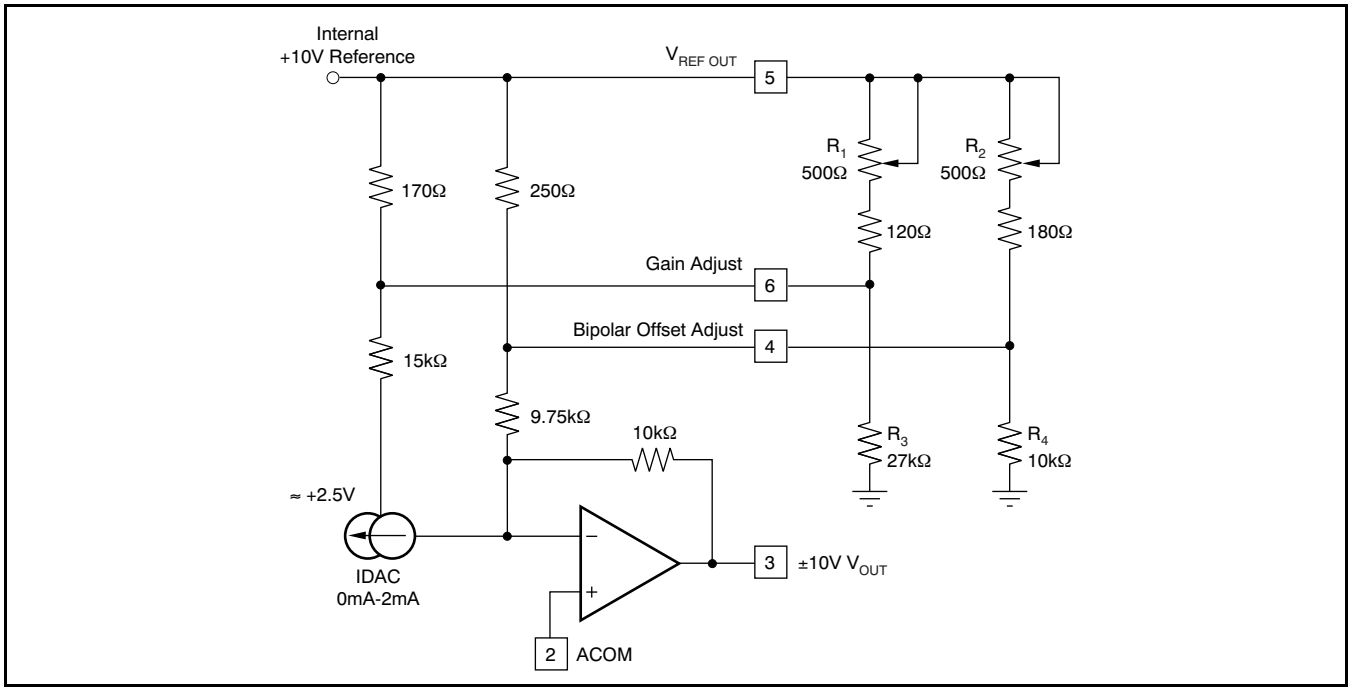
Using D/A Converters

The GAIN ADJUST and OFFSET ADJUST circuits of the DAC712 have been arranged so that these points may be easily driven by external D/A converters; see Figure 14. 12-bit D/A converters provide an OFFSET adjust resolution and a GAIN adjust resolution of 30µV to 50µV per LSB step.

Nominal values of GAIN and OFFSET occur when the D/A converter outputs are at approximately half scale, +5V.

OUTPUT VOLTAGE RANGE CONNECTIONS

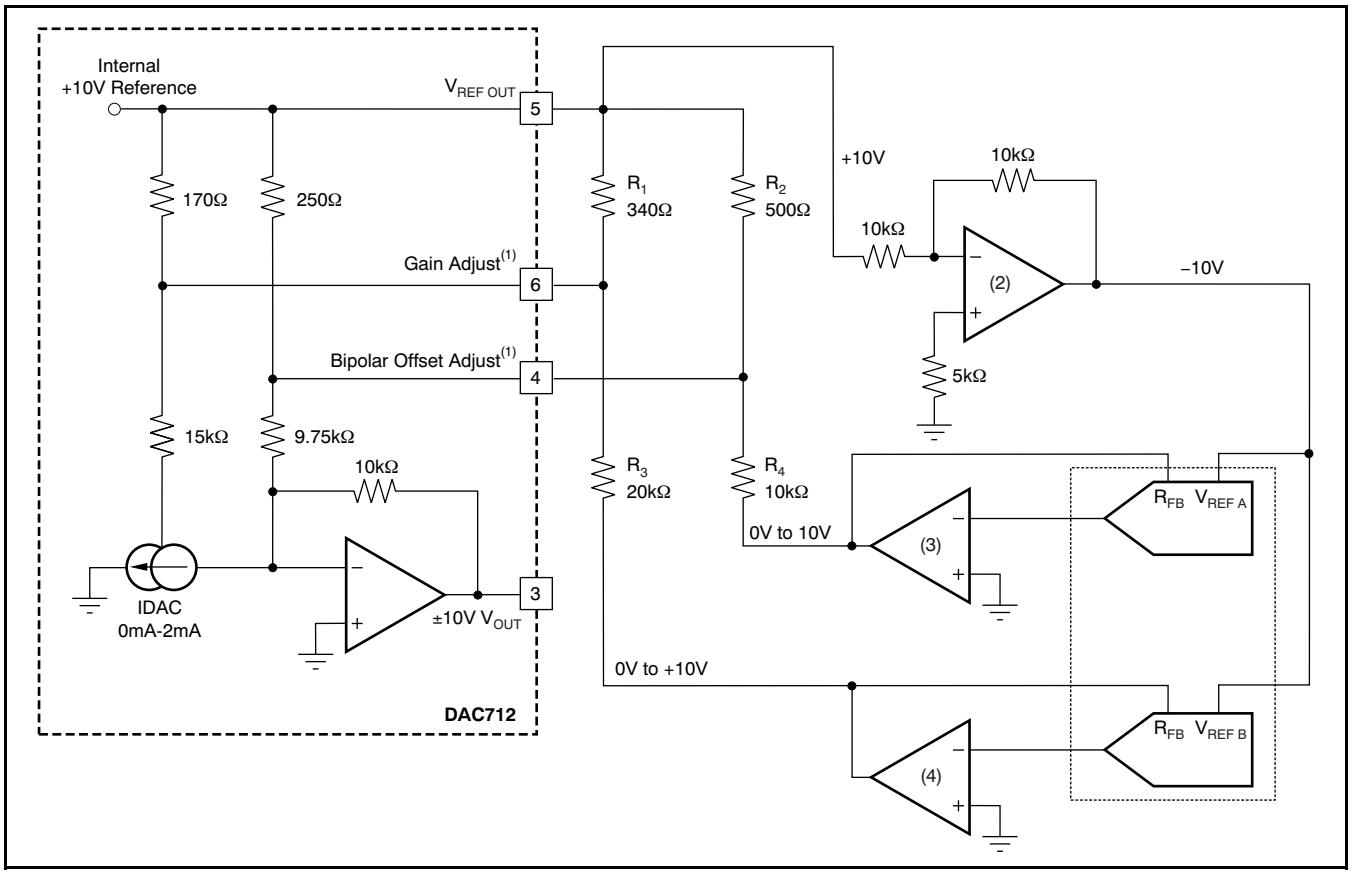
The DAC712 output amplifier is connected internally for the ±10V bipolar (20V) output range. That is, the bipolar offset resistor is connected to an internal reference voltage and the 20V range resistor is connected internally to V_{OUT}. The DAC712 cannot be connected for unipolar operation.



(1) For no external adjustments, pins 4 and 6 are not connected. External Resistors R_1 to R_4 are standard ±1% values. Range of adjustment is at least ±0.3% FSR.

Figure 13. Manual Offset and Gain Adjust Circuits

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(1) For no external adjustments, pins 4 and 6 are not connected. External Resistors R_1 to R_4 tolerance is ±1% values. Range of adjustment is at least ±0.3% FSR.

(2) Suggested op amps: OPA177GP, GS or OPA604AP, AU.

(3) Suggested op amps: single OPA177GP, GS or dual OPA2604AP, AU.

(4) Suggested D/A converters: dual DAC7800 (serial input, 12-bit resolution); dual DAC7801 (8-bit port input, 12-bit resolution); dual DAC7802 (12-bit port input, 12-bit resolution); dual DAC7545 (12-bit port input, 12-bit resolution); or single DAC8043 (serial input, 12-bit resolution). BIPOLAR (complete): DAC813 (use 11-bit resolution for 0V to +10V output; no op-amps required).

Figure 14. Gain and Offset Adjustment Using D/A Converters

DIGITAL INTERFACE

BUS INTERFACE

The DAC712 has 16-bit, double-buffered data bus interface with control lines for easy interface to interface to a 16-bit bus. The double-buffered feature permits update of several D/A converters simultaneously.

$\overline{A_0}$ is the enable control for the DATA INPUT LATCH. $\overline{A_1}$ is the enable for the D/A LATCH. $\overline{WR}$ is used to strobe data into latches enabled by $\overline{A_0}$ and $\overline{A_1}$. Refer to the block diagram of Figure 8 and to Figure 1.

$\overline{CLR}$ sets the INPUT DATA LATCH to all zeros and the D/A LATCH to a code that gives bipolar 0V at the D/A converter output.

SINGLE-BUFFERED OPERATION

To operate the DAC712 interface as a single-buffered latch, the DATA INPUT LATCH is permanently enabled by connecting $\overline{A_0}$ to DCOM. If $\overline{A_1}$ is not used to enable the D/A converter, it should be connected to DCOM as well. For this mode of operation, the width of $\overline{WR}$ must be at least 80ns minimum to pass data through the DATA INPUT LATCH and into the D/A LATCH.

TRANSPARENT INTERFACE

The digital interface of the DAC712 can be made transparent by asserting $\overline{A_0}$, $\overline{A_1}$, and $\overline{WR}$ LOW, and asserting $\overline{CLR}$ HIGH.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 200) to Revision A	Page
• Updated document format to current standards	1
• Changed max specification for Accuracy, *Gain Error, T_{MIN} to T_{MAX}* parameter in *Electrical Characteristics: DAC712PK, UK, PL, UL* table	5

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DAC712P	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
DAC712PB	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
DAC712PBG4	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
DAC712PG4	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
DAC712PK	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
DAC712PKG4	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
DAC712PL	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
DAC712PLG4	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
DAC712U	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC712UB	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC712UB/1K	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	
DAC712UB/1KG4	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	
DAC712UBG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC712UG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC712UK	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC712UK/1K	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	
DAC712UK/1KG4	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	
DAC712UKG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DAC712UL	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC712UL/1K	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	
DAC712UL/1KG4	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	
DAC712ULG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

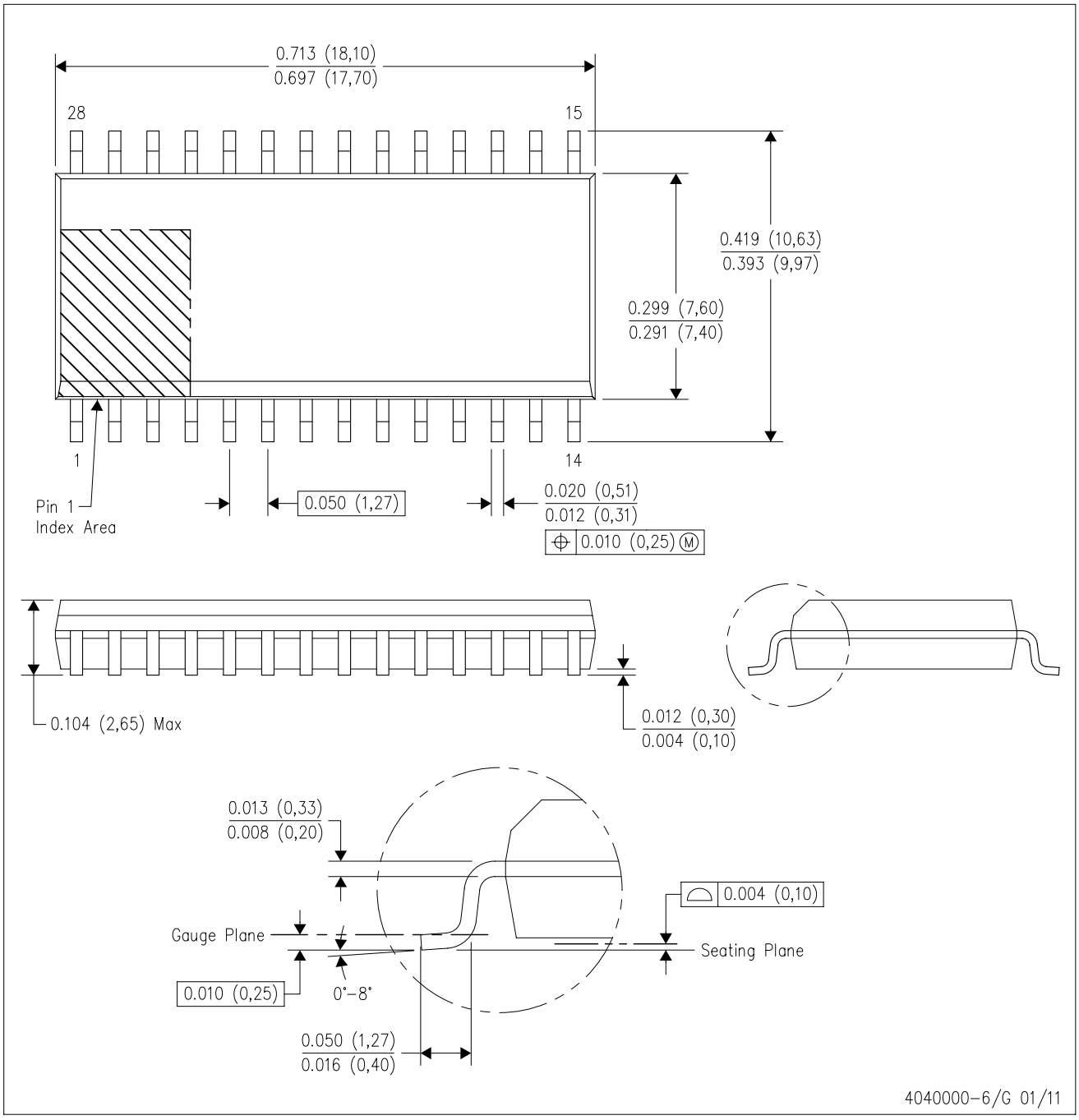
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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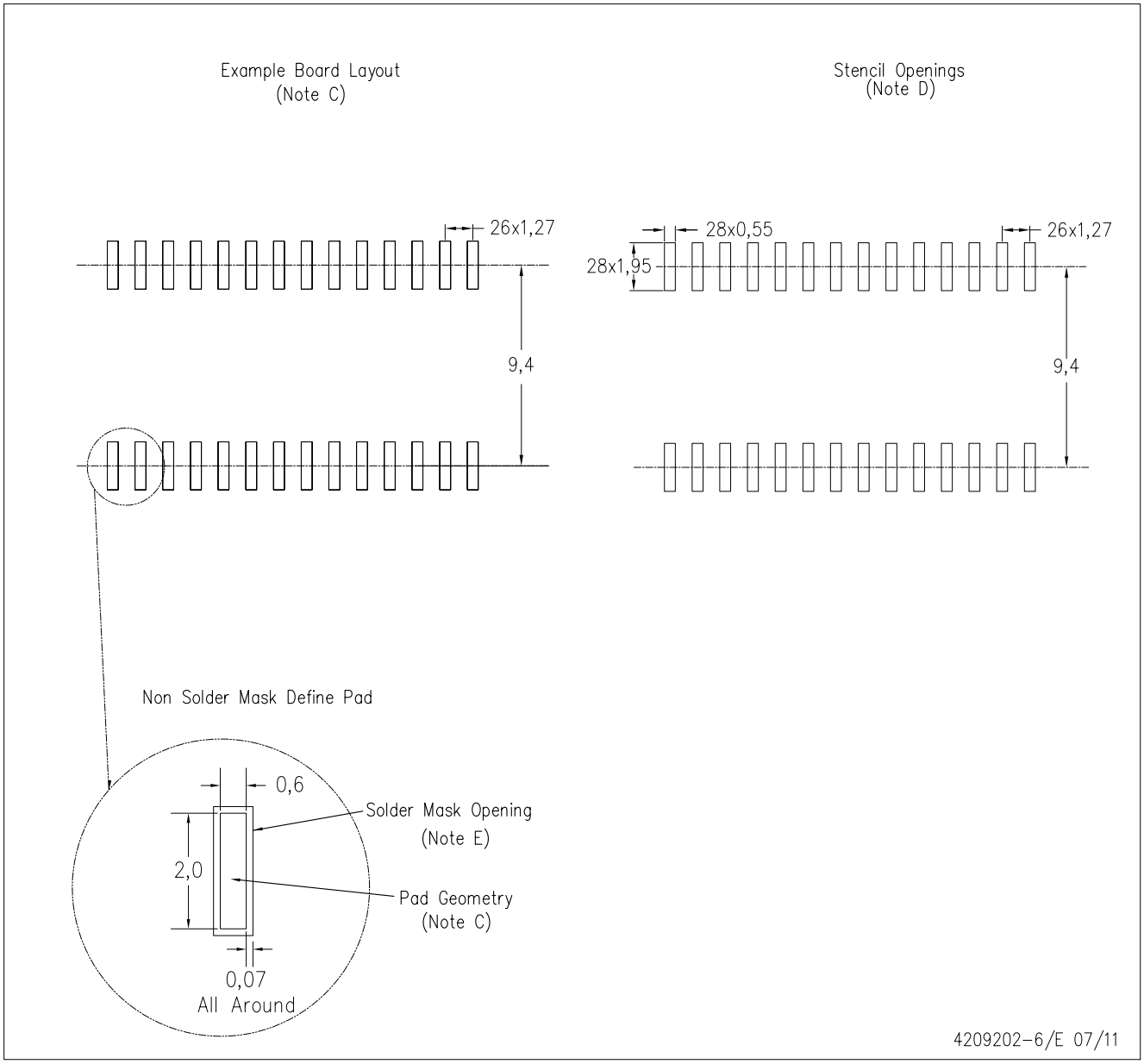
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NOTES:
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B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



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A. All linear dimensions are in millimeters.
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D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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