National Semiconductor

July 1998

54ABT16500
18-Bit Universal Bus Transceivers with TRI-STATE® Outputs

General Description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable OEAB is active-high. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Features

- Combines D-Type latches and D-Type flip-flops for operation in transparent, latched, or clocked mode
- Flow-through architecture optimizes PCB layout
- Guaranteed latch-up protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9687001

Ordering Code

Military	Package Number	Package Description
54ABT16500W-QML	WA56A	56-Lead Cerpack

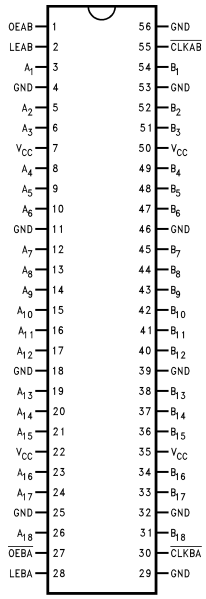
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Connection Diagram

Pin Assignment for Cerpack



DS100225-1

Function Table (Note 1)

Inputs				Output
OEAB	**LEAB**	**$\overline{\text{CLKAB}}$**	**A**	**B**
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0 (Note 2)
H	L	L	X	B_0 (Note 3)

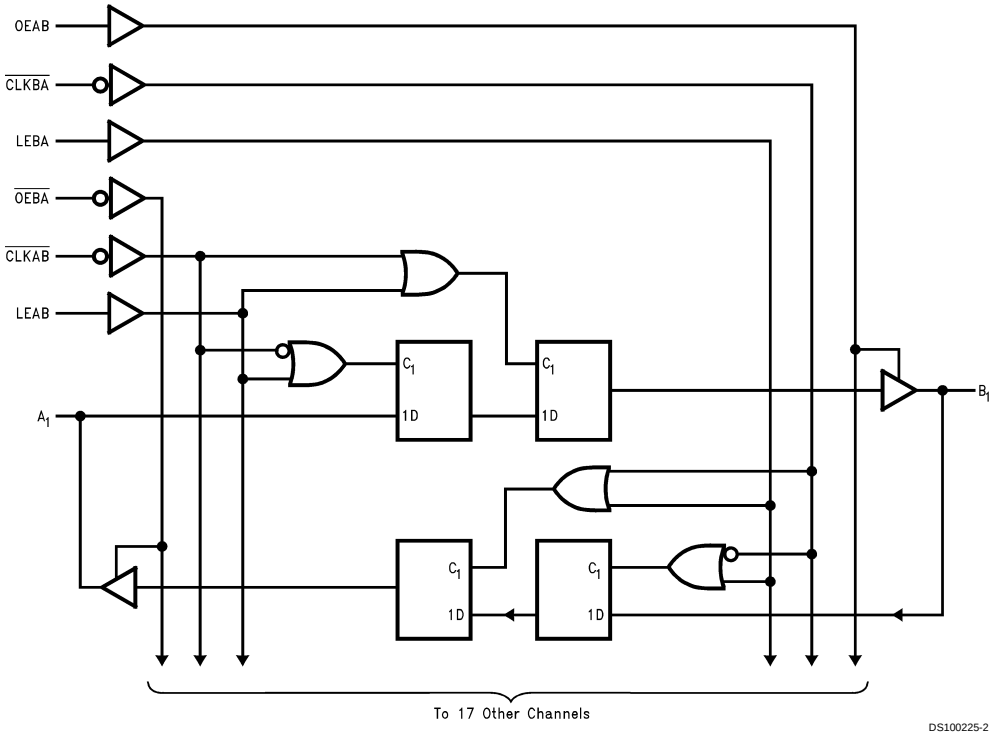
Note 1: A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$.

Note 2: Output level before the indicated steady-state input conditions were established.

Note 3: Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low.

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Logic Diagram



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Absolute Maximum Ratings (Note 4)

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage (Note 4)	−0.5V to +7.0V
Input Current (Note 4)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 4: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 5: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		ABT16500			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −24 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V (Note 6)
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V (Note 6)
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA
								All Other Pins Grounded
I_{IH} + I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$, OE = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$, OE = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				1.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				68	μA	Max	An or Bn Outputs Low
I_{CCZ}	Power Supply Current				1.0	mA	Max	$\overline{OE}_n$ = V_{CC},
								All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input				2.5	mA	Max	V_i = V_{CC} − 2.1V
								All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC}	No Load				mA/	Max	Outputs Open
	(Note 6)				0.23	MHz		Transparent Mode
								One Bit Toggling, 50% Duty Cycle

Note 6: Guaranteed, but not tested.

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DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V_{CC}	Conditions C_L = 50 pF; R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		1.1	V	5.0	T_A = 25˚C (Note 7)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}		-1.7	V	5.0	T_A = 25˚C (Note 7)

Note 7: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT T_A = −55˚C to +125˚C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Max		
f_{max}	Maximum Clock Frequency	150		MHz	
t_{PLH}	Propagation Delay	1.0	6.5	ns	*Figure 4*
t_{PHL}	A or B to B or A	1.0	7.0		
t_{PLH}	Propagation Delay	1.0	7.0	ns	*Figure 4*
t_{PHL}	LEAB or LEBA to B or A	1.0	7.8		
t_{PLH}	Propagation Delay	1.0	7.5	ns	*Figure 4*
t_{PHL}	$\overline{CLKAB}$ or $\overline{CLKBA}$ to B or A	1.0	8.0		
t_{PZH}	Propagation Delay	1.0	6.3	ns	*Figure 6*
t_{PZL}	OEAB or $\overline{OEBA}$ to B or A	1.0	6.5		
t_{PHZ}	Propagation Delay	1.0	7.2	ns	*Figure 6*
t_{PLZ}	OEAB or $\overline{OEBA}$ to B or A	1.0	6.8		

AC Operating Requirements

Symbol	Parameter	54ABT T_A = −55˚C to +125˚C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Max		
t_s(H)	Setup Time,	4.5		ns	*Figure 7*
t_s(L)	A to $\overline{CLKAB}$	4.5			
t_h(H)	Hold Time,	0		ns	*Figure 7*
t_h(L)	A to $\overline{CLKAB}$	0			
t_s(H)	Setup Time,	4.0		ns	*Figure 7*
t_s(L)	B to $\overline{CLKBA}$	4.0			
t_h(H)	Hold Time,	0		ns	*Figure 7*
t_h(L)	B to $\overline{CLKBA}$	0			
t_s(H)	Setup Time, A to LEAB	1.5		ns	*Figure 7*
t_s(L)	or B to LEBA, $\overline{CLK}$ High	1.5			
t_h(H)	Hold Time, A to LEAB	1.5		ns	*Figure 7*
t_h(L)	or B to LEBA, $\overline{CLK}$ High	1.5			
t_s(H)	Setup Time, A to LEAB	4.5		ns	*Figure 7*
t_s(L)	or B to LEBA, $\overline{CLK}$ Low	4.5			
t_h(H)	Hold Time, A to LEAB	1.5		ns	*Figure 7*
t_h(L)	or B to LEBA, $\overline{CLK}$ Low	1.5			
t_w(H)	Pulse Width,	3.3		ns	*Figure 5*
t_w(L)	LEAB or LEBA, High	3.3			

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AC Operating Requirements (Continued)

Symbol	Parameter	54ABT		Units	Fig. No.
		$T_A = -55^\circ C$ to $+125^\circ C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF			
		Min	Max		
$t_w(H)$	Pulse Width, $\overline{CLKAB}$	3.3		ns	*Figure 5*
$t_w(L)$	or $\overline{CLKBA}$, High or Low	3.3			

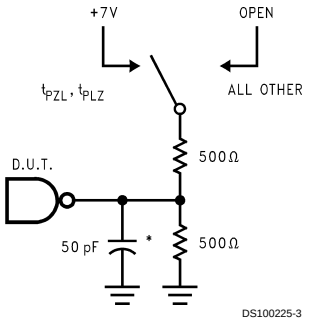
Capacitance

Symbol	Parameter	Typ	Units	Conditions, $T_A = 25^\circ C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0.0V$
$C_{I/O}$ (Note 8)	Output Capacitance	11.0	pF	$V_{CC} = 5.0V$

Note 8: $C_{I/O}$ is measured at frequency f = 1 MHz per MIL-STD-883B, Method 3012.

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AC Loading



*Includes jig and probe capacitance.

FIGURE 1. Standard AC Test Load

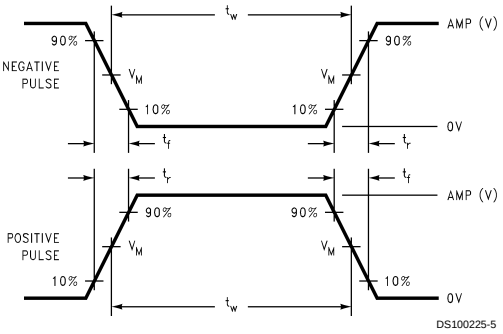


FIGURE 2. V_M = 1.5V

Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

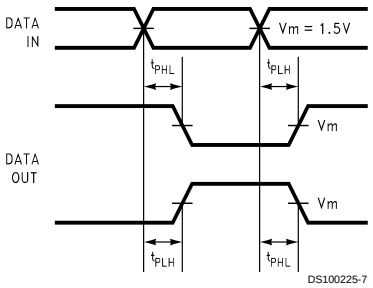


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

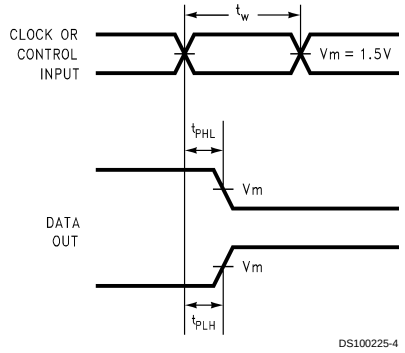


FIGURE 5. Propagation Delay, Pulse Width Waveforms

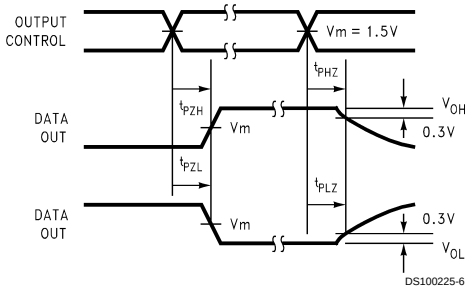


FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

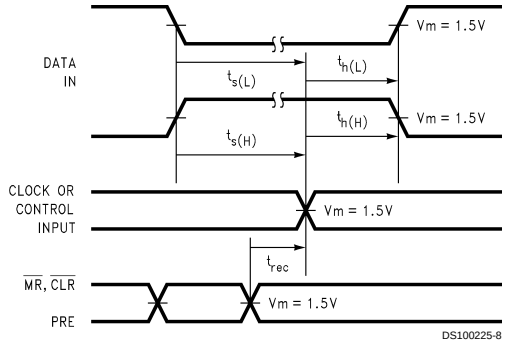
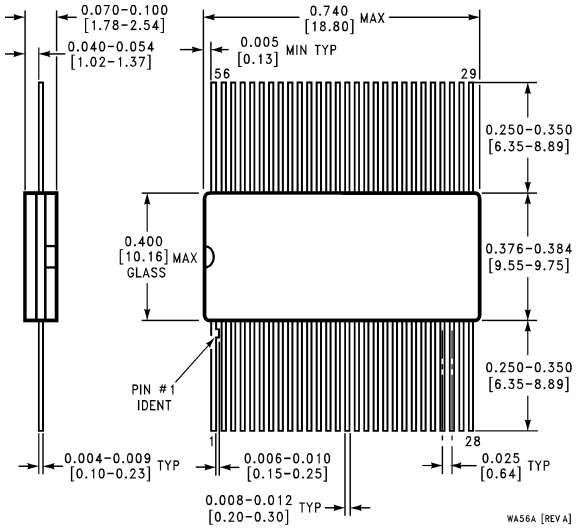


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

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Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Cerpack
NS Package Number WA56A

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