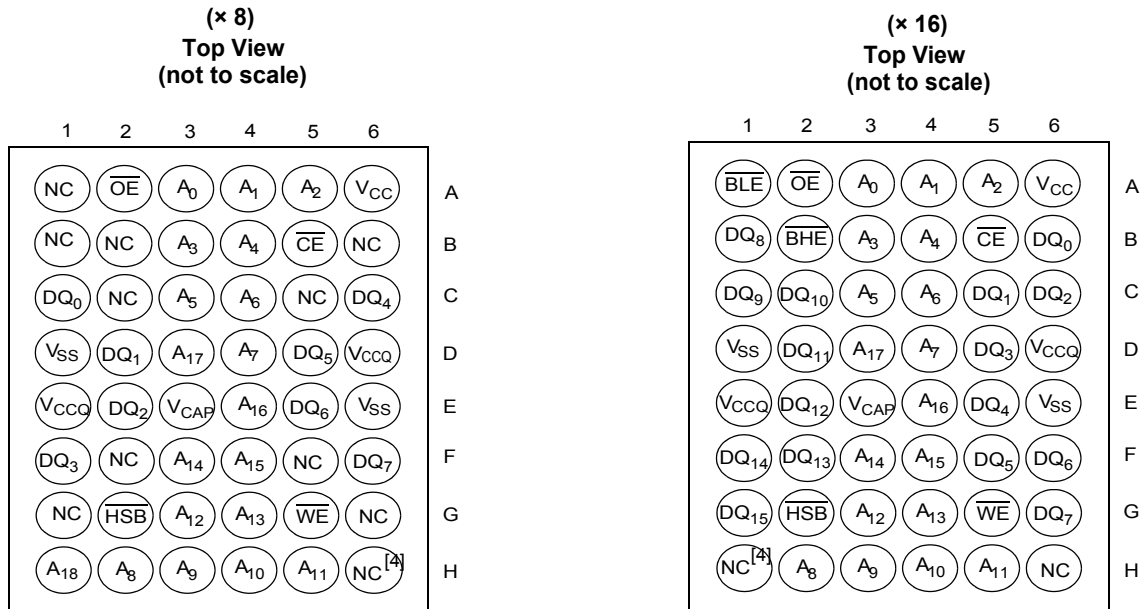


Contents

Pinouts	3	AC Switching Characteristics	11
Pin Definitions	3	SRAM Read Cycle	11
Device Operation	4	SRAM Write Cycle	11
SRAM Read	4	Switching Waveforms	11
SRAM Write	4	AutoStore/Power-Up RECALL	14
AutoStore Operation	4	Switching Waveforms	14
Hardware STORE Operation	4	Software Controlled STORE/RECALL Cycle	15
Hardware RECALL (Power-Up)	5	Switching Waveforms	15
Software STORE	5	Hardware STORE Cycle	16
Software RECALL	5	Switching Waveforms	16
Preventing AutoStore	6	Truth Table For SRAM Operations	17
Data Protection	6	Ordering Information	18
Noise Considerations	6	Ordering Code Definitions	18
Best Practices	7	Package Diagrams	19
Maximum Ratings	8	Acronyms	20
Operating Range	8	Document Conventions	20
DC Electrical Characteristics	8	Units of Measure	20
Data Retention and Endurance	9	Document History Page	21
Capacitance	9	Sales, Solutions, and Legal Information	22
Thermal Resistance	9	Worldwide Sales and Design Support	22
AC Test Loads	10	Products	22
AC Test Conditions	10	PSoC Solutions	22

Pinouts

Figure 1. Pin Diagram – 48-ball FBGA



Pin Definitions

Pin Name	I/O Type	Description
A ₀ –A ₁₈	Input	Address Inputs Used to Select One of the 524,288 bytes of the nvSRAM for × 8 Configuration.
A ₀ –A ₁₇		Address Inputs Used to Select One of the 262,144 words of the nvSRAM for × 16 Configuration.
DQ ₀ –DQ ₇	Input/output	Bidirectional Data I/O Lines for × 8 Configuration. Used as input or output lines depending on operation.
DQ ₀ –DQ ₁₅		Bidirectional Data I/O Lines for × 16 Configuration. Used as input or output lines depending on operation.
WE	Input	Write Enable Input, Active LOW. When selected LOW, data on the I/O pins is written to the specific address location.
CE	Input	Chip Enable Input, Active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
OE	Input	Output Enable, Active LOW. The active LOW OE input enables the data output buffers during read cycles. I/O pins are tri-stated on deasserting OE HIGH.
BHE	Input	Byte High Enable, Active LOW. Controls DQ ₁₅ –DQ ₈ .
BLE	Input	Byte Low Enable, Active LOW. Controls DQ ₇ –DQ ₀ .
V _{SS}	Ground	Ground for the Device. Must be connected to the ground of the system.
V _{CC}	Power supply	Power Supply Inputs to the Core of the Device.
V _{CCQ}	Power supply	Power Supply Inputs for the Inputs and Outputs of the Device.
HSB	Input/output	Hardware Store Busy (HSB). When LOW this output indicates that a Hardware STORE is in progress. When pulled LOW external to the chip it initiates a non-volatile STORE operation. After each Hardware and Software STORE operation HSB is driven HIGH for a short time (t _{HHHD}) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (External pull-up resistor connection optional).
V _{CAP}	Power supply	AutoStore Capacitor. Supplies power to the nvSRAM during power loss to store data from SRAM to non-volatile elements.
NC	No Connect	No Connect. This pin is not connected to the die.

Note

4. Address expansion for 8-Mbit. NC pin not connected to die.

Device Operation

The CY14V104LA/CY14V104NA nvSRAM is made up of two functional components paired in the same physical cell. They are a SRAM memory cell and a non-volatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the non-volatile cell (the STORE operation), or from the non-volatile cell to the SRAM (the RECALL operation). Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The CY14V104LA/CY14V104NA supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the non-volatile cells and up to 1 million STORE operations. See [Truth Table For SRAM Operations on page 17](#) for a complete description of read and write modes.

SRAM Read

The CY14V104LA/CY14V104NA performs a read cycle when $\overline{CE}$ and $\overline{OE}$ are LOW and $\overline{WE}$ and HSB are HIGH. The address specified on pins A_{0-18} or A_{0-17} determines which of the 524,288 data bytes or 262,144 words of 16 bits each are accessed. Byte enables (BHE, BLE) determine which bytes are enabled to the output, in the case of 16-bit words. When the read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (read cycle 1). If the read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE} , whichever is later (read cycle 2). The data output repeatedly responds to address changes within the t_{AA} access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or HSB is brought LOW.

SRAM Write

A write cycle is performed when $\overline{CE}$ and $\overline{WE}$ are LOW and HSB is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins DQ_{0-15} are written into the memory if the data is valid t_{SD} before the end of a $\overline{WE}$ controlled write or before the end of an $\overline{CE}$ controlled write. The Byte Enable inputs (BHE, BLE) determine which bytes are written, in the case of 16-bit words. It is recommended that $\overline{OE}$ be kept HIGH during the entire write cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation

The CY14V104LA/CY14V104NA stores data to the nvSRAM using one of the following three storage operations: Hardware Store activated by HSB; Software Store activated by an address sequence; AutoStore on device power-down. The AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14V104LA/CY14V104NA.

During a normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH} , the part automatically disconnects the V_{CAP} pin from V_{CC} . A STORE operation is initiated with power provided by the V_{CAP} capacitor.

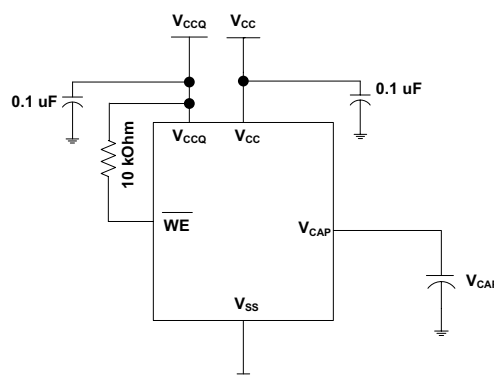
Note If a capacitor is not connected to V_{CAP} pin, AutoStore must be disabled using the soft sequence specified in [Preventing AutoStore on page 6](#). If AutoStore is enabled without a capacitor

on V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the Store. This may corrupt the data stored in nvSRAM.

Figure 2 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to [DC Electrical Characteristics on page 8](#) for the size of V_{CAP} . The voltage on the V_{CAP} pin is driven to V_{CC} by a regulator on the chip. A pull-up should be placed on $\overline{WE}$ to hold it inactive during power-up. This pull-up is effective only if the $\overline{WE}$ signal is tristate during power-up. Many MPUs tristate their controls on power-up. This should be verified when using the pull-up. When the nvSRAM comes out of power-on-recall, the MPU must be active or the $\overline{WE}$ held inactive until the MPU comes out of reset.

To reduce unnecessary non-volatile stores, AutoStore and hardware store operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place. The HSB signal is monitored by the system to detect if an AutoStore cycle is in progress.

Figure 2. AutoStore Mode



Hardware STORE Operation

The CY14V104LA/CY14V104NA provides the HSB pin to control and acknowledge the STORE operations. Use the HSB pin to request a hardware STORE cycle. When the HSB pin is driven LOW, the CY14V104LA/CY14V104NA conditionally initiates a STORE operation after t_{DELAY} . An actual STORE cycle only begins if a write to the SRAM has taken place since the last STORE or RECALL cycle. The HSB pin also acts as an open drain driver (internal 100 k Ω weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

Note After each Hardware and Software STORE operation HSB is driven HIGH for a short time (t_{HHHD}) with standard output high current and then remains HIGH by internal 100 k Ω pull-up resistor.

SRAM write operations that are in progress when HSB is driven LOW by any means are given time (t_{DELAY}) to complete before the STORE operation is initiated. However, any SRAM write cycles requested after HSB goes LOW are inhibited until HSB returns HIGH. In case the write latch is not set, HSB is not driven LOW by the CY14V104LA/CY14V104NA. But any SRAM read and write cycles are inhibited until HSB is returned HIGH by MPU or other external source.

During any STORE operation, regardless of how it is initiated, the CY14V104LA/CY14V104NA continues to drive the HSB pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the CY14V104LA/CY14V104NA remains disabled until the HSB pin returns HIGH. Leave the HSB unconnected if it is not used.

Hardware RECALL (Power-Up)

During power-up or after any low power condition ($V_{CC} < V_{SWITCH}$), an internal RECALL request is latched. When V_{CC} again exceeds the sense voltage of V_{SWITCH} , a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time, HSB is driven LOW by the HSB driver.

Software STORE

Data is transferred from SRAM to the non-volatile memory by a software address sequence. The CY14V104LA/CY14V104NA software STORE cycle is initiated by executing sequential CE controlled read cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous non-volatile data is first performed, followed by a program of the non-volatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence, or the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following read sequence must be performed.

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ

4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x8FC0 Initiate STORE Cycle

The software sequence may be clocked with $\overline{CE}$ controlled reads or $\overline{OE}$ controlled reads, with $\overline{WE}$ kept HIGH for all the six READ sequences. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. HSB is driven LOW. After the t_{STORE} cycle time is fulfilled, the SRAM is activated again for the read and write operation.

Software RECALL

Data is transferred from non-volatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of read operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of CE controlled read operations must be performed.

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x4C63 Initiate RECALL Cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared; then, the non-volatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the non-volatile elements.

Table 1. Mode Selection

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}, \overline{BLE}^{[5]}$	$A_{15}-A_0^{[6]}$	Mode	I/O	Power
H	X	X	X	X	Not Selected	Output High Z	Standby
L	H	L	L	X	Read SRAM	Output Data	Active
L	L	X	L	X	Write SRAM	Input Data	Active
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active ^[7]

Notes

5. $\overline{BHE}$ and $\overline{BLE}$ are applicable for $\times 16$ configuration only.
6. While there are 19 address lines on the CY14V104LA (18 address lines on the CY14V104NA), only the 13 address lines ($A_{14}-A_2$) are used to control software modes. Rest of the address lines are don't care.
7. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a non-volatile cycle.

Table 1. Mode Selection (continued)

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}, \overline{\text{BLE}}^{[5]}$	$\text{A}_{15}\text{--}\text{A}_0^{[6]}$	Mode	I/O	Power
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active ^[8]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Non-volatile Store	Output Data Output Data Output Data Output Data Output Data Output High Z	Active $\text{I}_{\text{CC2}}^{[8]}$
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Non-volatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active ^[8]

Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of $\overline{\text{CE}}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8B45 AutoStore Disable

The AutoStore is re-enabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of $\overline{\text{CE}}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (hardware or software) must be issued to save the AutoStore state through subsequent power-down cycles. The part comes from the factory with AutoStore enabled.

Data Protection

The CY14V104LA/CY14V104NA protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and write operations. The low voltage condition is detected when $V_{\text{CC}} < V_{\text{SWITCH}}$. If the CY14V104LA/CY14V104NA is in a write mode (both $\overline{\text{CE}}$ and $\overline{\text{WE}}$ are LOW) at power-up, after a RECALL or STORE, the write is inhibited until the SRAM is enabled after t_{LZHSB} (HSB to output active). When $V_{\text{CCQ}} < V_{\text{IODIS}}$, I/Os are disabled (no STORE takes place). This protects against inadvertent writes during brown out conditions on V_{CCQ} supply.

Noise Considerations

Refer to Cypress application note, [AN1064](#).

Note

8. The six consecutive address locations must be in the order listed. $\overline{\text{WE}}$ must be HIGH during all six cycles to enable a non-volatile cycle.

Best Practices

nvSRAM products have been used effectively for over 26 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The non-volatile cells in this nvSRAM product are delivered from Cypress with 0x00 written in all cells. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on should always program a unique NV pattern (that is, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power-up boot firmware routines should rewrite the nvSRAM into the desired state (for example, autostore enabled). While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently such as program bugs and incoming inspection routines.
- The V_{CAP} value specified in this data sheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the maximum V_{CAP} value because the nvSRAM internal algorithm calculates V_{CAP} charge and discharge time based on this max V_{CAP} value. Customers that want to use a larger V_{CAP} value to make sure there is extra store charge and store time should discuss their V_{CAP} size selection with Cypress to understand any impact on the V_{CAP} voltage level at the end of a t_{RECALL} period.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Maximum accumulated storage time

At 150 °C ambient temperature 1000 h

At 85 °C ambient temperature 20 Years

Ambient temperature with power applied -55 °C to +150 °C

Supply voltage on V_{CC} relative to V_{SS} -0.5 V to 4.1 V

Supply voltage on V_{CCQ} relative to V_{SS} -0.5 V to 2.45 V

Voltage applied to outputs in High Z state -0.5 V to $V_{CCQ} + 0.5$ V

Input voltage -0.5 V to $V_{CCQ} + 0.5$ V

Transient voltage (< 20 ns) on any pin to ground potential -2.0 V to $V_{CCQ} + 2.0$ V

Package power dissipation capability ($T_A = 25$ °C) 1.0 W

Surface mount Pb soldering temperature (3 seconds) +260 °C

DC output current (1 output at a time, 1s duration) 15 mA

Static discharge voltage (per MIL-STD-883, Method 3015) > 2001 V

Latch up current > 140 mA

Operating Range

Range	Ambient Temperature	V_{CC}	V_{CCQ}
Industrial	-40 °C to +85 °C	3.0 V – 3.6 V	1.65 V – 1.95 V

DC Electrical Characteristics

Over the [Operating Range](#)

Parameter	Description	Test Conditions	Min	Typ ^[9]	Max	Unit
V_{CC}	Power supply voltage	–	3.0	3.3	3.6	V
V_{CCQ}			1.65	1.8	1.95	V
I_{CC1}	Average V_{CC} current	$t_{RC} = 25$ ns $t_{RC} = 45$ ns Values obtained without output loads ($I_{OUT} = 0$ mA)	–	–	70	mA
I_{CCQ1}	Average V_{CCQ} current	All inputs don't care, $V_{CC} = \text{Max}$ Average current for duration t_{STORE}	–	–	52	mA
I_{CC2}	Average V_{CC} current during STORE		–	–	15	mA
I_{CC3}	Average V_{CCQ} current	All inputs don't care, $V_{CC} = \text{Max}$ Average current for duration t_{STORE}	–	–	10	mA
I_{CCQ3}	Average V_{CCQ} current during STORE		–	–	10	mA
I_{CC4}	Average V_{CC} current at $t_{RC} = 200$ ns, $V_{CC}(\text{Typ})$, 25 °C	All inputs cycling at CMOS levels. Values obtained without output loads ($I_{OUT} = 0$ mA).	–	35	–	mA
I_{CCQ4}	Average V_{CCQ} current at $t_{RC} = 200$ ns, $V_{CCQ}(\text{Typ})$, 25 °C		–	5	–	mA
I_{CC5}	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}	–	–	8	mA
I_{SB}	V_{CC} standby current	$CE \geq (V_{CC} - 0.2$ V). $V_{IN} \leq 0.2$ V or $\geq (V_{CC} - 0.2$ V). Standby current level after non-volatile cycle is complete. Inputs are static. $f = 0$ MHz.	–	–	8	mA
$I_{IX}^{[10]}$	Input leakage current (except HSB)	$V_{CCQ} = \text{Max}$, $V_{SS} \leq V_{IN} \leq V_{CCQ}$	–1	–	+1	μA
	Input leakage current (for HSB)	$V_{CCQ} = \text{Max}$, $V_{SS} \leq V_{IN} \leq V_{CCQ}$	–100	–	+1	μA
I_{OZ}	Off-state output leakage current	$V_{CCQ} = \text{Max}$, $V_{SS} \leq V_{OUT} \leq V_{CCQ}$, CE or $OE \geq V_{IH}$ or $BHE/BLE \geq V_{IH}$ or $WE \leq V_{IL}$	–1	–	+1	μA
$V_{CAP}^{[11]}$	Storage capacitor	Between V_{CAP} pin and V_{SS} , 5 V rated	61	68	180	μF

Notes

9. Typical values are at 25 °C, $V_{CC} = V_{CC}(\text{Typ})$ and $V_{CCQ} = V_{CCQ}(\text{Typ})$. Not 100% tested.

10. The HSB pin has $I_{OUT} = -4$ μA for V_{OH} of 1.07 V when both active HIGH and LOW drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.

11. Min V_{CAP} value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V_{CAP} value guarantees that the capacitor on V_{CAP} is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore it is always recommended to use a capacitor within the specified min and max limits. Refer application note [AN43593](#) for more details on V_{CAP} options.

DC Electrical Characteristics (continued)

Over the [Operating Range](#)

Parameter	Description	Test Conditions	Min	Typ ^[9]	Max	Unit
V _{IH}	Input HIGH voltage	–	0.7 × V _{CCQ}	–	V _{CCQ} + 0.3	V
V _{IL}	Input LOW voltage	–	– 0.3	–	0.3 × V _{CCQ}	V
V _{OH}	Output HIGH voltage	I _{OUT} = –1 mA	V _{CCQ} – 0.45	–	–	V
V _{OL}	Output LOW voltage	I _{OUT} = 2 mA		–	0.45	V

Data Retention and Endurance

Over the [Operating Range](#)

Parameter	Description	Min	Unit
DATA _R	Data retention	20	Years
NV _C	Non-volatile STORE operation	1,000	K

Capacitance

Parameter ^[12]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance (except BLE, BHE and HSB)	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC} (Typ), V _{CCQ} = V _{CCQ} (Typ)	7	pF
	Input capacitance (for BLE, BHE and HSB)		8	pF
C _{OUT}	Output capacitance (except HSB)		7	pF
	Output capacitance (for HSB)		8	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed.

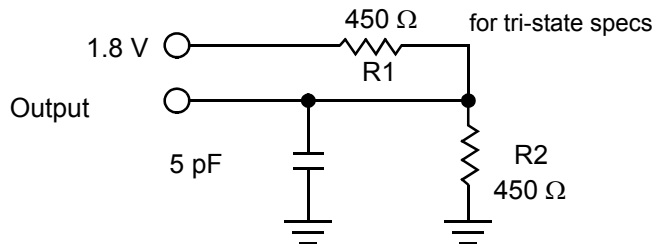
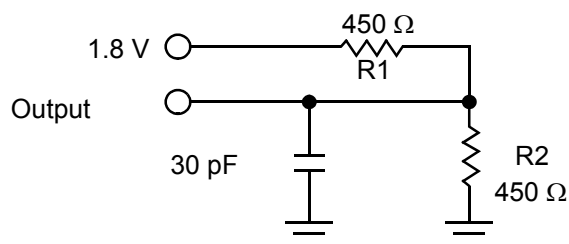
Parameter ^[12]	Description	Test Conditions	48-ball FBGA	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	46.09	°C/W
Θ _{JC}	Thermal resistance (junction to case)		7.84	°C/W

Note

12. These parameters are guaranteed by design but not tested.

AC Test Loads

Figure 3. AC Test Loads



AC Test Conditions

Input pulse levels 0 V to 1.8 V
 Input rise and fall times (10%–90%) ≤1.8 ns
 Input and output timing reference levels 0.9 V

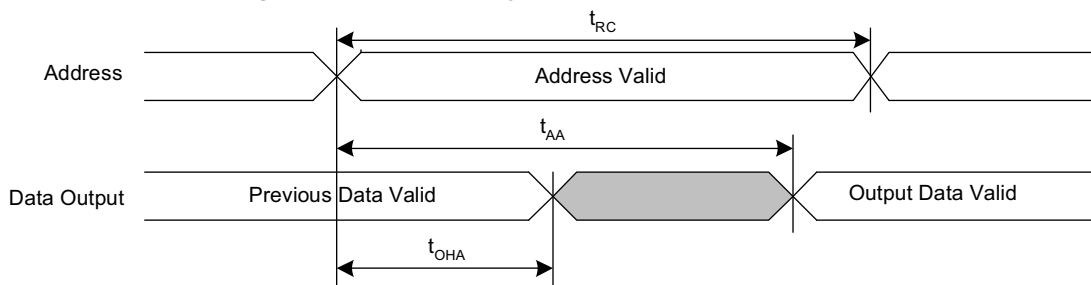
AC Switching Characteristics

Over the [Operating Range](#)

Parameters ^[13]		Description	25 ns		45 ns		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	
SRAM Read Cycle							
t _{ACE}	t _{ACS}	Chip enable access time	–	25	–	45	ns
t _{RC} ^[14]	t _{RC}	Read cycle time	25	–	45	–	ns
t _{AA} ^[15]	t _{AA}	Address access time	–	25	–	45	ns
t _{DOE}	t _{OE}	Output enable to data valid	–	12	–	20	ns
t _{OHA} ^[15]	t _{OH}	Output hold after address change	3	–	3	–	ns
t _{LZCE} ^[16, 17]	t _{LZ}	Chip enable to output active	3	–	3	–	ns
t _{HZCE} ^[16, 17]	t _{HZ}	Chip disable to output inactive	–	10	–	15	ns
t _{LZOE} ^[16, 17]	t _{OLZ}	Output enable to output active	0	–	0	–	ns
t _{HZOE} ^[16, 17]	t _{OHZ}	Output disable to output inactive	–	10	–	15	ns
t _{PU} ^[16]	t _{PA}	Chip enable to power active	0	–	0	–	ns
t _{PD} ^[16]	t _{PS}	Chip disable to power standby	–	25	–	45	ns
t _{DBE}	–	Byte enable to data valid	–	12	–	20	ns
t _{LZBE} ^[16]	–	Byte enable to output active	0	–	0	–	ns
t _{HZBE} ^[16]	–	Byte disable to output inactive	–	10	–	15	ns
SRAM Write Cycle							
t _{WC}	t _{WC}	Write cycle time	25	–	45	–	ns
t _{PWE}	t _{WP}	Write pulse width	20	–	30	–	ns
t _{SCE}	t _{CW}	Chip enable to end of write	20	–	30	–	ns
t _{SD}	t _{DW}	Data setup to end of write	10	–	15	–	ns
t _{HD}	t _{DH}	Data hold after end of write	0	–	0	–	ns
t _{AW}	t _{AW}	Address setup to end of write	20	–	30	–	ns
t _{SA}	t _{AS}	Address setup to start of write	0	–	0	–	ns
t _{HA}	t _{WR}	Address hold after end of write	0	–	0	–	ns
t _{HZWE} ^[16, 17, 18]	t _{WZ}	Write enable to output disable	–	10	–	15	ns
t _{LZWE} ^[16, 17]	t _{OW}	Output active after end of write	3	–	3	–	ns
t _{BW}	–	Byte enable to end of write	20	–	30	–	ns

Switching Waveforms

Figure 4. SRAM Read Cycle #1 (Address Controlled) ^[14, 15, 19]



Notes

13. Test conditions assume signal transition time of 1.8 ns or less, timing reference levels of $V_{CCQ}/2$, input pulse levels of 0 to $V_{CCQ(typ)}$, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in [Figure 3 on page 10](#).
14. WE must be HIGH during SRAM read cycles.
15. Device is continuously selected with CE, OE and $\overline{BHE} / \overline{BLE}$ LOW.
16. These parameters are guaranteed by design but not tested.
17. Measured ± 200 mV from steady state output voltage.
18. If WE is LOW when CE goes LOW, the outputs remain in the high impedance state.
19. HSB must remain HIGH during read and write cycles.

Switching Waveforms (continued)

Figure 5. SRAM Read Cycle #2 ($\overline{\text{CE}}$ and $\overline{\text{OE}}$ Controlled) [20, 21, 22]

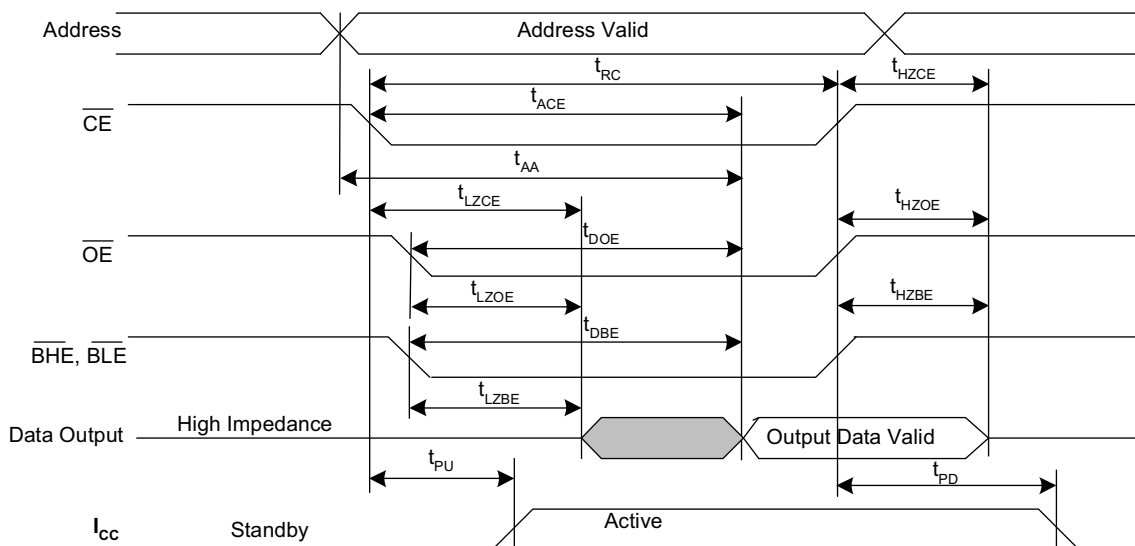
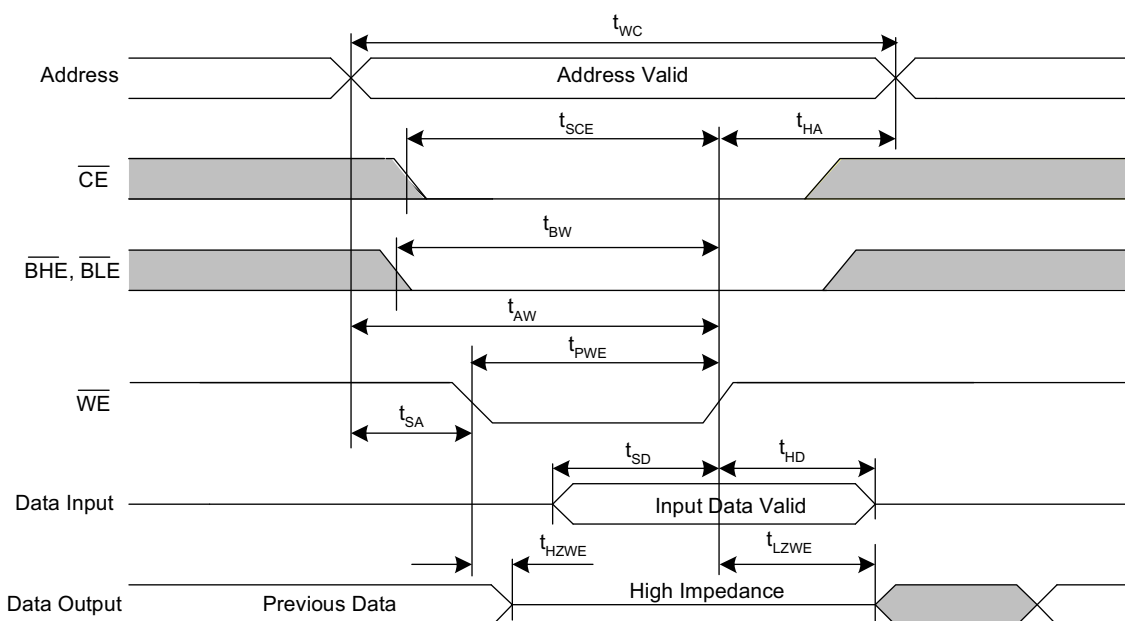


Figure 6. SRAM Write Cycle #1 ($\overline{\text{WE}}$ Controlled) [22, 23, 24, 25]



Notes

20. Typical values are at 25 °C, $V_{\text{CC}} = V_{\text{CC(Typ)}}$ and $V_{\text{CCQ}} = V_{\text{CCQ(Typ)}}$. Not 100% tested.
21. $\overline{\text{WE}}$ must be HIGH during SRAM read cycles.
22. $\overline{\text{HSB}}$ must remain HIGH during read and write cycles.
23. BHE and BLE are applicable for x16 configuration only.
24. If $\overline{\text{WE}}$ is LOW when $\overline{\text{CE}}$ goes LOW, the outputs remain in the high impedance state.
25. $\overline{\text{CE}}$ or $\overline{\text{WE}}$ must be $\geq V_{\text{IH}}$ during address transitions.

Switching Waveforms (continued)

Figure 7. SRAM Write Cycle #2 ($\overline{\text{CE}}$ Controlled) [26, 27, 28, 29]

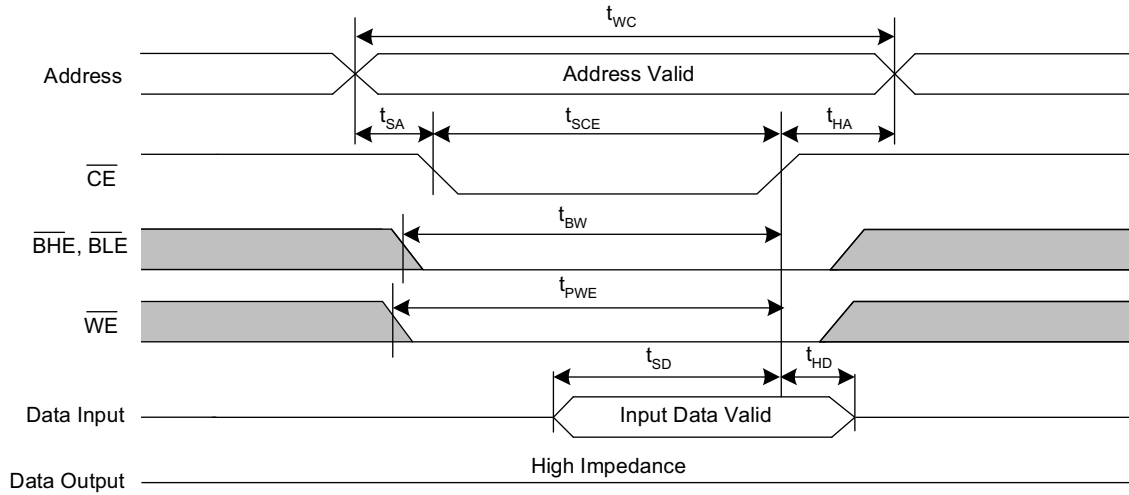
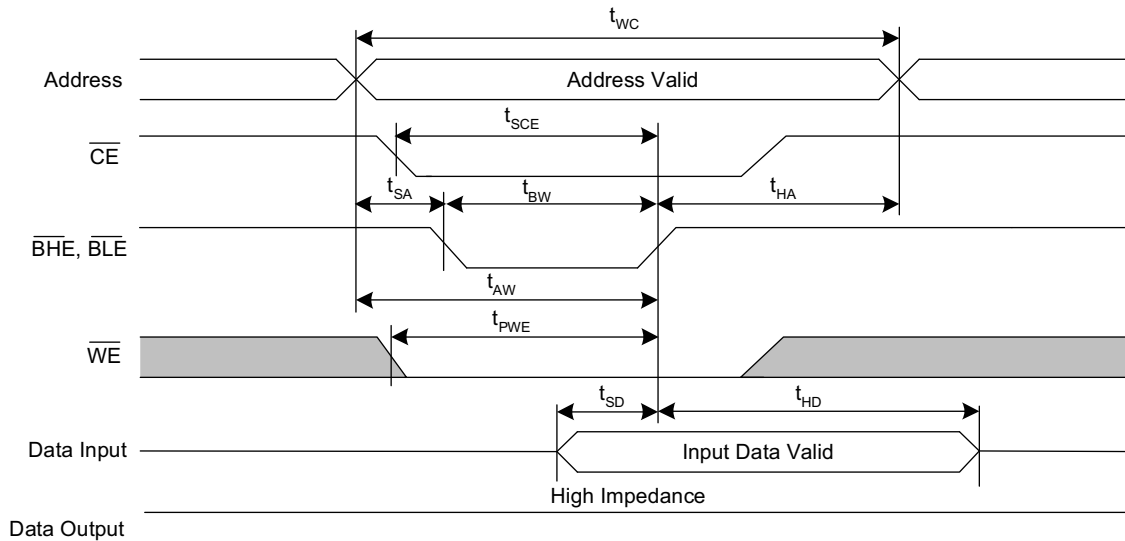


Figure 8. SRAM Write Cycle #3 ($\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ Controlled) [26, 27, 28, 29]



Notes

26. $\overline{\text{HSB}}$ must remain HIGH during read and write cycles.
27. $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ are applicable for $\times 16$ configuration only.
28. If $\overline{\text{WE}}$ is LOW when $\overline{\text{CE}}$ goes LOW, the outputs remain in the high impedance state.
29. $\overline{\text{CE}}$ or $\overline{\text{WE}}$ must be $\geq V_{IH}$ during address transitions.

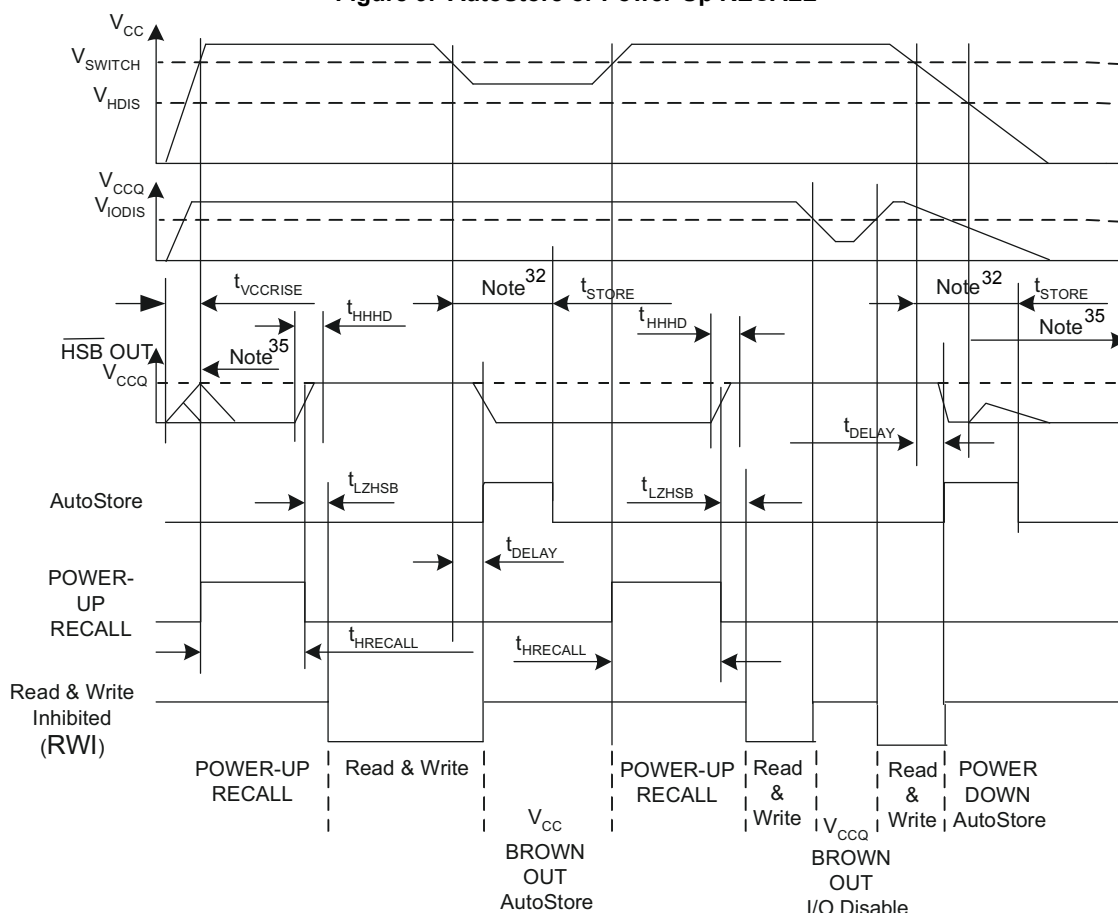
AutoStore/Power-Up RECALL

Over the [Operating Range](#)

Parameter	Description	CY14V104LA/CY14V104NA		Unit
		Min	Max	
$t_{HRECALL}^{[30]}$	Power-Up RECALL duration	–	20	ms
$t_{STORE}^{[31]}$	STORE cycle duration	–	8	ms
$t_{DELAY}^{[32]}$	Time allowed to complete SRAM write cycle	–	25	ns
V_{SWITCH}	Low voltage trigger level for V_{CC}	–	2.90	V
$V_{IODIS}^{[33]}$	I/O disable voltage on V_{CCQ}	–	1.50	V
$t_{VCCRRISE}^{[36]}$	V_{CC} rise time	150	–	μ s
$V_{HDIS}^{[36]}$	HSB output disable voltage on V_{CC}	–	1.9	V
$t_{LZHSB}^{[36]}$	HSB to output active time	–	5	μ s
$t_{HHHD}^{[36]}$	HSB high active time	–	500	ns

Switching Waveforms

Figure 9. AutoStore or Power-Up RECALL ^[34]



Notes

30. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH} .
31. If an SRAM write has not taken place since the last non-volatile cycle, no AutoStore or Hardware Store takes place.
32. On a Hardware Store and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY} .
33. HSB will not be defined below V_{IODIS} voltage.
34. Read and write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH} .
35. During power-up and power-down, HSB glitches when HSB pin is pulled up through an external resistor.
36. These parameters are guaranteed by design but not tested.

Software Controlled STORE/RECALL Cycle

Over the [Operating Range](#)

Parameters [37, 38]	Description	25 ns		45 ns		Unit
		Min	Max	Min	Max	
t_{RC}	STORE/RECALL initiation cycle time	25	—	45	—	ns
t_{SA}	Address setup time	0	—	0	—	ns
t_{CW}	Clock pulse width	20	—	30	—	ns
t_{HA}	Address hold time	0	—	0	—	ns
t_{RECALL}	RECALL duration	—	200	—	200	μ s

Switching Waveforms

Figure 10. $\overline{CE}$ and $\overline{OE}$ Controlled Software STORE/RECALL Cycle [38]

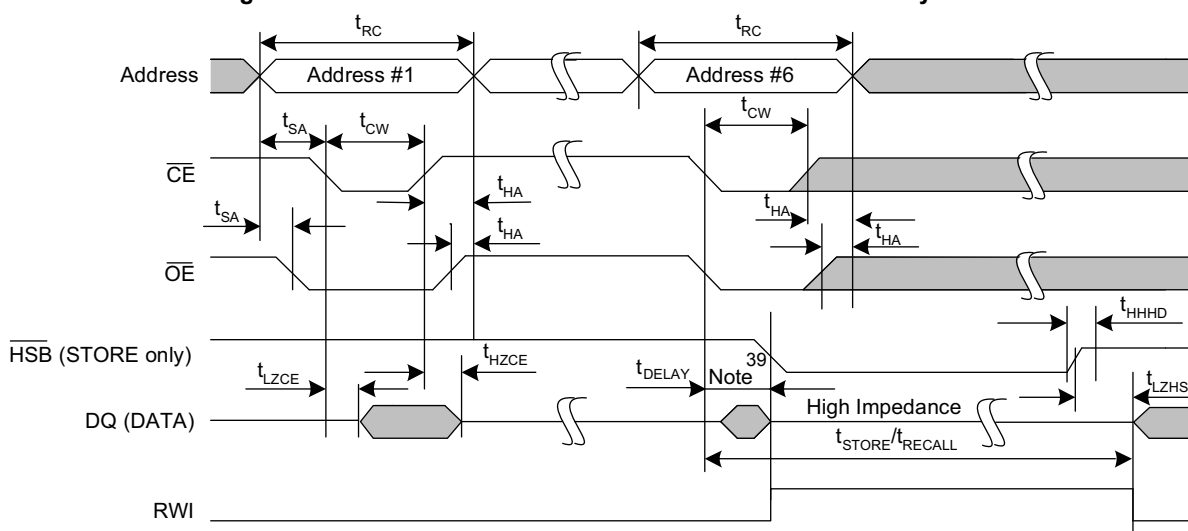
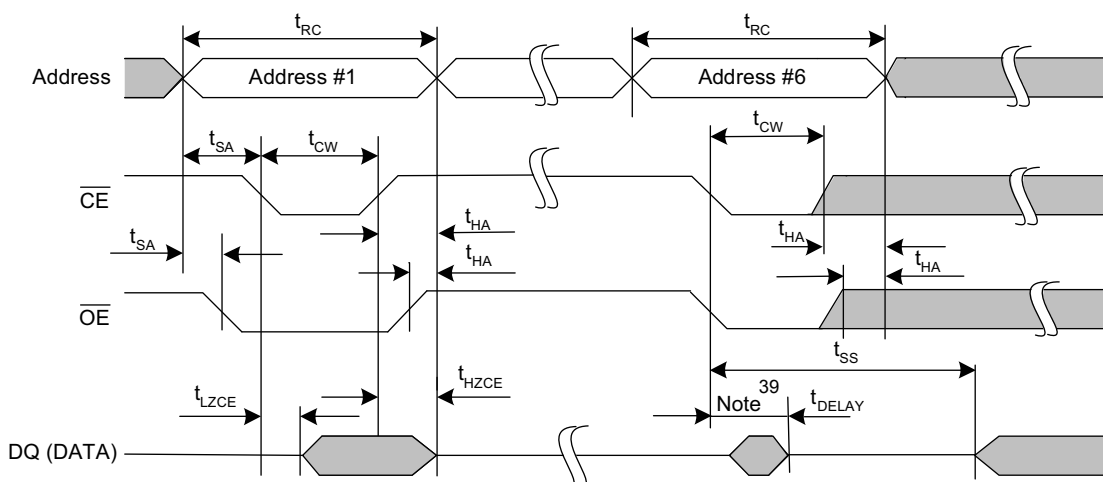


Figure 11. AutoStore Enable/Disable Cycle



Notes

37. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled reads.

38. The six consecutive addresses must be read in the order listed in [Table 1 on page 5](#). $\overline{WE}$ must be HIGH during all six consecutive cycles.

39. DQ output data at the sixth read may be invalid since the output is disabled at t_{DELAY} time.

Hardware STORE Cycle

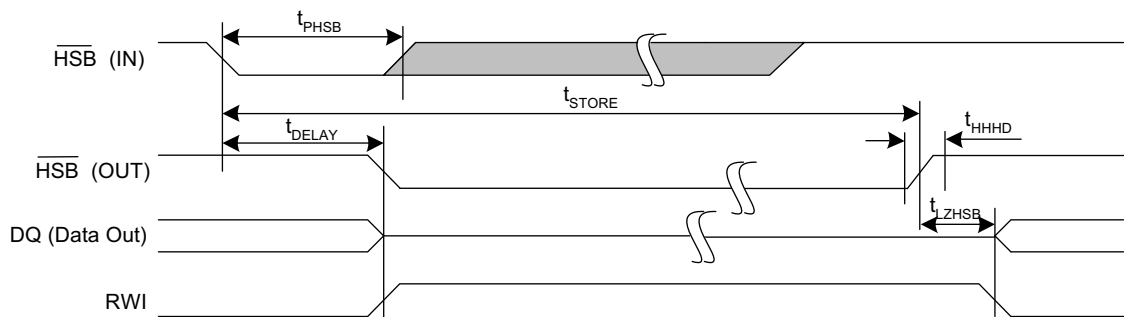
Over the [Operating Range](#)

Parameters	Description	CY14V104LA/CY14V104NA		Unit
		Min	Max	
t_{DHSB}	HSB to output active time when write latch not set	–	25	ns
t_{PHSB}	Hardware STORE pulse width	15	–	ns
$t_{\text{SS}}^{[40, 41]}$	Soft sequence processing time	–	100	μs

Switching Waveforms

Figure 12. Hardware STORE Cycle ^[42]

Write latch set



Write latch not set

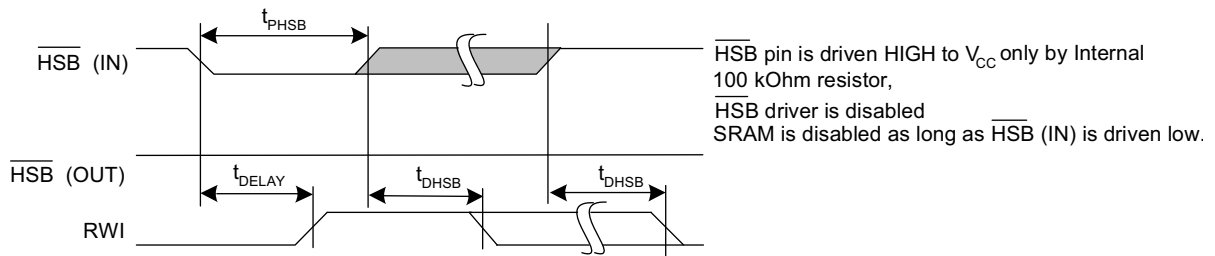
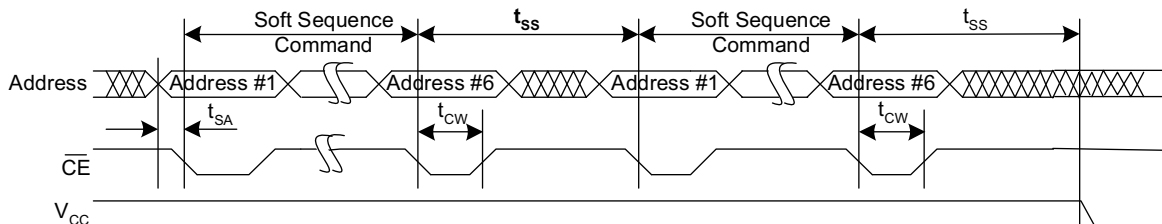


Figure 13. Soft Sequence Processing ^[40, 41]



Notes

40. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
41. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.
42. If an SRAM write has not taken place since the last non-volatile cycle, no AutoStore or Hardware Store takes place.

Truth Table For SRAM Operations

HSB should remain HIGH for SRAM Operations.

Table 2. Truth Table for × 8 Configuration

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs ^[43]	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby
L	H	L	Data out (DQ ₀ –DQ ₇)	Read	Active
L	H	H	High Z	Output disabled	Active
L	L	X	Data in (DQ ₀ –DQ ₇)	Write	Active

Table 3. Truth Table for × 16 Configuration

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$ ^[44]	$\overline{\text{BLE}}$ ^[44]	Inputs/Outputs ^[43]	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-down	Standby
L	X	X	H	H	High Z	Output disabled	Active
L	H	L	L	L	Data out (DQ ₀ –DQ ₁₅)	Read	Active
L	H	L	H	L	Data out (DQ ₀ –DQ ₇); DQ ₈ –DQ ₁₅ in High Z	Read	Active
L	H	L	L	H	Data out (DQ ₈ –DQ ₁₅); DQ ₀ –DQ ₇ in High Z	Read	Active
L	H	H	L	L	High Z	Output disabled	Active
L	H	H	H	L	High Z	Output disabled	Active
L	H	H	L	H	High Z	Output disabled	Active
L	L	X	L	L	Data in (DQ ₀ –DQ ₁₅)	Write	Active
L	L	X	H	L	Data in (DQ ₀ –DQ ₇); DQ ₈ –DQ ₁₅ in High Z	Write	Active
L	L	X	L	H	Data in (DQ ₈ –DQ ₁₅); DQ ₀ –DQ ₇ in High Z	Write	Active

Notes

43. Data DQ₀–DQ₇ for × 8 configuration and Data DQ₀–DQ₁₅ for × 16 configuration.

44. BHE and BLE are applicable for × 16 configuration only.

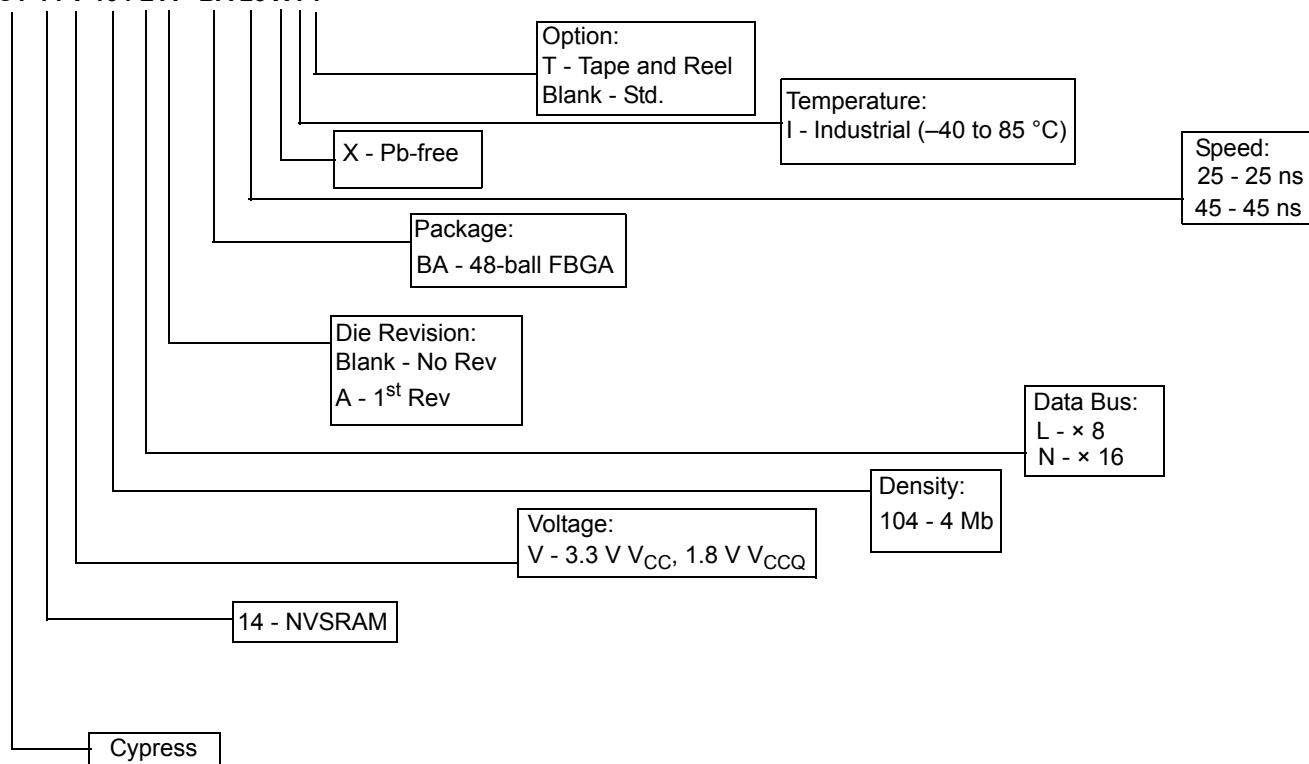
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14V104LA-BA25XIT	51-85128	48-ball FBGA	Industrial
	CY14V104LA-BA25XI			
	CY14V104NA-BA25XIT			
	CY14V104NA-BA25XI			
45	CY14V104LA-BA45XIT			
	CY14V104LA-BA45XI			
	CY14V104NA-BA45XIT			
	CY14V104NA-BA45XI			

Contact your local Cypress sales representative for availability of these parts.

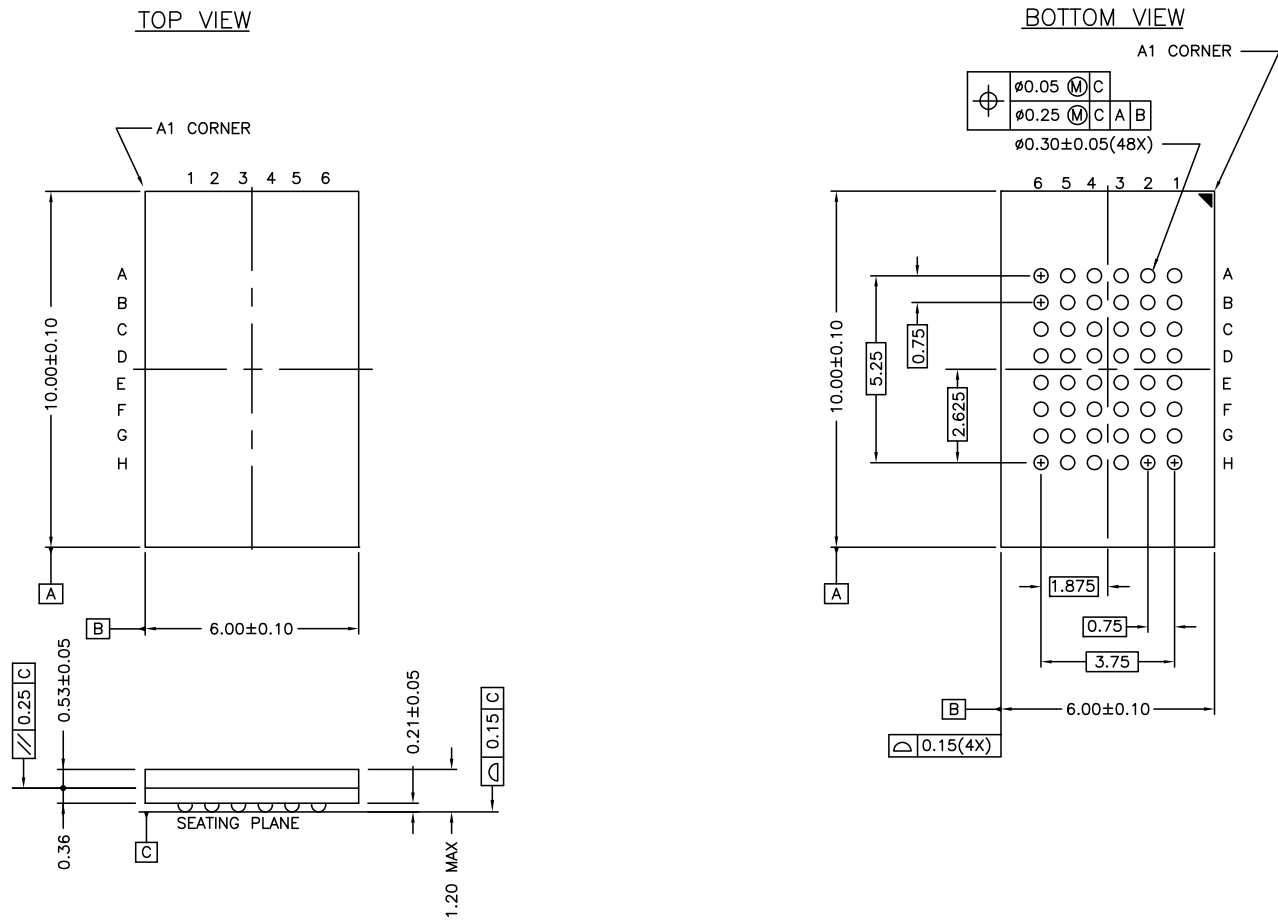
Ordering Code Definitions

CY 14 V 104 L A - BA 25 X I T



Package Diagrams

Figure 14. 48-ball FBGA (6 × 10 × 1.2 mm) BA48B, 51-85128



51-85128 *F

Acronyms

Acronym	Description
BHE	byte high enable
BLE	byte low enable
CE	chip enable
CMOS	complementary metal oxide semiconductor
EIA	electronic industries alliance
FBGA	fine-pitch ball grid array
HSB	hardware store busy
I/O	input/output
nvSRAM	non-volatile static random access memory
OE	output enable
RoHS	restriction of hazardous substances
SRAM	static random access memory
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilo ohms
MHz	Mega Hertz
μA	micro Amperes
mA	milli Amperes
μF	micro Farads
μs	micro seconds
ms	milli seconds
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farads
V	Volts
W	Watts

Document History Page

Document Title: CY14V104LA/CY14V104NA, 4-Mbit (512 K × 8 / 256 K × 16) nvSRAM Document Number: 001-53954				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2729117	GVCH / AESA	07/02/2009	New Data Sheet
*A	2826127	GVCH / AESA	12/11/2009	Removed commercial temperature related specs Changed part number from CY14A104L/CY14A104N to CY14V104LA/CY14V104NA Removed 20 ns Access speed specs Removed 44/54 TSOP II package related information Updated STORE cycles to QuantumTrap from 200K to 1 million Figure 3: Updated Autostore Mode Page 4: Updated Hardware STORE (HSB) Operation description Page 5: Updated Software STORE Operation description Maximum Ratings: Supply Voltage on V _{CCQ} Relative to GND from -0.5V to 2.5V to -0.5V to 2.45V Added I _{CCQ1} and I _{CCQ3} for V _{CCQ} operation Updated I _{CC4} test condition Updated footnote 8 Updated V _{IH} /V _{IL} as 70%/30% of V _{CCQ} Updated V _{OH} test condition. Updated Input Rise and Fall Times (10% - 90%) from 3ns to 1.8 ns Updated footnote 19, 22 and added footnote 20, 25 Updated V _{IODIS} parameter value from 1.6V to 1.5V Updated Figure 10, 11 and 12
*B	2858300	GVCH	01/19/2010	Changed latch up current from 200 mA to 140 mA. Changed status from Advance to Preliminary. Added Contents.
*C	2951754	GVCH / AESA	06/14/2010	Pin Definitions : Added more clarity on HSB pin operation Hardware STORE Operation : Added more clarity on HSB pin operation Table 1 : Added more clarity on status of BHE/BLE pin operation Updated HSB pin operation in Figure 9 Updated footnote 22
*D	3115647	GVCH	12/20/2010	Change datasheet status from "Preliminary" to "Final" 48 FBGA package: 16 Mb address expansion is not supported Changed I _{SB} and I _{CC4} value from 5 mA to 8 mA Changed I _{CCQ1} value from 25 mA to 15 mA for 25 ns access speed and 15 mA to 10 mA for 45 ns access speed. Added Acronyms and Units of Measure table
*E	3150253	GVCH	01/21/11	Updated input capacitance for BHE and BLE pin
*F	3303659	GVCH	07/06/2011	Updated DC Electrical Characteristics (Added Note 11 and referred the same note in V _{CAP} parameter). Updated AC Switching Characteristics (Added Note 13 and referred the same note in Parameters). Updated Thermal Resistance (Values of Θ_{JA} for 48-ball FBGA package). Updated Package Diagrams .

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