

## High-Speed CMOS Logic Octal D-Type Flip-Flop, Three-State Inverting Positive-Edge Triggered

### Features

- Buffered Inputs
- Common Three-State Output-Enable Control
- Three-State Outputs
- Bus Line Driving Capability
- Typical Propagation Delay = 13ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$  (Clock to Output)
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ C$  to  $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC534, 'HCT534, 'HC564, and 'HCT564 are high speed Octal D-Type Flip-Flops manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL loads. Due to the large output drive capability and the three-state feature, these devices are ideally suited for interfacing with bus lines in a bus organized system. The two types are functionally identical and differ only in their pinout arrangements.

The 'HC534, 'HCT534, 'HC564, and 'HCT564 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are inverted and transferred to the Q outputs on the positive going transition of the CLOCK input. When a high logic level is applied to the OUTPUT ENABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

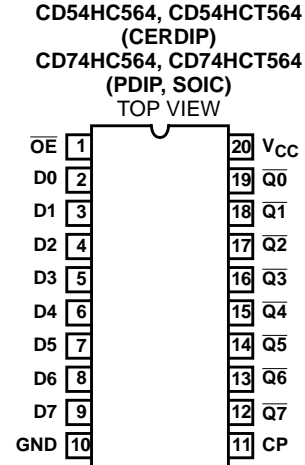
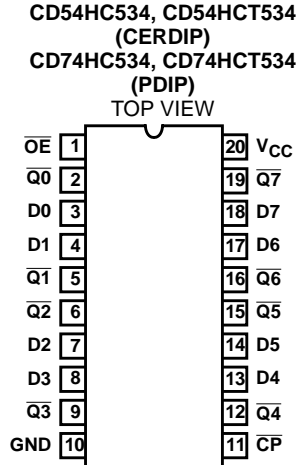
The HCT logic family is speed, function, and pin compatible with the standard LS logic family.

### Ordering Information

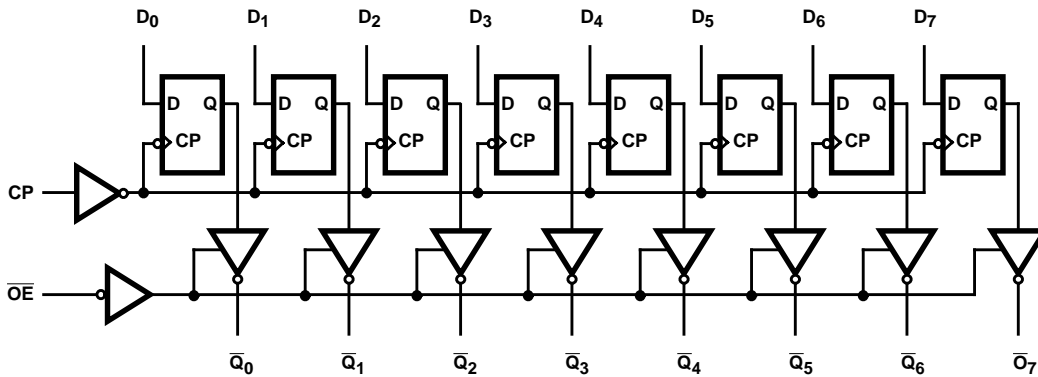
| PART NUMBER   | TEMP. RANGE (°C) | PACKAGE      |
|---------------|------------------|--------------|
| CD54HC534F3A  | -55 to 125       | 20 Ld CERDIP |
| CD54HC564F3A  | -55 to 125       | 20 Ld CERDIP |
| CD54HCT534F3A | -55 to 125       | 20 Ld CERDIP |
| CD54HCT564F3A | -55 to 125       | 20 Ld CERDIP |
| CD74HC534E    | -55 to 125       | 20 Ld PDIP   |
| CD74HC564E    | -55 to 125       | 20 Ld PDIP   |
| CD74HC564M    | -55 to 125       | 20 Ld SOIC   |
| CD74HC564M96  | -55 to 125       | 20 Ld SOIC   |
| CD74HCT534E   | -55 to 125       | 20 Ld PDIP   |
| CD74HCT564E   | -55 to 125       | 20 Ld PDIP   |
| CD74HCT564M   | -55 to 125       | 20 Ld SOIC   |

# CD54/74HC534, CD54/74HCT534, CD54/74HC564, CD54/74HCT564

## Pinouts



## Functional Diagram



TRUTH TABLE

| INPUTS          |    |                | OUTPUT           |
|-----------------|----|----------------|------------------|
| $\overline{OE}$ | CP | D <sub>n</sub> | $\overline{Q_n}$ |
| L               | ↑  | H              | L                |
| L               | ↑  | L              | H                |
| L               | L  | X              | No Change        |
| H               | X  | X              | Z                |

H = High Level (Steady State)  
L = Low Level (Steady State)  
X = Don't Care  
↑ = Transition from Low to High Level  
Z = High Impedance State

# CD54/74HC534, CD54/74HCT534, CD54/74HC564, CD54/74HCT564

## Absolute Maximum Ratings

|  |             |
|--|-------------|
| DC Supply Voltage, $V_{CC}$ .....                      | -0.5V to 7V |
| DC Input Diode Current, $I_{IK}$                       |             |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....       | $\pm 20mA$  |
| DC Output Diode Current, $I_{OK}$                      |             |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....       | $\pm 20mA$  |
| DC Drain Current, per Output, $I_O$                    |             |
| For $-0.5V < V_O < V_{CC} + 0.5V$ .....                | $\pm 35mA$  |
| DC Output Source or Sink Current per Output Pin, $I_O$ |             |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....       | $\pm 25mA$  |
| DC $V_{CC}$ or Ground Current, $I_{CC}$ .....          | $\pm 50mA$  |

## Thermal Information

|  |                                  |
|--|----------------------------------|
| Thermal Resistance (Typical, Note 1)           | $\theta_{JA}$ (°C/W)             |
| E (PDIP) Package .....                         | 69                               |
| M (SOIC) Package .....                         | 58                               |
| Maximum Junction Temperature .....             | 150°C                            |
| Maximum Storage Temperature Range .....        | -65°C to 150°C                   |
| Maximum Lead Temperature (Soldering 10s) ..... | 300°C<br>(SOIC - Lead Tips Only) |

## Operating Conditions

|  |                |
|--|----------------|
| Temperature Range, $T_A$ .....               | -55°C to 125°C |
| Supply Voltage Range, $V_{CC}$               |                |
| HC Types .....                               | .2V to 6V      |
| HCT Types .....                              | 4.5V to 5.5V   |
| DC Input or Output Voltage, $V_I, V_O$ ..... | 0V to $V_{CC}$ |
| Input Rise and Fall Time                     |                |
| 2V .....                                     | 1000ns (Max)   |
| 4.5V .....                                   | 500ns (Max)    |
| 6V .....                                     | 400ns (Max)    |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

- The package impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL   | TEST CONDITIONS      |            | $V_{CC}$<br>(V) | 25°C |      |           | -40°C TO 85°C |         | -55°C TO 125°C |         | UNITS   |   |
|---|----------|----------------------|------------|-----------------|------|------|-----------|---------------|---------|----------------|---------|---------|---|
|   |          | $V_I$ (V)            | $I_O$ (mA) |                 | MIN  | TYP  | MAX       | MIN           | MAX     | MIN            | MAX     |         |   |
| <b>HC TYPES</b>                         |          |                      |            |                 |      |      |           |               |         |                |         |         |   |
| High Level Input Voltage                | $V_{IH}$ | -                    | -          | 2               | 1.5  | -    | -         | 1.5           | -       | 1.5            | -       | V       |   |
|   |          |                      |            | 4.5             | 3.15 | -    | -         | 3.15          | -       | 3.15           | -       | V       |   |
|   |          |                      |            | 6               | 4.2  | -    | -         | 4.2           | -       | 4.2            | -       | V       |   |
| Low Level Input Voltage                 | $V_{IL}$ | -                    | -          | 2               | -    | -    | 0.5       | -             | 0.5     | -              | 0.5     | V       |   |
|   |          |                      |            | 4.5             | -    | -    | 1.35      | -             | 1.35    | -              | 1.35    | V       |   |
|   |          |                      |            | 6               | -    | -    | 1.8       | -             | 1.8     | -              | 1.8     | V       |   |
| High Level Output Voltage<br>CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02      | -0.02           | 2    | 1.9  | -         | -             | 1.9     | -              | 1.9     | -       | V |
|   |          |                      | -0.02      | -0.02           | 4.5  | 4.4  | -         | -             | 4.4     | -              | 4.4     | -       | V |
|   |          |                      | -0.02      | -0.02           | 6    | 5.9  | -         | -             | 5.9     | -              | 5.9     | -       | V |
| High Level Output Voltage<br>TTL Loads  | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -          | -               | -    | -    | -         | -             | -       | -              | -       | V       |   |
|   |          |                      | -6         | -6              | 4.5  | 3.98 | -         | -             | 3.84    | -              | 3.7     | -       | V |
|   |          |                      | -7.8       | -7.8            | 6    | 5.48 | -         | -             | 5.34    | -              | 5.2     | -       | V |
| Low Level Output Voltage<br>CMOS Loads  | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02       | 0.02            | 2    | -    | -         | 0.1           | -       | 0.1            | -       | 0.1     | V |
|   |          |                      | 0.02       | 0.02            | 4.5  | -    | -         | 0.1           | -       | 0.1            | -       | 0.1     | V |
|   |          |                      | 0.02       | 0.02            | 6    | -    | -         | 0.1           | -       | 0.1            | -       | 0.1     | V |
| Low Level Output Voltage<br>TTL Loads   | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | -          | -               | -    | -    | -         | -             | -       | -              | -       | V       |   |
|   |          |                      | 6          | 6               | 4.5  | -    | -         | 0.26          | -       | 0.33           | -       | 0.4     | V |
|   |          |                      | 7.8        | 7.8             | 6    | -    | -         | 0.26          | -       | 0.33           | -       | 0.4     | V |
| Input Leakage Current                   | $I_I$    | $V_{CC}$ or GND      | -          | 6               | -    | -    | $\pm 0.1$ | -             | $\pm 1$ | -              | $\pm 1$ | $\mu A$ |   |

**CD54/74HC534, CD54/74HCT534, CD54/74HC564, CD54/74HCT564**

**DC Electrical Specifications (Continued)**

| PARAMETER  | SYMBOL                             | TEST CONDITIONS                         |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |     | UNITS |
|--|------------------------------------|---|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
|  |                                    | V <sub>I</sub> (V)                      | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX |       |
| Quiescent Device Current                                       | I <sub>CC</sub>                    | V <sub>CC</sub> or GND                  | 0                   | 6                   | -    | -   | 8    | -             | 80   | -              | 160 | μA    |
| Three- State Leakage Current                                   | V <sub>IL</sub> or V <sub>IH</sub> | V <sub>O</sub> = V <sub>CC</sub> or GND | -                   | 6                   | -    | -   | ±0.5 | -             | ±5.0 | -              | ±10 | μA    |
| <b>HCT TYPES</b>   |                                    |   |                     |                     |      |     |      |               |      |                |     |       |
| High Level Input Voltage                                       | V <sub>IH</sub>                    | -                                       | -                   | 4.5 to 5.5          | 2    | -   | -    | 2             | -    | 2              | -   | V     |
| Low Level Input Voltage  | V <sub>IL</sub>                    | -                                       | -                   | 4.5 to 5.5          | -    | -   | 0.8  | -             | 0.8  | -              | 0.8 | V     |
| High Level Output Voltage<br>CMOS Loads                        | V <sub>OH</sub>                    | V <sub>IH</sub> or V <sub>IL</sub>      | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -   | V     |
| High Level Output Voltage<br>TTL Loads                         |                                    |   | -6                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -   | V     |
| Low Level Output Voltage<br>CMOS Loads                         | V <sub>OL</sub>                    | V <sub>IH</sub> or V <sub>IL</sub>      | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1 | V     |
| Low Level Output Voltage<br>TTL Loads                          |                                    |   | 6                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4 | V     |
| Input Leakage Current  | I <sub>I</sub>                     | V <sub>CC</sub> and GND                 | 0                   | 5.5                 | -    | -   | ±0.1 | -             | ±1   | -              | ±1  | μA    |
| Quiescent Device Current                                       | I <sub>CC</sub>                    | V <sub>CC</sub> or GND                  | 0                   | 5.5                 | -    | -   | 8    | -             | 80   | -              | 160 | μA    |
| Three- State Leakage Current                                   | V <sub>IL</sub> or V <sub>IH</sub> | V <sub>O</sub> = V <sub>CC</sub> or GND | -                   | 5.5                 | -    | -   | ±0.5 | -             | ±5.0 | -              | ±10 | μA    |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI <sub>CC</sub> (Note 2)          | V <sub>CC</sub> -2.1                    | -                   | 4.5 to 5.5          | -    | 100 | 360  | -             | 450  | -              | 490 | μA    |

NOTE:

- For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

| INPUT   | UNIT LOADS |
|---------|------------|
| D0 - D7 | 0.15       |
| CP      | 0.30       |
| OE      | 0.55       |

NOTE: Unit Load is ΔI<sub>CC</sub> limit specific in DC Electrical Specifications Table, e.g., 360μA max. at 25°C.

**CD54/74HC534, CD54/74HCT534, CD54/74HC564, CD54/74HCT564**

**Prerequisite for Switching Specifications**

| PARAMETER                     | SYMBOL           | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     |     | -55°C TO 125°C |     |     | UNITS |
|-------------------------------|------------------|---------------------|------|-----|-----|---------------|-----|-----|----------------|-----|-----|-------|
|                               |                  |                     | MIN  | TYP | MAX | MIN           | TYP | MAX | MIN            | TYP | MAX |       |
| <b>HC TYPES</b>               |                  |                     |      |     |     |               |     |     |                |     |     |       |
| Maximum Clock Frequency       | f <sub>MAX</sub> | 2                   | 6    | -   | -   | 5             | -   | -   | 4              | -   | -   | MHz   |
|                               |                  | 4.5                 | 30   | -   | -   | 25            | -   | -   | 20             | -   | -   | MHz   |
|                               |                  | 6                   | 35   | -   | -   | 29            | -   | -   | 23             | -   | -   | MHz   |
| Clock Pulse Width             | t <sub>W</sub>   | 2                   | 80   | -   | -   | 100           | -   | -   | 120            | -   | -   | ns    |
|                               |                  | 4.5                 | 16   | -   | -   | 20            | -   | -   | 24             | -   | -   | ns    |
|                               |                  | 6                   | 14   | -   | -   | 17            | -   | -   | 20             | -   | -   | ns    |
| Setup Time Data to Clock      | t <sub>SU</sub>  | 2                   | 60   | -   | -   | 75            | -   | -   | 90             | -   | -   | ns    |
|                               |                  | 4.5                 | 12   | -   | -   | 15            | -   | -   | 18             | -   | -   | ns    |
|                               |                  | 6                   | 10   | -   | -   | 13            | -   | -   | 15             | -   | -   | ns    |
| Hold Time Data to Clock       | t <sub>H</sub>   | 2                   | 5    | -   | -   | 5             | -   | -   | 5              | -   | -   | ns    |
|                               |                  | 4.5                 | 5    | -   | -   | 5             | -   | -   | 5              | -   | -   | ns    |
|                               |                  | 6                   | 5    | -   | -   | 5             | -   | -   | 5              | -   | -   | ns    |
| <b>HCT TYPES</b>              |                  |                     |      |     |     |               |     |     |                |     |     |       |
| Maximum Clock Frequency       | f <sub>MAX</sub> | 4.5                 | 25   | -   | -   | 20            | -   | -   | 16             | -   | -   | MHz   |
| Clock Pulse Width             | t <sub>W</sub>   | 4.5                 | 20   | -   | -   | 25            | -   | -   | 30             | -   | -   | ns    |
| Setup Time Data to Clock      | t <sub>SU</sub>  | 4.5                 | 20   | -   | -   | 25            | -   | -   | 30             | -   | -   | ns    |
| Hold Time Data to Clock (534) | t <sub>H</sub>   | 4.5                 | 5    | -   | -   | 5             | -   | -   | 5              | -   | -   | ns    |
| Hold Time Data to Clock (564) | t <sub>H</sub>   | 4.5                 | 3    | -   | -   | 3             | -   | -   | 3              | -   | -   | ns    |

**Switching Specifications** C<sub>L</sub> = 50pF, Input t<sub>r</sub>, t<sub>f</sub> = 6ns

| PARAMETER                         | SYMBOL                              | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-----------------------------------|-------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                   |                                     |                       |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| <b>HC TYPES</b>                   |                                     |                       |                     |      |     |     |               |     |                |     |       |
| Propagation Delay Clock to Output | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 165 | -             | 205 | -              | 250 | ns    |
|                                   |                                     |                       | 4.5                 | -    | -   | 33  | -             | 41  | -              | 50  | ns    |
|                                   |                                     | C <sub>L</sub> = 15pF | 5                   | -    | 13  | -   | -             | -   | -              | -   | ns    |
|                                   |                                     | C <sub>L</sub> = 50pF | 6                   | -    | -   | 28  | -             | 35  | -              | 43  | ns    |
| Output Disable to Q (534)         | t <sub>PLZ</sub> , t <sub>PHZ</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 150 | -             | 190 | -              | 225 | ns    |
|                                   |                                     |                       | 4.5                 | -    | -   | 30  | -             | 38  | -              | 45  | ns    |
|                                   |                                     | C <sub>L</sub> = 15pF | 5                   | -    | 12  | -   | -             | -   | -              | -   | ns    |
|                                   |                                     | C <sub>L</sub> = 50pF | 6                   | -    | -   | 26  | -             | 33  | -              | 38  | ns    |

**CD54/74HC53A, CD54/74HCT53A, CD54/74HC56A, CD54/74HCT56A**

**Switching Specifications**  $C_L = 50\text{pF}$ , Input  $t_r, t_f = 6\text{ns}$  (Continued)

| PARAMETER                                  | SYMBOL             | TEST CONDITIONS     | $V_{CC}$ (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|--|--------------------|---------------------|--------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|  |                    |                     |              | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| Output Disable to Q (564)                  | $t_{PLZ}, t_{PHZ}$ | $C_L = 50\text{pF}$ | 2            | -    | -   | 135 | -             | 170 | -              | 205 | ns    |
|  |                    |                     | 4.5          | -    | -   | 27  | -             | 34  | -              | 41  | ns    |
|  |                    | $C_L = 15\text{pF}$ | 5            | -    | 12  | -   | -             | -   | -              | -   | ns    |
|  |                    | $C_L = 50\text{pF}$ | 6            | -    | -   | 23  | -             | 29  | -              | 35  | ns    |
| Output Enable to Q                         | $t_{PZL}, t_{PZH}$ | $C_L = 50\text{pF}$ | 2            | -    | -   | 150 | -             | 190 | -              | 225 | ns    |
|  |                    |                     | 4.5          | -    | -   | 30  | -             | 38  | -              | 45  | ns    |
|  |                    | $C_L = 15\text{pF}$ | 5            | -    | 12  | -   | -             | -   | -              | -   | ns    |
|  |                    | $C_L = 50\text{pF}$ | 6            | -    | -   | 26  | -             | 33  | -              | 38  | ns    |
| Maximum Clock Frequency                    | $f_{MAX}$          | $C_L = 15\text{pF}$ | 5            | -    | 60  | -   | -             | -   | -              | MHz |       |
| Output Transition Time                     | $t_{THL}, t_{TLH}$ | $C_L = 50\text{pF}$ | 2            | -    | -   | 60  | -             | 75  | -              | 90  | ns    |
|  |                    |                     | 4.5          | -    | -   | 12  | -             | 15  | -              | 18  | ns    |
|  |                    |                     | 6            | -    | -   | 10  | -             | 13  | -              | 15  | ns    |
| Input Capacitance                          | $C_I$              | $C_L = 50\text{pF}$ | -            | 10   | -   | 10  | -             | 10  | -              | 10  | pF    |
| Three-State Output Capacitance             | $C_O$              | -                   | -            | 20   | -   | 20  | -             | 20  | -              | 20  | pF    |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$           | -                   | 5            | -    | 32  | -   | -             | -   | -              | -   | pF    |

**HCT TYPES**

|  |                    |                     |                     |    |    |    |   |    |   |    |     |
|--|--------------------|---------------------|---------------------|----|----|----|---|----|---|----|-----|
| Propagation Delay<br>Clock to Output       | $t_{PHL}, t_{PLH}$ | $C_L = 50\text{pF}$ | 4.5                 | -  | -  | 35 | - | 44 | - | 53 | ns  |
|  |                    |                     | $C_L = 15\text{pF}$ | 5  | -  | 14 | - | -  | - | -  | -   |
| Output Disable to Q                        | $t_{PLZ}, t_{PHZ}$ | $C_L = 50\text{pF}$ | 4.5                 | -  | -  | 30 | - | 38 | - | 45 | ns  |
|  |                    |                     | $C_L = 15\text{pF}$ | 5  | -  | 12 | - | -  | - | -  | -   |
| Output Enable to Q                         | $t_{PZL}, t_{PZH}$ | $C_L = 50\text{pF}$ | 4.5                 | -  | -  | 35 | - | 44 | - | 53 | ns  |
|  |                    |                     | $C_L = 15\text{pF}$ | 5  | -  | 14 | - | -  | - | -  | -   |
| Maximum Clock Frequency                    | $f_{MAX}$          | $C_L = 15\text{pF}$ | 5                   | -  | 50 | -  | - | -  | - | -  | MHz |
| Output Transition Time                     | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 4.5                 | -  | -  | 12 | - | 15 | - | 18 | ns  |
| Input Capacitance                          | $C_I$              | $C_L = 50\text{pF}$ | -                   | 10 | -  | 10 | - | 10 | - | 10 | pF  |
| Three-State Output Capacitance             | $C_O$              | -                   | -                   | 20 | -  | 20 | - | 20 | - | 20 | pF  |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$           | -                   | 5                   | -  | 36 | -  | - | -  | - | -  | pF  |

NOTES:

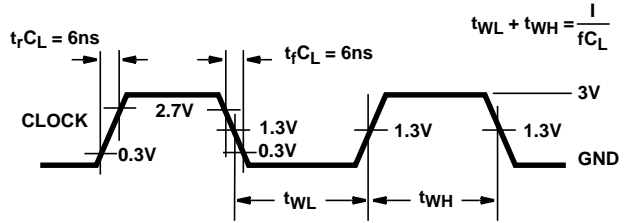
- $C_{PD}$  is used to determine the dynamic power consumption, per package.
- $P_D = C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_O$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V<sub>CC</sub> to 90% V<sub>CC</sub> in accordance with device truth table. For f<sub>MAX</sub>, input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V<sub>CC</sub> to 90% V<sub>CC</sub> in accordance with device truth table. For f<sub>MAX</sub>, input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

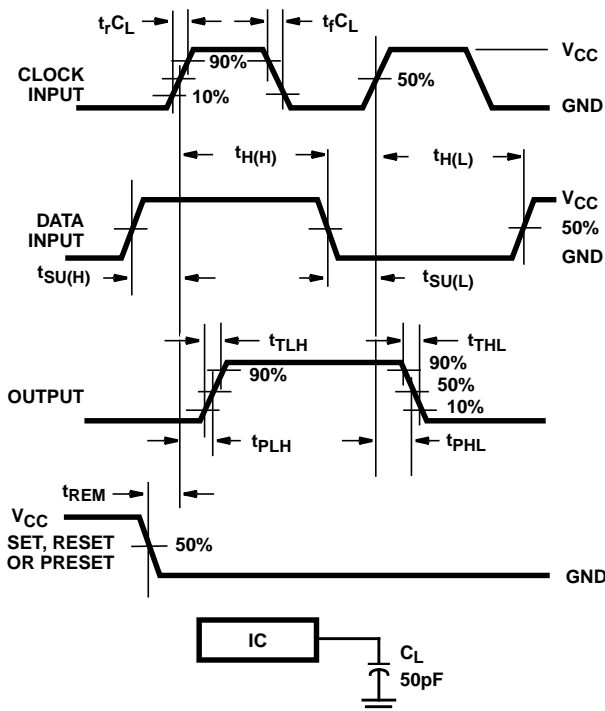


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

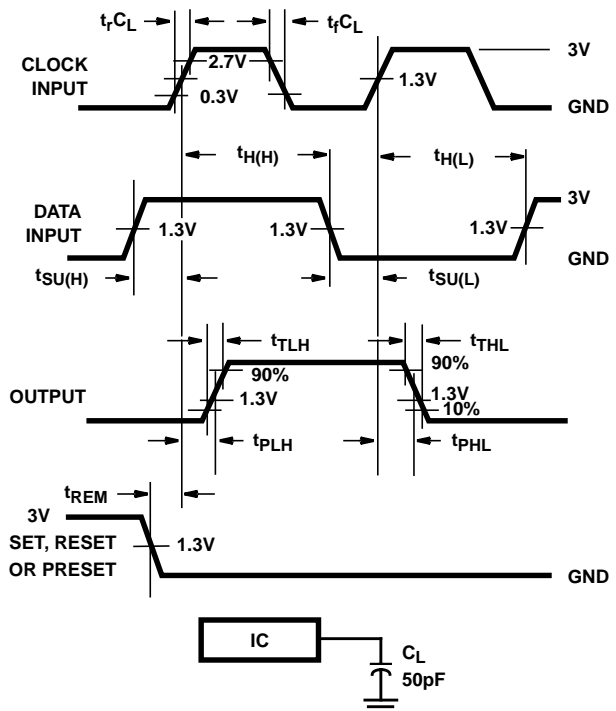


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

**Test Circuits and Waveforms** (Continued)

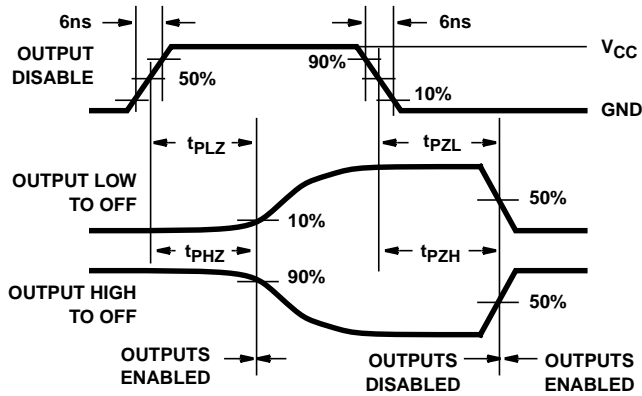


FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

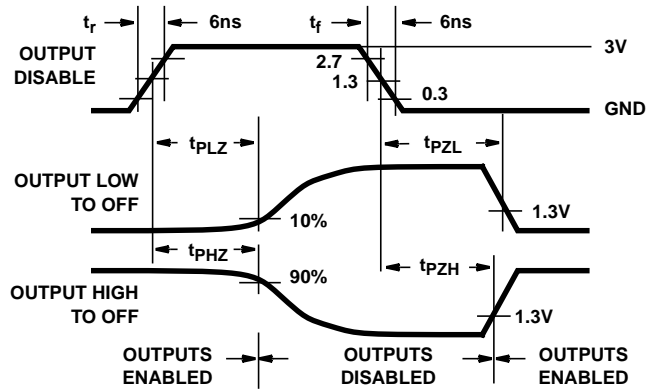


FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT



**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| 5962-8681401RA   | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                        | Call TI              | Call TI                      |                             |
| 5962-8681501RA   | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                        | Call TI              | Call TI                      |                             |
| 5962-8984901RA   | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                        | Call TI              | Call TI                      |                             |
| CD54HC534F3A     | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| CD54HC564F3A     | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| CD54HCT534F3A    | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| CD54HCT564F3A    | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| CD74HC534E       | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD74HC534EE4     | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD74HC564E       | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD74HC564EE4     | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD74HC564M       | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC564M96     | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC564M96E4   | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC564M96G4   | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC564ME4     | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC564MG4     | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HCT534E      | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD74HCT534EE4    | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD74HCT564E      | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD74HCT564EE4    | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD74HCT564M      | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HCT564ME4    | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| CD74HCT564MG4    | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF CD54HC534, CD54HC564, CD54HCT534, CD54HCT564, CD74HC534, CD74HC564, CD74HCT534, CD74HCT564 :**

● Catalog: [CD74HC534](#), [CD74HC564](#), [CD74HCT534](#), [CD74HCT564](#)

● Military: [CD54HC534](#), [CD54HC564](#), [CD54HCT534](#), [CD54HCT564](#)

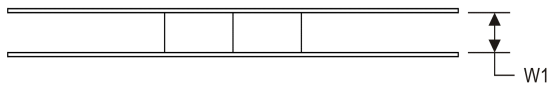
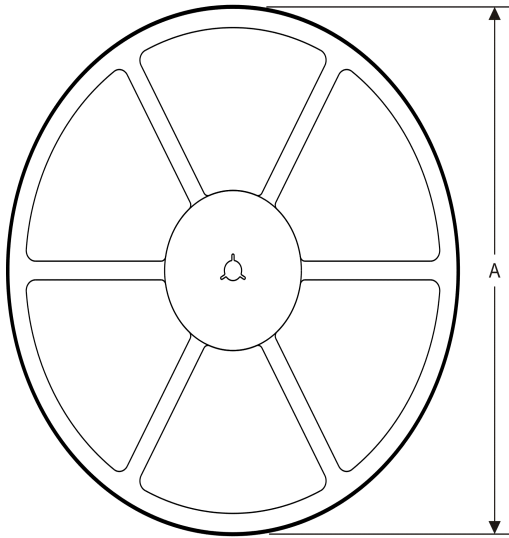
NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

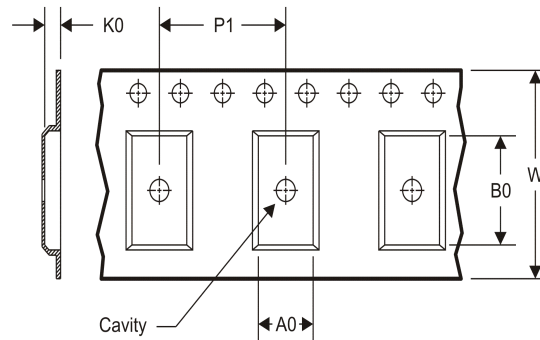
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC564M96 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.0    | 2.7     | 12.0    | 24.0   | Q1            |

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC564M96 | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

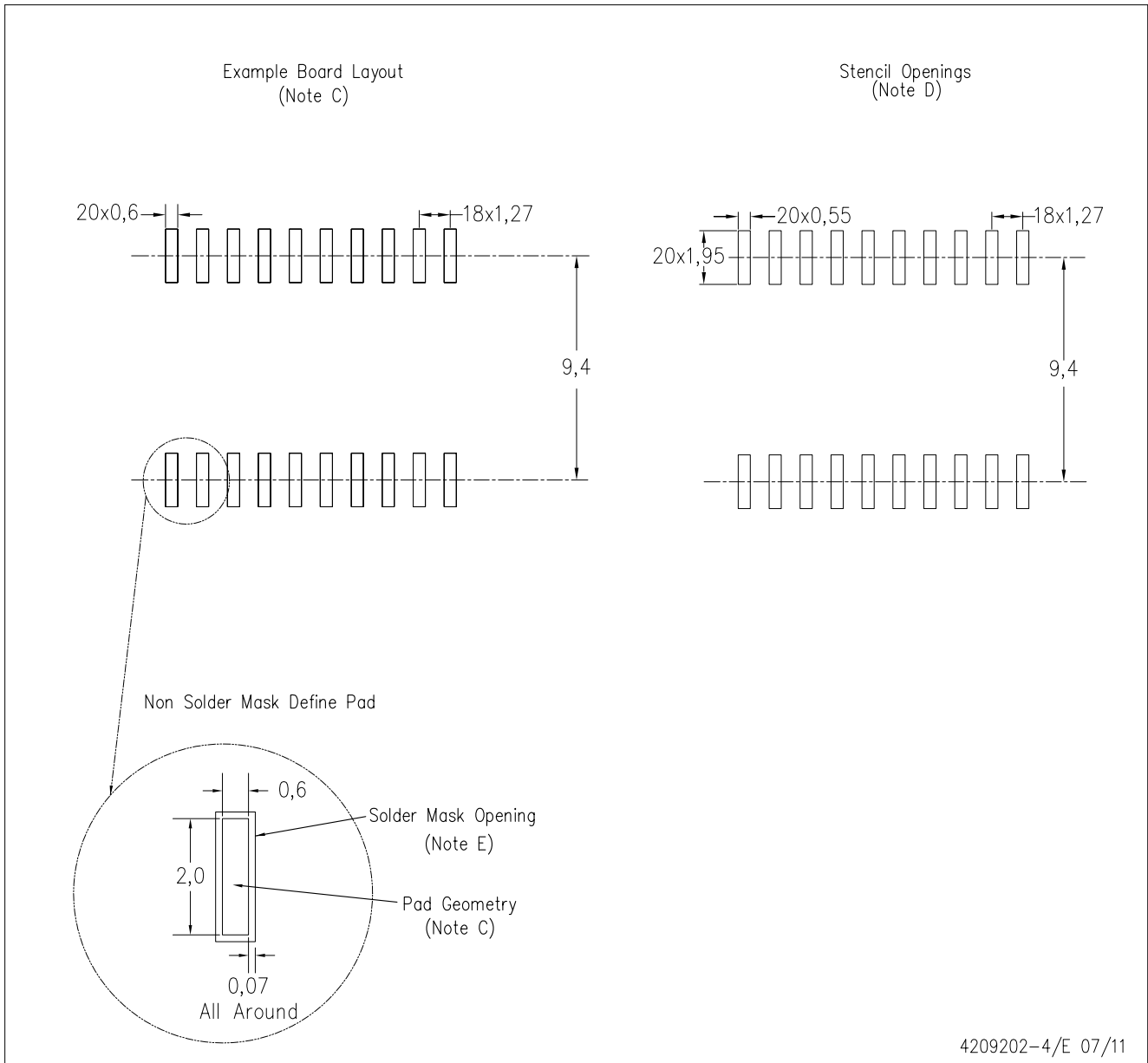


- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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