

SN54HC574, SN74HC574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS148F – DECEMBER 1982 – REVISED AUGUST 2003

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Noninverting Outputs Drive Bus Lines Directly or Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 22$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Bus-Structured Pinout

description/ordering information

These octal edge-triggered D-type flip-flops feature 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

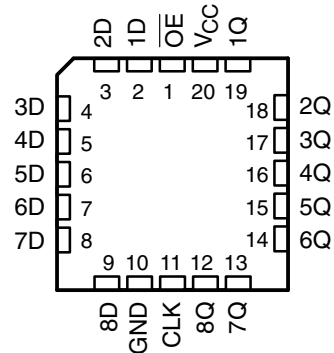
The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

SN54HC574 . . . J OR W PACKAGE
SN74HC574 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC574 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|--------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube of 20 | SN74HC574N | SN74HC574N |
| | SOIC – DW | Tube of 25 | SN74HC574DW | HC574 |
| | | Reel of 2000 | SN74HC574DWR | |
| | SSOP – DB | Reel of 2000 | SN74HC574DBR | HC574 |
| | SOP – NS | Reel of 2000 | SN74HC574NSR | HC574 |
| | TSSOP – PW | Tube of 70 | SN74HC574PW | HC574 |
| Reel of 2000 | | SN74HC574PWR | | |
| Reel of 250 | | SN74HC574PWT | | |
| -55°C to 125°C | CDIP – J | Tube of 20 | SNJ54HC574J | SNJ54HC574J |
| | CFP – W | Tube of 85 | SNJ54HC574W | SNJ54HC574W |
| | LCCC – FK | Tube of 55 | SNJ54HC574FK | SNJ54HC574FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT |
|-----------------|--------|---|--------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q_0 |
| H | X | X | Z |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±35 mA |
| Continuous current through V_{CC} or GND | ±70 mA |
| Package thermal impedance, θ_{JA} (see Note 2): | |
| DB package | 70°C/W |
| DW package | 58°C/W |
| N package | 69°C/W |
| NS package | 60°C/W |
| PW package | 83°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

| | | SN54HC574 | | | SN74HC574 | | | UNIT | |
|---------------------|---------------------------------|-------------------------|-----|----------|-------------------------|-------------------------|----------|------|----|
| | | MIN | NOM | MAX | MIN | NOM | MAX | | |
| V_{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V | |
| V_{IH} | High-level input voltage | $V_{CC} = 2\text{ V}$ | | 1.5 | $V_{CC} = 2\text{ V}$ | | 1.5 | V | |
| | | $V_{CC} = 4.5\text{ V}$ | | 3.15 | $V_{CC} = 4.5\text{ V}$ | | 3.15 | | |
| | | $V_{CC} = 6\text{ V}$ | | 4.2 | $V_{CC} = 6\text{ V}$ | | 4.2 | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2\text{ V}$ | | | 0.5 | $V_{CC} = 2\text{ V}$ | | 0.5 | V |
| | | $V_{CC} = 4.5\text{ V}$ | | | 1.35 | $V_{CC} = 4.5\text{ V}$ | | 1.35 | |
| | | $V_{CC} = 6\text{ V}$ | | | 1.8 | $V_{CC} = 6\text{ V}$ | | 1.8 | |
| V_I | Input voltage | 0 | | V_{CC} | 0 | | V_{CC} | V | |
| V_O | Output voltage | 0 | | V_{CC} | 0 | | V_{CC} | V | |
| $\Delta t/\Delta v$ | Input transition rise/fall time | $V_{CC} = 2\text{ V}$ | | | 1000 | $V_{CC} = 2\text{ V}$ | | 1000 | ns |
| | | $V_{CC} = 4.5\text{ V}$ | | | 500 | $V_{CC} = 4.5\text{ V}$ | | 500 | |
| | | $V_{CC} = 6\text{ V}$ | | | 400 | $V_{CC} = 6\text{ V}$ | | 400 | |
| T_A | Operating free-air temperature | -55 | | 125 | -40 | | 85 | °C | |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC574 | | SN74HC574 | | UNIT |
|-----------|--------------------------------|-----------------------------|------------|--------------------------|------------|-----------|-----------|------------|-----------|------------|---------------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V_{OH} | $V_I = V_{IH}$ or V_{IL} | $I_{OH} = -20\ \mu\text{A}$ | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V | |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | $I_{OH} = -6\text{ mA}$ | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | $I_{OH} = -7.8\text{ mA}$ | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| V_{OL} | $V_I = V_{IH}$ or V_{IL} | $I_{OL} = 20\ \mu\text{A}$ | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL} = 6\text{ mA}$ | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | $I_{OL} = 7.8\text{ mA}$ | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| I_I | $V_I = V_{CC}$ or 0 | | 6 V | | ± 0.1 | ± 100 | | ± 1000 | | ± 1000 | nA |
| I_{OZ} | $V_O = V_{CC}$ or 0 | | 6 V | | ± 0.01 | ± 0.5 | | ± 10 | | ± 5 | μA |
| I_{CC} | $V_I = V_{CC}$ or 0, $I_O = 0$ | | 6 V | | | 8 | | 160 | | 80 | μA |
| C_i | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |



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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | V_{CC} | $T_A = 25^\circ\text{C}$ | | SN54HC574 | | SN74HC574 | | UNIT |
|--|----------|--------------------------|-----|-----------|-----|-----------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{clock} Clock frequency | 2 V | | 6 | | 4 | | 5 | MHz |
| | 4.5 V | | 30 | | 20 | | 24 | |
| | 6 V | | 38 | | 24 | | 28 | |
| t_w Pulse duration, CLK high or low | 2 V | 80 | | 120 | | 100 | | ns |
| | 4.5 V | 16 | | 24 | | 20 | | |
| | 6 V | 14 | | 20 | | 17 | | |
| t_{su} Setup time, data before CLK \uparrow | 2 V | 100 | | 150 | | 125 | | ns |
| | 4.5 V | 20 | | 30 | | 25 | | |
| | 6 V | 17 | | 26 | | 21 | | |
| t_h Hold time, data after CLK \uparrow | 2 V | 5 | | 5 | | 5 | | ns |
| | 4.5 V | 5 | | 5 | | 5 | | |
| | 6 V | 5 | | 5 | | 5 | | |

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC574 | | SN74HC574 | | UNIT |
|------------------|------------------------|-------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 2 V | 6 | 11 | | 4 | | 5 | MHz | |
| | | | 4.5 V | 30 | 36 | | 20 | | 24 | | |
| | | | 6 V | 36 | 40 | | 24 | | 28 | | |
| t_{pd} | CLK | Any Q | 2 V | | 90 | 180 | | 270 | | 225 | ns |
| | | | 4.5 V | | 28 | 36 | | 54 | | 45 | |
| | | | 6 V | | 24 | 31 | | 46 | | 38 | |
| t_{en} | $\overline{\text{OE}}$ | Any Q | 2 V | | 77 | 150 | | 225 | | 190 | ns |
| | | | 4.5 V | | 26 | 30 | | 45 | | 38 | |
| | | | 6 V | | 23 | 26 | | 38 | | 32 | |
| t_{dis} | $\overline{\text{OE}}$ | Any Q | 2 V | | 52 | 150 | | 225 | | 190 | ns |
| | | | 4.5 V | | 24 | 30 | | 45 | | 38 | |
| | | | 6 V | | 22 | 26 | | 38 | | 32 | |
| t_t | | Any Q | 2 V | | 28 | 60 | | 90 | | 75 | ns |
| | | | 4.5 V | | 8 | 12 | | 18 | | 15 | |
| | | | 6 V | | 6 | 10 | | 15 | | 13 | |



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switching characteristics over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC574 | | SN74HC574 | | UNIT |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 2 V | 6 | | | | | 5 | | MHz |
| | | | 4.5 V | 30 | | | | | 24 | | |
| | | | 6 V | 36 | | | | | 28 | | |
| t_{pd} | CLK | Any Q | 2 V | 105 | 265 | 400 | | 330 | | ns | |
| | | | 4.5 V | 36 | 53 | 80 | | 66 | | | |
| | | | 6 V | 31 | 46 | 68 | | 57 | | | |
| t_{en} | \overline{OE} | Any Q | 2 V | 95 | 235 | 355 | | 295 | | ns | |
| | | | 4.5 V | 32 | 47 | 71 | | 59 | | | |
| | | | 6 V | 28 | 41 | 60 | | 51 | | | |
| t_t | | Any Q | 2 V | 60 | 210 | 315 | | 265 | | ns | |
| | | | 4.5 V | 17 | 42 | 63 | | 53 | | | |
| | | | 6 V | 14 | 36 | 53 | | 45 | | | |

operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C_{pd} Power dissipation capacitance per flip-flop | No load | 100 | pF |

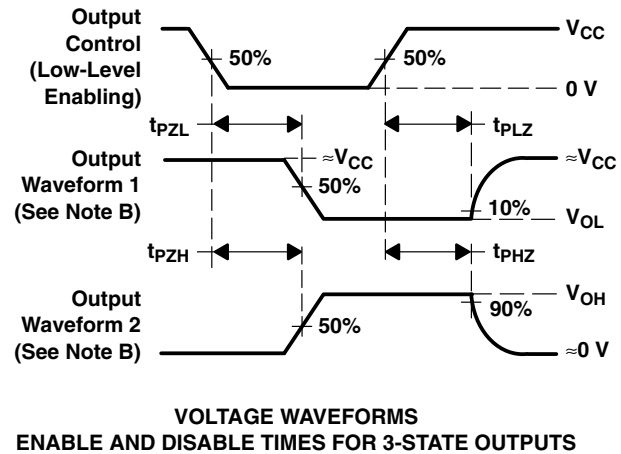
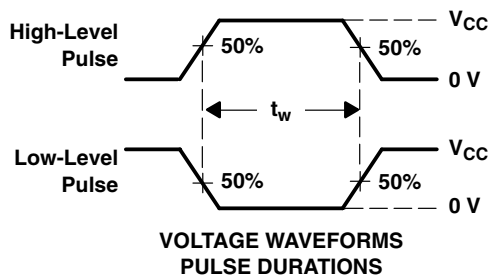
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PARAMETER MEASUREMENT INFORMATION



| PARAMETER | R_L | C_L | S1 | S2 |
|-------------------|--------------|-----------------------|--------|--------|
| t_{en} | 1 k Ω | 50 pF or 150 pF | Open | Closed |
| | | | Closed | Open |
| t_{dis} | 1 k Ω | 50 pF | Open | Closed |
| | | | Closed | Open |
| t_{pd} or t_t | -- | 50 pF or 150 pF | Open | Open |



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 E. The outputs are measured one at a time with one input transition per measurement.
 F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 G. t_{PZL} and t_{PZH} are the same as t_{en} .
 H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| JM38510/65604BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 65604BRA | Samples |
| M38510/65604BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 65604BRA | Samples |
| SN54HC574J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54HC574J | Samples |
| SN74HC574DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574DBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574DBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574DWRE4 | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74HC574DWRG4 | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | -40 to 85 | HC574 | |
| SN74HC574N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC574N | Samples |
| SN74HC574N3 | OBSOLETE | PDIP | N | 20 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74HC574NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC574N | Samples |
| SN74HC574NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574PW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74HC574PWE4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574PWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574PWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574PWRG3 | PREVIEW | TSSOP | PW | 20 | 2000 | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74HC574PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574PWT | ACTIVE | TSSOP | PW | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574PWTE4 | ACTIVE | TSSOP | PW | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SN74HC574PWTG4 | ACTIVE | TSSOP | PW | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC574 | Samples |
| SNJ54HC574FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54HC574FK | Samples |
| SNJ54HC574J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54HC574J | Samples |
| SNJ54HC574W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SNJ54HC574W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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OTHER QUALIFIED VERSIONS OF SN54HC574, SN74HC574 :

- Catalog: [SN74HC574](#)
- Military: [SN54HC574](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC574DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC574DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74HC574NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74HC574PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74HC574PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74HC574PWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74HC574PWT | TSSOP | PW | 20 | 250 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC574DBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74HC574DWR | SOIC | DW | 20 | 2000 | 366.0 | 364.0 | 50.0 |
| SN74HC574NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74HC574PWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74HC574PWR | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74HC574PWRG4 | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74HC574PWT | TSSOP | PW | 20 | 250 | 367.0 | 367.0 | 38.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW (R-PDSO-G20)

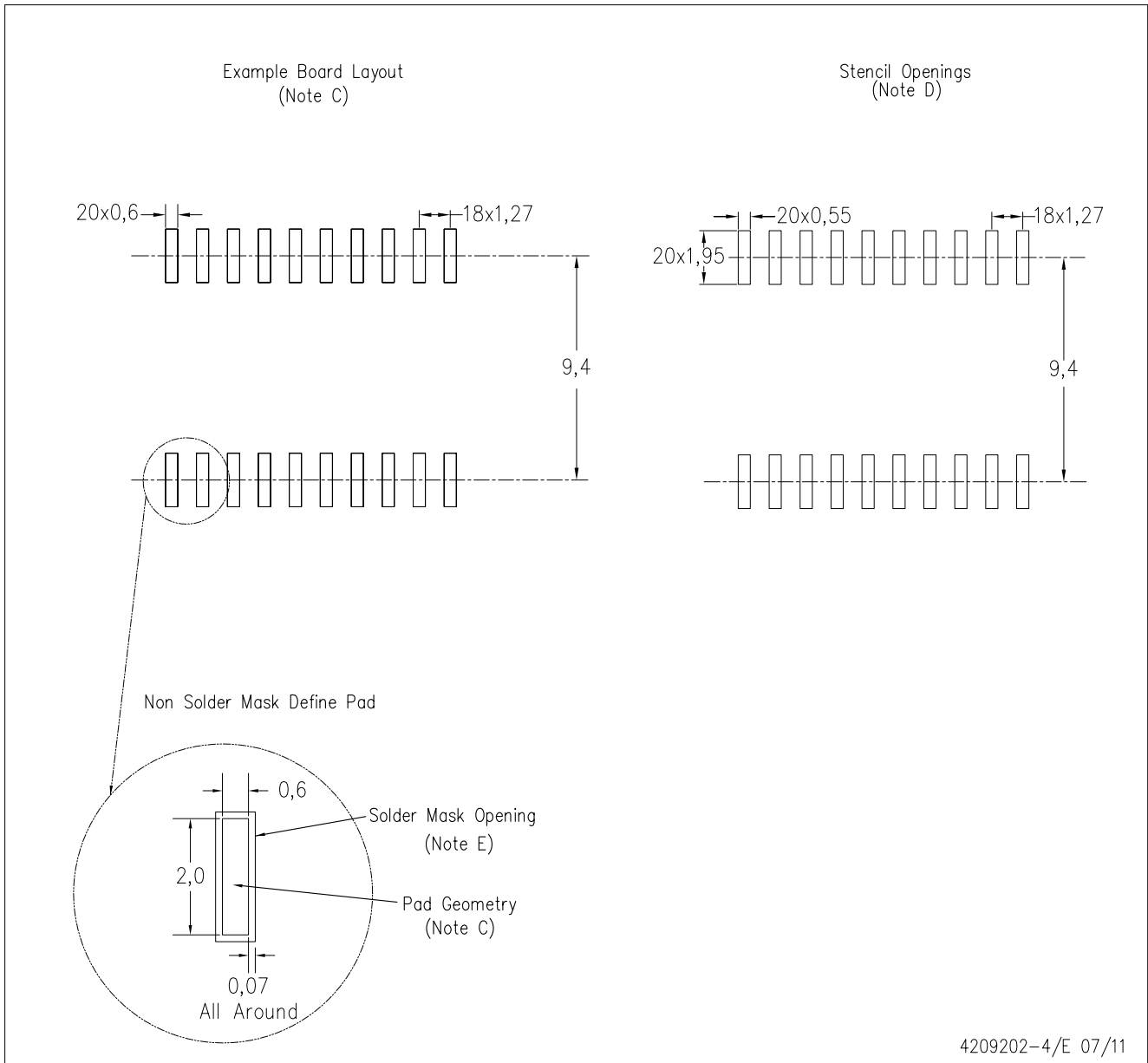
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4209202-4/E 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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