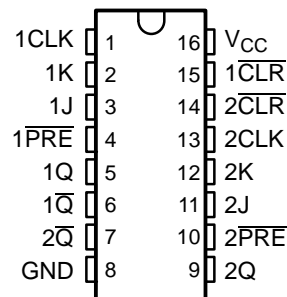


## FEATURES

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.8 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

D, DB, DGV, NS, OR PW PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

This dual negative-edge-triggered J-K flip-flop is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the J and K inputs meeting the setup-time requirements is transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and K inputs can be changed without affecting the levels at the outputs. The SN74LVC112A can perform as a toggle flip-flop by tying J and K high.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

## ORDERING INFORMATION

| $T_A$         | PACKAGE <sup>(1)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|--------------|-----------------------|------------------|
| –40°C to 85°C | SOIC – D               | Tube of 40   | SN74LVC112AD          | LVC112A          |
|               |                        | Reel of 2500 | SN74LVC112ADR         |                  |
|               |                        | Reel of 250  | SN74LVC112ADT         |                  |
|               | SOP – NS               | Reel of 2000 | SN74LVC112ANSR        | LVC112A          |
|               | SSOP – DB              | Reel of 2000 | SN74LVC112ADBR        | LC112A           |
|               | TSSOP – PW             | Tube of 90   | SN74LVC112APW         | LC112A           |
|               |                        | Reel of 2000 | SN74LVC112APWR        |                  |
|               |                        | Reel of 250  | SN74LVC112APWT        |                  |
|               | TVSOP – DGV            | Reel of 2000 | SN74LVC112ADGVR       | LC112A           |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**SN74LVC112A**  
**DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP**  
**WITH CLEAR AND PRESET**

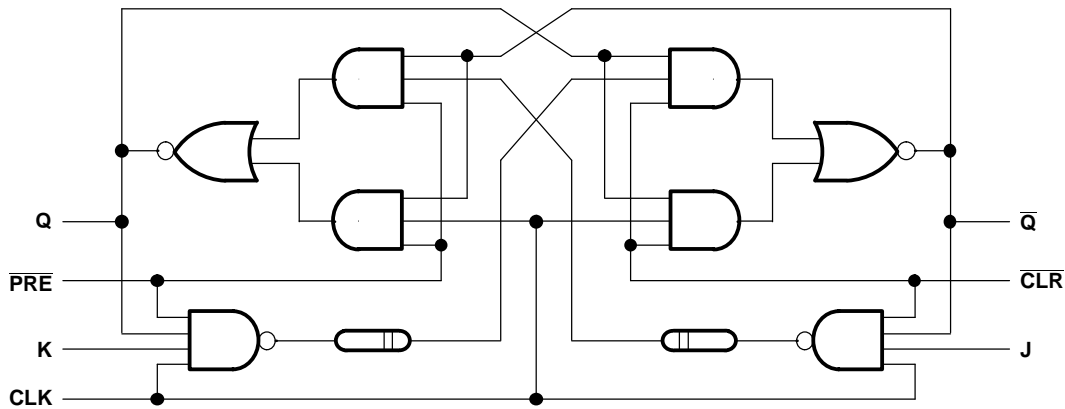
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**FUNCTION TABLE**

| INPUTS |     |     |   |   | OUTPUTS          |                  |
|--------|-----|-----|---|---|------------------|------------------|
| PRE    | CLR | CLK | J | K | Q                | $\bar{Q}$        |
| L      | H   | X   | X | X | H                | L                |
| H      | L   | X   | X | X | L                | H                |
| L      | L   | X   | X | X | H <sup>(1)</sup> | H <sup>(1)</sup> |
| H      | H   | ↓   | L | L | Q <sub>0</sub>   | $\bar{Q}_0$      |
| H      | H   | ↓   | H | L | H                | L                |
| H      | H   | ↓   | L | H | L                | H                |
| H      | H   | ↓   | H | H | Toggle           |                  |
| H      | H   | H   | X | X | Q <sub>0</sub>   | $\bar{Q}_0$      |

- (1) The output levels in this configuration may not meet the minimum levels for V<sub>OH</sub>. Furthermore, this configuration is nonstable; that is, it does not persist when either  $\overline{PRE}$  or  $\overline{CLR}$  returns to its inactive (high) level.

**LOGIC DIAGRAM, EACH FLIP-FLOP (POSITIVE LOGIC)**



**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

|                  |   | MIN                | MAX                   | UNIT |
|------------------|---|--------------------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage range                              | -0.5               | 6.5                   | V    |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>                | -0.5               | 6.5                   | V    |
| V <sub>O</sub>   | Output voltage range <sup>(2)(3)</sup>            | -0.5               | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Input clamp current                               | V <sub>I</sub> < 0 | -50                   | mA   |
| I <sub>OK</sub>  | Output clamp current                              | V <sub>O</sub> < 0 | -50                   | mA   |
| I <sub>O</sub>   | Continuous output current                         |                    | ±50                   | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND |                    | ±100                  | mA   |
| θ <sub>JA</sub>  | Package thermal impedance <sup>(4)</sup>          | D package          | 73                    | °C/W |
|                  |   | DB package         | 82                    |      |
|                  |   | DGV package        | 120                   |      |
|                  |   | NS package         | 64                    |      |
|                  |   | PW package         | 108                   |      |
| T <sub>stg</sub> | Storage temperature range                         | -65                | 150                   | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

|                 |                                    | MIN                                | MAX                    | UNIT                   |    |
|-----------------|------------------------------------|------------------------------------|------------------------|------------------------|----|
| V <sub>CC</sub> | Supply voltage                     | Operating                          | 1.65                   | 3.6                    | V  |
|                 |                                    | Data retention only                | 1.5                    |                        |    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.65 × V <sub>CC</sub> |                        | V  |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.7                    |                        |    |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V   | 2                      |                        |    |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 1.65 V to 1.95 V |                        | 0.35 × V <sub>CC</sub> | V  |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V   |                        | 0.7                    |    |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V   |                        | 0.8                    |    |
| V <sub>I</sub>  | Input voltage                      | 0                                  | 5.5                    | V                      |    |
| V <sub>O</sub>  | Output voltage                     | 0                                  | V <sub>CC</sub>        | V                      |    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 1.65 V           |                        | -4                     | mA |
|                 |                                    | V <sub>CC</sub> = 2.3 V            |                        | -8                     |    |
|                 |                                    | V <sub>CC</sub> = 2.7 V            |                        | -12                    |    |
|                 |                                    | V <sub>CC</sub> = 3 V              |                        | -24                    |    |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 1.65 V           |                        | 4                      | mA |
|                 |                                    | V <sub>CC</sub> = 2.3 V            |                        | 8                      |    |
|                 |                                    | V <sub>CC</sub> = 2.7 V            |                        | 12                     |    |
|                 |                                    | V <sub>CC</sub> = 3 V              |                        | 24                     |    |
| Δt/Δv           | Input transition rise or fall rate |                                    | 10                     | ns/V                   |    |
| T <sub>A</sub>  | Operating free-air temperature     | -40                                | 85                     | °C                     |    |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74LVC112A

## DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

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### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS  | V <sub>CC</sub> | MIN                   | TYP <sup>(1)</sup> | MAX | UNIT |
|------------------|--|-----------------|-----------------------|--------------------|-----|------|
| V <sub>OH</sub>  | I <sub>OH</sub> = –100 μA  | 1.65 V to 3.6 V | V <sub>CC</sub> – 0.2 |                    |     | V    |
|                  | I <sub>OH</sub> = –4 mA  | 1.65 V          | 1.2                   |                    |     |      |
|                  | I <sub>OH</sub> = –8 mA  | 2.3 V           | 1.7                   |                    |     |      |
|                  | I <sub>OH</sub> = –12 mA   | 2.7 V           | 2.2                   |                    |     |      |
|                  |  | 3 V             | 2.4                   |                    |     |      |
|                  | I <sub>OH</sub> = –24 mA   | 3 V             | 2.2                   |                    |     |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = 100 μA   | 1.65 V to 3.6 V | 0.2                   |                    |     | V    |
|                  | I <sub>OL</sub> = 4 mA   | 1.65 V          | 0.45                  |                    |     |      |
|                  | I <sub>OL</sub> = 8 mA   | 2.3 V           | 0.7                   |                    |     |      |
|                  | I <sub>OL</sub> = 12 mA  | 2.7 V           | 0.4                   |                    |     |      |
|                  | I <sub>OL</sub> = 24 mA  | 3 V             | 0.55                  |                    |     |      |
| I <sub>I</sub>   | V <sub>I</sub> = 5.5 V or GND  | 3.6 V           | ±5                    |                    |     | μA   |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                  | 3.6 V           | 10                    |                    |     | μA   |
| ΔI <sub>CC</sub> | One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND | 2.7 V to 3.6 V  | 500                   |                    |     | μA   |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           | 4.5                   |                    |     | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

### Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

|                    |                                 | V <sub>CC</sub> = 1.8 V ± 0.15 V                            |     | V <sub>CC</sub> = 2.5 V ± 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V ± 0.3 V |     | UNIT |    |
|--------------------|---------------------------------|---|-----|---------------------------------|-----|-------------------------|-----|---------------------------------|-----|------|----|
|                    |                                 | MIN   | MAX | MIN                             | MAX | MIN                     | MAX | MIN                             | MAX |      |    |
| f <sub>clock</sub> | Clock frequency                 | (1)   |     | (1)                             |     | 150                     |     | 150                             |     | MHz  |    |
| t <sub>w</sub>     | Pulse duration, CLK high or low | (1)   |     | (1)                             |     | 3.3                     |     | 3.3                             |     | ns   |    |
| t <sub>su</sub>    | Setup time                      | Data before CLK↓  | (1) |                                 | (1) |                         | 3.1 |                                 | 2.3 |      | ns |
|                    |                                 | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive | (1) |                                 | (1) |                         | 2.4 |                                 | 1.1 |      |    |
| t <sub>h</sub>     | Hold time, data after CLK↓      | (1)   |     | (1)                             |     | 2.5                     |     | 0.7                             |     | ns   |    |

(1) This information was not available at the time of publication.

### Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM (INPUT)                                       | TO (OUTPUT)                | V <sub>CC</sub> = 1.8 V ± 0.15 V |     | V <sub>CC</sub> = 2.5 V ± 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V ± 0.3 V |     |     | UNIT |
|------------------|--|----------------------------|----------------------------------|-----|---------------------------------|-----|-------------------------|-----|---------------------------------|-----|-----|------|
|                  |  |                            | MIN                              | MAX | MIN                             | MAX | MIN                     | MAX | MIN                             | TYP | MAX |      |
| f <sub>max</sub> |  |                            | (1)                              |     | (1)                             |     | 150                     |     | 150                             |     |     | MHz  |
| t <sub>pd</sub>  | $\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ | Q or $\overline{\text{Q}}$ | (1)                              | (1) | (1)                             | (1) | 5.5                     |     | 1                               | 3.4 | 4.8 | ns   |
|                  | CLK  |                            | (1)                              | (1) | (1)                             | (1) | 7.1                     |     | 1                               | 3.5 | 5.9 |      |

(1) This information was not available at the time of publication.

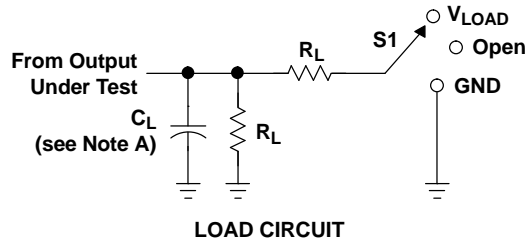
### Operating Characteristics

T<sub>A</sub> = 25°C

| PARAMETER       | TEST CONDITIONS               | V <sub>CC</sub> = 1.8 V | V <sub>CC</sub> = 2.5 V | V <sub>CC</sub> = 3.3 V | UNIT |    |
|-----------------|-------------------------------|-------------------------|-------------------------|-------------------------|------|----|
|                 |                               | TYP                     | TYP                     | TYP                     |      |    |
| C <sub>pd</sub> | Power dissipation capacitance | f = 10 MHz              | (1)                     | (1)                     | 24   | pF |

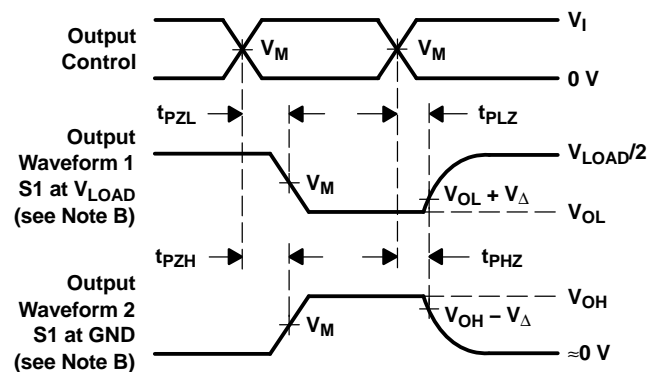
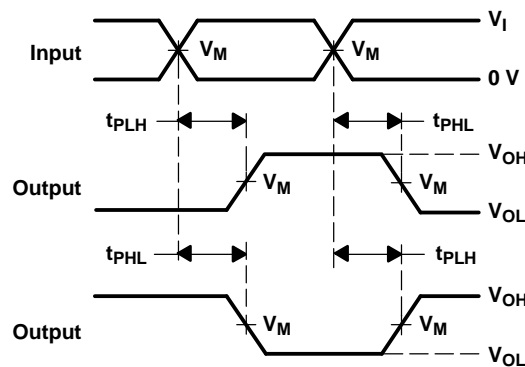
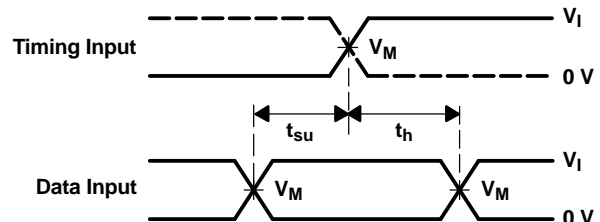
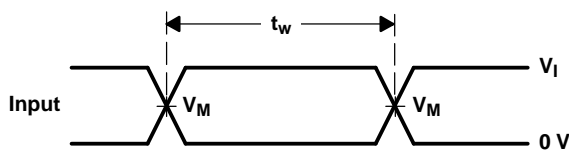
(1) This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION



| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| 2.7 V                            | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74LVC112AD      | ACTIVE        | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LVC112A                  | <a href="#">Samples</a> |
| SN74LVC112ADBLE   | OBSOLETE      | SSOP         | DB              | 16   |             | TBD                     | Call TI          | Call TI              | -40 to 85    |                          |                         |
| SN74LVC112ADBR    | ACTIVE        | SSOP         | DB              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |
| SN74LVC112ADBRE4  | ACTIVE        | SSOP         | DB              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |
| SN74LVC112ADBRG4  | ACTIVE        | SSOP         | DB              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |
| SN74LVC112ADE4    | ACTIVE        | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LVC112A                  | <a href="#">Samples</a> |
| SN74LVC112ADG4    | ACTIVE        | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LVC112A                  | <a href="#">Samples</a> |
| SN74LVC112ADGVR   | ACTIVE        | TVSOP        | DGV             | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |
| SN74LVC112ADGVRE4 | ACTIVE        | TVSOP        | DGV             | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |
| SN74LVC112ADGVRG4 | ACTIVE        | TVSOP        | DGV             | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |
| SN74LVC112ADR     | ACTIVE        | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LVC112A                  | <a href="#">Samples</a> |
| SN74LVC112ADRE4   | ACTIVE        | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LVC112A                  | <a href="#">Samples</a> |
| SN74LVC112ADRG4   | ACTIVE        | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LVC112A                  | <a href="#">Samples</a> |
| SN74LVC112ADT     | ACTIVE        | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LVC112A                  | <a href="#">Samples</a> |
| SN74LVC112ADTE4   | ACTIVE        | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LVC112A                  | <a href="#">Samples</a> |
| SN74LVC112ADTG4   | ACTIVE        | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LVC112A                  | <a href="#">Samples</a> |
| SN74LVC112ANSR    | ACTIVE        | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LVC112A                  | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74LVC112ANSRE4 | ACTIVE        | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LVC112A                  | <a href="#">Samples</a> |
| SN74LVC112ANSRG4 | ACTIVE        | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LVC112A                  | <a href="#">Samples</a> |
| SN74LVC112APW    | ACTIVE        | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |
| SN74LVC112APWE4  | ACTIVE        | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |
| SN74LVC112APWG4  | ACTIVE        | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |
| SN74LVC112APWLE  | OBSOLETE      | TSSOP        | PW              | 16   |             | TBD                     | Call TI          | Call TI              | -40 to 85    |                          |                         |
| SN74LVC112APWR   | ACTIVE        | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |
| SN74LVC112APWRE4 | ACTIVE        | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |
| SN74LVC112APWRG4 | ACTIVE        | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |
| SN74LVC112APWT   | ACTIVE        | TSSOP        | PW              | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |
| SN74LVC112APWTE4 | ACTIVE        | TSSOP        | PW              | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |
| SN74LVC112APWTG4 | ACTIVE        | TSSOP        | PW              | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | LC112A                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

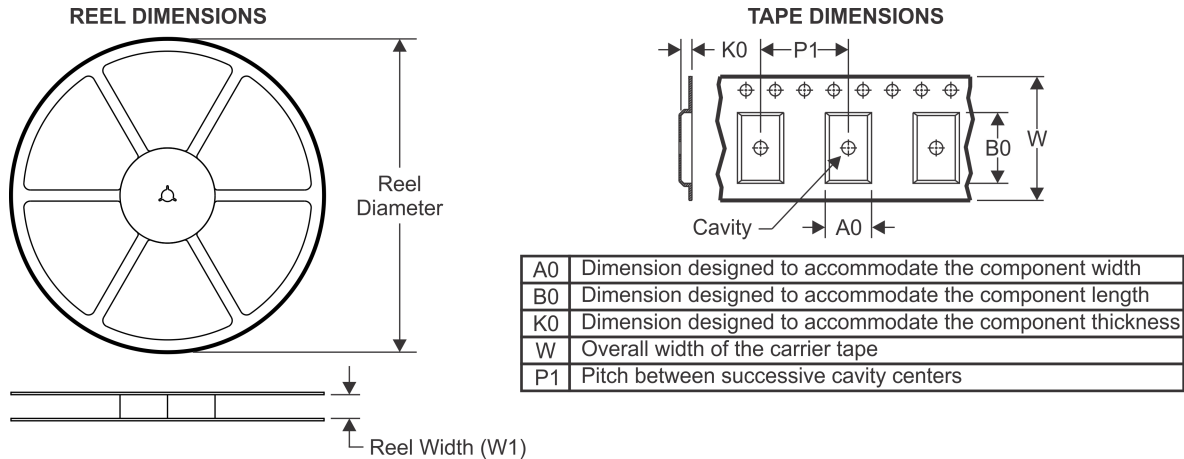
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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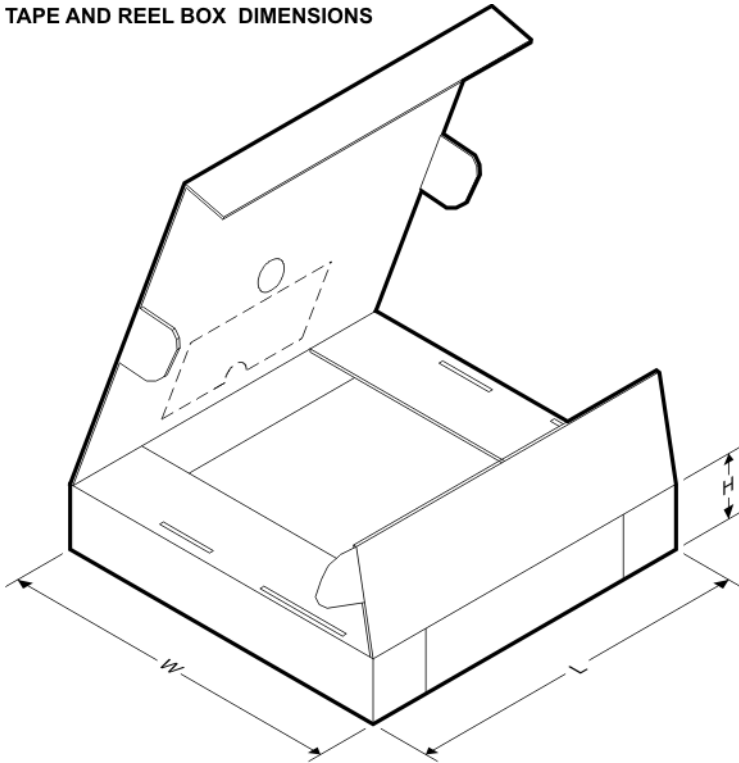
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC112ADBR  | SSOP         | DB              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 6.6     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LVC112ADGVR | TVSOP        | DGV             | 16   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC112ADR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC112ANSR  | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LVC112APWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC112APWT  | TSSOP        | PW              | 16   | 250  | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


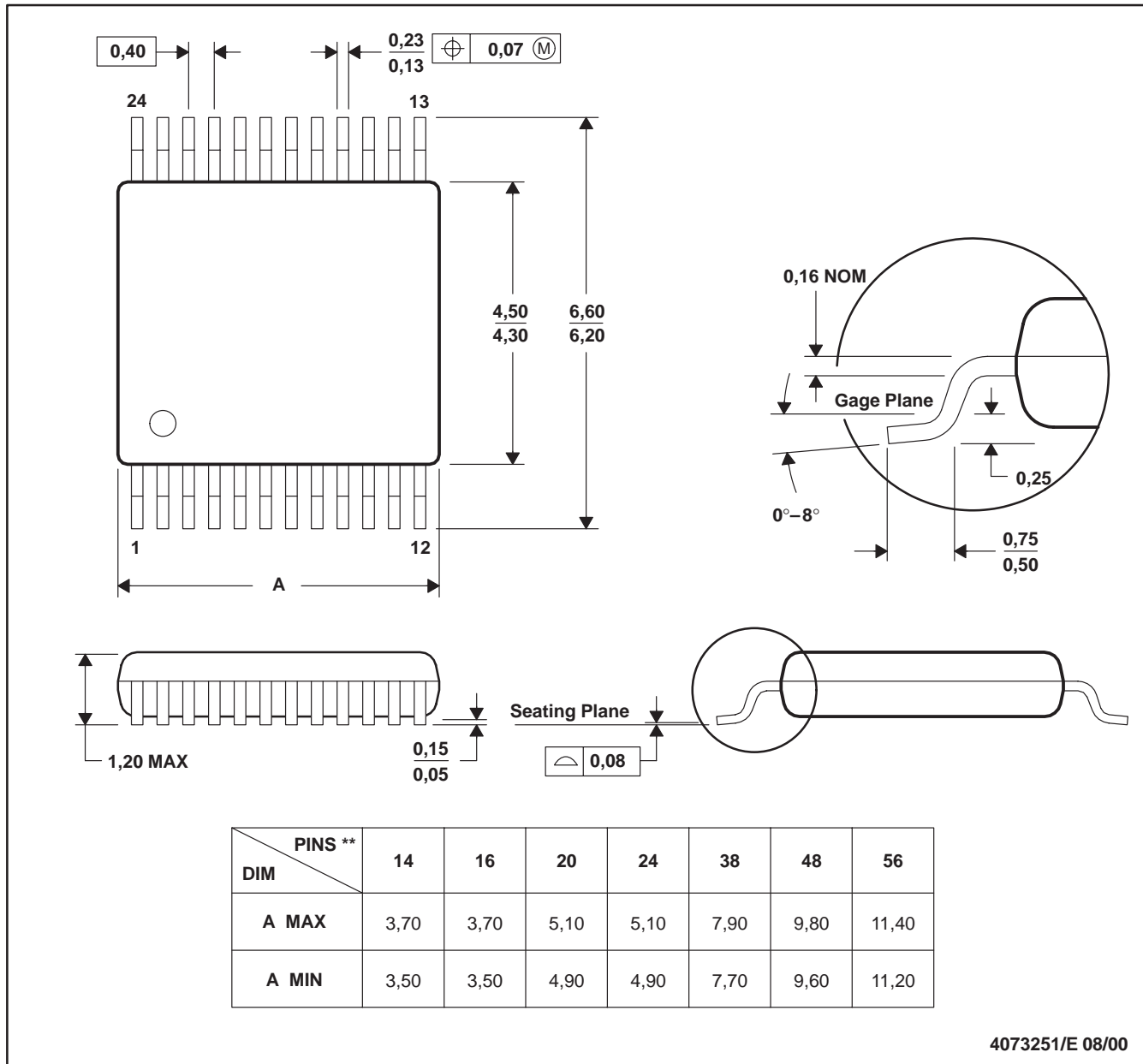
\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC112ADBR  | SSOP         | DB              | 16   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LVC112ADGVR | TVSOP        | DGV             | 16   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74LVC112ADR   | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| SN74LVC112ANSR  | SO           | NS              | 16   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LVC112APWR  | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74LVC112APWT  | TSSOP        | PW              | 16   | 250  | 367.0       | 367.0      | 35.0        |

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

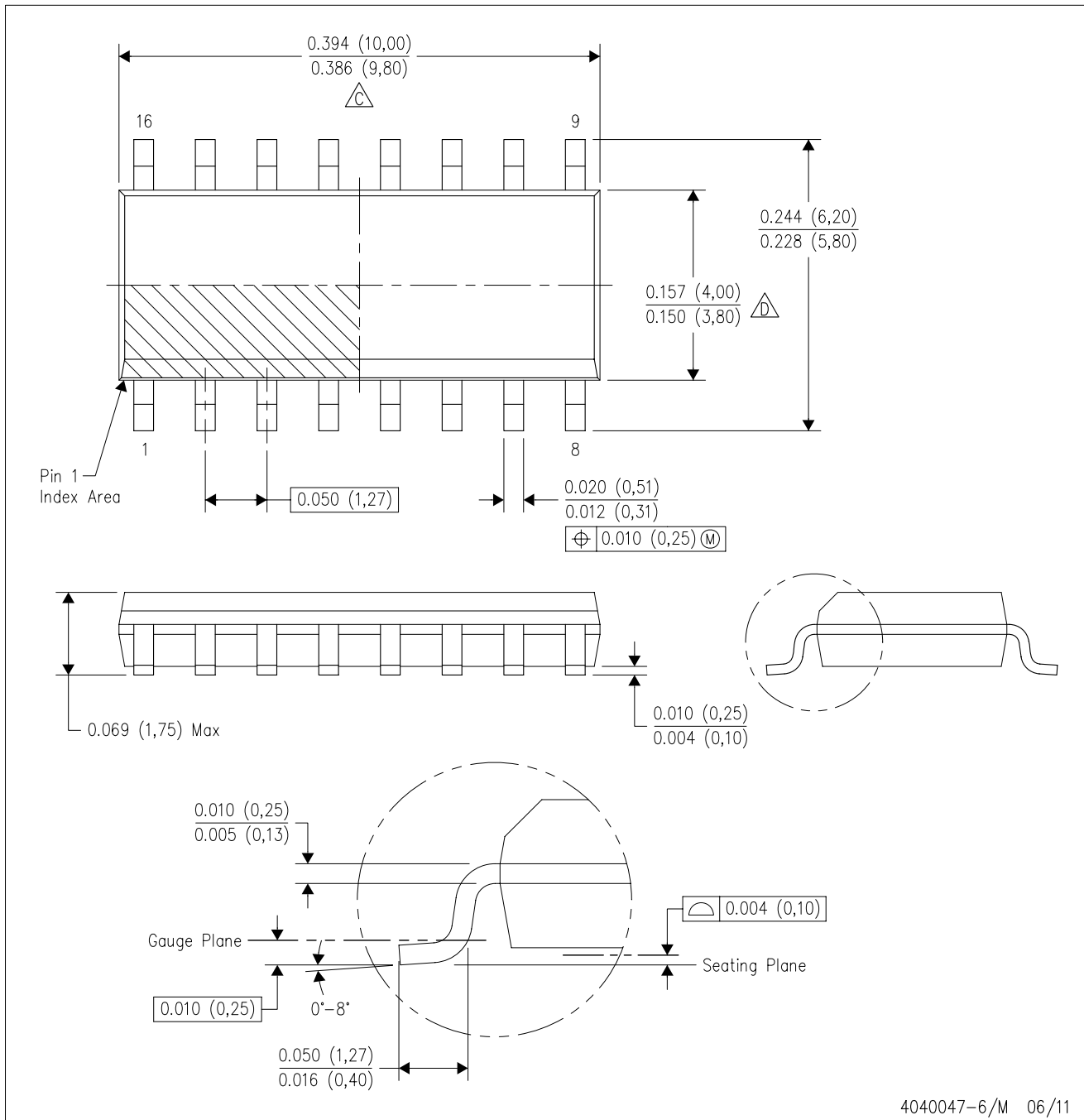
24 PINS SHOWN





- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

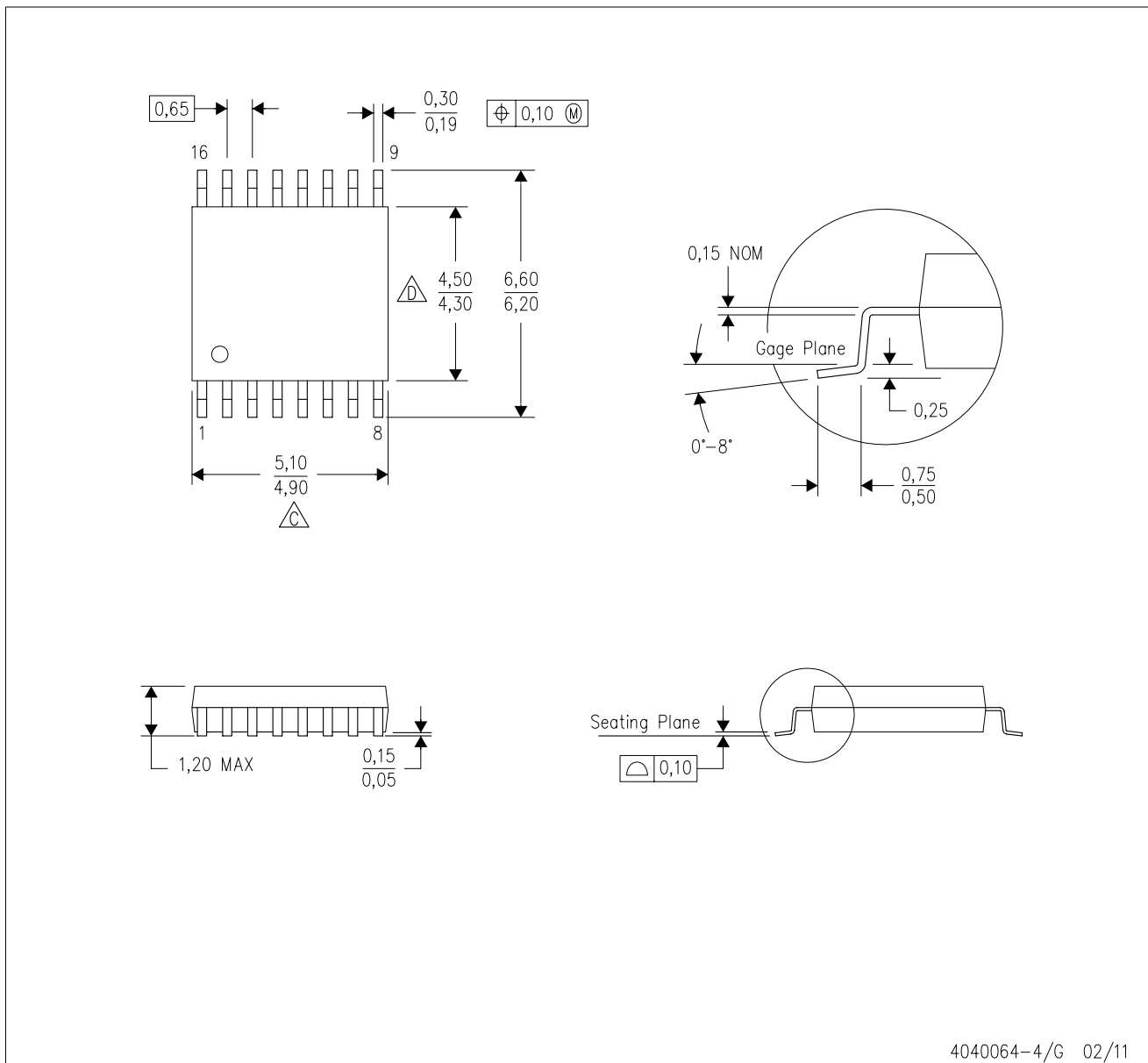


4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G16)

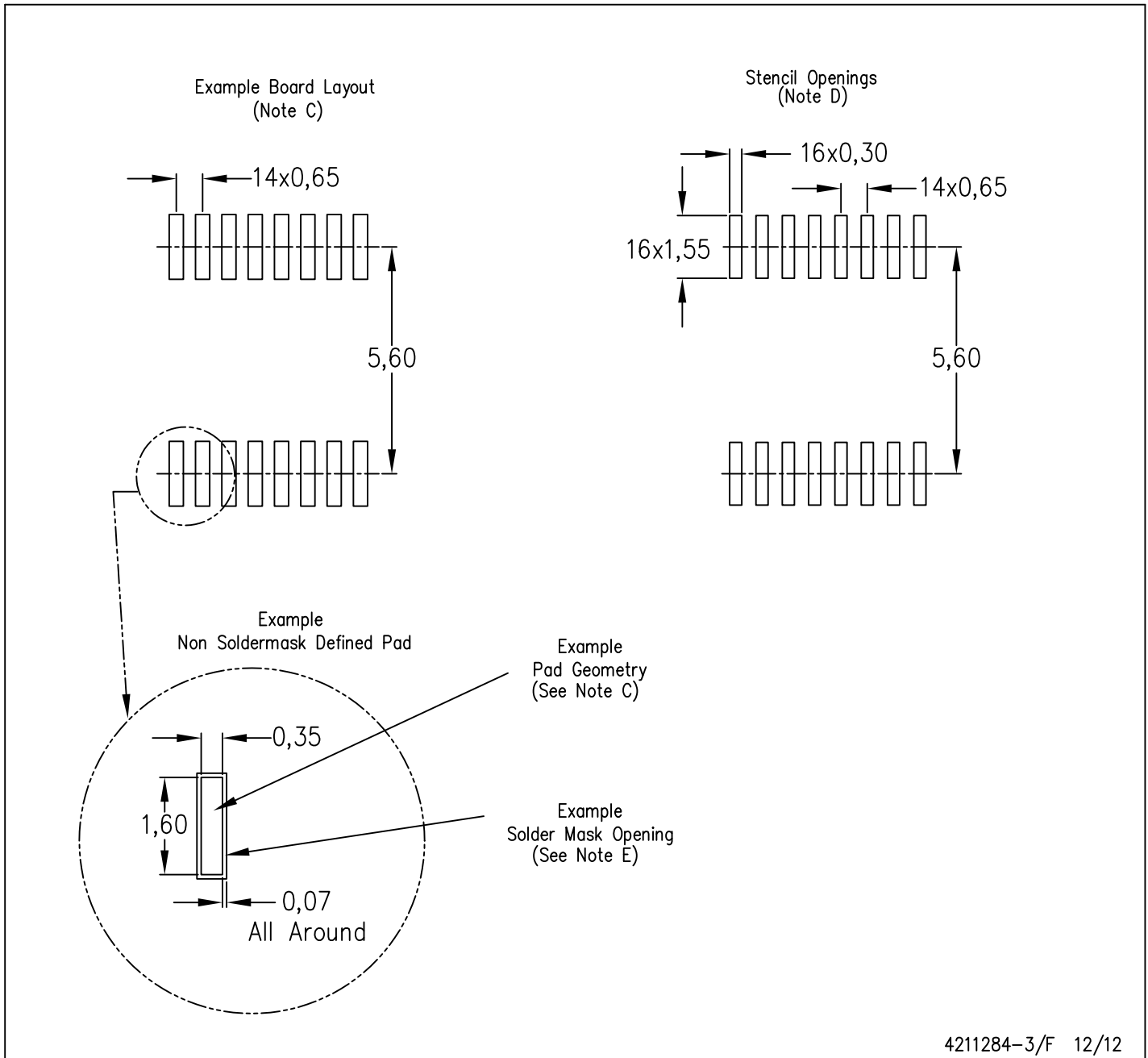
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



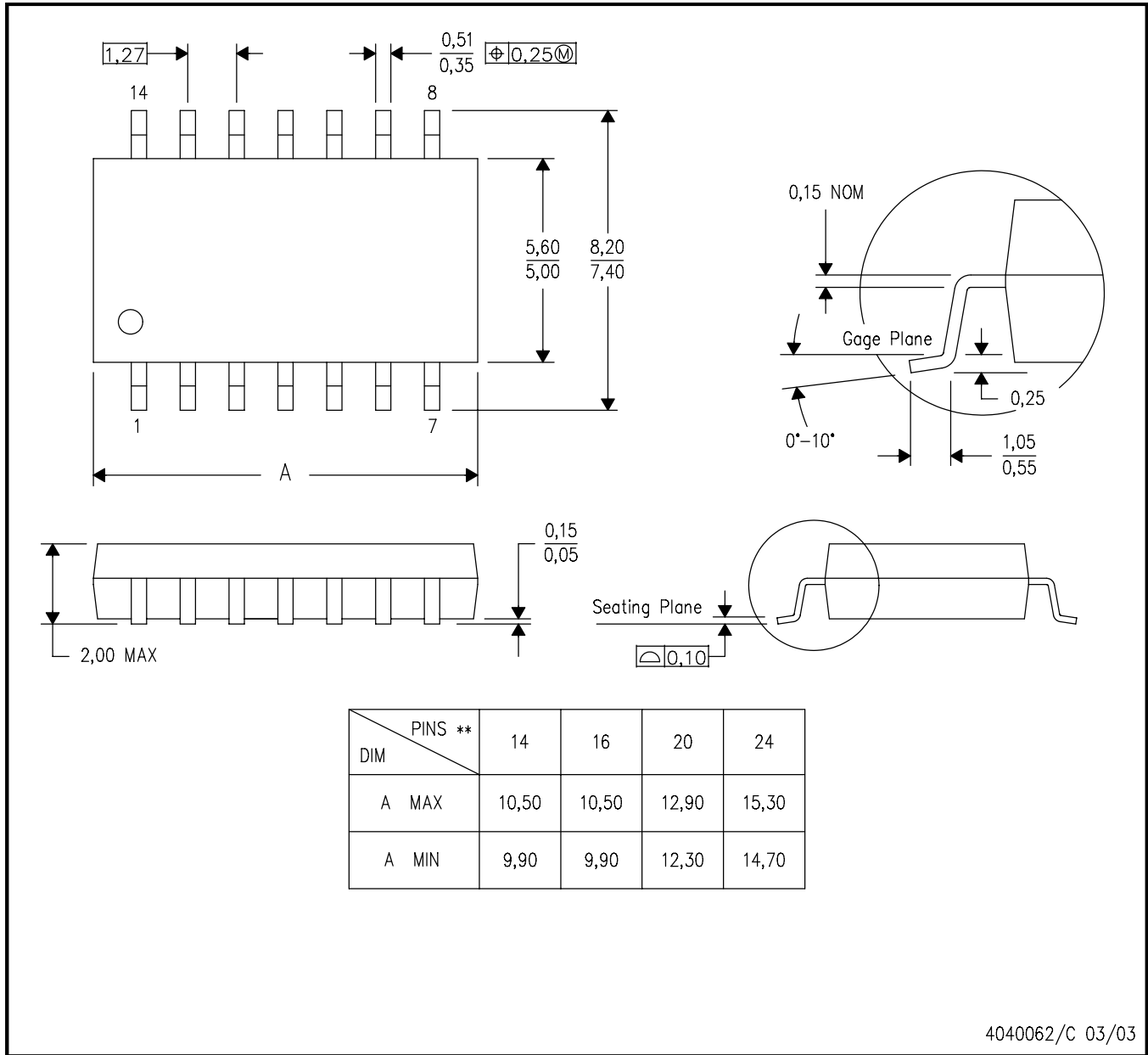
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

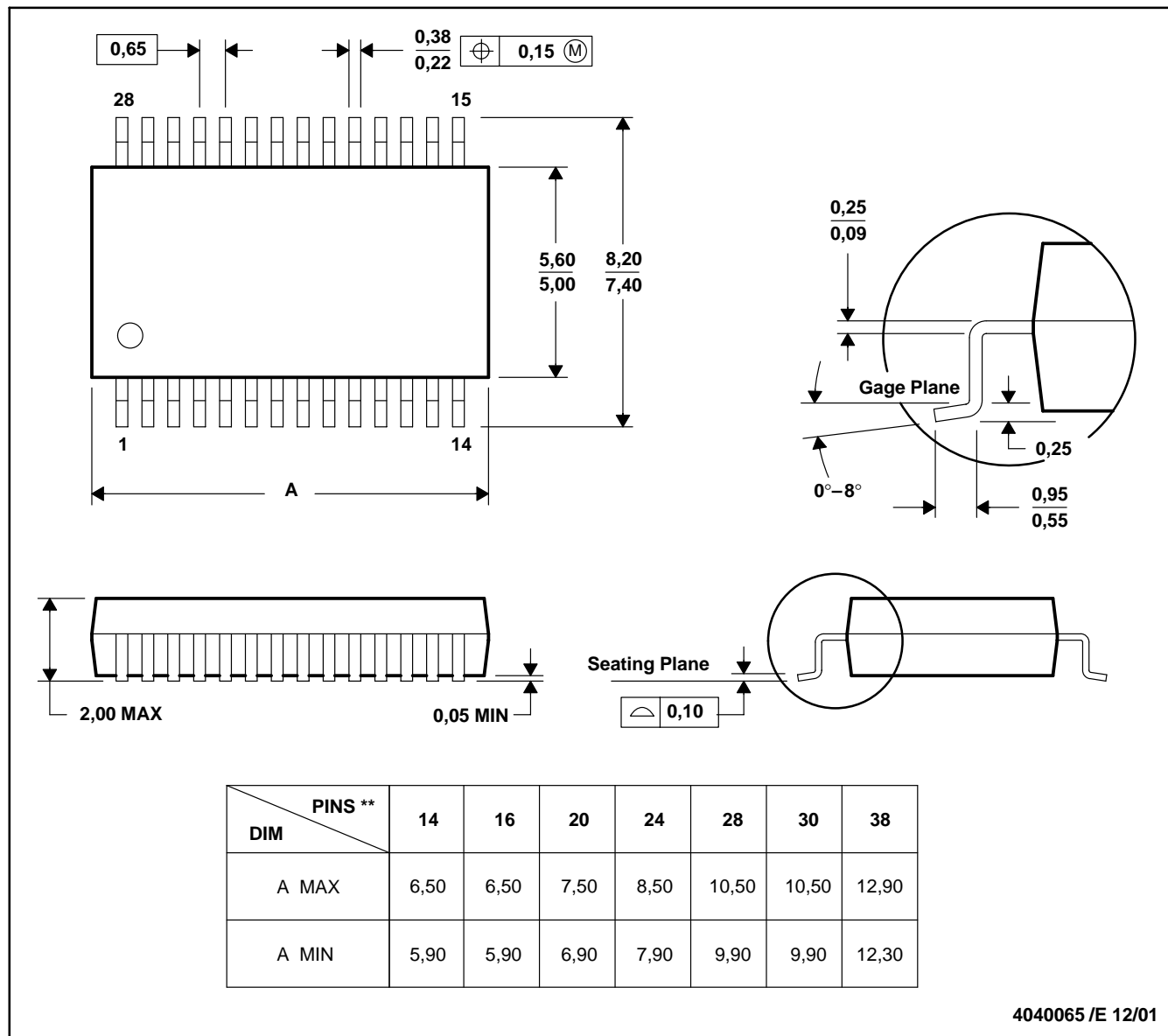


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150



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