

DS25BR110 3.125 Gbps LVDS Buffer with Receive Equalization

Check for Samples: [DS25BR110](#)

FEATURES

- DC - 3.125 Gbps Low Jitter, High Noise Immunity, Low Power Operation
- Four Levels of Receive Equalization Reduce ISI Jitter
- On-Chip 100Ω Input and Output Termination Minimizes Insertion and Return Losses, Reduces Component Count, and Minimizes Board Space
- 7 kV ESD on LVDS I/O Pins Protects Adjoining Components
- Small 3 mm x 3 mm 8-WSON Space Saving Package

APPLICATIONS

- Clock and Data Buffering
- Metallic Cable Equalization
- FR-4 Equalization

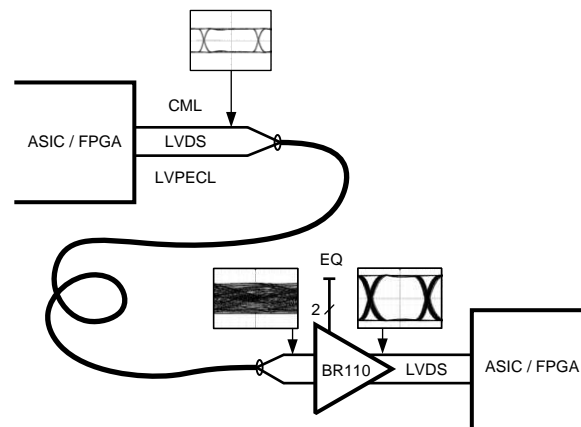
DESCRIPTION

The DS25BR110 is a single channel 3.125 Gbps LVDS buffer optimized for high-speed signal transmission over lossy FR-4 printed circuit board backplanes and balanced metallic cables. A fully differential signal path ensures exceptional signal integrity and noise immunity.

The DS25BR110 features four levels of receive equalization (EQ), making it ideal for use as a receiver device. Other LVDS devices with similar IO characteristics include the following products. The DS25BR120 features four levels of pre-emphasis for use as an optimized driver device, while the DS25BR100 features both pre-emphasis and equalization for use as an optimized repeater device. The DS25BR150 is a buffer/repeater with the lowest power consumption and does not feature transmit pre-emphasis nor receive equalization.

Wide input common mode range allows the receiver to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires minimal space on the board while the flow-through pinout allows easy board layout. The differential inputs and outputs are internally terminated with a 100Ω resistor to lower device input and output return losses, reduce component count, and further minimize board space.

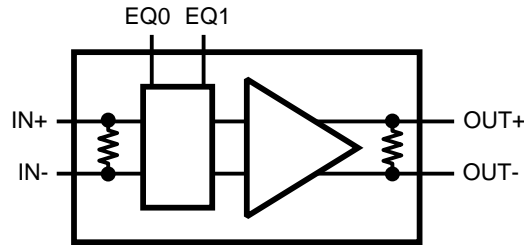
Typical Application



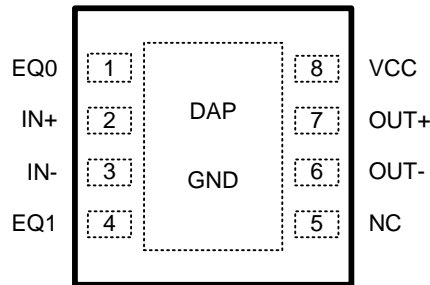
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Block Diagram



Pin Diagram



Pin Descriptions

Pin		Type	Description
Name	Number		
EQ0	1	Input	Equalizer select pin.
IN+	2	Input	Non-inverting LVDS input pin.
IN-	3	Input	Inverting LVDS input pin.
EQ1	4	Input	Equalizer select pin.
NC	5	NA	"NO CONNECT" pin.
OUT-	6	Output	Inverting LVDS output pin.
OUT+	7	Output	Non-inverting LVDS Output pin.
VCC	8	Power	Power supply pin.
GND	DAP	Power	Ground pad (DAP - die attach pad)

Control Pins (EQ0 and EQ1) Truth Tables

EQ1	EQ0	Equalization Level
0	0	Off
0	1	Low (Approx. 4 dB at 1.56 GHz)
1	0	Medium (Approx. 8 dB at 1.56 GHz)
1	1	High (Approx. 16 dB at 1.56 GHz)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage (V_{CC})	-0.3V to +4V
LVCMOS Input Voltage (EQ0, EQ1)	-0.3V to ($V_{CC} + 0.3V$)
LVDS Input Voltage (IN+, IN-)	-0.3V to +4V
Differential Input Voltage VID	1.0V
LVDS Output Voltage (OUT+, OUT-)	-0.3V to ($V_{CC} + 0.3V$)
LVDS Differential Output Voltage ((OUT+) - (OUT-))	0V to 1.0V
LVDS Output Short Circuit Current Duration	5 ms
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
NGQ0008A Package	2.08W
Derate NGQ0008A Package	16.7 mW/°C above +25°C
Package Thermal Resistance	
θ_{JA}	+60.0°C/W
θ_{JC}	+12.3°C/W
ESD Susceptibility	
HBM ⁽³⁾	≥7 kV
MM ⁽⁴⁾	≥250V
CDM ⁽⁵⁾	≥1250V

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Human Body Model, applicable std. JESD22-A114C
- (4) Machine Model, applicable std. JESD22-A115-A
- (5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID})			1.0	V
Operating Free Air Temperature (T_A)	-40	+25	+85	°C

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. ⁽¹⁾ ⁽²⁾ ⁽³⁾

Parameter		Test Conditions	Min	Typ	Max	Units
LVC MOS INPUT DC SPECIFICATIONS (EQ0, EQ1)						
V _{IH}	High Level Input Voltage		2.0		V _{CC}	V
V _{IL}	Low Level Input Voltage		GND		0.8	V
I _{IH}	High Level Input Current	V _{IN} = 3.6V V _{CC} = 3.6V		0	±10	µA
I _{IL}	Low Level Input Current	V _{IN} = GND V _{CC} = 3.6V		0	±10	µA
V _{CL}	Input Clamp Voltage	I _{CL} = -18 mA, V _{CC} = 0V		-0.9	-1.5	V
LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)						
V _{OD}	Differential Output Voltage		250	350	450	mV
ΔV _{OD}	Change in Magnitude of V _{OD} for Complimentary Output States	R _L = 100Ω	-35		35	mV
V _{OS}	Offset Voltage		1.05	1.2	1.375	V
ΔV _{OS}	Change in Magnitude of V _{OS} for Complimentary Output States	R _L = 100Ω	-35		35	mV
I _{OS}	Output Short Circuit Current ⁽⁴⁾	OUT to GND		-35	-55	mA
		OUT to V _{CC}		7	55	mA
C _{OUT}	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R _{OUT}	Output Termination Resistor	Between OUT+ and OUT-		100		Ω
LVDS INPUT DC SPECIFICATIONS (IN+, IN-)						
V _{ID}	Input Differential Voltage		0		1	V
V _{TH}	Differential Input High Threshold	V _{CM} = +0.05V or V _{CC} -0.05V		0	+100	mV
V _{TL}	Differential Input Low Threshold		-100	0		mV
V _{CMR}	Common Mode Voltage Range	V _{ID} = 100 mV	0.05		V _{CC} - 0.05	V
I _{IN}	Input Current	V _{IN} = 3.6V or 0V V _{CC} = 3.6V or 0V		±1	±10	µA
C _{IN}	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R _{IN}	Input Termination Resistor	Between IN+ and IN-		100		Ω
SUPPLY CURRENT						
I _{CC}	Supply Current	EQ0 = 0, EQ1 = 0		35	43	mA

- (1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or notes. Typical specifications are estimations only and are not guaranteed.
- (2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
- (3) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.
- (4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics ⁽¹⁾

Over recommended operating supply and temperature ranges unless otherwise specified. ⁽²⁾ ⁽³⁾

Parameter		Test Conditions	Min	Typ	Max	Units	
LVDS OUTPUT AC SPECIFICATIONS (OUT+, OUT-)							
t_{PHLD}	Differential Propagation Delay High to Low	$R_L = 100\Omega$		350	465	ps	
t_{PLHD}	Differential Propagation Delay Low to High			350	465	ps	
t_{SKD1}	Pulse Skew $ t_{PLHD} - t_{PHLD} $ ⁽⁴⁾			45	100	ps	
t_{SKD2}	Part to Part Skew ⁽⁵⁾			45	150	ps	
t_{LHT}	Rise Time	$R_L = 100\Omega$		80	150	ps	
t_{HLT}	Fall Time			80	150	ps	
JITTER PERFORMANCE WITH EQ = OFF							
t_{RJ1A}	Random Jitter (RMS Value)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{V}$ Clock (RZ) $EQ0 = 0, EQ1 = 0$	2.5 Gbps		0.5	1	ps
t_{RJ2A}	No Test Channels ⁽⁶⁾		3.125 Gbps		0.5	1	ps
t_{DJ1A}	Deterministic Jitter (Peak to Peak)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{V}$ K28.5 (NRZ) $EQ0 = 0, EQ1 = 0$	2.5 Gbps		11	40	ps
t_{DJ2A}	No Test Channels ⁽⁷⁾		3.125 Gbps		11	47	ps
t_{TJ1A}	Total Jitter (Peak to Peak)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{V}$ PRBS-23 (NRZ) $EQ0 = 0, EQ1 = 0$	2.5 Gbps		0.05	0.16	UI _{P-P}
t_{TJ2A}	No Test Channels ⁽⁸⁾		3.125 Gbps		0.08	0.20	UI _{P-P}
JITTER PERFORMANCE WITH EQ = LOW (Figure 5 and Figure 6)							
t_{RJ1B}	Random Jitter (RMS Value)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{V}$ Clock (RZ) $EQ0 = 1, EQ1 = 0$	2.5 Gbps		0.5	1	ps
t_{RJ2B}	Test Channel D ⁽⁶⁾		3.125 Gbps		0.5	1	ps
t_{DJ1B}	Deterministic Jitter (Peak to Peak)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{V}$ K28.5 (NRZ) $EQ0 = 1, EQ1 = 0$	2.5 Gbps		1	16	ps
t_{DJ2B}	Test Channel D ⁽⁷⁾		3.125 Gbps		11	31	ps
t_{TJ1B}	Total Jitter (Peak to Peak)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{V}$ PRBS-23 (NRZ) $EQ0 = 1, EQ1 = 0$	2.5 Gbps		0.03	0.09	UI _{P-P}
t_{TJ2B}	Test Channel D ⁽⁸⁾		3.125 Gbps		0.06	0.14	UI _{P-P}
JITTER PERFORMANCE WITH EQ = MEDIUM (Figure 5 and Figure 6)							
t_{RJ1C}	Random Jitter (RMS Value)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{V}$ Clock (RZ) $EQ0 = 0, EQ1 = 1$	2.5 Gbps		0.5	1	ps
t_{RJ2C}	Test Channel E ⁽⁶⁾		3.125 Gbps		0.5	1	ps
t_{DJ1C}	Deterministic Jitter (Peak to Peak)	$V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{V}$ K28.5 (NRZ) $EQ0 = 0, EQ1 = 1$	2.5 Gbps		10	29	ps
t_{DJ2C}	Test Channel E ⁽⁷⁾		3.125 Gbps		27	43	ps

(1) Specification is guaranteed by characterization and is not tested in production.

(2) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or notes. Typical specifications are estimations only and are not guaranteed.

(3) Typical values represent most likely parametric norms for $V_{CC} = +3.3\text{V}$ and $T_A = +25^\circ\text{C}$, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

(4) t_{SKD1} , $|t_{PLHD} - t_{PHLD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

(5) t_{SKD2} , Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

(6) Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.

(7) Tested with a combination of the 110000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.

(8) Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

AC Electrical Characteristics ⁽¹⁾ (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. ⁽²⁾ ⁽³⁾

Parameter		Test Conditions	Min	Typ	Max	Units	
t _{TJ1C}	Total Jitter (Peak to Peak) Test Channel E (8)	V _{ID} = 350 mV V _{CM} = 1.2V PRBS-23 (NRZ) EQ0 = 0, EQ1 = 1	2.5 Gbps		0.07	0.12	UI _{P-P}
t _{TJ2C}			3.125 Gbps		0.12	0.17	UI _{P-P}
JITTER PERFORMANCE WITH EQ = HIGH (Figure 5 and Figure 6)							
t _{RJ1D}	Random Jitter (RMS Value) Test Channel F (6)	V _{ID} = 350 mV V _{CM} = 1.2V Clock (RZ) EQ0 = 1, EQ1 = 1	2.5 Gbps		1.6	2.1	ps
t _{RJ2D}			3.125 Gbps		1.7	2.3	ps
t _{DJ1D}	Deterministic Jitter (Peak to Peak) Test Channel F (7)	V _{ID} = 350 mV V _{CM} = 1.2V K28.5 (NRZ) EQ0 = 1, EQ1 = 1	2.5 Gbps		30	45	ps
t _{DJ2D}			3.125 Gbps		43	59	ps
t _{TJ1D}	Total Jitter (Peak to Peak) Test Channel F (8)	V _{ID} = 350 mV V _{CM} = 1.2V PRBS-23 (NRZ) EQ0 = 1, EQ1 = 1	2.5 Gbps		0.14	0.27	UI _{P-P}
t _{TJ2D}			3.125 Gbps		0.19	0.28	UI _{P-P}

DC TEST CIRCUITS

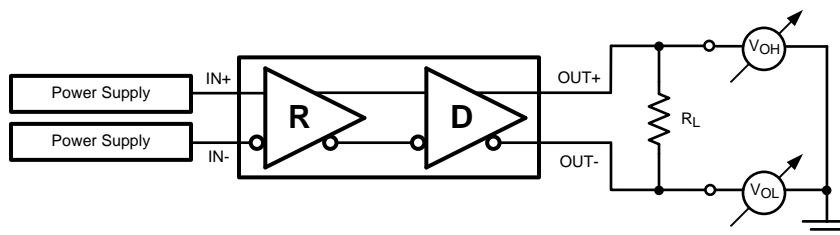


Figure 1. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams

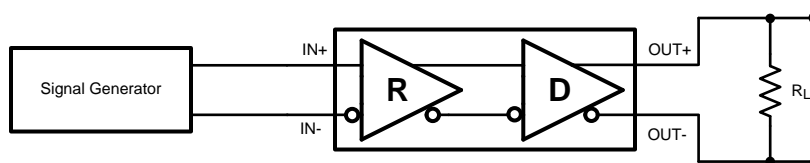


Figure 2. Differential Driver AC Test Circuit

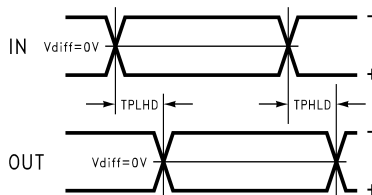


Figure 3. Propagation Delay Timing Diagram

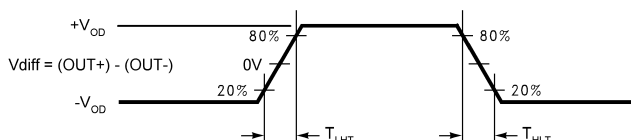


Figure 4. LVDS Output Transition Times

Equalization Test Circuits

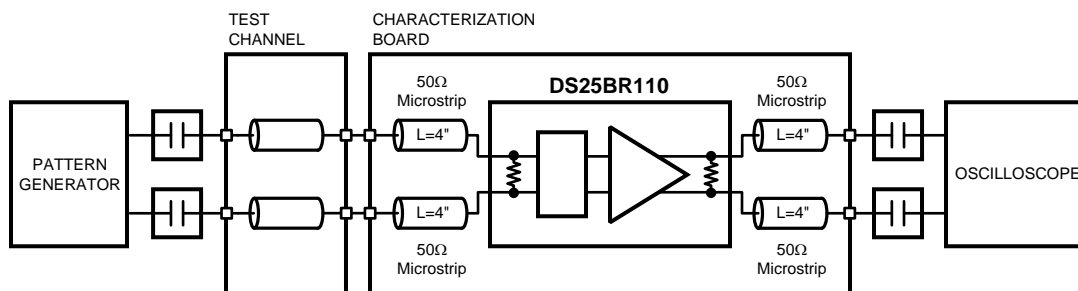


Figure 5. Equalization Performance Test Circuit

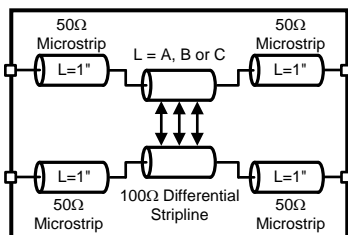


Figure 6. Test Channel Description

Test Channel Loss Characteristics

The test channel was fabricated with Polyclad PCL-FR-370-Laminate/PCL-FRP-370 Prepreg materials (Dielectric constant of 3.7 and Loss Tangent of 0.02). The edge coupled differential striplines have the following geometries: Trace Width (W) = 5 mils, Gap (S) = 5 mils, Height (B) = 16 mils.

Test Channel	Length (inches)	Insertion Loss (dB)					
		500 MHz	750 MHz	1000 MHz	1250 MHz	1500 MHz	1560 MHz
A	10	-1.2	-1.7	-2.0	-2.4	-2.7	-2.8
B	20	-2.6	-3.5	-4.1	-4.8	-5.5	-5.6
C	30	-4.3	-5.7	-7.0	-8.2	-9.4	-9.7
D	15	-1.6	-2.2	-2.7	-3.2	-3.7	-3.8
E	30	-3.4	-4.5	-5.6	-6.6	-7.7	-7.9
F	60	-7.8	-10.3	-12.4	-14.5	-16.6	-17.0

Device Operation

INPUT INTERFACING

The DS25BR110 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25BR110 can be DC-coupled with all common differential drivers (i.e., LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS25BR110 inputs are internally terminated with a 100Ω resistor.

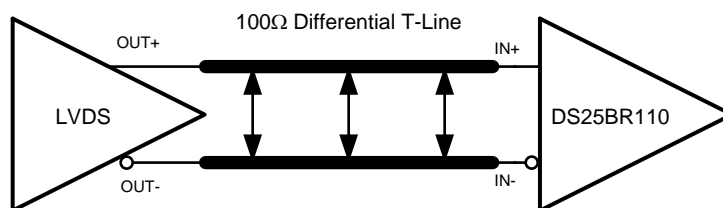


Figure 7. Typical LVDS Driver DC-Coupled Interface to DS25BR110 Input

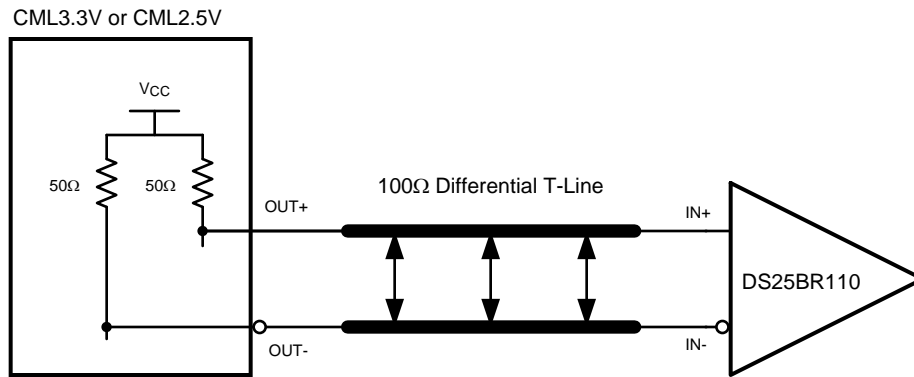


Figure 8. Typical CML Driver DC-Coupled Interface to DS25BR110 Input

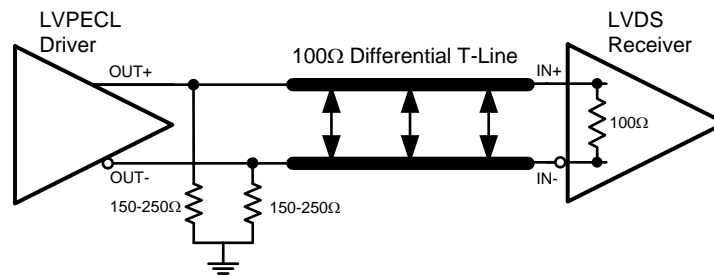


Figure 9. Typical LVPECL Driver DC-Coupled Interface to DS25BR110 Input

OUTPUT INTERFACING

The DS25BR110 outputs signals compliant to the LVDS standard. It can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check the respective receiver's datasheet prior to implementing the suggested interface implementation.

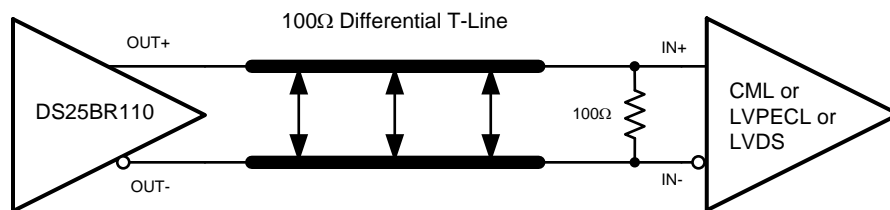


Figure 10. Typical DS25BR110 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

Typical Performance

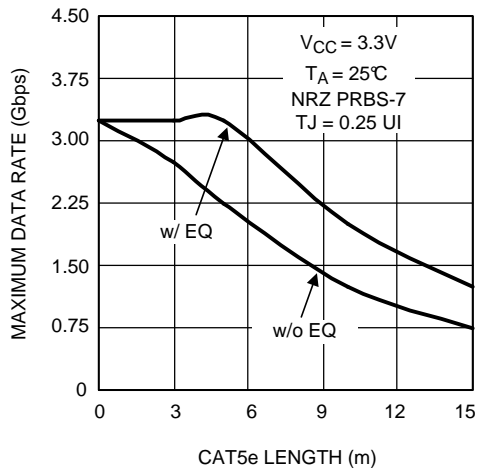


Figure 11. Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length

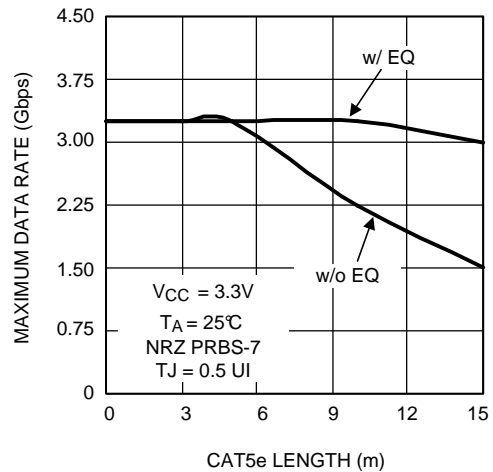


Figure 12. Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length

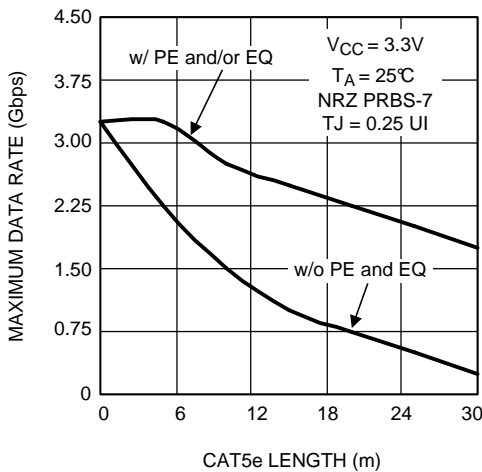


Figure 13. Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length
DS25BR120 Used as a Driver
DS25BR110 Used as a Receiver

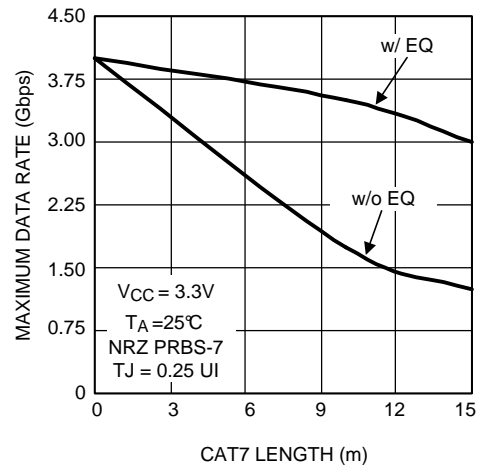


Figure 14. Maximum Data Rate as a Function of CAT7 (Siemon Tera) Length

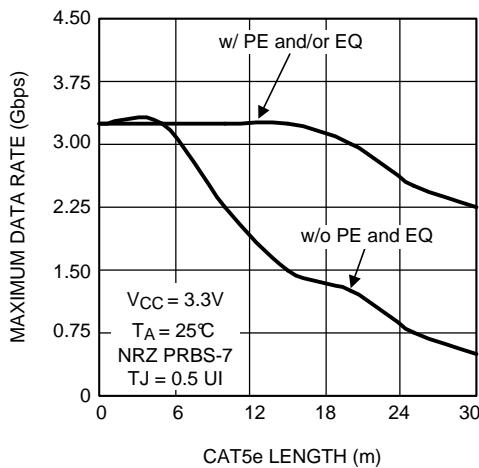


Figure 15. Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length
DS25BR120 Used as a Driver
DS25BR110 Used as a Receiver

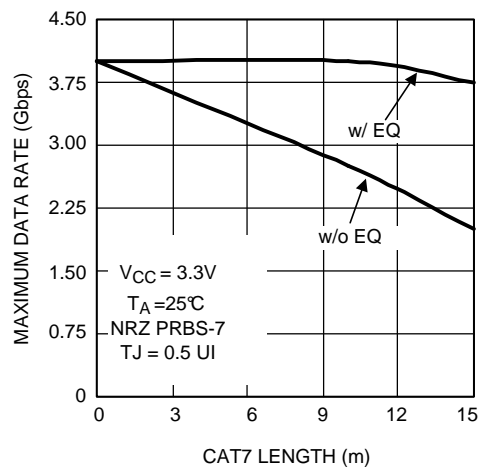


Figure 16. Maximum Data Rate as a Function of CAT7 (Slemon Tera) Length

Typical Performance (continued)

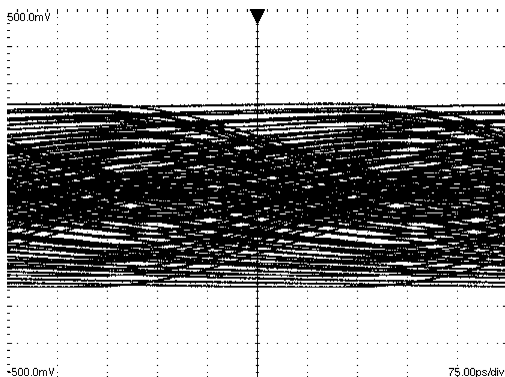


Figure 17. A 2.5 Gbps NRZ PRBS-7 After 70" Differential FR-4 Stripline
V:100 mV / DIV, H:75 ps / DIV

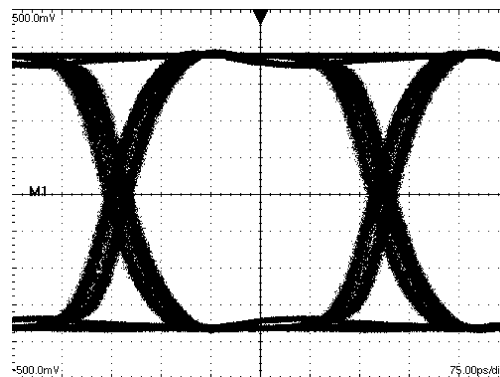


Figure 18. An Equalized 2.5 Gbps NRZ PRBS-7 After 70" Differential FR-4 Stripline
V:100 mV / DIV, H:75 ps / DIV

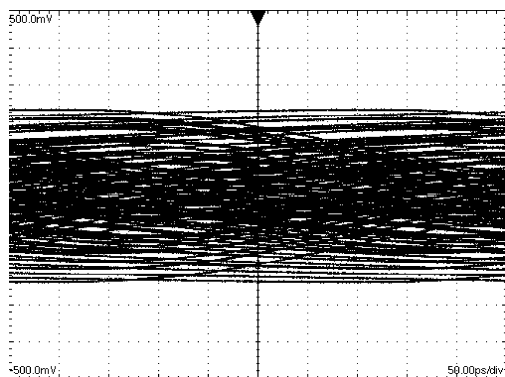


Figure 19. A 3.125 Gbps NRZ PRBS-7 After 70" Differential FR-4 Stripline
V:100 mV / DIV, H:50 ps / DIV

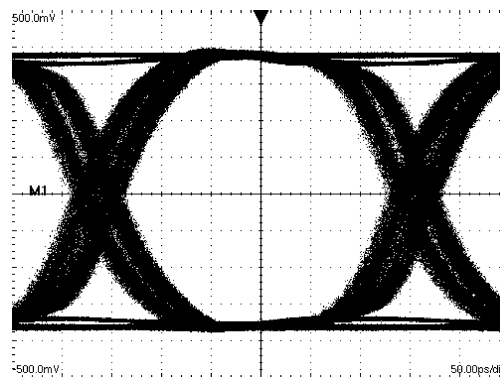


Figure 20. An Equalized 3.125 Gbps NRZ PRBS-7 After 70" Differential FR-4 Stripline
V:100 mV / DIV, H:50 ps / DIV

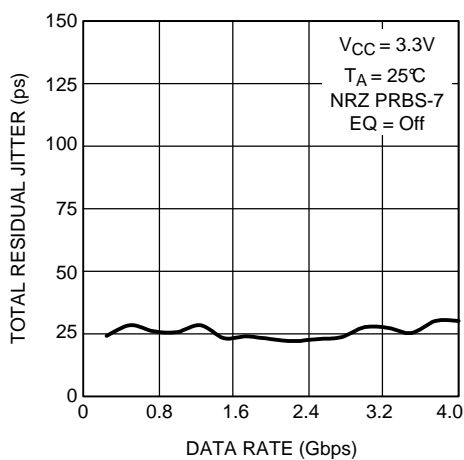


Figure 21. Total Jitter as a Function of Data Rate

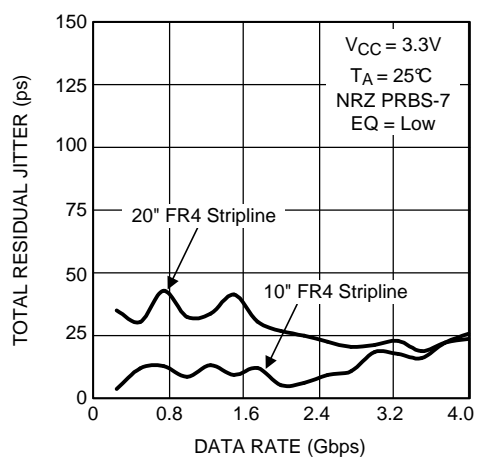


Figure 22. Total Jitter as a Function of Data Rate

Typical Performance (continued)

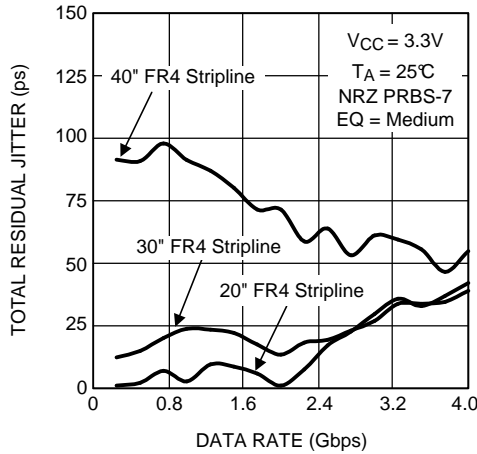


Figure 23. Total Jitter as a Function of Data Rate

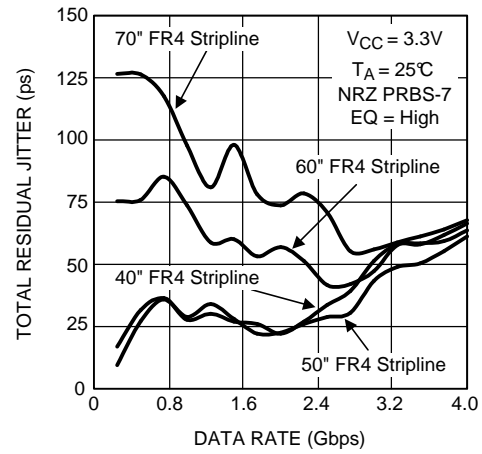


Figure 24. Total Jitter as a Function of Data Rate

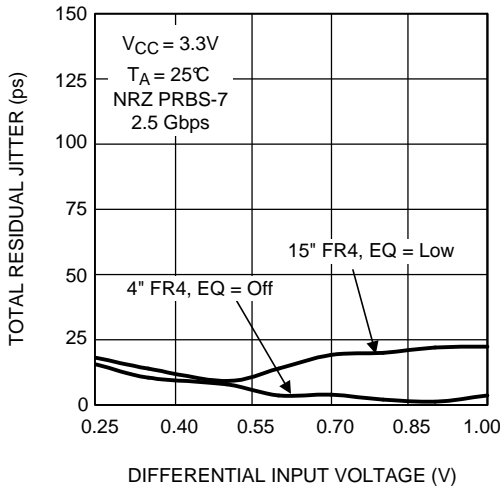


Figure 25. Total Jitter as a Function of Input Amplitude

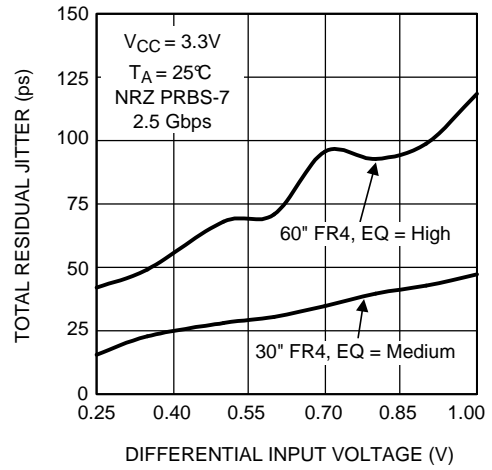


Figure 26. Total Jitter as a Function of Input Amplitude

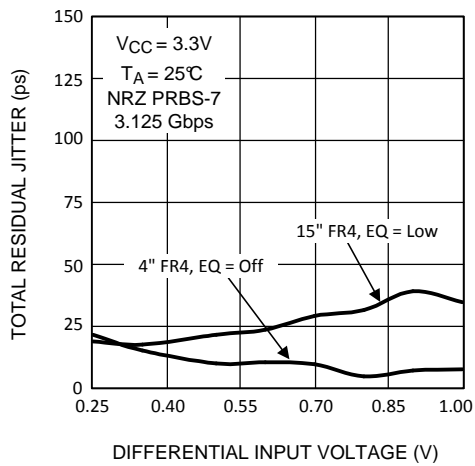


Figure 27. Total Jitter as a Function of Input Amplitude

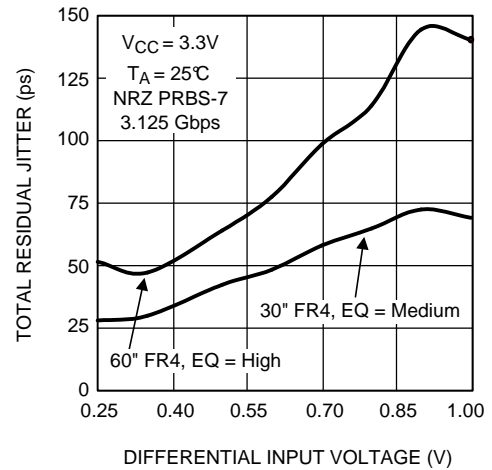




Figure 28. Total Jitter as a Function of Input Amplitude

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS25BR110TSD/NOPB	ACTIVE	WSON	NGQ	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	2R110	
DS25BR110TSDX/NOPB	ACTIVE	WSON	NGQ	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	2R110	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS25BR110TSD/NOPB	WSON	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DS25BR110TSDX/NOPB	WSON	NGQ	8	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

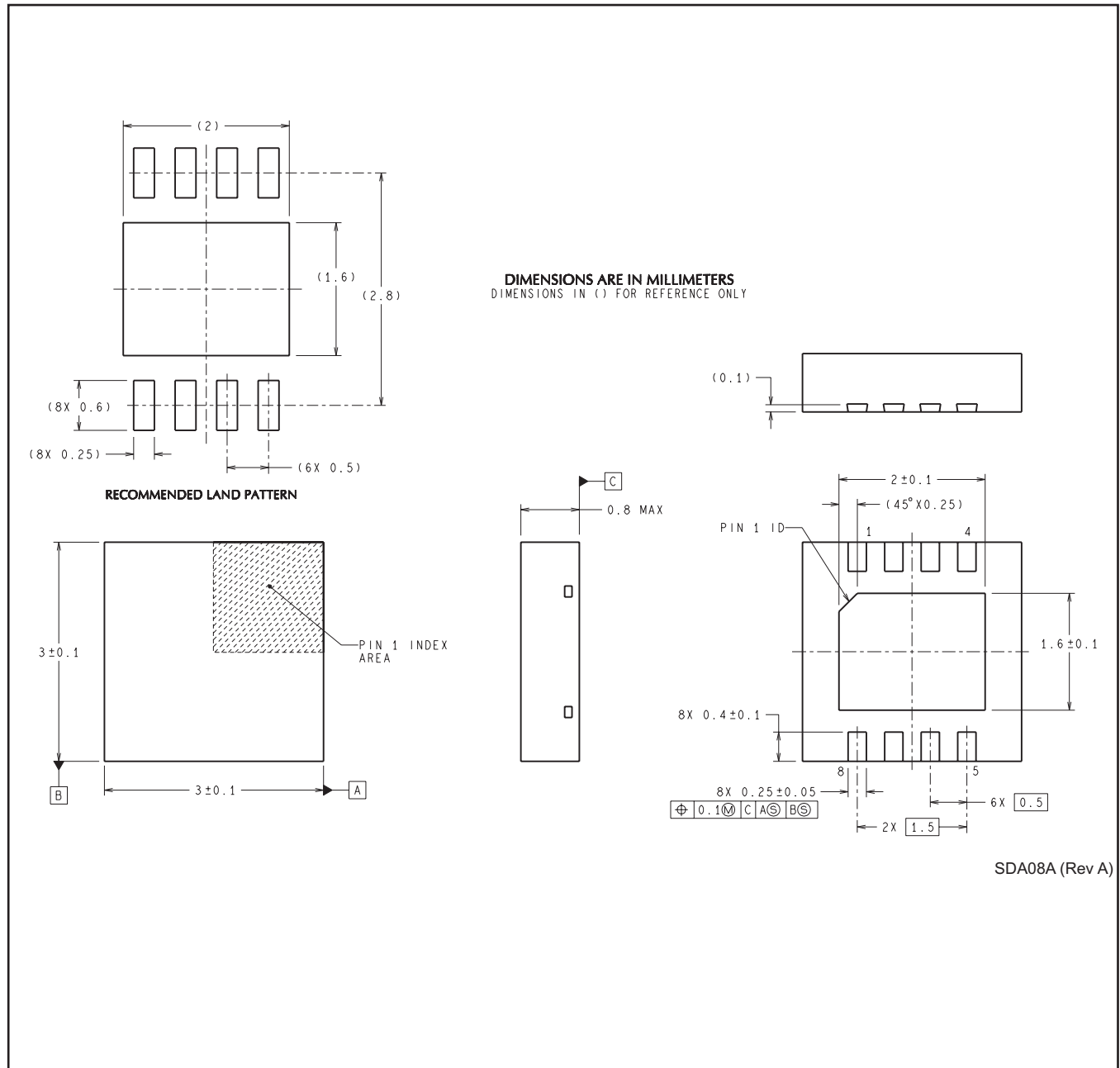
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS25BR110TSD/NOPB	WSON	NGQ	8	1000	213.0	191.0	55.0
DS25BR110TSDX/NOPB	WSON	NGQ	8	4500	367.0	367.0	35.0

NGQ0008A



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com



Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331