19-4621; 12/09

DS1254
2M x 8 NV SRAM with Phantom Clock

www.maxim-ic.com

GENERAL DESCRIPTION

The DS1254 is a fully nonvolatile static RAM (NV SRAM) (organized as 2M words by 8 bits) with built-in real-time clock. It has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the DS1254 makes use of an attached DS3800 battery cap to maintain clock information and preserve stored data while protecting that data by disallowing all memory accesses. Additionally, the DS1254 has dedicated circuitry for monitoring the status of an attached DS3800 battery cap.

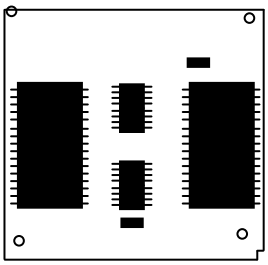
FEATURES

- Real-Time Clock (RTC) Keeps Track of Hundredths of Seconds, Seconds, Minutes, Hours, Days, Date, Months, and Years with Automatic Leap-Year Compensation Valid Up to the Year 2100
- 2M x 8 NV SRAM
- Watch Function is Transparent to RAM Operation
- Automatic Data Protection During Power Loss
- Unlimited Write-Cycle Endurance
- Surface-Mountable BGA Module Construction
- Over 10 Years of Data Retention in the Absence of Power
- Battery Monitor Checks Remaining Capacity Daily
- +3.3V Operation
- Underwriters Laboratory (UL) Recognized (www.maxim-ic.com/qa/info/ul/)

APPLICATIONS

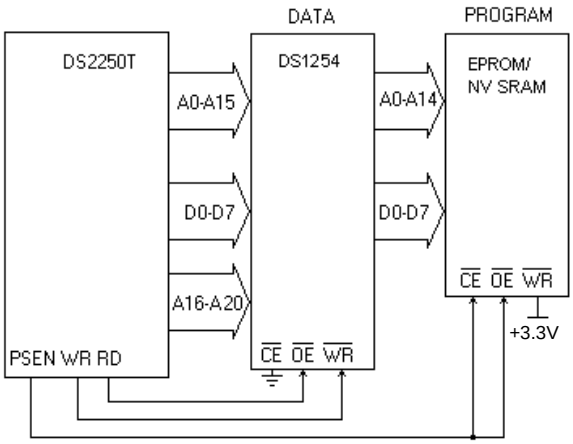
Telecom Switches
Routers
RAID Systems

PACKAGE OUTLINE



Side -A- Shown
(For Reference Only, Not to Scale)
Component placement may vary.

TYPICAL OPERATING CIRCUIT



ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE	VOLTAGE RANGE (V)	TOP MARK
DS1254WB-150	0°C to +70°C	40mm BGA	3.3	DS1254W-150
DS1254WB2-150	0°C to +70°C	40mm BGA	3.3	DS1254W-150

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

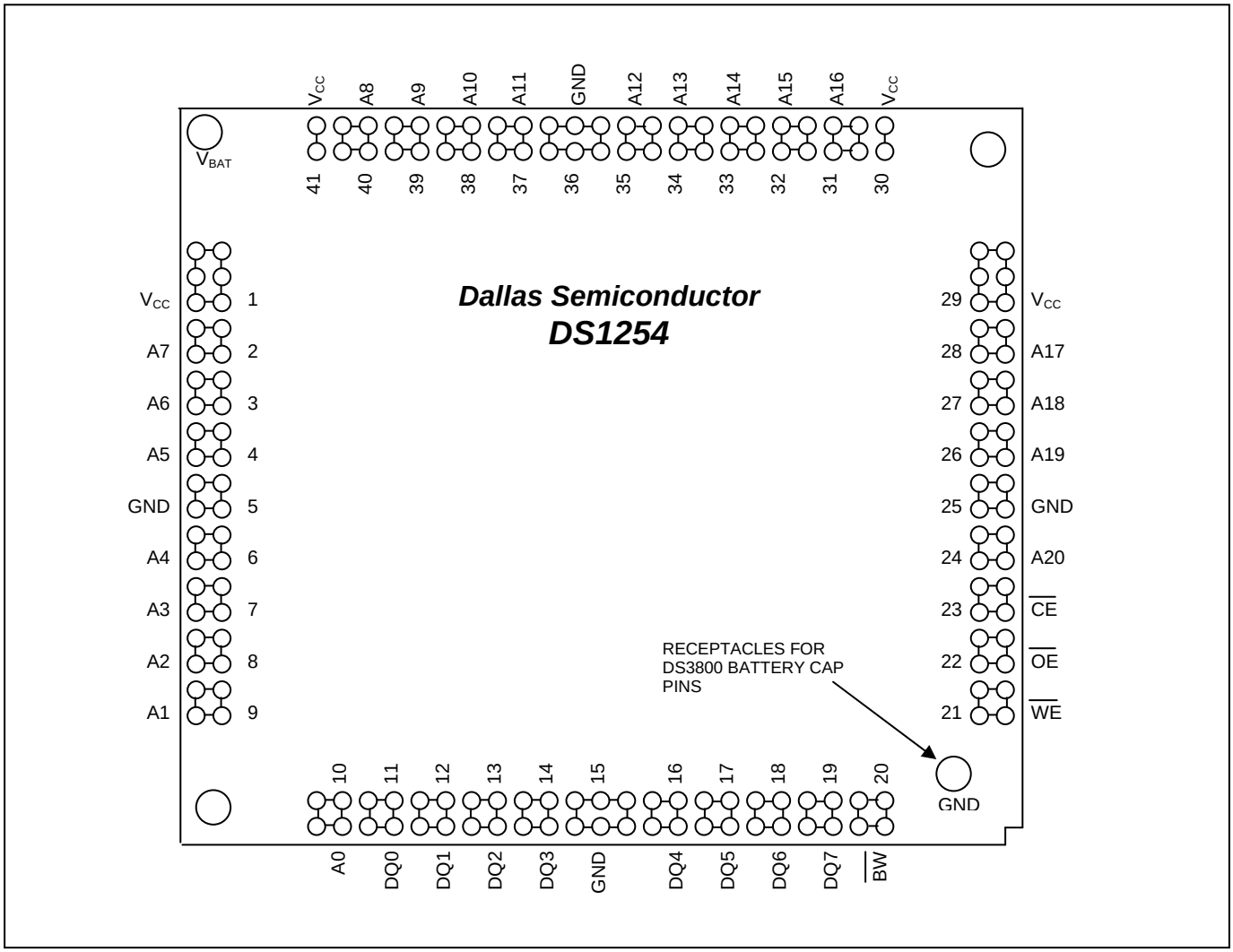
DETAILED DESCRIPTION

The DS1254 is a fully nonvolatile static RAM (NV SRAM) (organized as 2M words by 8 bits) with built-in real-time clock. It has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the DS1254 makes use of an attached DS3800 battery cap to maintain clock information and preserve stored data while protecting that data by disallowing all memory accesses. Additionally, the DS1254 has dedicated circuitry for monitoring the status of an attached DS3800 battery cap.

The phantom clock provides timekeeping information including hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years. The phantom clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

Because the DS1254 has a total of 168 balls and only 35 active signals, balls are wired together into groups, thus providing redundant connections for every signal.

Figure 1. Pin Configuration



RAM READ MODE

The DS1254 executes a read cycle whenever $\overline{WE}$ is inactive (high) and $\overline{CE}$ is active (low). The unique address specified by the 21 address inputs (A0–A20) defines which of the 2MB of data is to be accessed. Valid data will be available to the eight data-output drivers within t_{ACC} (access time) after the last address input is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times and states are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

RAM WRITE MODE

The DS1254 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active (low) state after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The device is fully accessible and data can be written and read only when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below the power-fail point, V_{PF} (point at which write protection occurs), the internal clock registers and SRAM are blocked from any access. When V_{CC} falls below V_{BAT}, device power is switched from the V_{CC} to V_{BAT}. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels. All signals must be powered down when V_{CC} is powered down.

PHANTOM CLOCK OPERATION

Communication with the phantom clock is established by pattern recognition on a serial bit stream of 64 bits that must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses that occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the phantom clock, and memory access is inhibited.

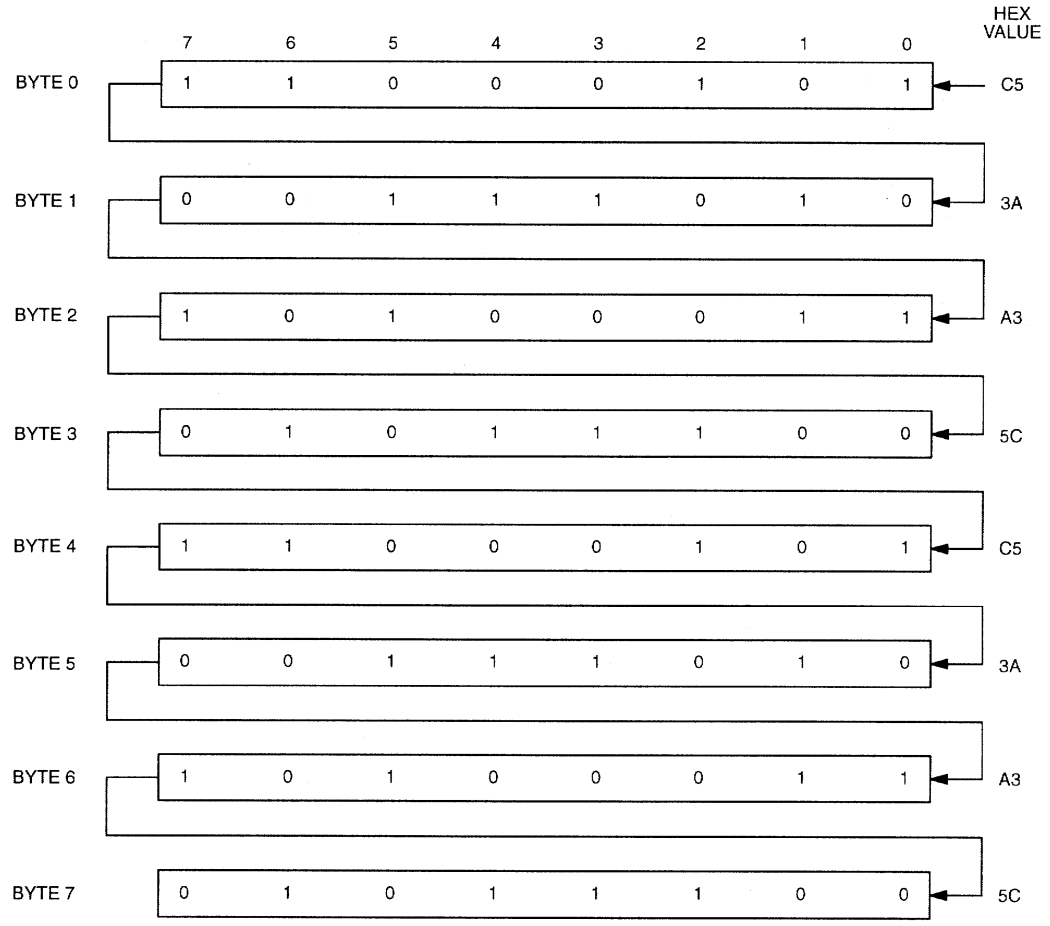
Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable ($\overline{CE}$), output enable ($\overline{OE}$), and write enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the phantom clock starts the pattern-recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ signals of the device. These 64 write cycles are used only to gain access to the phantom clock. Therefore, any address within the first 512kB of memory, (00h to 7FFFFh) is acceptable. However, the write cycles generated to gain access to the phantom clock are also writing data to a location in the memory. The preferred way to manage this requirement is to set aside just one address location in memory as a phantom clock scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 2). With a correct match for 64-bits, the phantom clock is enabled and

data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the phantom clock to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern-recognition sequence or data-transfer sequence to the phantom clock.

PHANTOM CLOCK REGISTER INFORMATION

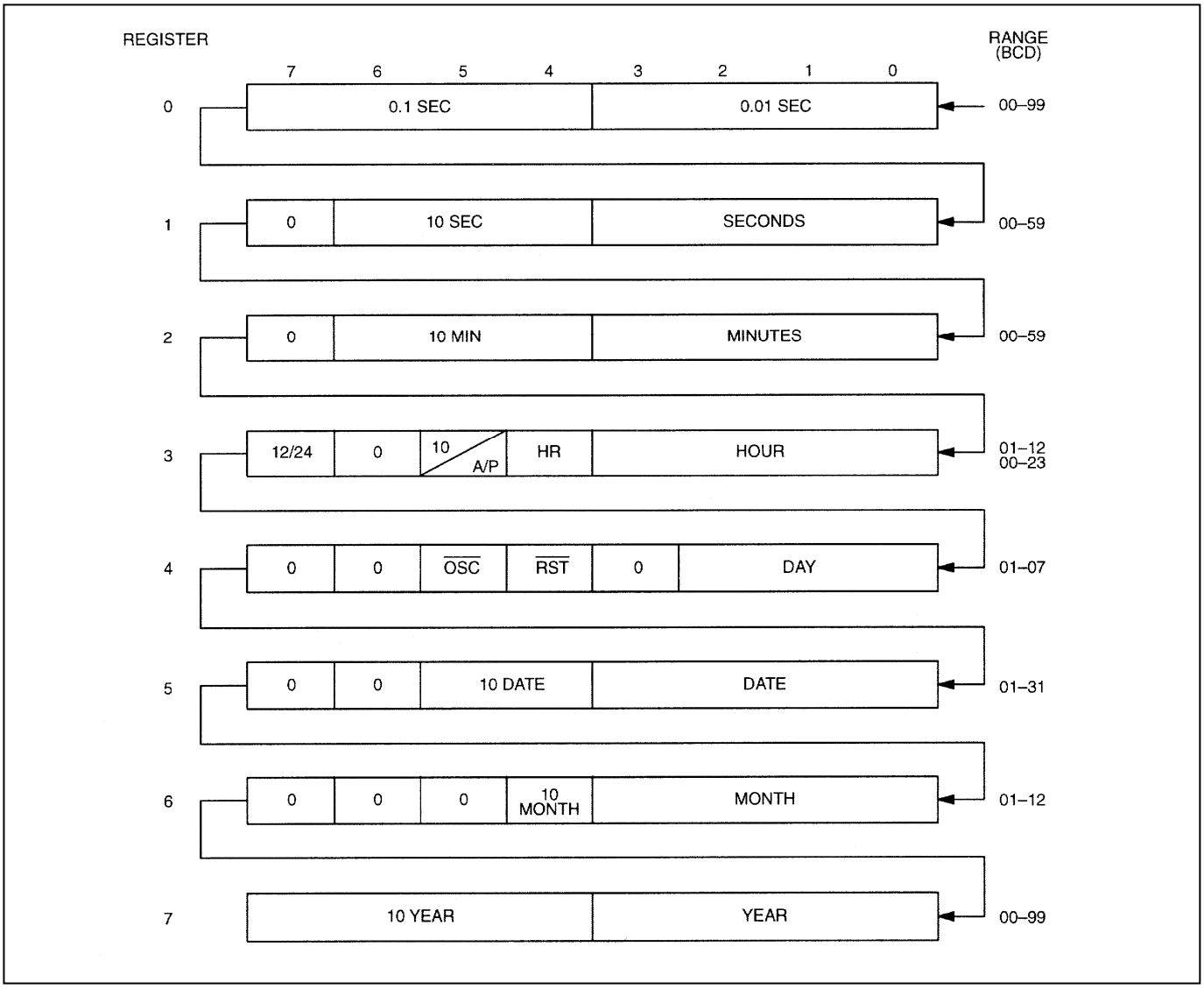
The phantom clock information is contained in eight registers of 8 bits, each of which is sequentially accessed one bit at a time after the 64-bit pattern-recognition sequence has been completed. When updating the phantom clock registers, each register must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 3.

Figure 2. Phantom Clock Protocol Definition



NOTE: THE PATTERN RECOGNITION IN HEX IS C5, 3A, A3, 5C, C5, 3A, A3, 5C. THE ODDS OF THIS PATTERN BEING ACCIDENTALLY DUPLICATED AND CAUSING INADVERTENT ENTRY TO THE PHANTOM CLOCK IS LESS THAN 1 IN 10^{19}. THIS PATTERN IS SENT TO THE PHANTOM CLOCK LSB TO MSB.

Figure 3. Phantom Clock Register Definition



AM/PM/12/24 MODE

Bit 7 of the hours register is defined as the 12-hour or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours).

OSCILLATOR BIT

Bit 5 of the day register controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits that will always read logic 0. When writing these locations, either a logic 1 or logic 0 is acceptable.

BATTERY MONITORING

The DS1254 automatically monitors the battery in an attached DS3800 battery cap on a 24-hour time interval. Such monitoring begins within t_{REC} after V_{CC} rises above V_{PF} and is suspended when power failure occurs.

After each 24-hour period has elapsed, the battery is connected to an internal 1MΩ test resistor for one second. During this one second, if the battery voltage falls below the battery-voltage trip point (~2.6V), the battery warning output $\overline{BW}$ is asserted. Once asserted, $\overline{BW}$ remains active until the attached DS3800 battery cap is replaced. However, the battery is still retested after each V_{CC} power-up, even if it was active on power-down. If the battery voltage is found to be higher than ~2.6V during such testing, $\overline{BW}$ is de-asserted and regular testing resumes. $\overline{BW}$ has an open-drain output driver.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground	-0.3V to +4.6V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-40°C to +70°C
Soldering Temperature	See IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Power-Supply Voltage	V_{CC}		3.0	3.3	3.7	V	1
Logic 1 Voltage (All Inputs)	V_{IH}		2.0		V_{CC} + 0.3	V	1
Logic 0 Voltage (All Inputs)	V_{IL}		-0.3		0.6	V	1

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-4.0		+4.0	µA	
I/O Leakage Current	I_{IO}	-4.0		+4.0	µA	
Output Current at 2.4V	I_{OH}	-1.0			mA	3
Output Current at 0.4V	I_{OL}	2.0			mA	3
Standby Current ($\overline{CE}$ = 2.2V)	I_{CCS1}		5.0	7	mA	
Standby Current ($\overline{CE}$ = V_{CC} - 0.5V)	I_{CCS2}		2.0	3.0	mA	
Operating Current, t_{CYC} = 100ns	I_{CCO1}			50	mA	
Write Protection Voltage	V_{PF}	2.8		2.97	V	1

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance: A0 to A18, $\overline{OE}$, $\overline{WE}$, $\overline{CE}$	C_{IN}		25	50	pF	
Input Capacitance: A19 to A20	C_{IN}		5	10	pF	
I/O Capacitance: DQ0 to DQ7	C_{IO}		25	50	pF	
Output Capacitance: $\overline{BW}$	C_{OUT}		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	150		ns	
Address Access Time	t_{AAC}		150	ns	
$\overline{OE}$ to Output Valid	t_{OE}		75	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150	ns	
$\overline{CE}$ or $\overline{OE}$ to Output Active	t_{COE}	0		ns	2
Output High-Z from Deselection	t_{OD}		70	ns	2
Output Hold from Address Change	t_{OH}	5		ns	
Write Cycle Time	t_{WC}	150		ns	
$\overline{WE}$, $\overline{CE}$ Pulse Width	t_{WP}	100		ns	5
Address Setup Time	t_{AW}	10		ns	
Address Hold Time	t_{AH1}	5		ns	6
	t_{AH2}	25		ns	7
Output High-Z from $\overline{WE}$	t_{ODW}		70	ns	2
Output Active from $\overline{WE}$	t_{OEW}	5		ns	2
Data Setup Time	t_{DS}	60		ns	8
Data Hold Time	t_{DH1}	0		ns	6
	t_{DH2}	20		ns	8
Read Recovery (Clock Access Only)	t_{RR}	20		ns	
Write Recovery (Clock Access Only)	t_{WR}	20		ns	

POWER-UP/POWER-DOWN CHARACTERISTICS

(V_{CC} = 3.3V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ and $\overline{WE}$ at V_{IH} Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Fall Time: $V_{PF(MIN)}$ to V_{BAT}	t_{FB}	10			µs	
V_{CC} Rise Time: 0V to $V_{PF(MIN)}$	t_R	150			µs	
V_{CC} Valid to End of Write Protection	t_{REC}			125	ms	
V_{CC} Valid to $\overline{BW}$ Valid	t_{BPU}			1	s	3

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data-Retention Time (Oscillator On)	t_{DR}	10			years	4

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

BATTERY WARNING TIMING

(V_{CC} = 3.3V ±10%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Test Cycle	t_{BTC}		24		hour	
Battery Test Pulse Width	t_{BTPW}			1	seconds	
Battery Test to $\overline{BW}$ Active	t_{BW}			1	seconds	
V_{CC} Valid to $\overline{BW}$ Valid	t_{BPU}			1	seconds	3

AC TEST CONDITIONS

Output Load: 100pF + 1 TTL Gate
Input Pulse Levels: 0V to 3.0V
Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

Figure 4. Memory Read Cycle Timing (Note 9)

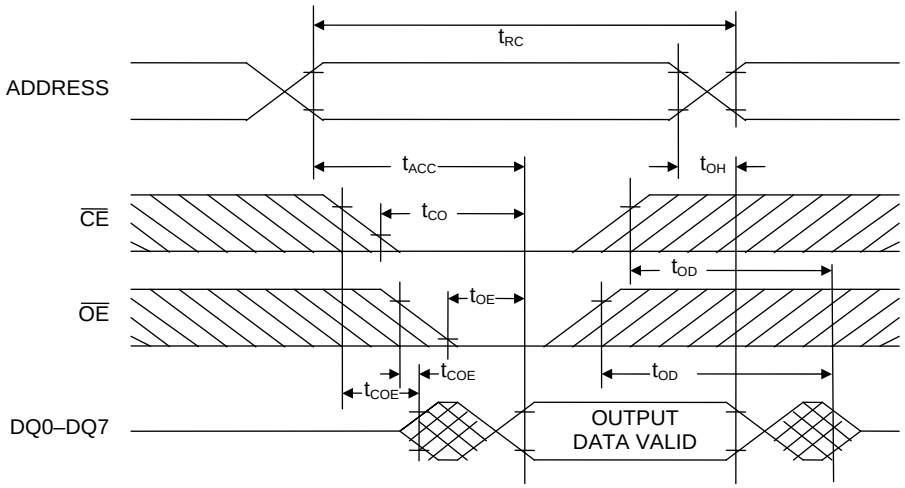


Figure 5. Memory Write Cycle Timing, Write-Enable Controlled (Notes 5, 6, 8, 10, 11, 12, and 13)

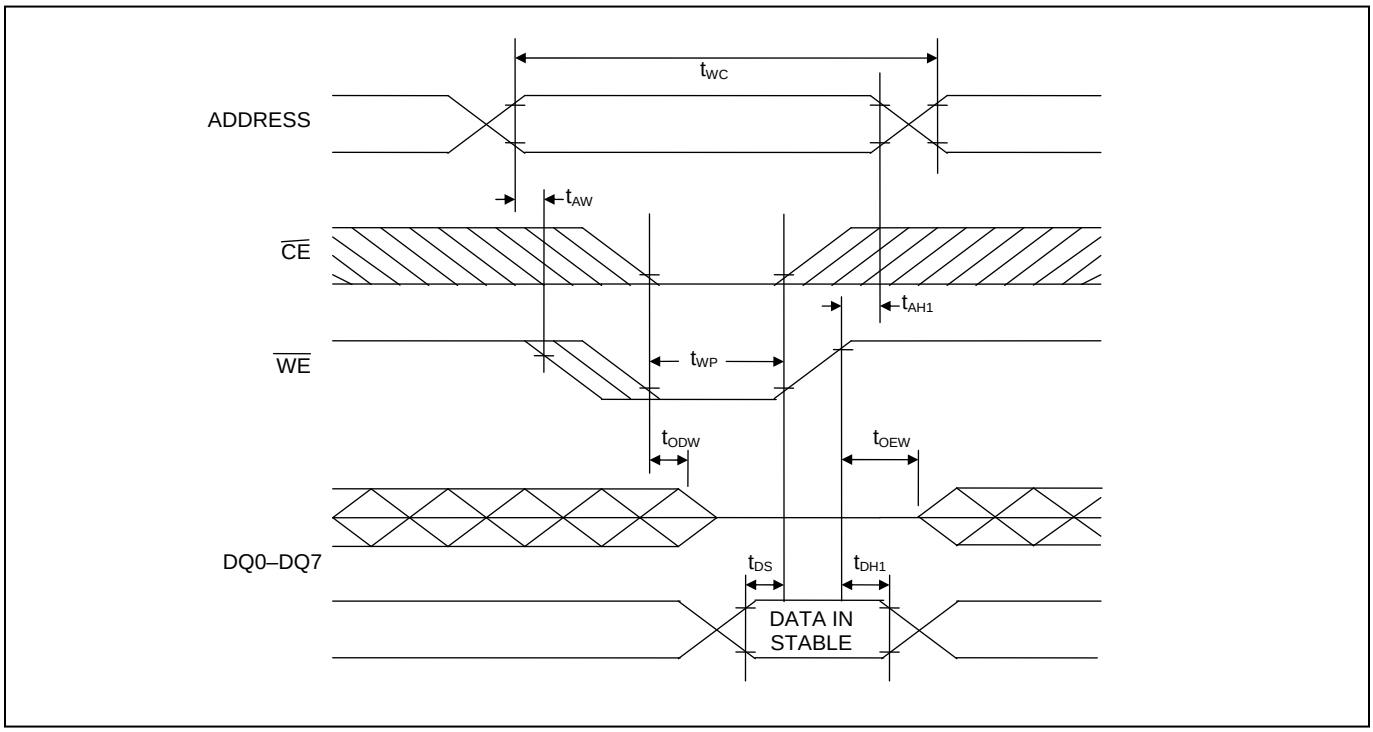


Figure 6. Memory Write Cycle Timing, Chip-Enable Controlled (Notes 5, 7, 8, 10, 11, 12, and 13)

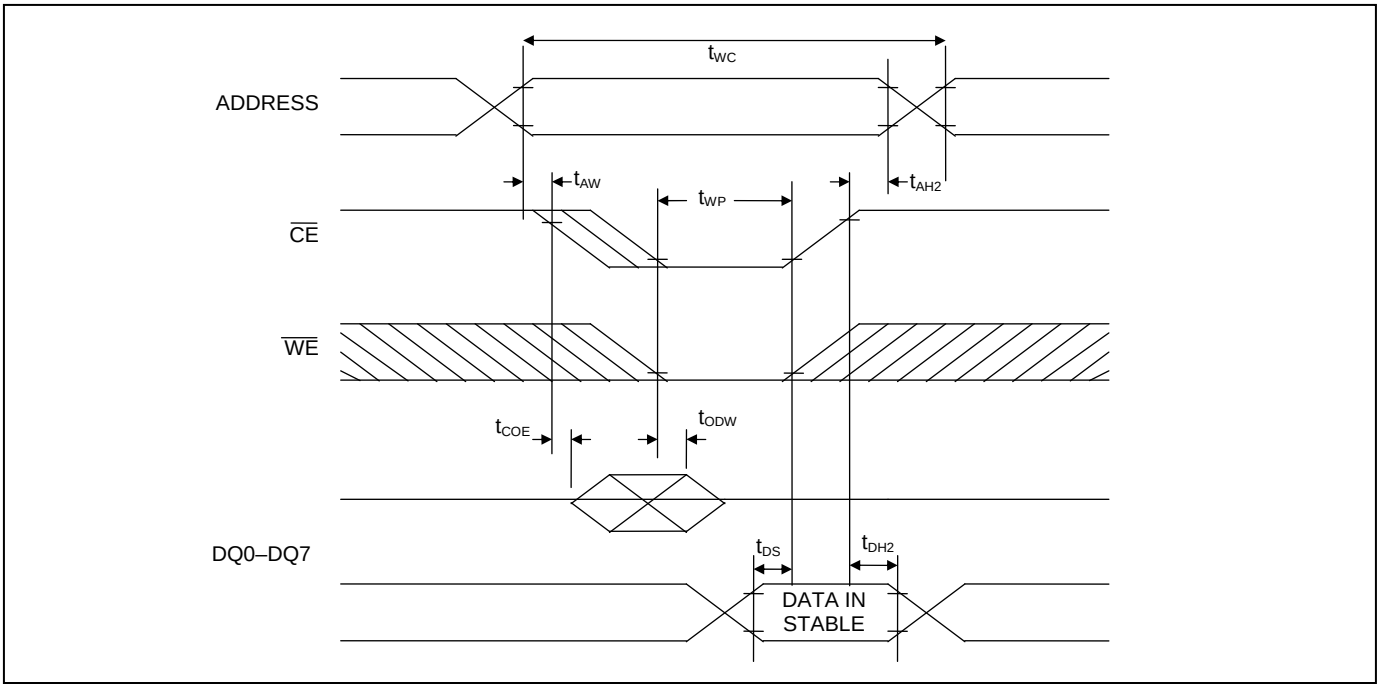


Figure 7. Read Cycle to Phantom Clock

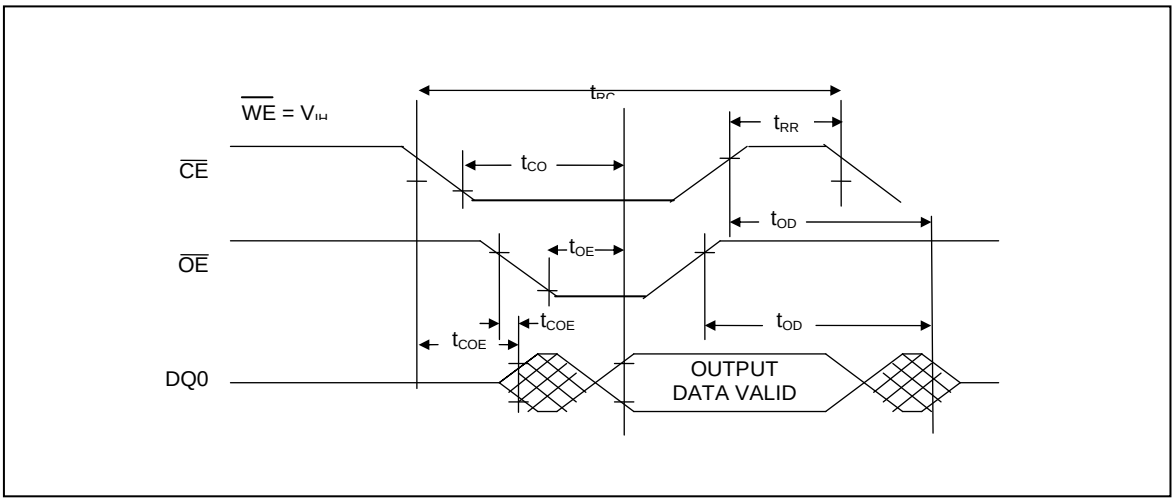


Figure 8. Write Cycle to Phantom Clock

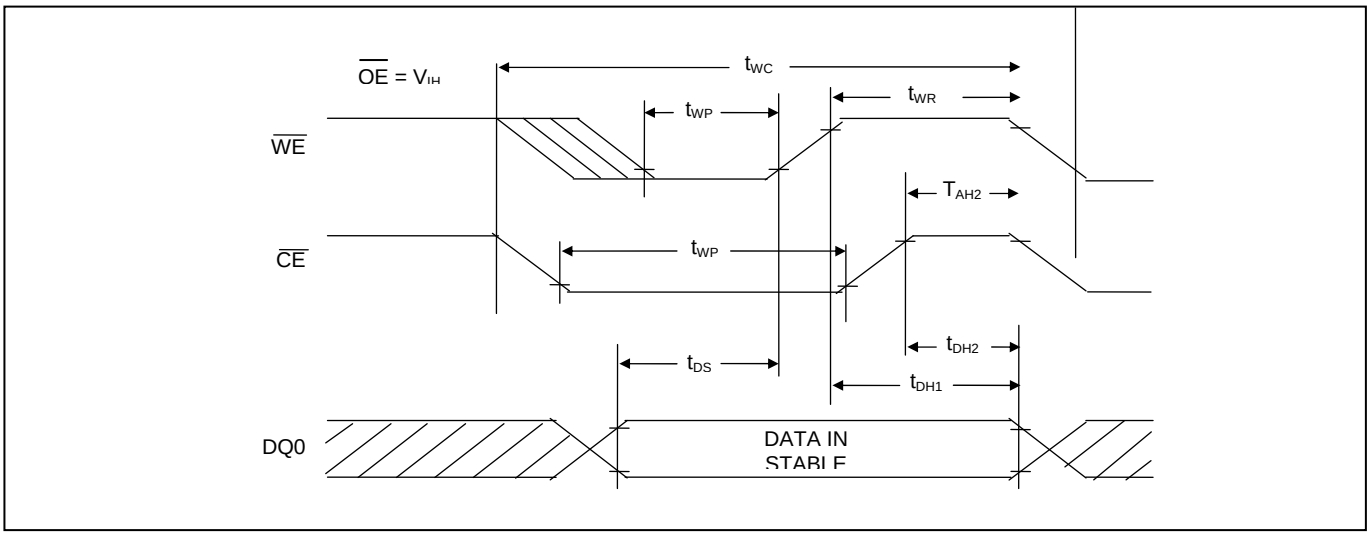


Figure 9. Power-Up/Power-Down Waveform Timing (Note 14)

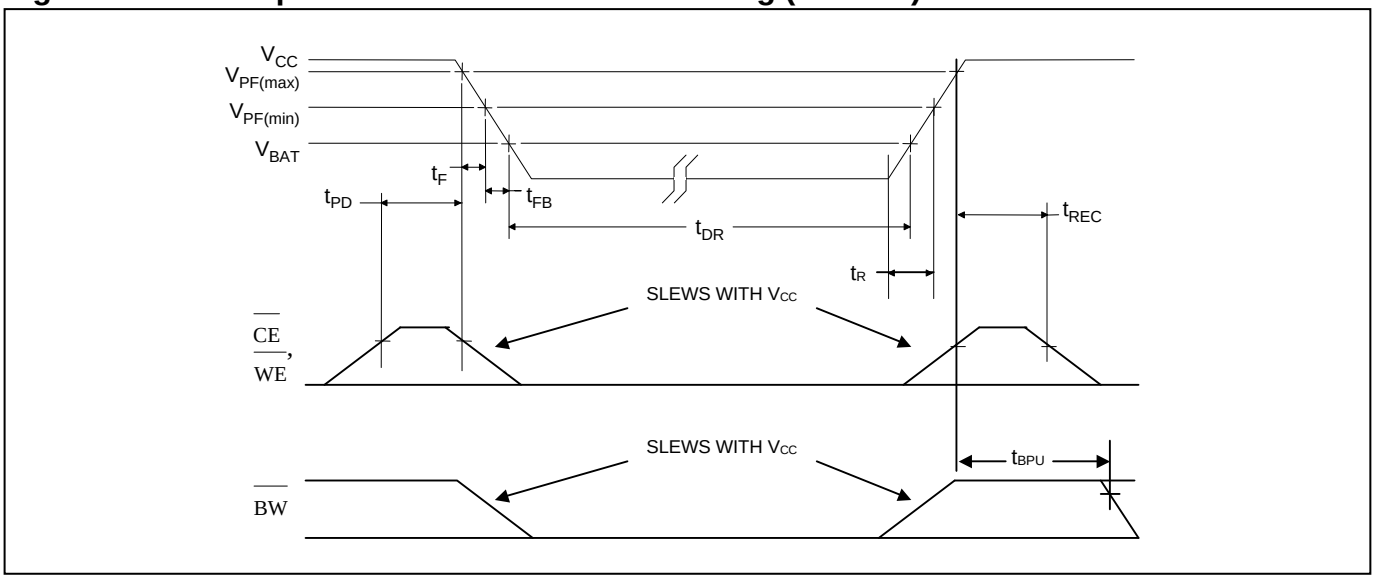
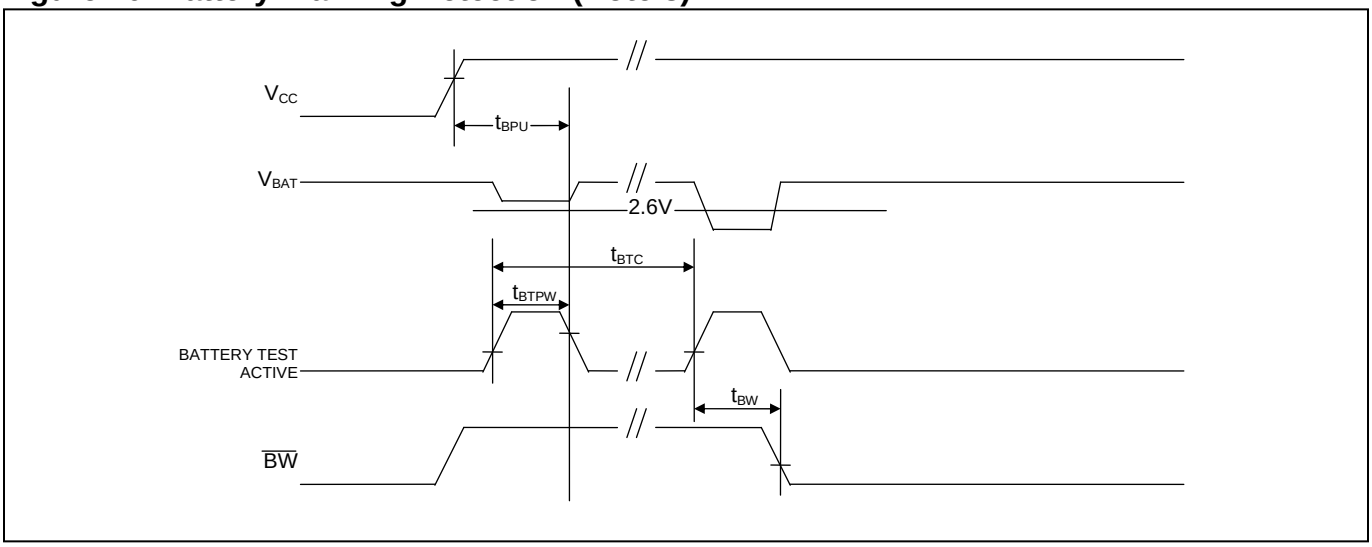


Figure 10. Battery Warning Detection (Note 3)

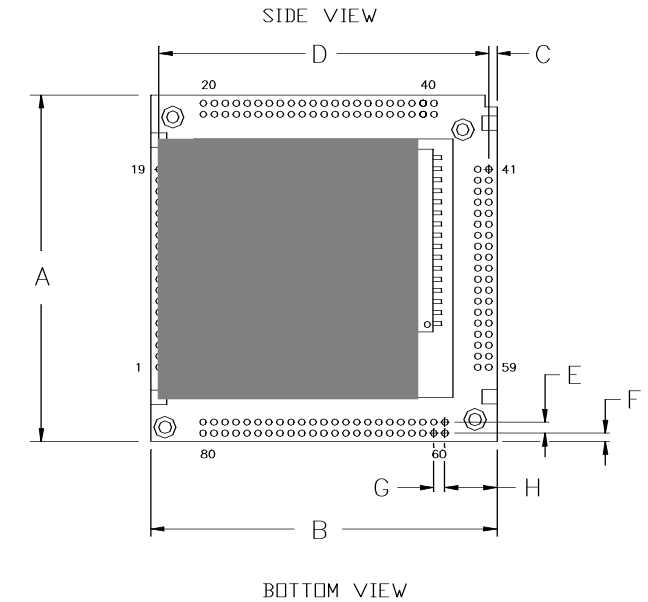


NOTES:

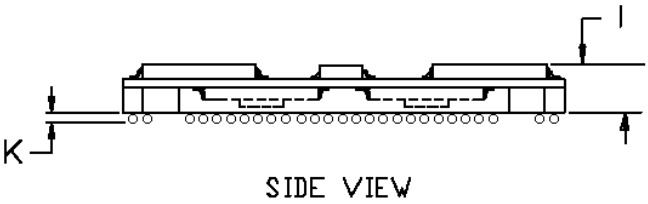
1) Voltage referenced to ground.
2) These parameters are sampled with a 50pF load and are not 100% tested.
3) $\overline{BW}$ is an open-drain output and, as such, cannot source current. An external pullup resistor should be connected to this pin for proper operation. $\overline{BW}$ can sink 10mA.
4) The DS3800 battery cap is a one-time use part, but can be removed and replaced. By design, DS3800 removal will mechanically damage the battery cap, which eliminates the accidental use of a previously attached and possibly low-capacity battery cap.
5) t_{WP} specified as the logical AND of $\overline{CE}$ and $\overline{WE}$, t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
6) t_{AH1}, t_{DH1} are measured from $\overline{WE}$ going high.
7) t_{AH2}, t_{DH2} are measured from $\overline{CE}$ going high.
8) t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
9) $\overline{WE}$ is high for a read cycle.
10) $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high-impedance state.
11) If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in a write-enable-controlled write cycle, the output buffers remain in a high-impedance state during this period.
12) If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high-impedance state during this period.
13) If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high-impedance state during this period.
14) In a power-down condition, the voltage on any pin cannot exceed the voltage on V_{CC}.

PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



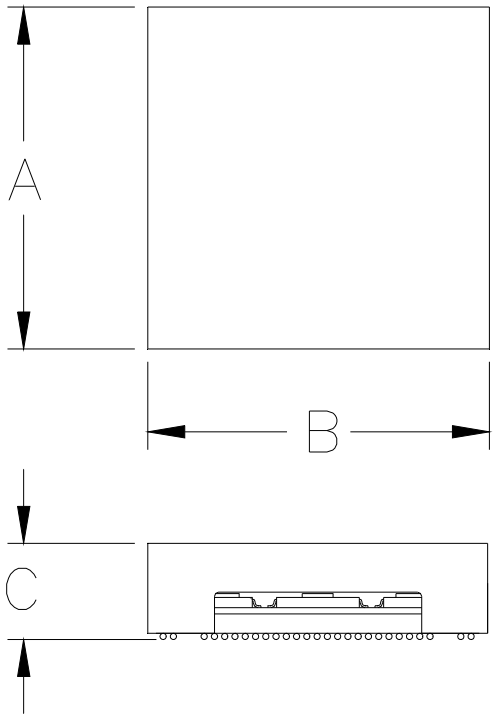
PKG		MIN	MAX
A	IN	1.570	1.580
	MM	39.88	40.13
B	IN	1.570	1.580
	MM	39.88	40.13
C	IN	0.033	0.043
	MM	0.84	1.09
D	IN	1.497	1.503
	MM	38.02	38.18
E	IN	0.047	0.053
	MM	1.19	1.35
F	IN	0.033	0.043
	MM	0.84	1.09
G	IN	0.047	0.053
	MM	1.19	1.35
H	IN	0.234	0.240
	MM	5.94	6.10
I	IN	0.160	0.200
	MM	4.00	5.10
K	IN	0.025	0.032
	MM	0.64	0.82



PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

DS1254 with Attached DS3800 Battery Cap



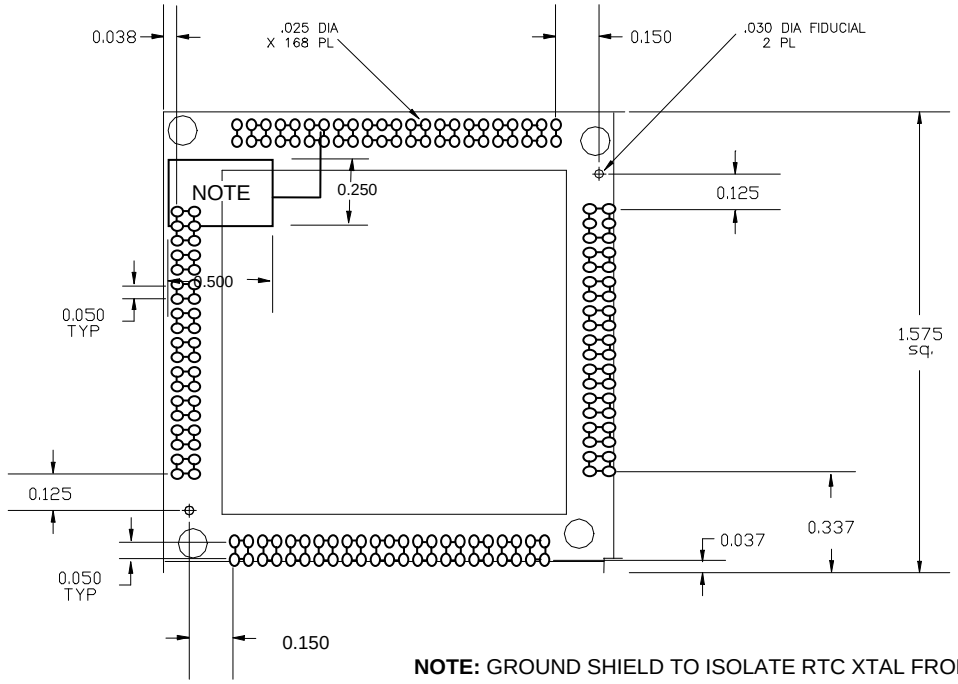
PKG		MIN	MAX
A	IN	1.656	1.668
	MM	42.06	42.37
B	IN	1.656	1.668
	MM	42.06	42.37
C	IN	—	0.485
	MM	—	12.32

PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

Recommended Land Pattern (with Overlaid Package Outline)

The DS1254 BGA is a subset of the industry-standard 40mm BGA format, with all balls on a 50-mil grid. Corner balls have been removed to provide space for the electrical and mechanical interface features that facilitate attachment of the DS3800 battery cap.



NOTE: GROUND SHIELD TO ISOLATE RTC XTAL FROM EMI.

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
5/09	Changed t_{AWMIN} = 0ns to t_{AWMIN} = 10ns in the *Electrical Characteristics* table.	8, 9
12/09	Removed the DS1254YB ordering information and 5V operational characteristics.	1, 7–10

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