Analog Devices

Dual, 12-/14-/16-Bit *nano*DACs® with 5 ppm/°C On-Chip Reference, I²C® Interface

AD5627R/AD5647R/AD5667R, AD5627/AD5667

FEATURES

Low power, smallest pin-compatible, dual *nano*DACs
AD5627R/AD5647R/AD5667R
- **12-/14-/16-bit**
- **On-chip 1.25 V/2.5 V, 5 ppm/°C reference**

AD5627/AD5667
- **12-/16-bit**
- **External reference only**

3 mm x 3 mm LFCSP and 10-lead MSOP
2.7 V to 5.5 V power supply
Guaranteed monotonic by design
Power-on reset to zero scale
Per channel power-down
Hardware $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ functions
I²C-compatible serial interface supports standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) modes

APPLICATIONS

Process control
Data acquisition systems
Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators

FUNCTIONAL BLOCK DIAGRAMS

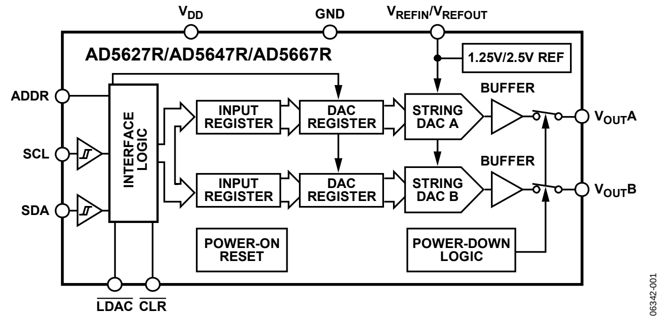

Figure 1. AD5627R/AD5647R/AD5667R

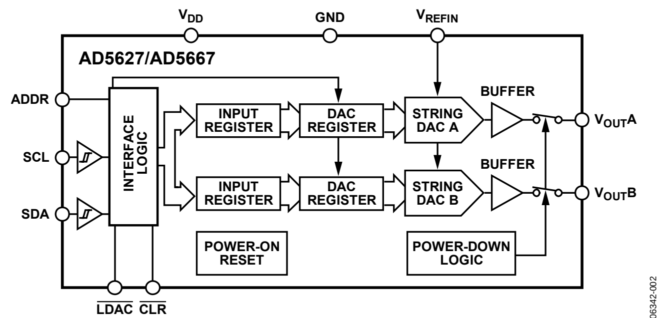

Figure 2. AD5627/AD5667

GENERAL DESCRIPTION

The AD5627R/AD5647R/AD5667R, AD5627/AD5667 members of the *nano*DAC family are low power, dual, 12-, 14-, 16-bit buffered voltage-out DACs with/without on-chip reference. All devices operate from a single 2.7 V to 5.5 V supply, are guaranteed monotonic by design, and have an I²C-compatible serial interface.

The AD5627R/AD5647R/AD5667R have an on-chip reference. The AD56x7RBCPZ have a 1.25 V, 5 ppm/°C reference, giving a full-scale output range of 2.5 V; the AD56x7RBRMZ have a 2.5 V, 5 ppm/°C reference, giving a full-scale output range of 5 V. The on-chip reference is off at power-up, allowing the use of an external reference. The internal reference is enabled via a software write. The AD5667 and AD5627 require an external reference voltage to set the output range of the DAC.

The AD56x7R/AD56x7 incorporate a power-on reset circuit that ensures the DAC output powers up to 0 V, and remains there until a valid write takes place. The part contains a per-channel power-down feature that reduces the current consumption of the device to 480 nA at 5 V and provides software-selectable output loads while in power-down mode. The low power consumption of this part in normal operation makes it ideally suited to portable battery-operated equipment. The on-chip precision output amplifier enables rail-to-rail output swing.

The AD56x7R/AD56x7 use a 2-wire I²C-compatible serial interface that operates in standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) modes.

Table 1. Related Devices

Part No.	Description
AD5663	2.7 V to 5.5 V, dual 16-bit DAC, external reference, SPI® interface
AD5623R/AD5643R/AD5663R	2.7 V to 5.5 V, dual 12-, 14-, 16-bit DACs, internal reference, SPI interface
AD5625R/AD5645R/AD5665R, AD5625/AD5665	2.7 V to 5.5 V, quad 12-, 14-, 16-bit DACs, with/without internal reference, I²C interface

Rev. 0

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REVISION HISTORY

1/07—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; V_{REFIN} = V_{DD}; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Conditions/Comments[1]
STATIC PERFORMANCE[2]					
AD5667R/AD5667					
Resolution	16			Bits	
Relative Accuracy		±8	±12	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic by design
AD5647R					
Resolution	14			Bits	
Relative Accuracy		±2	±4	LSB	
Differential Nonlinearity			±0.5	LSB	Guaranteed monotonic by design
AD5627R/AD5627					
Resolution	12			Bits	
Relative Accuracy		±0.5	±1	LSB	
Differential Nonlinearity			±0.25	LSB	Guaranteed monotonic by design
Zero-Code Error		2	10	mV	All 0s loaded to DAC register
Offset Error		±1	±10	mV	
Full-Scale Error		−0.1	±1	% of FSR	All 1s loaded to DAC register
Gain Error			±1.5	% of FSR	
Zero-Code Error Drift		±2		μV/°C	
Gain Temperature Coefficient		±2.5		ppm	Of FSR/°C
DC Power Supply Rejection Ratio		−100		dB	DAC code = midscale ; V_{DD} = 5 V ± 10%
DC Crosstalk (External Reference)		15		μV	Due to full-scale output change, R_L = 2 kΩ to GND or 2 kΩ to V_{DD}
		10		μV/mA	Due to load current change
		8		μV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25		μV	Due to full-scale output change, R_L = 2 kΩ to GND or 2 kΩ to V_{DD}
		20		μV/mA	Due to load current change
		10		μV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Capacitive Load Stability		2		nF	R_L = ∞
		10		nF	R_L = 2 kΩ
DC Output Impedance		0.5		Ω	
Short-Circuit Current		30		mA	V_{DD} = 5 V
Power-Up Time		4		μs	Coming out of power-down mode; V_{DD} = 5 V
REFERENCE INPUTS					
Reference Current		110	130	μA	V_{REF} = V_{DD} = 5.5 V
Reference Input Range	0.75		V_{DD}	V	
Reference Input Impedance		50		kΩ	
REFERENCE OUTPUT (LFCSP_WD PACKAGE)					
Output Voltage	1.247		1.253	V	At ambient
Reference TC[3]		±10		ppm/°C	
Output Impedance		7.5		kΩ	
REFERENCE OUTPUT (MSOP PACKAGE)					
Output Voltage	2.495		2.505	V	At ambient
Reference TC[3]		±5	±10	ppm/°C	
Output Impedance		7.5		kΩ	

Parameter	Min	Typ	Max	Unit	Conditions/Comments[1]
LOGIC INPUTS (ADDR, $\overline{CLR}$, $\overline{LDAC}$)[3]					
I_{IN}, Input Current			±1	μA	
V_{INL}, Input Low Voltage			$0.15 \times V_{DD}$	V	
V_{INH}, Input High Voltage	$0.85 \times V_{DD}$			V	
C_{IN}, Pin Capacitance		2		pF	ADDR
		20		pF	$\overline{CLR}$, $\overline{LDAC}$
V_{HYST}, Input Hysteresis	$0.1 \times V_{DD}$			V	
LOGIC INPUTS (SDA, SCL)					
I_{IN}, Input Current			±1	μA	
V_{INL}, Input Low Voltage			$0.3 \times V_{DD}$	V	
V_{INH}, Input High Voltage	$0.7 \times V_{DD}$			V	
C_{IN}, Pin Capacitance		2		pF	
V_{HYST}, Input Hysteresis	$0.1 \times V_{DD}$			V	
LOGIC OUTPUTS (OPEN-DRAIN)					
V_{OL}, Output Low Voltage			0.4	V	$I_{SINK} = 3$ mA
			0.6	V	$I_{SINK} = 6$ mA
Floating-State Leakage Current			±1	μA	
Floating-State Output Capacitance		2		pF	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD} (Normal Mode)[4]					$V_{IH} = V_{DD}$, $V_{IL} = GND$
$V_{DD} = 4.5$ V to 5.5 V		0.4	0.5	mA	Internal reference off
$V_{DD} = 2.7$ V to 3.6 V		0.35	0.45	mA	Internal reference off
$V_{DD} = 4.5$ V to 5.5 V		0.95	1.15	mA	Internal reference on
$V_{DD} = 2.7$ V to 3.6 V		0.8	0.95	mA	Internal reference on
I_{DD} (All Power-Down Modes)[5]		0.48	1	μA	$V_{IH} = V_{DD}$, $V_{IL} = GND$

[1] Temperature range: B grade: −40°C to +105°C.
[2] Linearity calculated using a reduced code range: AD5567R/AD5667 (Code 512 to Code 65,024); AD5647R (Code 128 to Code 16,256); AD5627R/AD5627 (Code 32 to Code 4064). Output unloaded.
[3] Guaranteed by design and characterization, not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All DACs powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; V_{REFIN} = V_{DD}; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 3.

Parameter[2]	Min	Typ	Max	Unit	Conditions/Comments[3]
Output Voltage Settling Time					
AD5627R/AD5627		3	4.5	µs	¼ to ¾ scale settling to ±0.5 LSB
AD5647R		3.5	5	µs	¼ to ¾ scale settling to ±0.5 LSB
AD5667R/AD5667		4	7	µs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		1.8		V/µs	
Digital-to-Analog Glitch Impulse		15		nV-s	1 LSB change around major carry transition
Digital Feedthrough		0.1		nV-s	
Reference Feedthrough		−90		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency 10 Hz to 20 MHz
Digital Crosstalk		0.1		nV-s	
Analog Crosstalk		1		nV-s	External reference
		4		nV-s	Internal reference
DAC-to-DAC Crosstalk		1		nV-s	External reference
		4		nV-s	Internal reference
Multiplying Bandwidth		340		kHz	V_{REF} = 2 V ± 0.1 V p-p
Total Harmonic Distortion		−80		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 kHz
Output Noise Spectral Density		120		nV/√Hz	DAC code = midscale, 1 kHz
		100		nV/√Hz	DAC code = midscale, 10 kHz
Output Noise		15		µV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization, not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to +105°C, typical @ 25°C.

I²C TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, f_{SCL} = 3.4 MHz, unless otherwise noted.[1]

Table 4.

Parameter	Conditions[2]	Min	Max	Unit	Description
f_{SCL}[3]	Standard mode		100	kHz	Serial clock frequency
	Fast mode		400	kHz	
	High speed mode, C_B = 100 pF		3.4	MHz	
	High speed mode, C_B = 400 pF		1.7	MHz	
t_1	Standard mode	4		µs	t_{HIGH}, SCL high time
	Fast mode	0.6		µs	
	High speed mode, C_B = 100 pF	60		ns	
	High speed mode, C_B = 400 pF	120		ns	
t_2	Standard mode	4.7		µs	t_{LOW}, SCL low time
	Fast mode	1.3		µs	
	High speed mode, C_B = 100 pF	160		ns	
	High speed mode, C_B = 400 pF	320		ns	
t_3	Standard mode	250		ns	$t_{SU;DAT}$, data setup time
	Fast mode	100		ns	
	High speed mode	10		ns	
t_4	Standard mode	0	3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0	0.9	µs	
	High speed mode, C_B = 100 pF	0	70	ns	
	High speed mode, C_B = 400 pF	0	150	ns	
t_5	Standard mode	4.7		µs	$t_{SU;STA,}$ setup time for a repeated start condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_6	Standard mode	4		µs	$t_{HD;STA}$, hold time (repeated) start condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_7	Standard mode	4.7		µs	t_{BUF}, bus free time between a stop and a start condition
	Fast mode	1.3		µs	
t_8	Standard mode	4		µs	$t_{SU;STO}$, setup time for a stop condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_9	Standard mode		1000	ns	t_{RDA}, rise time of SDA signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	
t_{10}	Standard mode		300	ns	t_{FDA}, fall time of SDA signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	
t_{11}	Standard mode		1000	ns	t_{RCL}, rise time of SCL signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	40	ns	
	High speed mode, C_B = 400 pF	20	80	ns	
t_{11A}	Standard mode		1000	ns	t_{RCL1}, rise time of SCL signal after a repeated start condition and after an acknowledge bit
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	

Parameter	Conditions[2]	Min	Max	Unit	Description
t_{12}	Standard mode		300	ns	t_{FCL}, fall time of SCL signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	40	ns	
	High speed mode, C_B = 400 pF	20	80	ns	
t_{13}	Standard mode	10		ns	$\overline{\text{LDAC}}$ pulse width low
	Fast mode	10		ns	
	High speed mode	10		ns	
t_{14}	Standard mode	300		ns	Falling edge of 9th SCL clock pulse of last byte of valid write to $\overline{\text{LDAC}}$ falling edge
	Fast mode	300		ns	
	High speed mode	30		ns	
t_{15}	Standard mode	20		ns	$\overline{\text{CLR}}$ pulse width low
	Fast mode	20		ns	
	High speed mode	20		ns	
t_{SP}[4]	Fast mode	0	50	ns	Pulse width of spike suppressed
	High speed mode	0	10	ns	

[1] See Figure 3. High speed mode timing specification applies only to the AD5627RBRMZ-2/AD5627BRMZ-2REEL7 and AD5667RBRMZ-2/AD5667BRMZ-2REEL7.
[2] CB refers to the capacitance on the bus line.
[3] The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate but has a negative effect on EMC behavior of the part.
[4] Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns for fast mode or 10 ns for high speed mode.

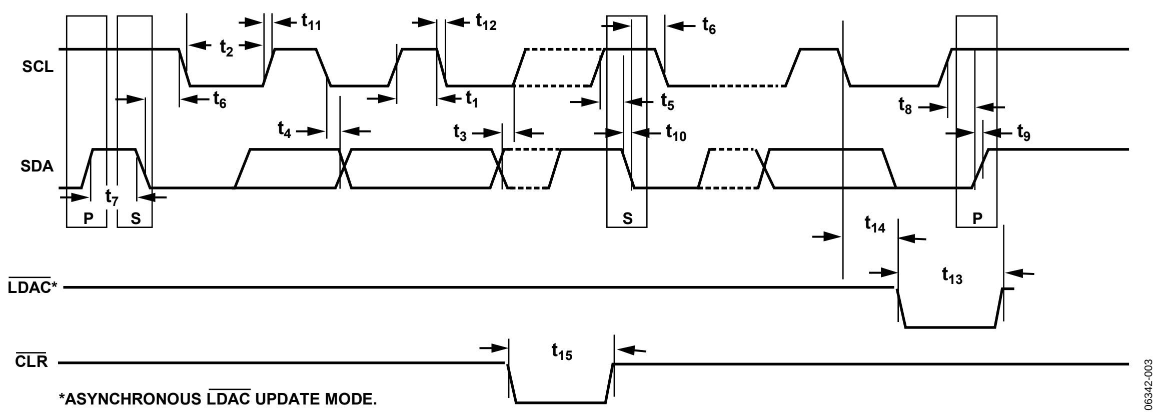


Figure 3. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REFIN}/V_{REFOUT} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range, Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J maximum)	150°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
θ_{JA} Thermal Impedance	
LFCSP_WD Package (4-Layer Board)	61°C/W
MSOP Package	150.4°C/W
Reflow Soldering Peak Temperature, Pb-Free	260°C ± 5°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

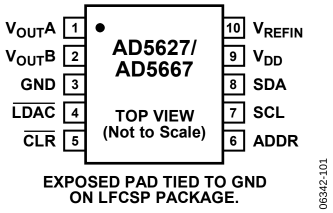


Figure 4. AD5627/AD5667 Pin Configuration

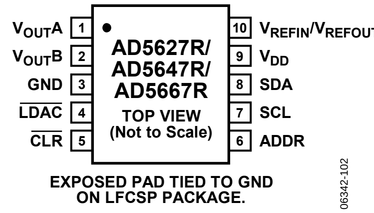


Figure 5. AD5627R/AD5647R/AD5667R Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
2	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
3	GND	Ground reference point for all circuitry on the part.
4	$\overline{\text{LDAC}}$	Pulsing this pin low allows any or all DAC registers to be updated if the inputs have new data. This allows simultaneous updates of all DAC outputs. Alternatively, this pin can be tied permanently low.
5	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling-edge sensitive. While $\overline{\text{CLR}}$ is low, all LDAC pulses are ignored. When $\overline{\text{CLR}}$ is activated, zero scale is loaded to all input and DAC registers. This clears the output to 0 V. The part exits clear code mode on the falling edge of the 9^{th} clock pulse of the last byte of valid write. If $\overline{\text{CLR}}$ is activated during a write sequence, the write is aborted. If $\overline{\text{CLR}}$ is activated during high speed mode the part will exit high speed mode.
6	ADDR	Three-State Address Input. Sets the two least significant bits (Bit A1, Bit A0) of the 7-bit slave address.
7	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into or out of the 24-bit input register.
8	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into or out of the 24-bit input register. It is a bidirectional, open-drain data line that should be pulled to the supply with an external pull-up resistor.
9	V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 μF capacitor in parallel with a 0.1 μF capacitor to GND.
10	V_{REFIN}/V_{REFOUT}	The AD56x7R have a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input. (The internal reference and reference output are only available on R suffix versions.) The AD56x7 has a reference input pin only.

TYPICAL PERFORMANCE CHARACTERISTICS

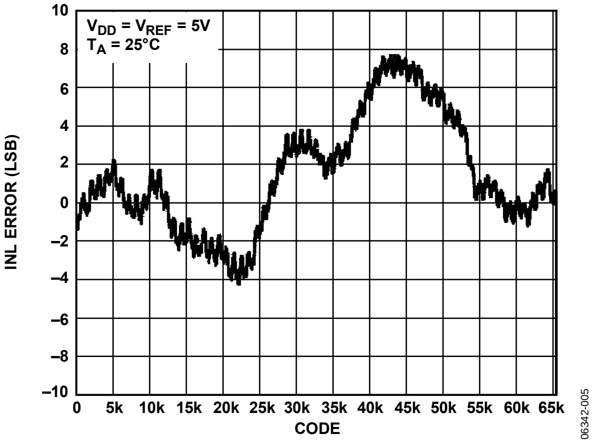


Figure 6. AD5667 INL, External Reference

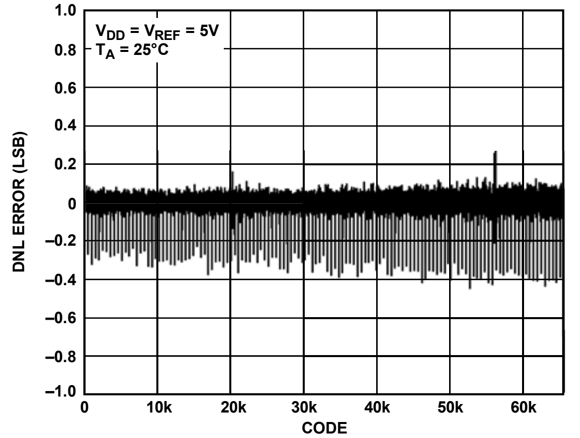


Figure 9. AD5667 DNL, External Reference

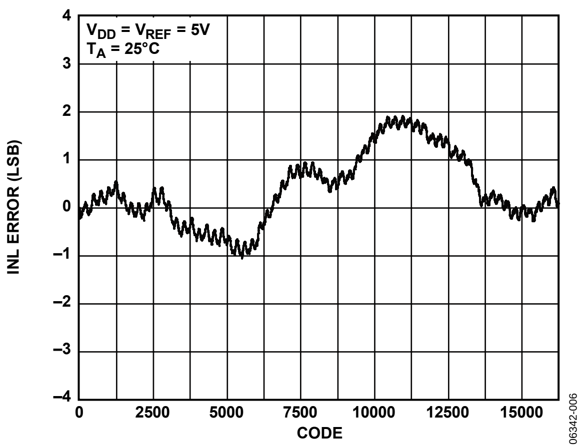


Figure 7. AD5647R INL, External Reference

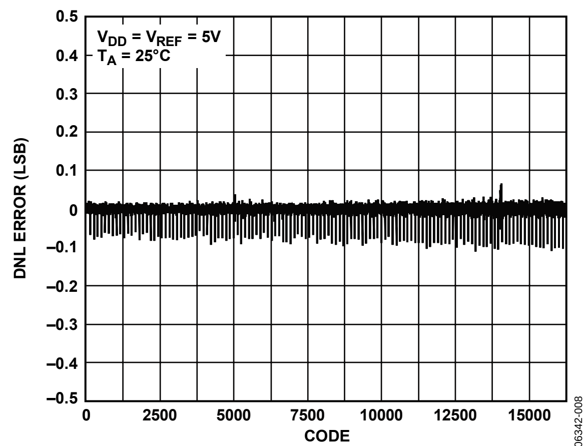


Figure 10. DNL AD5647R, External Reference

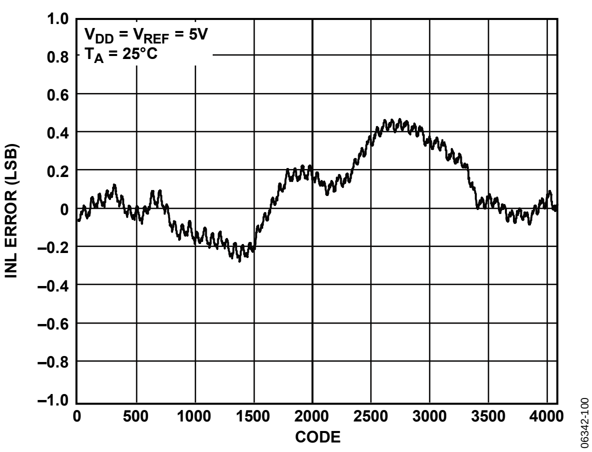


Figure 8. AD5627 INL, External Reference

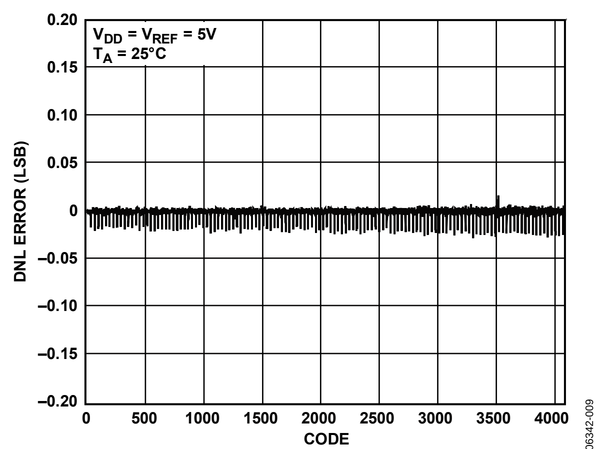


Figure 11. AD5627 DNL, External Reference

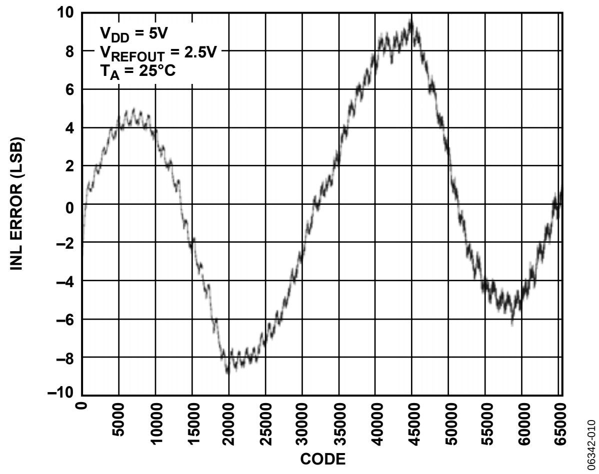


Figure 12. AD5667R INL, 2.5 V Internal Reference

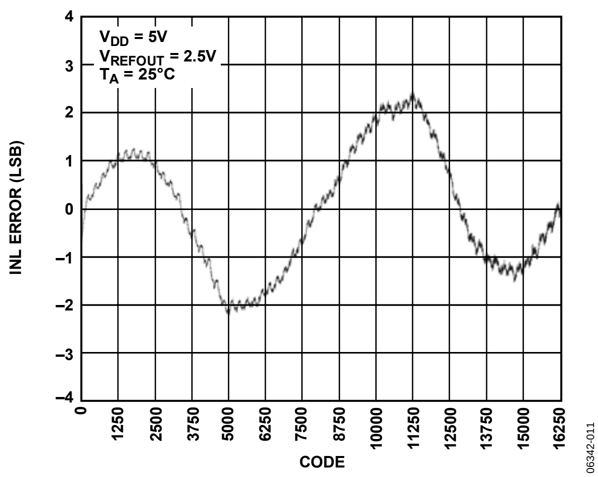


Figure 13. AD5647R INL, 2.5 V Internal Reference

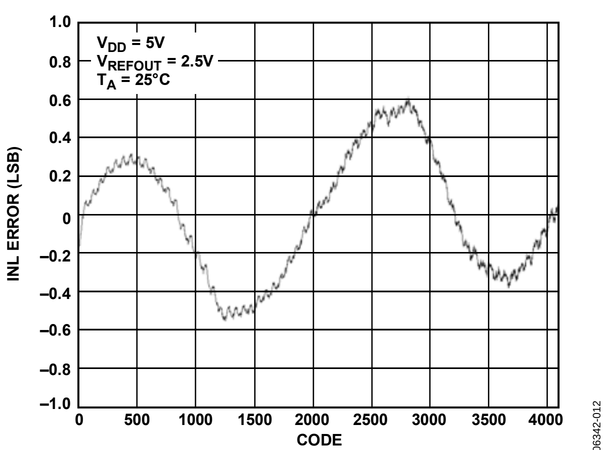


Figure 14. AD5627R INL, 2.5 V Internal Reference

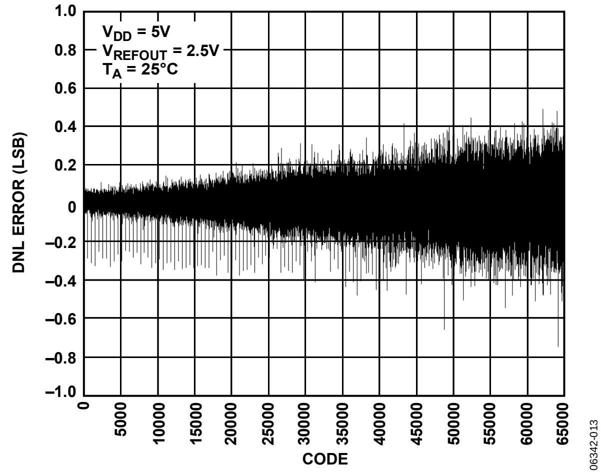


Figure 15. AD5667R DNL, 2.5 V Internal Reference

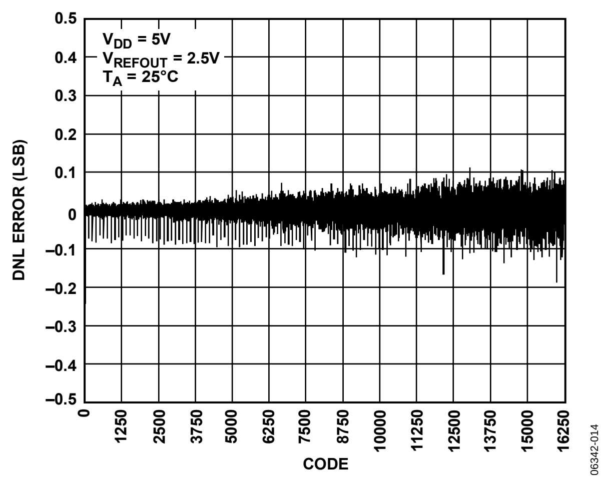


Figure 16. AD5647R DNL, 2.5 V Internal Reference

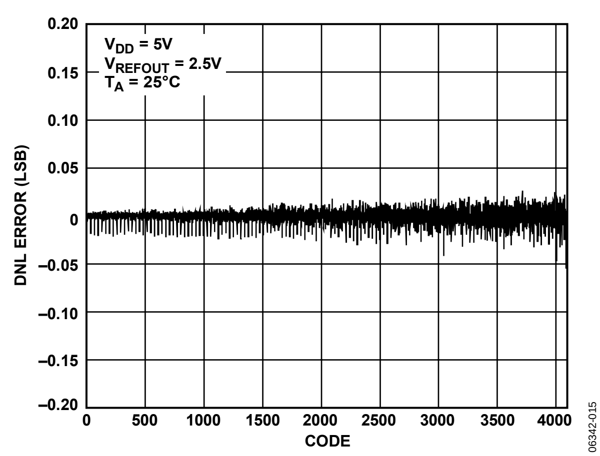


Figure 17. AD5627R DNL, 2.5 V Internal Reference

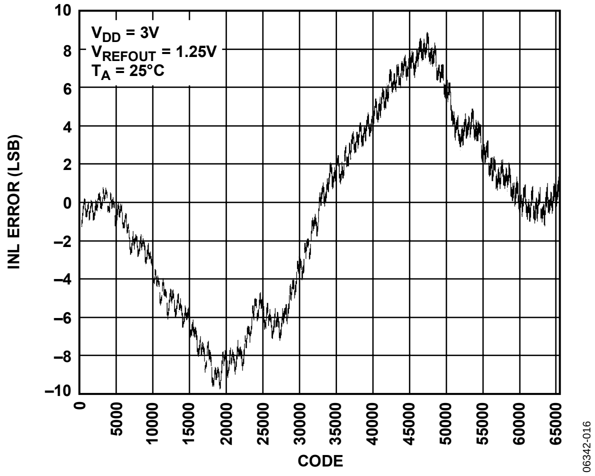


Figure 18. AD5667R INL,1.25 V Internal Reference

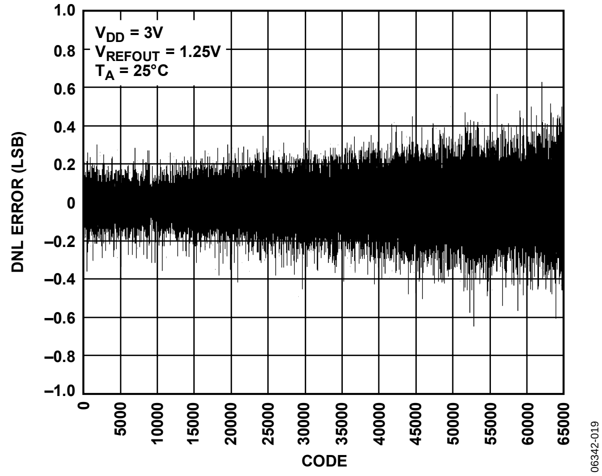


Figure 21. AD5667R DNL,1.25 V Internal Reference

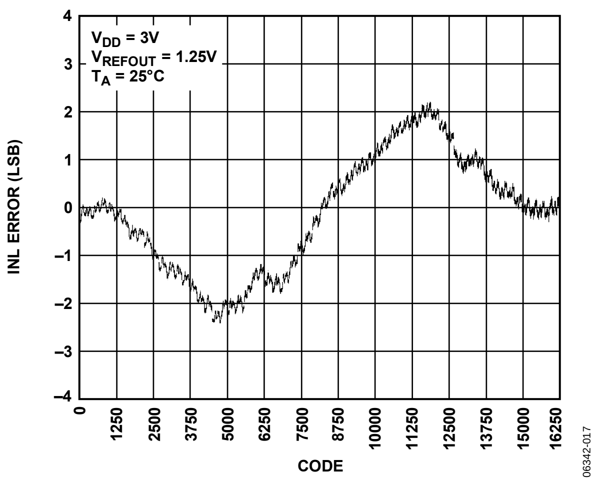


Figure 19. AD5647R INL, 1.25 V Internal Reference

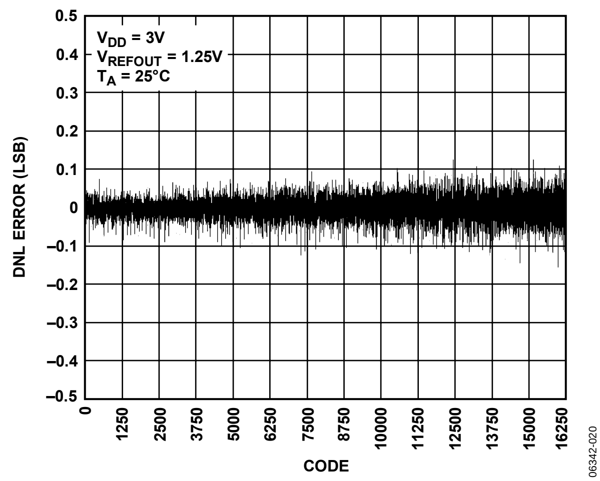


Figure 22. AD5647R DNL,1.25 V Internal Reference

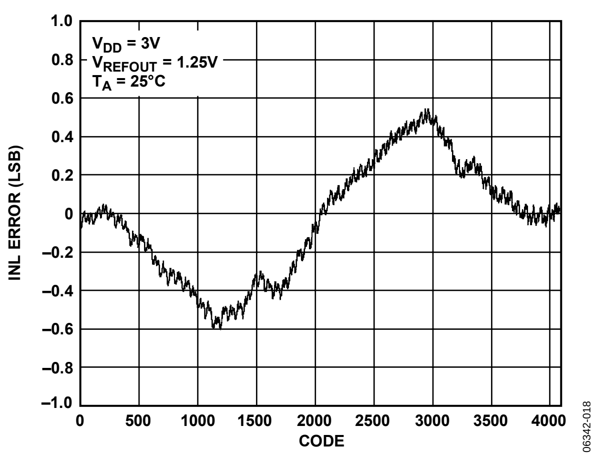


Figure 20. AD5627R INL,1.25 V Internal Reference

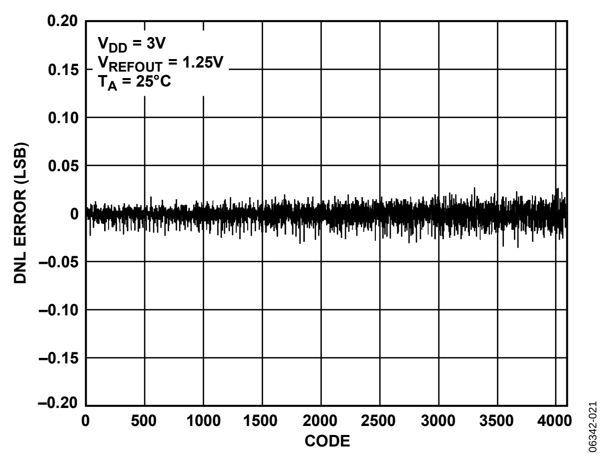


Figure 23. AD5627R DNL, 1.25 V Internal Reference

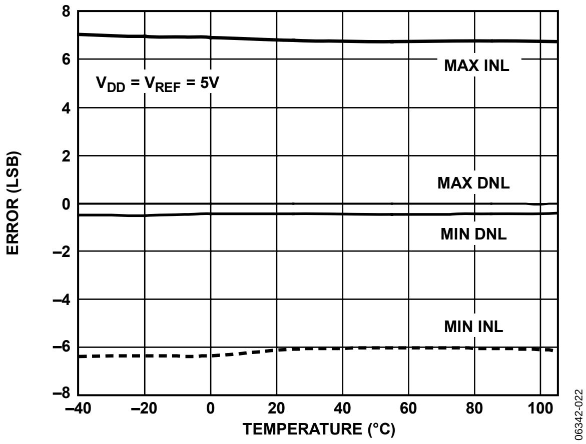


Figure 24. INL Error and DNL Error vs. Temperature

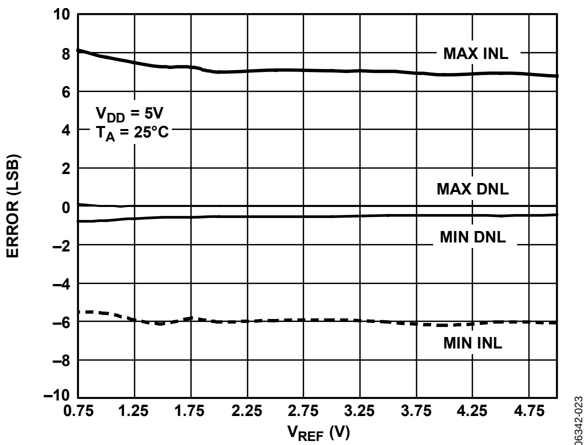


Figure 25. INL and DNL Error vs. V_{REF}

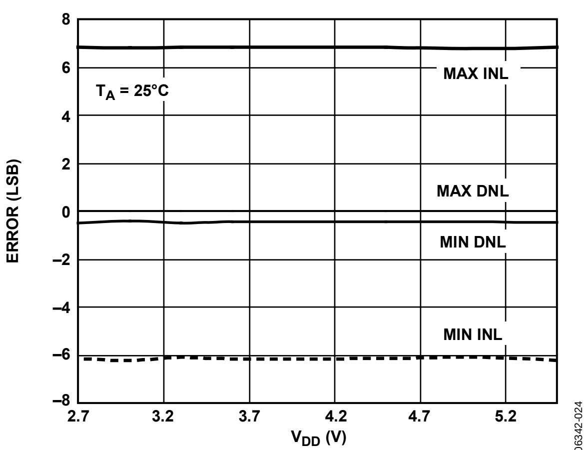


Figure 26. INL and DNL Error vs. Supply

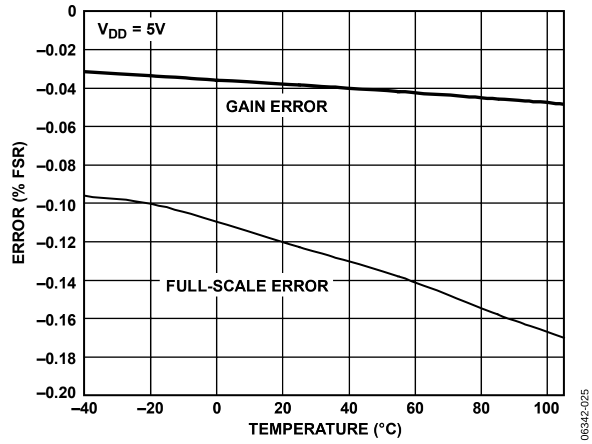


Figure 27. Gain Error and Full-Scale Error vs. Temperature

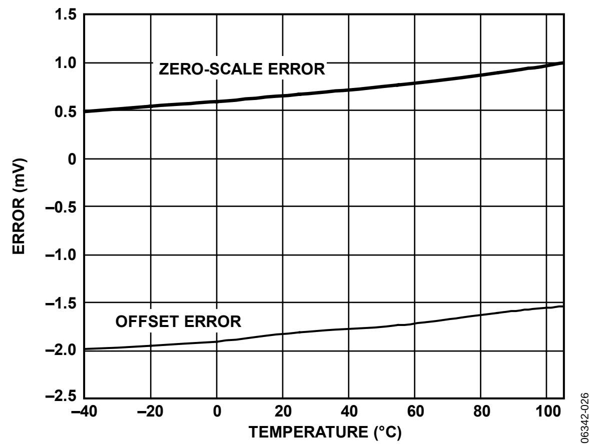


Figure 28. Zero-Scale Error and Offset Error vs. Temperature

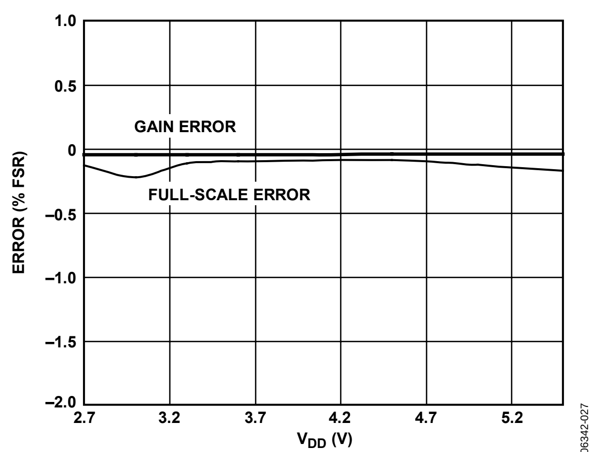


Figure 29. Gain Error and Full-Scale Error vs. Supply

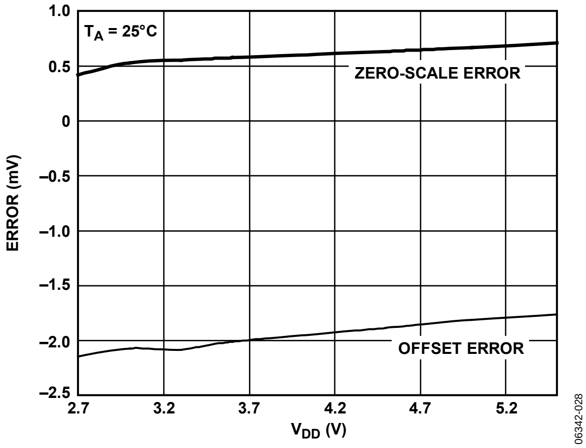


Figure 30. Zero-Scale Error and Offset Error vs. Supply

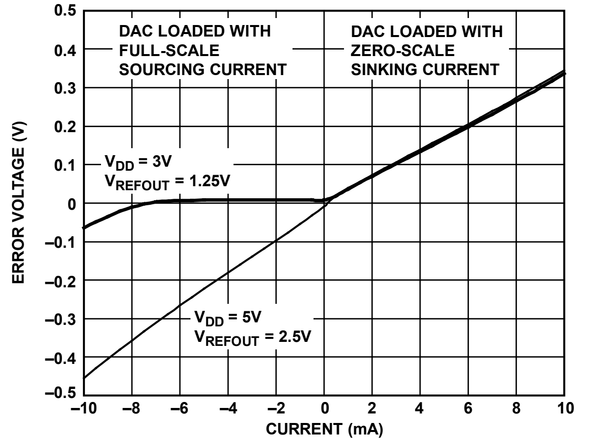


Figure 33. Headroom at Rails vs. Source and Sink

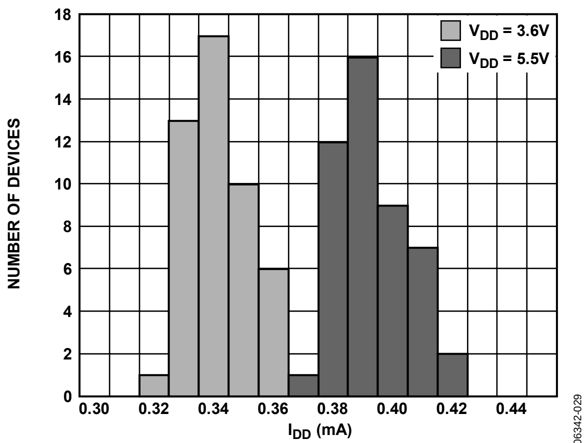


Figure 31. I_{DD} Histogram with External Reference

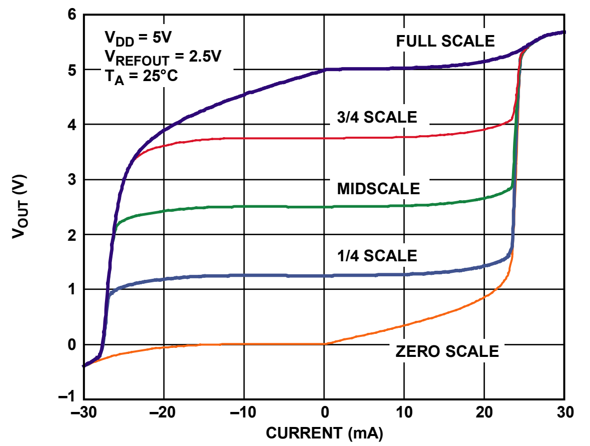


Figure 34. AD56x7R with 2.5 V Reference, Source and Sink Capability

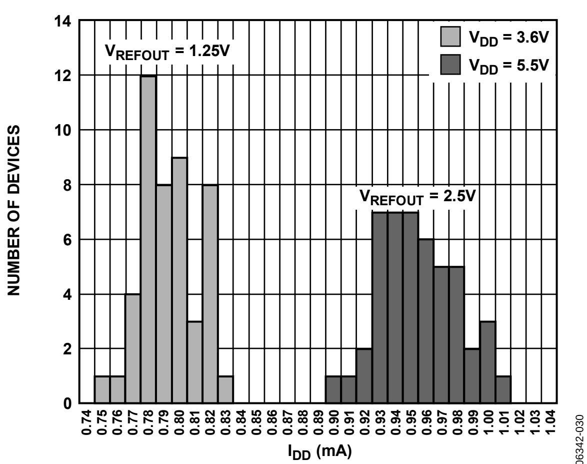


Figure 32. I_{DD} Histogram with Internal Reference

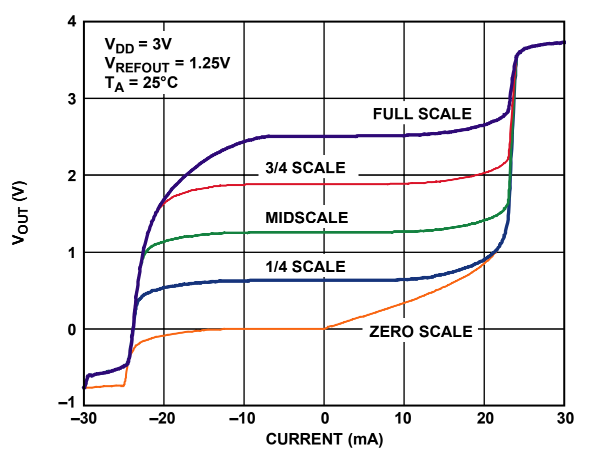


Figure 35. AD56x7R with 1.25 V Reference, Source and Sink Capability

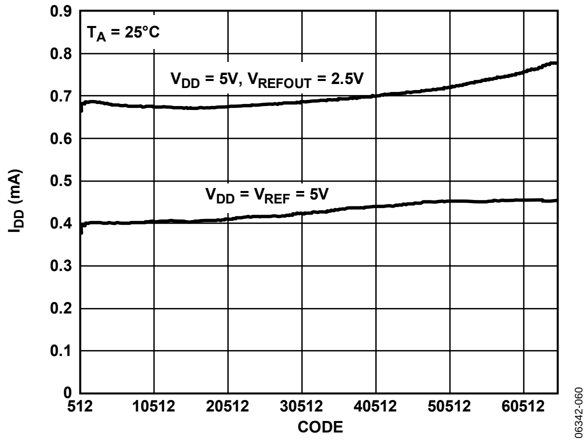


Figure 36. Supply Current vs. Code

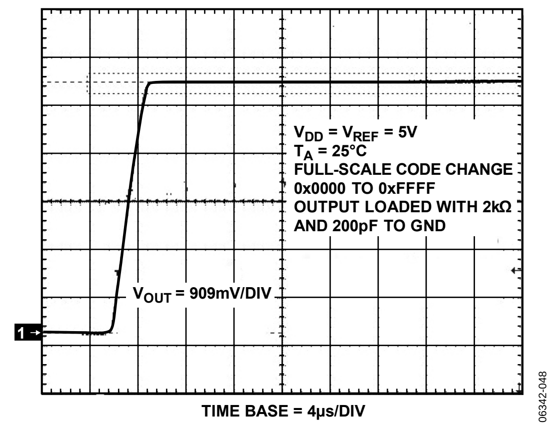


Figure 39. Full-Scale Settling Time, 5 V

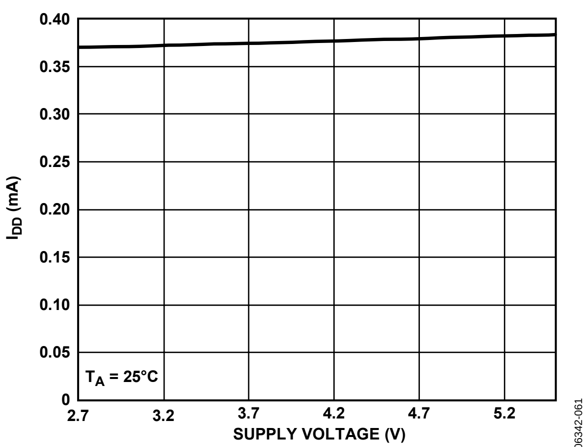


Figure 37. Supply Current vs. Supply Voltage

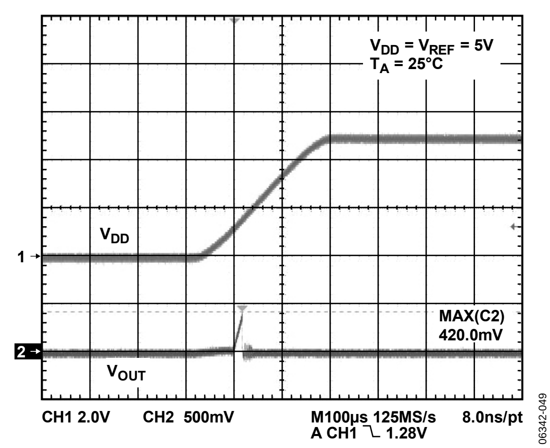


Figure 40. Power-On Reset to 0 V

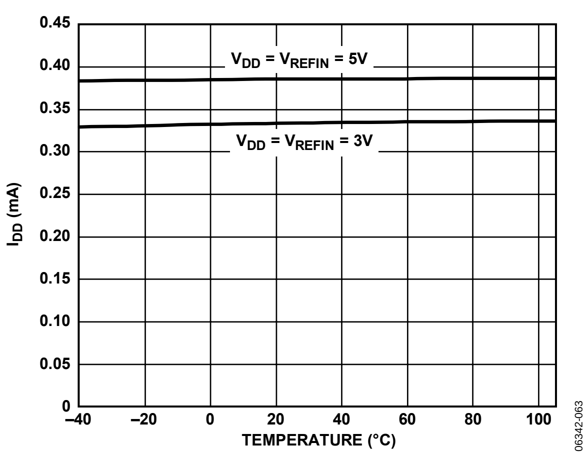


Figure 38. Supply Current vs. Temperature

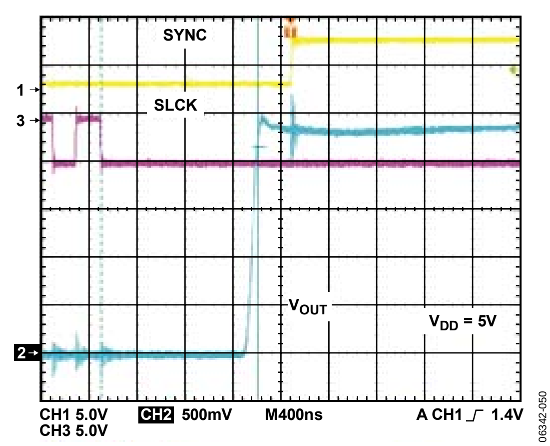


Figure 41. Exiting Power-Down to Midscale

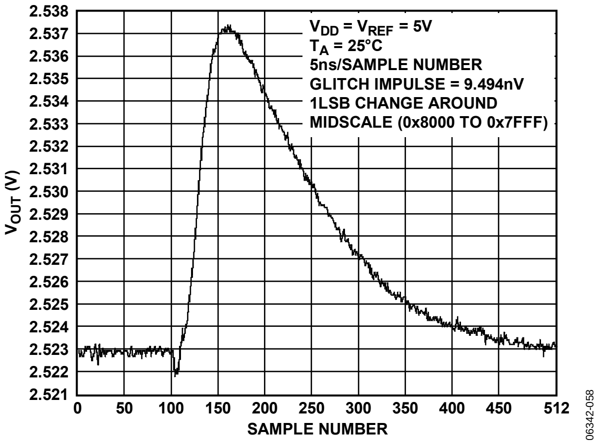


Figure 42. Digital-to-Analog Glitch Impulse (Negative)

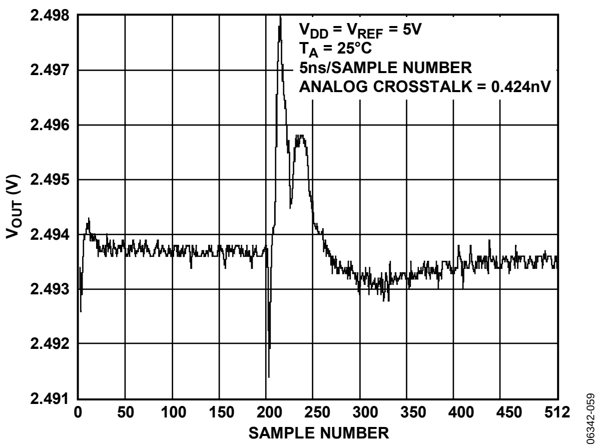


Figure 43. Analog Crosstalk, External Reference

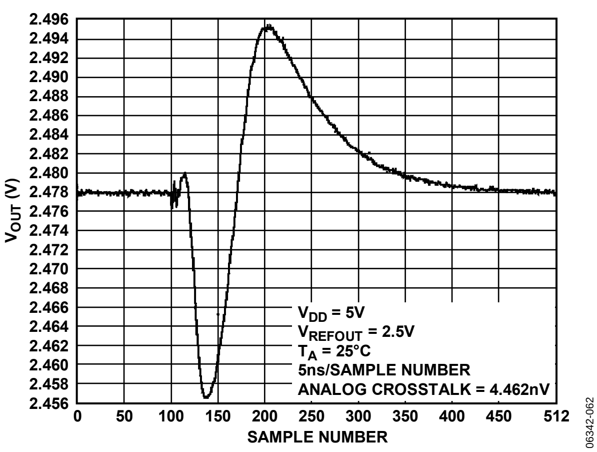


Figure 44. Analog Crosstalk, Internal Reference

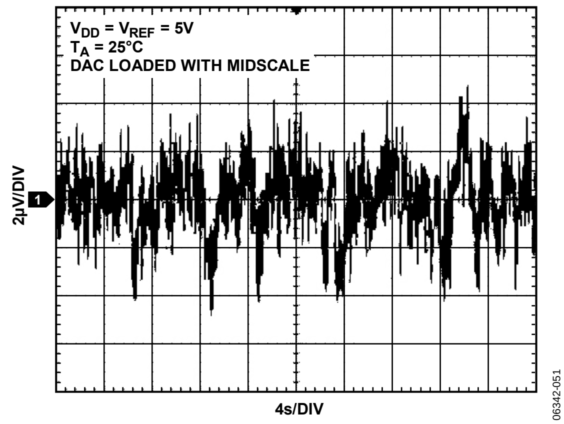


Figure 45. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

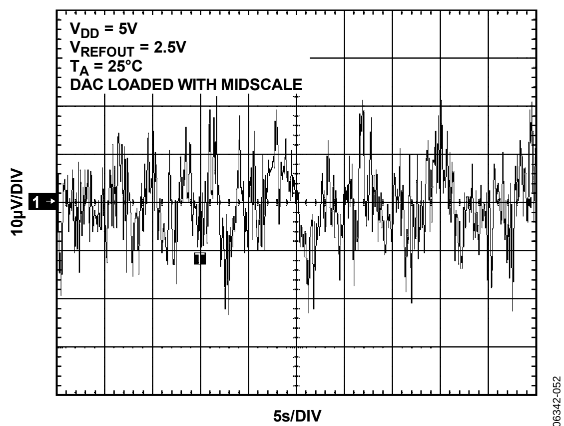


Figure 46. 0.1 Hz to 10 Hz Output Noise Plot, 2.5 V Internal Reference

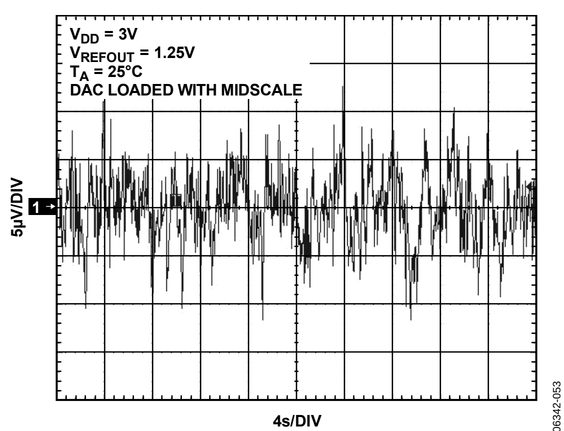


Figure 47. 0.1 Hz to 10 Hz Output Noise Plot,1.25 V Internal Reference

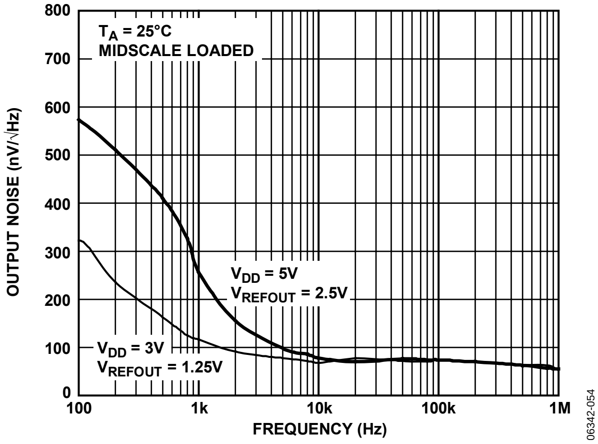


Figure 48. Noise Spectral Density, Internal Reference

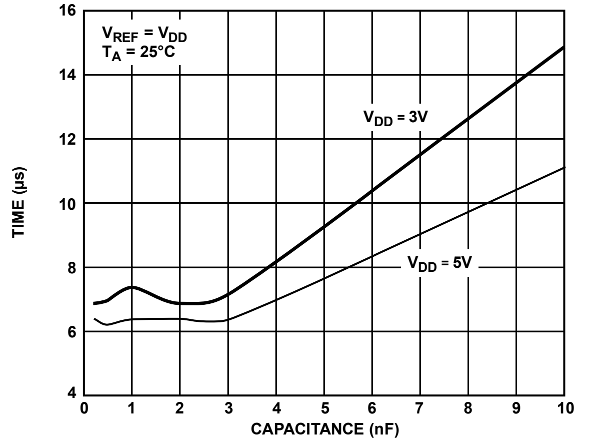


Figure 50. Settling Time vs. Capacitive Load

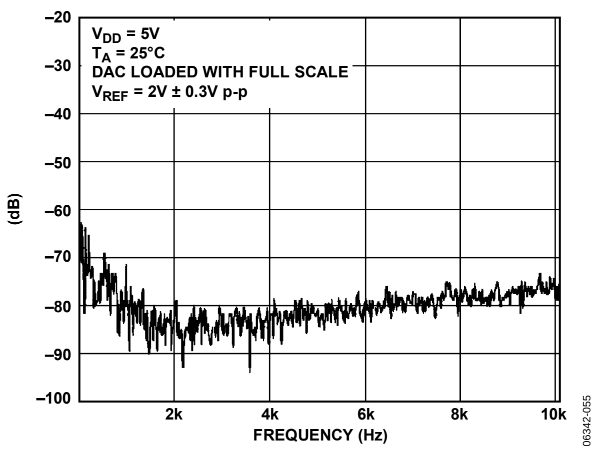


Figure 49. Total Harmonic Distortion

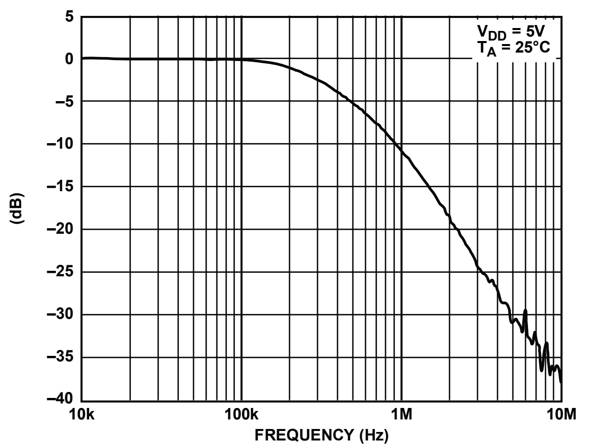


Figure 51. Multiplying Bandwidth

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design.

Zero-Code Error
Zero-code error is a measurement of the output error when zero scale (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5667R because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero-code error is expressed in mV.

Full-Scale Error
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed in % of full-scale range (FSR).

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed in % of FSR.

Zero-Code Error Drift
Zero-code error drift is a measurement of the change in zero-code error with a change in temperature. It is expressed in μV/°C.

Gain Temperature Coefficient
Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/°C.

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the AD5667R with code 512 loaded in the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
DC PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dB. V_{REF} is held at 2 V and V_{DD} is varied by ±10%.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change and is measured from the rising edge of the stop condition.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000) (see Figure 42).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in dB.

Output Noise Spectral Density
Output noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density. It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz. A plot of noise spectral density can be seen in Figure 48.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in μV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in μV/mA.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

Analog Crosstalk

Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa), then executing a software $\overline{\text{LDAC}}$ and monitoring the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa) with $\overline{\text{LDAC}}$ low while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth

The multiplying bandwidth is a measure of the finite bandwidth of the amplifiers within the DAC. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)

THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

THEORY OF OPERATION

D/A SECTION

The AD56x7R/AD56x7 DACs are fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Figure 52 shows a block diagram of the DAC architecture.

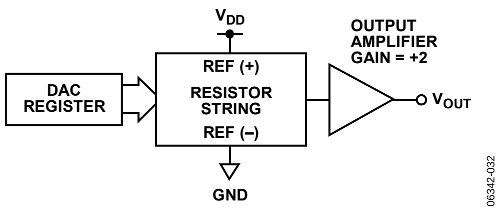


Figure 52. DAC Architecture

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N}\right)$$

The ideal output voltage when using the internal reference is given by

$$V_{OUT} = 2 \times V_{REFOUT} \times \left(\frac{D}{2^N}\right)$$

where:

D is the decimal equivalent of the binary code that is loaded to the DAC register:

0 to 4095 for AD5627R/AD5627 (12-bit).
0 to 16,383 for AD5647R (14-bit).
0 to 65,535 for AD5667R/AD5667 (16-bit).

N is the DAC resolution.

RESISTOR STRING

The resistor string is shown in Figure 53. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

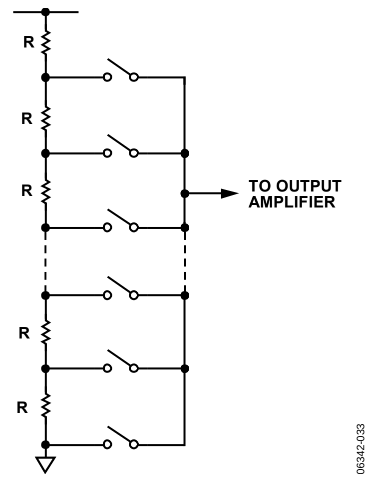


Figure 53. Resistor String

OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. It can drive a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 33 and Figure 34. The slew rate is 1.8 V/μs with a ¼ to ¾ full-scale settling time of 7 μs.

INTERNAL REFERENCE

The AD5627R/AD5647R/AD5667R feature an on-chip reference. Versions without the R suffix require an external reference. The on-chip reference is off at power-up and is enabled via a write to a control register. See the Internal Reference Setup section for details.

Versions packaged in a 10-lead LFCSP package have a 1.25 V reference, giving a full-scale output of 2.5 V. These parts can be operated with a V_{DD} supply of 2.7 V to 5.5 V. Versions packaged in a 10-lead MSOP package have a 2.5 V reference, giving a full-scale output of 5 V. The parts are functional with a V_{DD} supply of 2.7 V to 5.5 V, but with a V_{DD} supply of less than 5 V, the output is clamped to V_{DD}. See the Ordering Guide for a full list of models. The internal reference associated with each part is available at the V_{REFOUT} pin.

A buffer is required if the reference output is used to drive external loads. When using the internal reference, it is recommended that a 100 nF capacitor be placed between the reference output and GND for reference stability.

EXTERNAL REFERENCE

The AD5627/AD5667 require an external reference, which is applied at the V_{REFIN} pin. The V_{REFIN} pin on the AD56x7R allows the use of an external reference if the application requires it. The default condition of the on-chip reference is off at power-up. All devices can be operated from a single 2.7 V to 5.5 V supply.

SERIAL INTERFACE

The AD56x7R/AD56x7 have 2-wire I²C-compatible serial interfaces (refer to *I²C-Bus Specification*, Version 2.1, January 2000, available from Philips Semiconductor). The AD56x7R/AD56x7 can be connected to an I²C bus as a slave device, under the control of a master device. See Figure 3 for a timing diagram of a typical write sequence.

The AD56x7R/AD56x7 support standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) data transfer modes. High speed operation is only available on select models. See the Ordering Guide for a full list of models. Support is not provided for 10-bit addressing and general call addressing.

The AD56x7R/AD56x7 each have a 7-bit slave address. The five MSBs are 00011 and the two LSBs (A1, A0) are set by the state of the ADDR address pin. The facility to make hardwired changes to ADDR allows the user to incorporate up to three of these devices on one bus, as outlined in Table 7.

Table 7. Device Address Selection

ADDR Pin Connection	A1	A0
V_{DD}	0	0
No Connection	1	0
GND	1	1

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address. The slave address corresponding to the transmitted address responds by pulling SDA low during the 9th clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its shift register.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the 9th clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse, and then high during the 10th clock pulse to establish a stop condition.

WRITE OPERATION

When writing to the AD56x7R/AD56x7, the user must begin with a start command followed by an address byte ($R/\overline{W}$= 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The AD56x7R/AD56x7 requires two bytes of data for the DAC and a command byte that controls various DAC functions. Three bytes of data must therefore be written to the DAC, the command byte followed by the most significant data byte and the least significant data byte, as shown in Figure 54. All these data bytes are acknowledged by the AD56x7R/AD56x7. A stop condition follows.

READ OPERATION

When reading data back from the AD56x7R/AD56x7, the user begins with a start command followed by an address byte ($R/\overline{W}$ = 1), after which the DAC acknowledges that it is prepared to transmit data by pulling SDA low. Three bytes of data are then read from the DAC, which are acknowledged by the master, as shown in Figure 55. A stop condition follows.

HIGH SPEED MODE

The AD5627RBRMZ and the AD5667RBRMZ offer high speed serial communication with a clock frequency of 3.4 MHz. See the Ordering Guide for details.

High speed mode communication commences after the master addresses all devices connected to the bus with the Master Code 00001XXX to indicate that a high speed mode transfer is to begin (see Figure 56). No device connected to the bus is permitted to acknowledge the high speed master code. Therefore, the code is followed by a no acknowledge. The master must then issue a repeated start followed by the device address. The selected device then acknowledges its address.

All devices continue to operate in high speed mode until the master issues a stop condition. When the stop condition is issued, the devices return to standard/fast mode. The part also returns to standard/fast mode when $\overline{CLR}$ is activated while the part is in high speed mode.

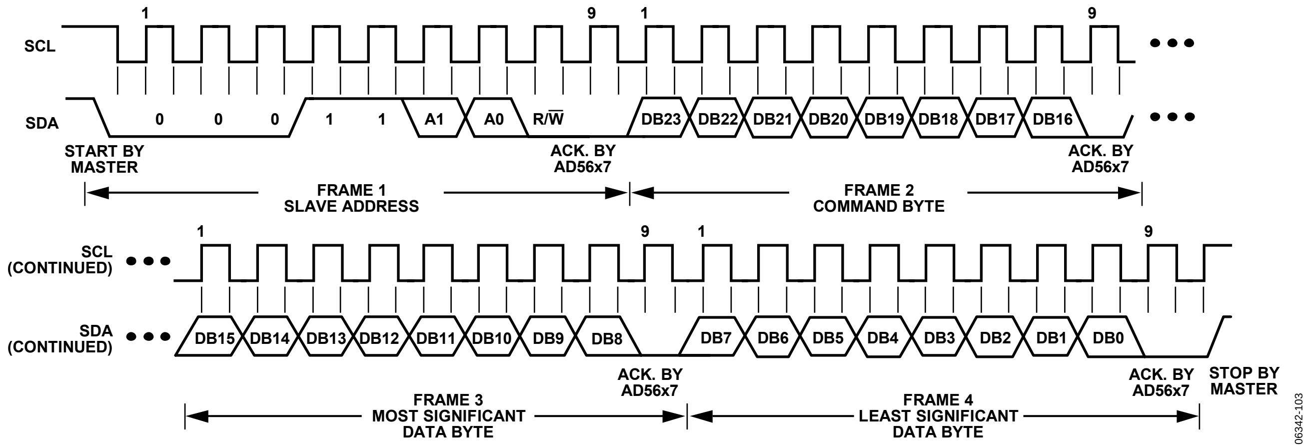


Figure 54. I²C Write Operation

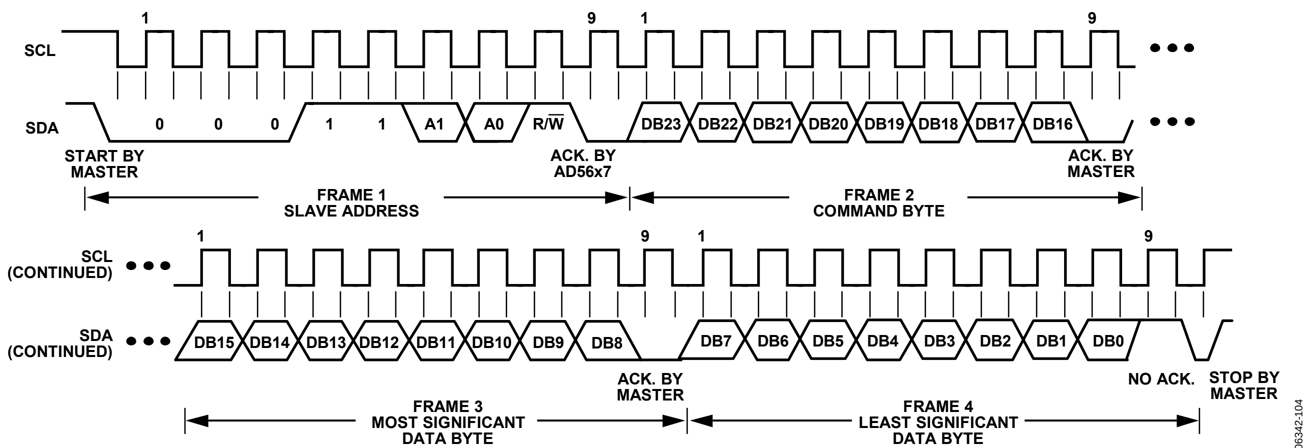


Figure 55. I²C Read Operation

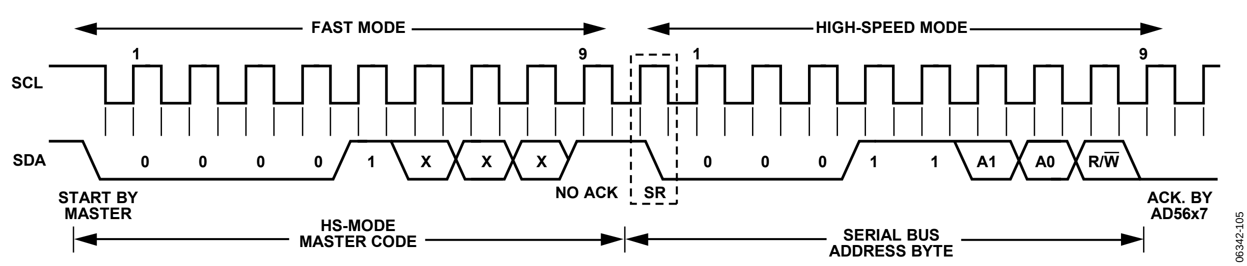


Figure 56. Placing the AD5627RBRMZ-2/AD5667RBRMZ-2 in High Speed Mode

INPUT SHIFT REGISTER

The input shift register is 24 bits wide. Data is loaded into the device as a 24-bit word under the control of a serial clock input, SCL. The timing diagram for this operation is shown in Figure 3. The 8 MSBs make up the command byte. DB23 is reserved and should always be set to 0 when writing to the device. DB22 (S) is used to select multiple byte operation The next three bits are the command bits (C2, C1, C0) that control the mode of operation of the device. See Table 8 for details. The last 3 bits of first byte are the address bits (A2, A1, A0). See Table 9 for details. The rest of the bits are the 16-, 14-, 12-bit data word. The data word comprises the 16-, 14-, 12-bit input code followed by two or four don't cares for the AD5647R and the AD5627R/AD5627, respectively (see Figure 59 through Figure 61).

MULTIPLE BYTE OPERATION

Multiple byte operation is supported on the AD56x7R/AD56x7. A 2-byte operation is useful for applications that require fast DAC updating and do not need to change the command byte. The S bit (DB22) in the command register can be set to 1 for 2-byte mode of operation (see Figure 57). For standard 3-byte and 4-byte operation, the S bit (DB22) in the command byte should be set to 0 (see Figure 58).

BROADCAST MODE

Broadcast addressing is supported on the AD56x7R/AD56x7. Broadcast addressing can be used to synchronously update or power down multiple AD56x7R/AD56x7 devices. Using the broadcast address, the AD56x7R/AD56x7 responds regardless of the states of the address pins. Broadcast is supported only in write mode. The AD56x7R/AD56x7 broadcast address is 00010000.

Table 8. Command Definition

C2	C1	C0	Command
0	0	0	Write to input register *n*
0	0	1	Update DAC register *n*
0	1	0	Write to input register *n*, update all (software $\overline{\text{LDAC}}$)
0	1	1	Write to and update DAC channel *n*
1	0	0	Power up/power down
1	0	1	Reset
1	1	0	$\overline{\text{LDAC}}$ register setup
1	1	1	Internal reference setup (on/off)

Table 9. DAC Address Command

A2	A1	A0	ADDRESS (*n*)
0	0	0	DAC A
0	0	1	DAC B
1	1	1	Both DACs

$\overline{\text{LDAC}}$ FUNCTION

The AD56x7R/AD56x7 DACs have double-buffered interfaces consisting of two banks of registers, input registers and DAC registers. The input registers are connected directly to the input shift register, and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC registers contain the digital codes used by the resistor strings.

Access to the DAC registers is controlled by the $\overline{\text{LDAC}}$ pin. When the $\overline{\text{LDAC}}$ pin is high, the DAC registers are latched and the input registers can change state without affecting the contents of the DAC registers. When $\overline{\text{LDAC}}$ is brought low, however, the DAC registers become transparent and the contents of the input registers are transferred to them. The double-buffered interface is useful if the user requires simultaneous updating of all DAC outputs. The user can write to one of the input registers individually and then, by bringing $\overline{\text{LDAC}}$ low when writing to the other DAC input register, all outputs update simultaneously.

These parts each contain an extra feature whereby a DAC register is not updated unless its input register has been updated since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the input registers. In the case of the AD56x7R/AD56x7, the DAC register updates only if the input register has changed since the last time the DAC register was updated, thereby removing unnecessary digital crosstalk.

The outputs of all DACs can be simultaneously updated, using the hardware $\overline{\text{LDAC}}$ pin.

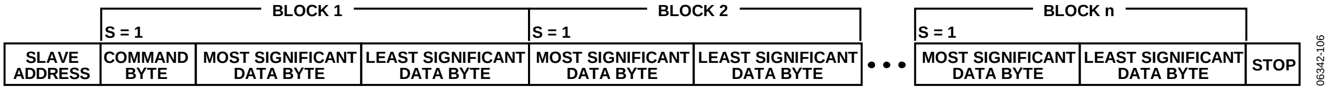


Figure 57. Multiple Block Write with Initial Command Byte Only (S = 1)

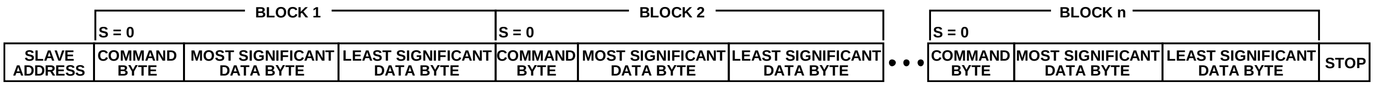


Figure 58. Multiple Block Write with Command Byte in Each Block (S = 0)

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	S	C2	C1	C0	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RESERVED	BYTE SELECTION	COMMAND			DAC ADDRESS			DAC DATA								DAC DATA							
COMMAND BYTE								DATA HIGH BYTE								DATA LOW BYTE							

06342-108

Figure 59. AD5667R/AD5667 Input Shift Register (16-Bit DAC)

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	S	C2	C1	C0	A2	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X
RESERVED	BYTE SELECTION	COMMAND			DAC ADDRESS			DAC DATA								DAC DATA							
COMMAND BYTE								DATA HIGH BYTE								DATA LOW BYTE							

06342-109

Figure 60. AD5647R Input Shift Register (14-Bit DAC)

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	S	C2	C1	C0	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
RESERVED	BYTE SELECTION	COMMAND			DAC ADDRESS			DAC DATA								DAC DATA							
COMMAND BYTE								DATA HIGH BYTE								DATA LOW BYTE							

06342-110

Figure 61. AD5627R/AD5627 Input Shift Register (12-Bit DAC)

Synchronous LDAC

The DAC registers are updated after new data is read in. LDAC can be permanently low or pulsed.

Asynchronous LDAC

The outputs are not updated at the same time that the input registers are written to. When LDAC goes low, the DAC registers are updated with the contents of the input register.

The LDAC register gives the user full flexibility and control over the hardware LDAC pin. This register allows the user to select which combination of channels to simultaneously update when the hardware LDAC pin is executed. Setting the LDAC bit register to 0 for a DAC channel means that the update of this channel is controlled by the LDAC pin. If this bit is set to 1, this channel synchronously updates, that is, the DAC register is updated after new data is read in, regardless of the state of the LDAC pin. It effectively sees the LDAC pin as being pulled low. See Table 10 for the LDAC register mode of operation. This flexibility is useful in applications when the user wants to simultaneously update select channels while the rest of the channels are synchronously updating.

Writing to the DAC using Command 110 loads the 2-bit LDAC register [DB1:DB0]. The default for each channel is 0, that is, the LDAC pin works normally. Setting the bits to 1 means the DAC register is updated, regardless of the state of the LDAC pin. See Figure 63 for contents of the input shift register during the LDAC register setup command.

Table 10. LDAC Register Mode of Operation: Load DAC Register

LDAC Bits (DB1 to DB0)	LDAC Pin	LDAC Operation
0	1/0	Determined by LDAC pin.
1	x = don't care	The DAC registers are updated after new data is read in.

POWER-DOWN MODES

Command 100 is reserved for the power-up/down function. The power-up/down modes are programmed by setting Bit DB5 and Bit DB4. This defines the output state of the DAC amplifier, as shown in Table 11. Bit DB1and Bit DB0 determine to which DAC or DACs the power-up/down command is applied. Setting one of these bits to 1 applies the power-up/down state defined by DB5 and DB4 to the corresponding DAC. If a bit is 0, the state of the DAC is unchanged. Figure 65 shows the contents of the input shift register for the power up/down command.

When Bit DB5 and Bit DB4 are set to 0, the part works normally with its normal power consumption of 400 µA at 5 V. However, for the three power-down modes, the supply current falls to 480 nA at 5 V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This allows the output impedance of the part to be known while the part is in power-down mode. The outputs can either be connected internally to GND through a 1 kΩ or 100 kΩ resistor, or left open-circuited (three-state) as shown in Figure 62.

Table 11. Modes of Operation for the AD56x7R/AD56x7

DB5	DB4	Operating Mode
0	0	Normal operation
		Power-down modes
0	1	1 kΩ pull-down to GND
1	0	100 kΩ pull-down to GND
1	1	Three-state, high impedance

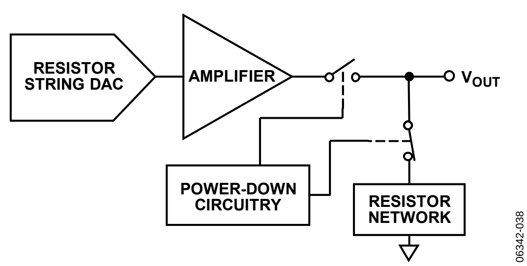


Figure 62. Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string, and other associated linear circuitry are shut down when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 4 µs for V_{DD} = 5 V.

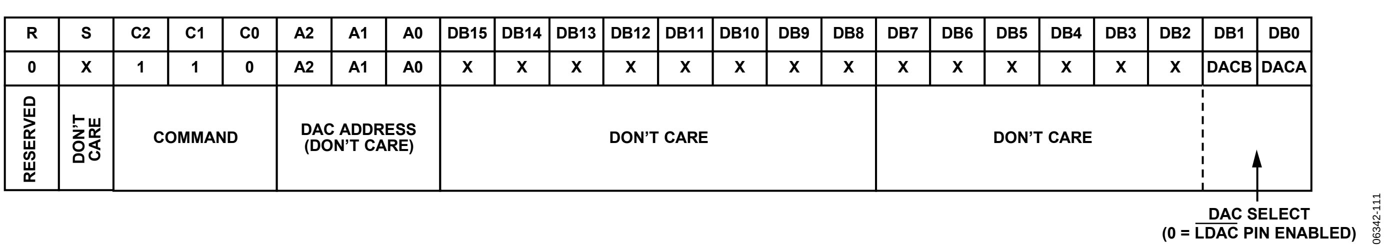


Figure 63. LDAC Setup Command

POWER-ON RESET AND SOFTWARE RESET

The AD56x7R/AD56x7 contain a power-on reset circuit that controls the output voltage during power-up. The device powers up to 0 V and the output remains powered up at this level until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. Any events on LDAC or CLR during power-on reset are ignored.

There is also a software reset function. Command 101 is the software reset command. The software reset command contains two reset modes that are software programmable by setting Bit DB0 in the input shift register.

Table 12 shows how the state of the bit corresponds to the software reset modes of operation of the devices. Figure 64 shows the contents of the input shift register during the software reset mode of operation.

Table 12. Software Reset Modes for the AD56x7R/AD56x7

DB0	Registers reset to zero
0	DAC register Input shift register
1 (Power-On Reset)	DAC register Input shift register LDAC register Power-down register Internal reference setup register

CLEAR PIN (CLR)

The AD56x7R/AD56x7 has an asynchronous clear input. The CLR input is falling-edge sensitive. While CLR is low, all LDAC pulses are ignored. When CLR is activated, zero scale is loaded to all input and DAC registers. This clears the output to 0 V. The part exits clear code mode on the on the falling edge of the 9th clock pulse of the last byte of valid write. If CLR is activated during a write sequence, the write is aborted. If CLR is activated during high speed mode, the part exits high speed mode to standard/fast mode.

INTERNAL REFERENCE SETUP (R VERSIONS)

The on-chip reference is off at power-up by default. It can be turned on by sending the reference setup command (111) and setting DB0 in the input shift register. Table 13 shows how the state of the bit corresponds to the mode of operation. See Figure 66 for the contents of the input shift register during the internal reference setup command.

Table 13. Reference Setup Command

DB0	Action
0	Internal reference off (default)
1	Internal reference on

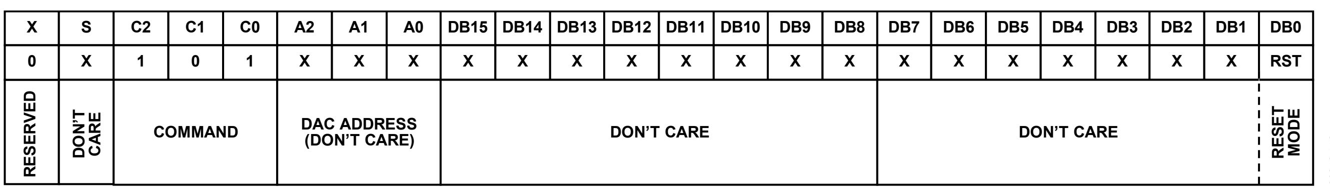


Figure 64. Software Reset Command

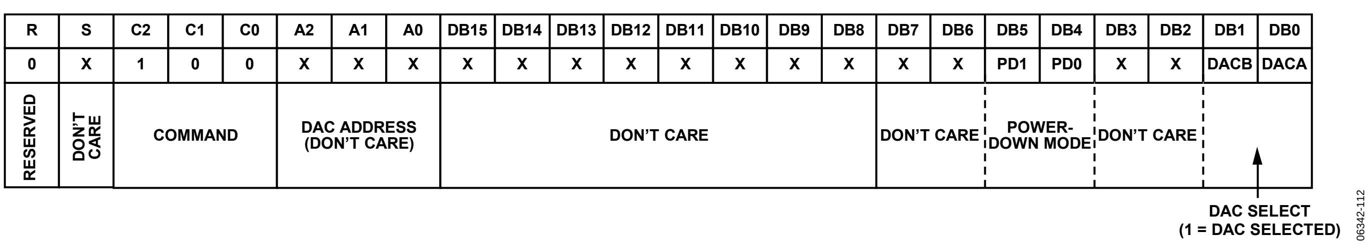


Figure 65. Power Up/Down Command

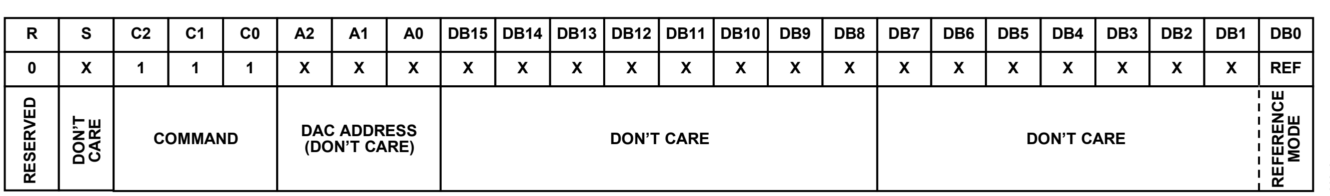


Figure 66. Reference Setup Command

APPLICATION INFORMATION

USING A REFERENCE AS A POWER SUPPLY FOR THE AD56x7R/AD56x7

Because the supply current required by the AD56x7R/AD56x7 is extremely low, an alternative option is to use a voltage reference to supply the required voltage to the part (see Figure 67). This is especially useful if the power supply is quite noisy, or if the system supply voltages are at some value other than 5 V or 3 V, for example, 15 V. The voltage reference outputs a steady supply voltage for the AD56x7R/AD56x7. If the low dropout REF195 is used, it must supply 450 μA of current to the AD56x7R/AD56x7 with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is

450 μA + (5 V/5 kΩ) = 1.45 mA

The load regulation of the REF195 is typically 2 ppm/mA, resulting in a 2.9 ppm (14.5 μV) error for the 1.45 mA current drawn from it. This corresponds to a 0.191 LSB error.

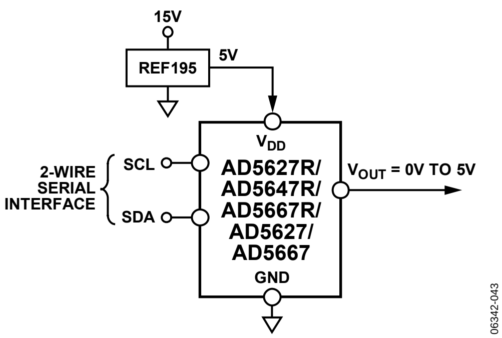


Figure 67. REF195 as Power Supply to the AD56x7R/AD56x7

BIPOLAR OPERATION USING THE AD56x7R/AD56x7

The AD56x7R/AD56x7 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 68. The circuit gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achieved using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{65{,}536} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 to 65535). With V_{DD} = 5 V, R1 = R2 = 10 kΩ,

$$V_O = \left(\frac{10 \times D}{65{,}536} \right) - 5 \text{ V}$$

This is an output voltage range of ±5 V, with 0x0000 corresponding to a −5 V output, and 0xFFFF corresponding to a +5 V output.

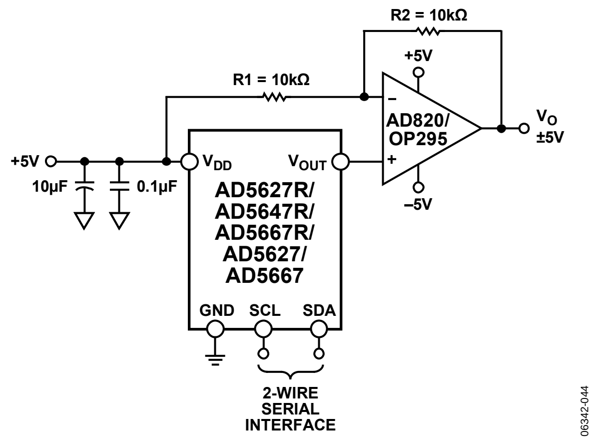


Figure 68. Bipolar Operation with the AD56x7R/AD56x7

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD56x7R/AD56x7 should have separate analog and digital sections, each having its own area of the board. If the AD56x7R/AD56x7 are in a system where other devices require an AGND to DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD56x7R/AD56x7.

The power supply to the AD56x7R/AD56x7 should be bypassed with 10 μF and 0.1 μF capacitors. The capacitors should be located as close as possible to the device, with the 0.1 μF capacitor ideally right up against the device. The 10 μF capacitor should be the tantalum bead type. It is important that the 0.1 μF capacitor have low effective series resistance (ESR) and effective series inductance (ESI), for example, common ceramic types of capacitors. This 0.1 μF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and to reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a two-layer board.

OUTLINE DIMENSIONS

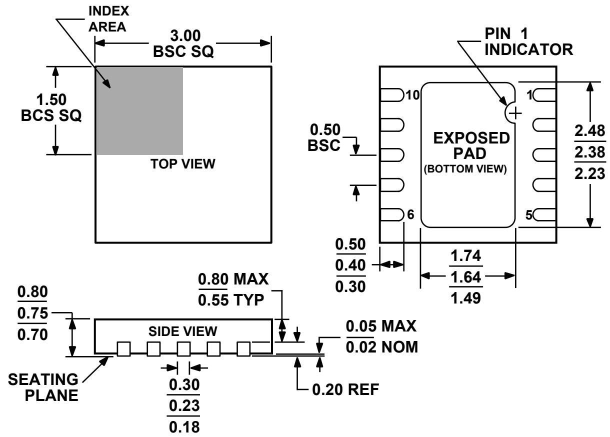
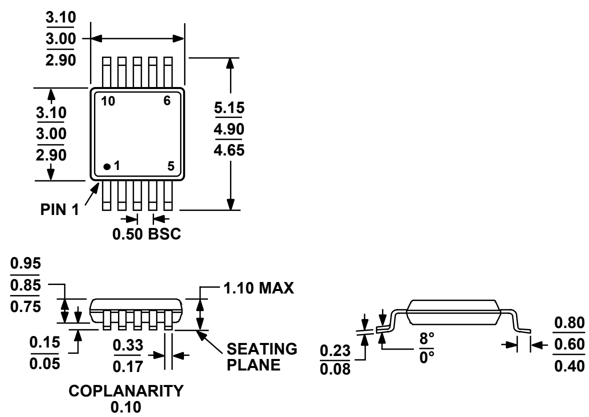


Figure 69. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm x 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 70. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Accuracy	On-Chip Reference	Max I²C Speed	Package Description	Package Option	Branding
AD5627BCPZ-R2[1]	−40°C to +105°C	±1 LSB INL	None	400 kHz	10-Lead LFCSP_WD	CP-10 -9	DA1
AD5627BCPZ-REEL7[1]	−40°C to +105°C	±1 LSB INL	None	400 kHz	10-Lead LFCSP_WD	CP-10-9	DA1
AD5627BRMZ[1]	−40°C to +105°C	±1 LSB INL	None	400 kHz	10-Lead MSOP	RM-10	DA1
AD5627BRMZ-REEL7[1]	−40°C to +105°C	±1 LSB INL	None	400 kHz	10-Lead MSOP	RM-10	DA1
AD5627RBCPZ-R2[1]	−40°C to +105°C	±1 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	CP-10-9	D9J
AD5627RBCPZ-REEL7[1]	−40°C to +105°C	±1 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	CP-10-9	D9J
AD5627RBRMZ-1[1]	−40°C to +105°C	±1 LSB INL	2.5 V	400 kHz	10-Lead MSOP	RM-10	DA7
AD5627RBRMZ-1REEL7[1]	−40°C to +105°C	±1 LSB INL	2.5 V	400 kHz	10-Lead MSOP	RM-10	DA7
AD5627RBRMZ-2[1]	−40°C to +105°C	±1 LSB INL	2.5 V	3.4 MHz	10-Lead MSOP	RM-10	DA8
AD5627RBRMZ-2REEL7[1]	−40°C to +105°C	±1 LSB INL	2.5 V	3.4 MHz	10-Lead MSOP	RM-10	DA8
AD5647RBCPZ-R2[1]	−40°C to +105°C	±4 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	RU-14	D9G
AD5647RBCPZ-REEL7[1]	−40°C to +105°C	±4 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	RU-14	D9G
AD5647RBRMZ[1]	−40°C to +105°C	±4 LSB INL	2.5 V	400 kHz	10-Lead MSOP	RM-10	D9G
AD5647RBRMZ-REEL7[1]	−40°C to +105°C	±4 LSB INL	2.5 V	400 kHz	10-Lead MSOP	RM-10	D9G
AD5667BCPZ-R2[1]	−40°C to +105°C	±12 LSB INL	None	400 kHz	10-Lead LFCSP_WD	CP-10-9	D9Z
AD5667BCPZ-REEL7[1]	−40°C to +105°C	±12 LSB INL	None	400 kHz	10-Lead LFCSP_WD	CP-10-9	D9Z
AD5667BRMZ[1]	−40°C to +105°C	±12 LSB INL	None	400 kHz	10-Lead MSOP	RM-10	D9Z
AD5667BRMZ-REEL7[1]	−40°C to +105°C	±12 LSB INL	None	400 kHz	10-Lead MSOP	RM-10	D9Z
AD5667RBCPZ-R2[1]	−40°C to +105°C	±12 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	CP-10-9	D8X
AD5667RBCPZ-REEL7[1]	−40°C to +105°C	±12 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	CP-10-9	D8X
AD5667RBRMZ-1[1]	−40°C to +105°C	±12 LSB INL	2.5 V	400 kHz	10-Lead MSOP	RM-10	DA5
AD5667RBRMZ-1REEL7[1]	−40°C to +105°C	±12 LSB INL	2.5 V	400 kHz	10-Lead MSOP	RM-10	DA5
AD5667RBRMZ-2[1]	−40°C to +105°C	±12 LSB INL	2.5 V	3.4 MHz	10-Lead MSOP	RM-10	DA6
AD5667RBRMZ-2REEL7[1]	−40°C to +105°C	±12 LSB INL	2.5 V	3.4 MHz	10-Lead MSOP	RM-10	DA6
EVAL-AD5667REBZ[1]					Evaluation Board		

[1] Z = Pb-free part.

NOTES

NOTES

NOTES

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D06342-0-1/07(0)

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