



MIC5841/5842

8-Bit Serial-Input Latched Drivers

General Description

Using BiCMOS technology, the MIC5841/5842 integrated circuits were fabricated to be used in a wide variety of peripheral power driver applications. The devices each have an eight-bit CMOS shift register, CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlington output drivers.

These two devices differ only in maximum voltage ratings. The MIC5842 offers premium performance with a minimum output breakdown voltage rating of 80V (50V sustaining). The drivers can be operated with a split supply where the negative supply is down to -20V.

The 500mA outputs, with integral transient-suppression diodes, are suitable for use with lamps, relays, solenoids and other inductive loads.

These devices have improved speed characteristics. With a 5V logic supply, they will typically operate faster than 5 MHz. With a 12V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL or DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

The MIC5840 family is available in DIP, PLCC, and SOIC packages. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current might require a reduction in duty cycle. A copper-alloy lead frame provides for maximum package power dissipation.

Features

- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Up/Pull-Down Resistors
- Low-Power CMOS Logic and Latches
- High-Voltage Current-Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation

Ordering Information

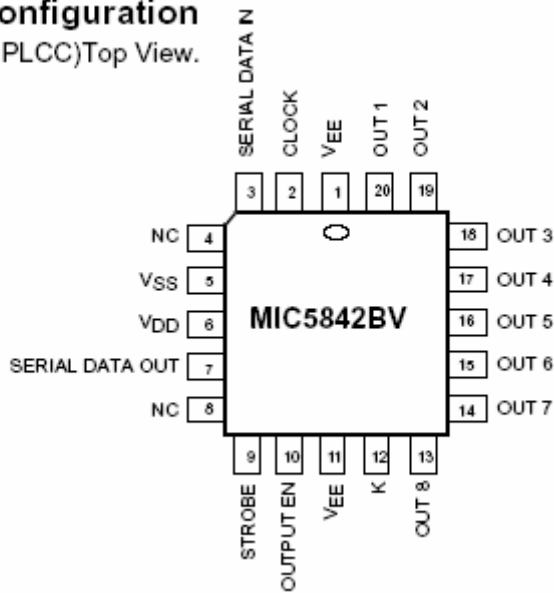
| Part Number | | Temperature Range | Package |
|-------------|------------|-------------------|--------------------|
| Standard | Pb-Free | | |
| MIC5841BN | MIC5841YN | -40°C to +85°C | 18-Pin Plastic DIP |
| MIC5841BV | MIC5841YV | -40°C to +85°C | 20-Pin PLCC |
| MIC5841BWM | MIC5841YWM | -40°C to +85°C | 18-Pin Wide SOIC |
| MIC5842BN | MIC5842YN | -40°C to +85°C | 18-Pin Plastic DIP |
| MIC5842BV | MIC5842YV | -40°C to +85°C | 20-Pin PLCC |
| MIC5842BWM | MIC5842YWM | -40°C to +85°C | 18-Pin Wide SOIC |

Functional Diagram



Pin Configuration

(20-Pin PLCC) Top View.



Absolute Maximum Ratings^(1,2,3)

| | |
|--|-----|
| At 25°C Free-Air Temperature and V_{SS} | 0V |
| Output Voltage, V_{CE} (MIC5841) | 50V |
| (MIC5842) | 80V |
| Output Voltage, $V_{CE(SUS)}$ (MIC5841) ⁽¹⁾ | 35V |
| (MIC5842) | 50V |
| Logic Supply Voltage, V_{DD} | 15V |
| VDD with Reference to V_{EE} | 25V |

| | |
|---|--------------------------|
| Emitter Supply Voltage, V_{EE} | -20V |
| Input Voltage Range, V_{IN} | -0.3V to $V_{DD} + 0.3V$ |
| Continuous Output Current, I_{OUT} | 500mA |
| Package Power Dissipation, P_D ⁽²⁾ | 1.82W |
| Operating Temperature Range, T_A | -55°C to +85°C |
| Storage Temperature Range, T_S | -65°C to +150°C |

Electrical CharacteristicsAt $T_A = 25^\circ\text{C}$ $V_{DD} = 5V$, $V_{SS} = V_{EE} = 0V$ (unless otherwise noted)

| Characteristic | Symbol | Applicable Devices | Test Conditions | Limits | | |
|--------------------------------------|---------------------|--------------------|--|--------|-----|------------------|
| | | | | Min | Max | Unit |
| Output Leakage Current | I_{CEX} | MIC5841 | $V_{OUT} = 50V$ | | 50 | μA |
| | | | $V_{OUT} = 50V, T_A = +70^\circ\text{C}$ | | 100 | |
| | | MIC5842 | $V_{OUT} = 80V$ | | 50 | |
| | | | $V_{OUT} = 80V, T_A = +70^\circ\text{C}$ | | 100 | |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | Both | $I_{OUT} = 100\text{mA}$ | | 1.1 | V |
| | | | $I_{OUT} = 200\text{mA}$ | | 1.3 | |
| | | | $I_{OUT} = 350\text{mA}, V_{DD} = 7.0V$ | | 1.6 | |
| Collector-Emitter Saturation Voltage | $V_{CE(SUS)}^{(5)}$ | MIC5841 | $I_{OUT} = 350\text{mA}, L = 2\text{mH}$ | 35 | | V |
| | | MIC5842 | $I_{OUT} = 350\text{mA}, L = 2\text{mH}$ | 50 | | |
| Input Voltage | $V_{IN(0)}$ | Both | | | 0.8 | V |
| | $V_{IN(1)}$ | Both | $V_{DD} = 12V$ | 10.5 | | |
| | | | $V_{DD} = 10V$ | 8.5 | | |
| Input Resistance | R_{IN} | Both | $V_{DD} = 12V$ | 50 | | $\text{k}\Omega$ |
| | | | $V_{DD} = 10V$ | 50 | | |
| | | | $V_{DD} = 5.0V$ | 50 | | |
| Supply Current | $I_{DD(ON)}$ | Both | All Drivers ON, $V_{DD} = 12V$ | | 16 | 1.6 |
| | | | All Drivers ON, $V_{DD} = 10V$ | | 14 | |
| | | | All Drivers ON, $V_{DD} = 5.0V$ | | 8.0 | |
| | $I_{DD(OFF)}$ | Both | All Drivers OFF, $V_{DD} = 12V$ | | 2.9 | |
| | | | All Drivers OFF, $V_{DD} = 10V$ | | 2.5 | |
| | | | All Drivers OFF, $V_{DD} = 5.0V$ | | 1.6 | |
| Clamp Diode Leakage Current | I_R | MIC5841 | $V_R = 50V$ | | 50 | μA |
| | | MIC5842 | $V_R = 80V$ | | 50 | |
| Clamp Diode Forward Voltage | V_F | Both | $I_F = 350\text{mA}$ | | 2.0 | V |

Electrical Characteristics

At $T_A = -55^\circ\text{C}$ $V_{DD} = 5\text{V}$, $V_{SS} = V_{EE} = 0\text{V}$ (unless otherwise noted)

| Characteristic | Symbol | Test Conditions | Limits | | |
|--------------------------------------|---------------|---|--------|-----|------------------|
| | | | Min | Max | Unit |
| Output Leakage Current | I_{CEX} | $V_{OUT} = 80\text{V}$ | | 50 | μA |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_{OUT} = 100\text{mA}$ | | 1.3 | V |
| | | $I_{OUT} = 200\text{mA}$ | | 1.5 | |
| | | $I_{OUT} = 350\text{mA}$, $V_{DD} = 7.0\text{V}$ | | 1.8 | |
| Input Voltage | $V_{IN(0)}$ | | | 0.8 | V |
| | $V_{IN(1)}$ | $V_{DD} = 12\text{V}$ | 10.5 | | |
| | | $V_{DD} = 5.0\text{V}$ | 3.5 | | |
| Input Resistance | R_{IN} | $V_{DD} = 12\text{V}$ | 35 | | $\text{k}\Omega$ |
| | | $V_{DD} = 10\text{V}$ | 35 | | |
| | | $V_{DD} = 5.0\text{V}$ | 35 | | |
| Supply Current | $I_{DD(ON)}$ | All Drivers ON, $V_{DD} = 12\text{V}$ | | 16 | mA |
| | | All Drivers ON, $V_{DD} = 10\text{V}$ | | 14 | |
| | | All Drivers ON, $V_{DD} = 5.0\text{V}$ | | 10 | |
| | $I_{DD(OFF)}$ | All Drivers OFF, $V_{DD} = 12\text{V}$ | | 3.5 | |
| | | All Drivers OFF, $V_{DD} = 5.0\text{V}$ | | 2.0 | |

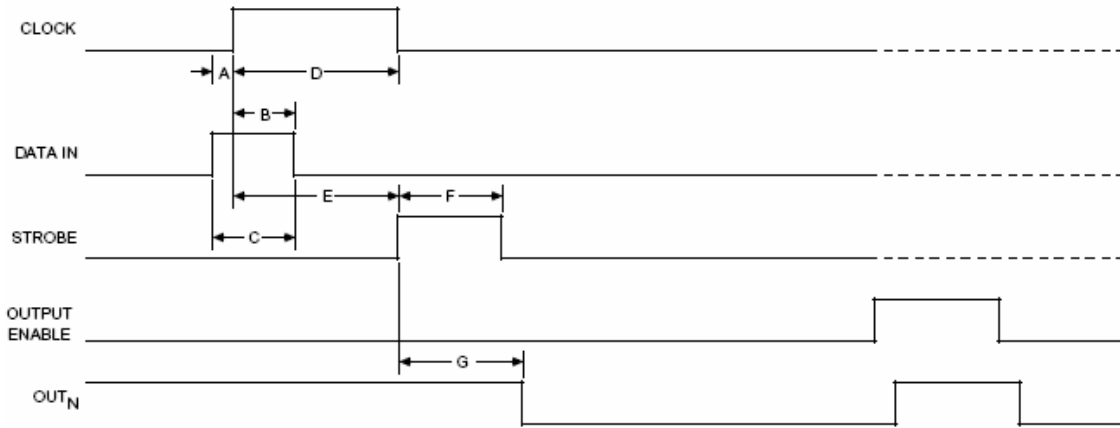
Electrical Characteristics

At $T_A = +125^\circ\text{C}$ $V_{DD} = 5\text{V}$, $V_{SS} = V_{EE} = 0\text{V}$ (unless otherwise noted)

| Characteristic | Symbol | Test Conditions | Limits | | |
|--------------------------------------|---------------|---|--------|-------|------------------|
| | | | Min | Max | Unit |
| Output Leakage Current | I_{CEX} | $V_{OUT} = 80\text{V}$ | | 500 | μA |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_{OUT} = 100\text{mA}$ | | 1.3 | V |
| | | $I_{OUT} = 200\text{mA}$ | | 1.5 | |
| | | $I_{OUT} = 350\text{mA}$, $V_{DD} = 7.0\text{V}$ | | 1.8 | |
| Input Voltage | $V_{IN(0)}$ | | | 0.8 | V |
| | $V_{IN(1)}$ | $V_{DD} = 12\text{V}$ | 10.5 | | |
| | | $V_{DD} = 5.0\text{V}$ | 3.5 | | |
| Input Resistance | R_{IN} | $V_{DD} = 12\text{V}$ | 50 | | $\text{k}\Omega$ |
| | | $V_{DD} = 10\text{V}$ | 50 | | |
| | | $V_{DD} = 5.0\text{V}$ | 50 | | |
| Supply Current | $I_{DD(ON)}$ | All Drivers ON, $V_{DD} = 12\text{V}$ | | 16 | mA |
| | | All Drivers ON, $V_{DD} = 10\text{V}$ | | 14 | |
| | | All Drivers ON, $V_{DD} = 5.0\text{V}$ | | 8 | |
| | $I_{DD(OFF)}$ | All Drivers OFF, $V_{DD} = 12\text{V}$ | | 2.9 | |
| | | All Drivers OFF, $V_{DD} = 5.0\text{V}$ | | 2.1.6 | |
| Clamp Diode Leakage Current | I_R | MIC5841A $V_R = 50\text{V}$ | | 1.6 | μA |
| | | MIC5842A $V_R = 80\text{V}$ | | 100 | |

Notes:

1. For Inductive load applications.
2. Derate at the rate of $18.2\text{mW}/^\circ\text{C}$ above $T_A = 25^\circ\text{C}$ (Plastic DIP)
3. CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.
4. Operation of these devices with standard TTL may require the use of appropriate pull-up resistors to insure an input logic HIGH.
5. Not 100% tested. Guaranteed by design.



Timing Conditions

(TA = 25°C Logic Levels are V_{DD} and V_{SS})

V_{DD} = 5V

| | |
|--|--------|
| A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)..... | 75 ns |
| B. Minimum Data Active Time After Clock Pulse (Data Hold Time) | 75 ns |
| C. Minimum Data Pulse Width | 150 ns |
| D. Minimum Clock Pulse Width..... | 150 ns |
| E. Minimum Time Between Clock Activation and Strobe | 300 ns |
| F. Minimum Strobe Pulse Width..... | 100 ns |
| G. Typical Time Between Strobe Activation and Output Transition..... | 500 ns |

SERIAL DATA present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

MIC5840 Family Truth Table

| Serial Data Input | Clock Input | Shift Register Contents | | | | | Serial Data Output | Strobe Input | Latch Contents | | | | | Output Enable | Output Contents | | | | | |
|-------------------|-------------|-------------------------|----------------|----------------|-----|----------------|--------------------|--------------|----------------|----------------|----------------|-----|----------------|---------------|-----------------|----------------|----------------|-----|----------------|--|
| | | I ₁ | I ₂ | I ₃ | ... | I ₈ | | | I ₁ | I ₂ | I ₃ | ... | I ₈ | | I ₁ | I ₂ | I ₃ | ... | I ₈ | |
| H | | H | R1 | R2 | ... | R7 | R7 | | | | | | | | | | | | | |
| L | | L | R1 | R2 | ... | R7 | R7 | | | | | | | | | | | | | |
| X | | R1 | R2 | R3 | ... | R8 | R8 | | | | | | | | | | | | | |
| | | X | X | X | ... | X | X | L | R1 | R2 | R3 | ... | R8 | | | | | | | |
| | | P1 | P2 | P3 | ... | P8 | P8 | H | P1 | P2 | P3 | ... | P8 | L | P1 | P2 | P3 | ... | P8 | |
| | | | | | | | | | X | X | X | ... | X | H | H | H | H | ... | H | |

L = Low Logic Level
 H = High Logic Level
 X = Irrelevant
 P = Present State
 R = Previous State

Typical Output Driver



Typical Input Circuits



Maximum Allowable Duty Cycle (Plastic DIP)

$V_{DD} = 5.0V$

| Number of Outputs ON ($I_{OUT} = 200mA$ $V_{DD} = 5.0V$) | Max. Allowable Duty Cycle at Ambient Temperature of | | | | |
|--|---|------|------|------|------|
| | 25°C | 40°C | 50°C | 60°C | 70°C |
| 8 | 85% | 72% | 64% | 55% | 46% |
| 7 | 97% | 82% | 73% | 63% | 53% |
| 6 | 100% | 96% | 85% | 73% | 62% |
| 5 | 100% | 100% | 100% | 88% | 75% |
| 4 | 100% | 100% | 100% | 100% | 93% |
| 3 | 100% | 100% | 100% | 100% | 100% |
| 2 | 100% | 100% | 100% | 100% | 100% |
| 1 | 100% | 100% | 100% | 100% | 100% |

$V_{DD} = 12V$

| Number of Outputs ON ($I_{OUT} = 200mA$ $V_{DD} = 12V$) | Max. Allowable Duty Cycle at Ambient Temperature of | | | | |
|---|---|------|------|------|------|
| | 25°C | 40°C | 50°C | 60°C | 70°C |
| 8 | 80% | 68% | 60% | 52% | 44% |
| 7 | 91% | 77% | 68% | 59% | 50% |
| 6 | 100% | 90% | 79% | 69% | 58% |
| 5 | 100% | 100% | 95% | 82% | 69% |
| 4 | 100% | 100% | 100% | 100% | 86% |
| 3 | 100% | 100% | 100% | 100% | 100% |
| 2 | 100% | 100% | 100% | 100% | 100% |
| 1 | 100% | 100% | 100% | 100% | 100% |

Typical Applications



Relay/Solenoid Driver MIC5842



MIC5841 Hammer Driver



MIC5841 Solenoid Driver with Output Enable



MIC5841 Level Shifting Lamp Driver with Darlington Emitters Tied to a Negative Supply

Typical Applications, Continued



MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
 TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

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Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331