

# 74HC4017-Q100; 74HCT4017-Q100

Johnson decade counter with 10 decoded outputs

Rev. 1 — 24 March 2014

Product data sheet

## 1. General description

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The 74HC4017-Q100; 74HCT4017-Q100 is a 5-stage Johnson decade counter with 10 decoded outputs ( $Q_0$  to  $Q_9$ ). It has an output from the most significant flip-flop ( $\overline{Q_5-9}$ ), two clock inputs ( $CP_0$  and  $\overline{CP_1}$ ) and an overriding asynchronous master reset input (MR). Either a LOW-to-HIGH transition at  $CP_0$  while  $\overline{CP_1}$  is LOW, or a HIGH-to-LOW transition at  $\overline{CP_1}$  while  $CP_0$  is HIGH, advances the counter. The  $\overline{Q_5-9}$  output is LOW while the counter is in states 5, 6, 7, 8 and 9. When cascading counters, it can be used to drive the  $CP_0$  input of the next counter. A HIGH on MR resets the counter to zero ( $Q_0 = \overline{Q_5-9} =$  HIGH;  $Q_1$  to  $Q_9 =$  LOW) independent of the clock inputs ( $CP_0$  and  $\overline{CP_1}$ ). An internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses provides automatic code correction of the counter. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

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- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
  - ◆ For 74HC4017-Q100: CMOS level
  - ◆ For 74HCT4017-Q100: TTL level
- Complies with JEDEC standard no. 7 A
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pF}$ ,  $R = 0\text{ }\Omega$ )
- Multiple package options



### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<b>74HC4017-Q100</b>				
74HC4017D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4017PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4017BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal-enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
<b>74HCT4017-Q100</b>				
74HCT4017D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4017BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal-enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

### 4. Functional diagram

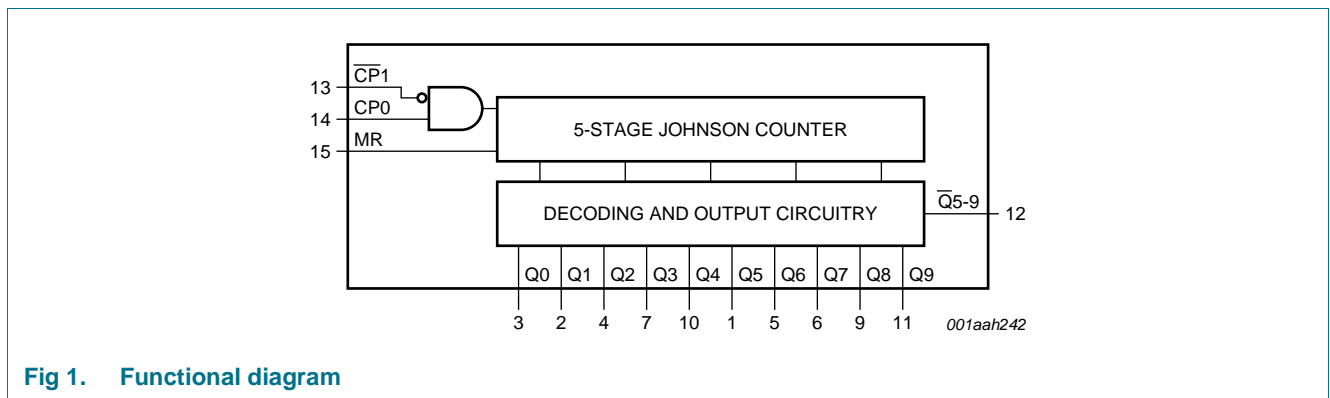


Fig 1. Functional diagram

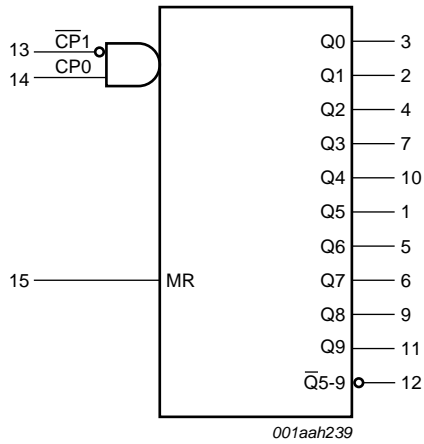


Fig 2. Logic symbol

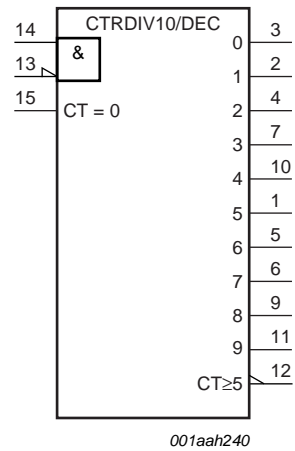


Fig 3. IEC logic symbol

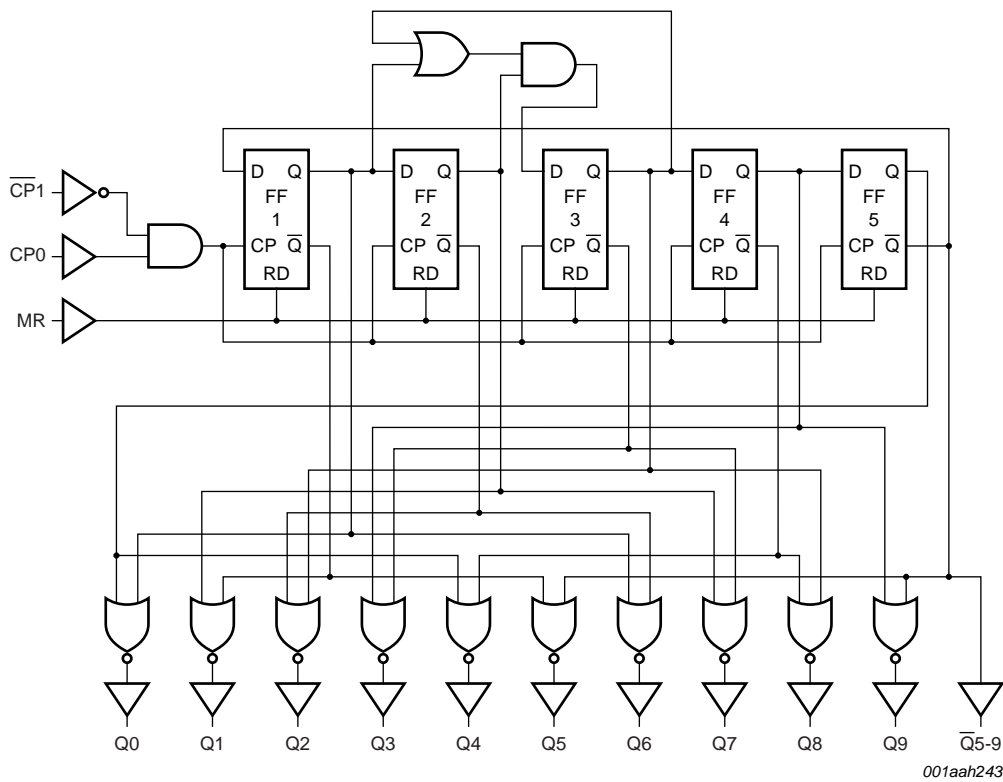
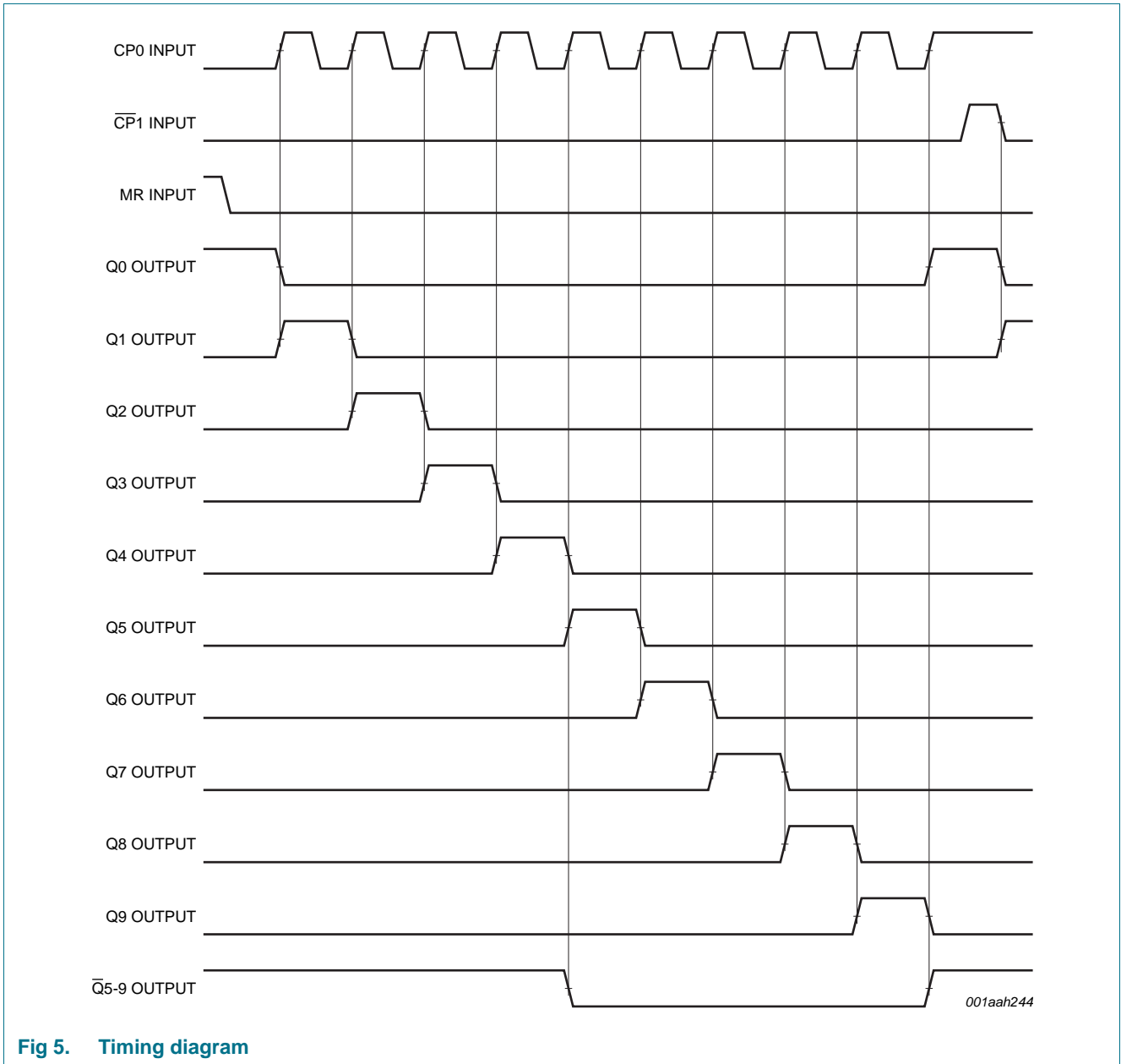


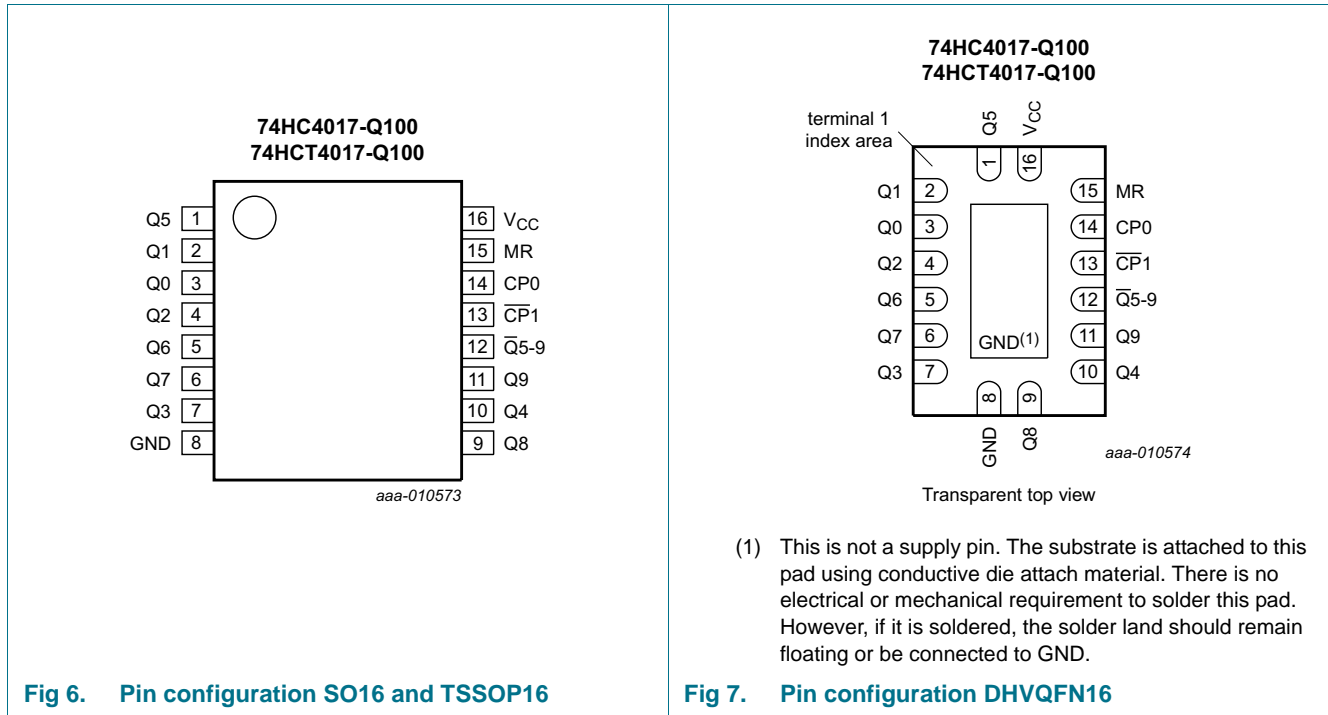
Fig 4. Logic diagram



**Fig 5. Timing diagram**

## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

**Table 2. Pin description**

Symbol	Pin	Description
Q[0:9]	3, 2, 4, 7, 10, 1, 5, 6, 9, 11	decoded output
GND	8	ground (0 V)
Q̄5-9	12	carry output (active LOW)
CP1	13	clock input (HIGH-to-LOW edge-triggered)
CP0	14	clock input (LOW-to-HIGH edge-triggered)
MR	15	master reset input (active HIGH)
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

MR	CP0	CP1	Operation
H	X	X	Q0 = $\overline{Q5-9}$ = HIGH; Q1 to Q9 = LOW
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

- [1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care;  
↑ = LOW-to-HIGH transition;  
↓ = HIGH-to-LOW transition;

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	[1]	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	[1]	±20	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C			
	SO16 package		[2]	500	mW
	TSSOP16 package		[3]	500	mW
	DHVQFN16 package		[4]	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
[2] P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.  
[3] P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.  
[4] P<sub>tot</sub> derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>74HC4017-Q100</b>						
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	ns/V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C
<b>74HCT4017-Q100</b>						
V <sub>CC</sub>	supply voltage		4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 4.5 V	-	1.67	139	ns/V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC4017-Q100</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT4017-Q100</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 0 A	-	-	8.0	-	80	-	160	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = 0 A								
		CP0 input	-	25	90	-	113	-	123	μA
		CP1 input	-	40	144	-	180	-	196	μA
		MR input	-	50	180	-	225	-	245	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF



## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$ ; see [Figure 11](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC4017-Q100</b>										
$t_{pd}$	propagation delay	CP0 to Qn; CP0 to $\overline{Q5-9}$ ; <a href="#">[1]</a> see <a href="#">Figure 10</a>								
		$V_{CC} = 2.0\text{ V}$	-	63	230	-	290	-	345	ns
		$V_{CC} = 4.5\text{ V}$	-	23	46	-	58	-	69	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	20	-	-	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	-	18	39	-	49	-	59	ns
		CP1 to Qn; $\overline{CP1}$ to $\overline{Q5-9}$ ; see <a href="#">Figure 10</a>								
		$V_{CC} = 2.0\text{ V}$	-	61	250	-	315	-	375	ns
		$V_{CC} = 4.5\text{ V}$	-	22	50	-	63	-	75	ns
$t_{PHL}$	HIGH to LOW propagation delay	MR to Q[1:9]; see <a href="#">Figure 10</a>								
		$V_{CC} = 2.0\text{ V}$	-	52	230	-	290	-	345	ns
		$V_{CC} = 4.5\text{ V}$	-	19	46	-	58	-	69	ns
		$V_{CC} = 6.0\text{ V}$	-	15	39	-	49	-	59	ns
$t_{PLH}$	LOW to HIGH propagation delay	MR to $\overline{Q5-9}$ , Q0; see <a href="#">Figure 10</a>								
		$V_{CC} = 2.0\text{ V}$	-	55	230	-	290	-	345	ns
		$V_{CC} = 4.5\text{ V}$	-	20	46	-	58	-	69	ns
$t_t$	transition time	see <a href="#">Figure 10</a> <a href="#">[2]</a>								
		$V_{CC} = 2.0\text{ V}$	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5\text{ V}$	-	7	15	-	19	-	22	ns
$t_w$	pulse width	$V_{CC} = 6.0\text{ V}$	-	6	13	-	16	-	19	ns
		CP0 and $\overline{CP1}$ (HIGH or LOW); see <a href="#">Figure 9</a>								
		$V_{CC} = 2.0\text{ V}$	80	17	-	100	-	120	-	ns
		$V_{CC} = 4.5\text{ V}$	16	6	-	20	-	24	-	ns
		$V_{CC} = 6.0\text{ V}$	14	5	-	17	-	20	-	ns
		MR (HIGH); see <a href="#">Figure 9</a>								
		$V_{CC} = 2.0\text{ V}$	80	19	-	100	-	120	-	ns
$V_{CC} = 4.5\text{ V}$	16	7	-	20	-	24	-	ns		
$V_{CC} = 6.0\text{ V}$	14	6	-	17	-	20	-	ns		

**Table 7. Dynamic characteristics ...continued**  
*GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF; see [Figure 11](#).*

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>su</sub>	set-up time	CP1 to CP0; CP0 to CP1; see <a href="#">Figure 8</a>								
		V <sub>CC</sub> = 2.0 V	50	-8	-	65	-	75	-	ns
		V <sub>CC</sub> = 4.5 V	10	-3	-	13	-	15	-	ns
		V <sub>CC</sub> = 6.0 V	9	-2	-	11	-	13	-	ns
t <sub>h</sub>	hold time	CP1 to CP0; CP0 to CP1; see <a href="#">Figure 8</a>								
		V <sub>CC</sub> = 2.0 V	50	17	-	65	-	75	-	ns
		V <sub>CC</sub> = 4.5 V	10	6	-	13	-	15	-	ns
		V <sub>CC</sub> = 6.0 V	9	5	-	11	-	13	-	ns
t <sub>rec</sub>	recovery time	MR to CP0 and MR to CP1; see <a href="#">Figure 9</a>								
		V <sub>CC</sub> = 2.0 V	5	-17	-	5	-	5	-	ns
		V <sub>CC</sub> = 4.5 V	5	-6	-	5	-	5	-	ns
		V <sub>CC</sub> = 6.0 V	5	-5	-	5	-	5	-	ns
f <sub>max</sub>	maximum frequency	CP0 or CP1; see <a href="#">Figure 9</a>								
		V <sub>CC</sub> = 2.0 V	6.0	23	-	4.8	-	4.0	-	MHz
		V <sub>CC</sub> = 4.5 V	30	70	-	24	-	20	-	MHz
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	77	-	-	-	-	-	MHz
		V <sub>CC</sub> = 6.0 V	25	83	-	28	-	24	-	MHz
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 5 V; f <sub>i</sub> = 1 MHz <a href="#">[3]</a>	-	35	-	-	-	-	-	pF
<b>74HCT4017-Q100</b>										
t <sub>pd</sub>	propagation delay	CP0 to Q <sub>n</sub> ; CP0 to Q5-9; see <a href="#">Figure 10</a> <a href="#">[1]</a>								
		V <sub>CC</sub> = 4.5 V	-	25	46	-	58	-	69	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	21	-	-	-	-	-	ns
		CP1 to Q <sub>n</sub> ; CP1 to Q5-9; see <a href="#">Figure 10</a>								
		V <sub>CC</sub> = 4.5 V	-	25	50	-	63	-	75	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	21	-	-	-	-	-	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	MR to Q[1:9]; see <a href="#">Figure 10</a>								
		V <sub>CC</sub> = 4.5 V	-	22	46	-	58	-	69	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	MR to Q5-9, Q0; see <a href="#">Figure 10</a>								
		V <sub>CC</sub> = 4.5 V	-	20	46	-	58	-	69	ns

**Table 7. Dynamic characteristics ...continued**  
*GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF; see [Figure 11](#).*

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_t$	transition time	see <a href="#">Figure 10</a> [2]								
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
$t_w$	pulse width	CP0 and $\overline{CP1}$ (HIGH or LOW); see <a href="#">Figure 9</a>								
		$V_{CC} = 4.5$ V	16	7	-	20	-	24	-	ns
		MR (HIGH); see <a href="#">Figure 9</a>								
		$V_{CC} = 4.5$ V	16	4	-	20	-	24	-	ns
$t_{su}$	set-up time	$\overline{CP1}$ to CP0; CP0 to $\overline{CP1}$ ; see <a href="#">Figure 8</a>								
		$V_{CC} = 4.5$ V	10	-3	-	13	-	15	-	ns
$t_h$	hold time	$\overline{CP1}$ to CP0; CP0 to $\overline{CP1}$ ; see <a href="#">Figure 8</a>								
		$V_{CC} = 4.5$ V	10	6	-	13	-	15	-	ns
$t_{rec}$	recovery time	MR to CP0 and MR to $\overline{CP1}$ ; see <a href="#">Figure 9</a>								
		$V_{CC} = 4.5$ V	5	-5	-	5	-	5	-	ns
$f_{max}$	maximum frequency	CP0 or $\overline{CP1}$ ; see <a href="#">Figure 9</a>								
		$V_{CC} = 4.5$ V	30	61	-	24	-	20	-	MHz
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	67	-	-	-	-	-	MHz
$C_{PD}$	power dissipation capacitance	$V_I = GND$ to $V_{CC} - 1.5$ V; [3] $V_{CC} = 5$ V; $f_i = 1$ MHz	-	36	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

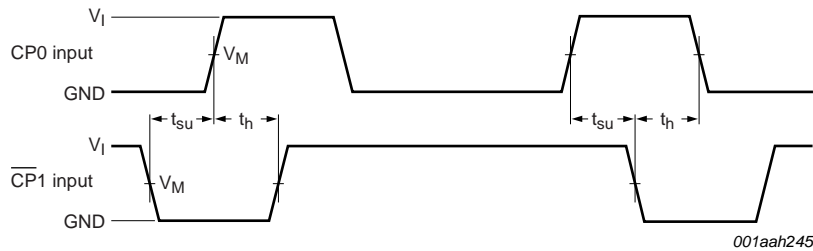
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

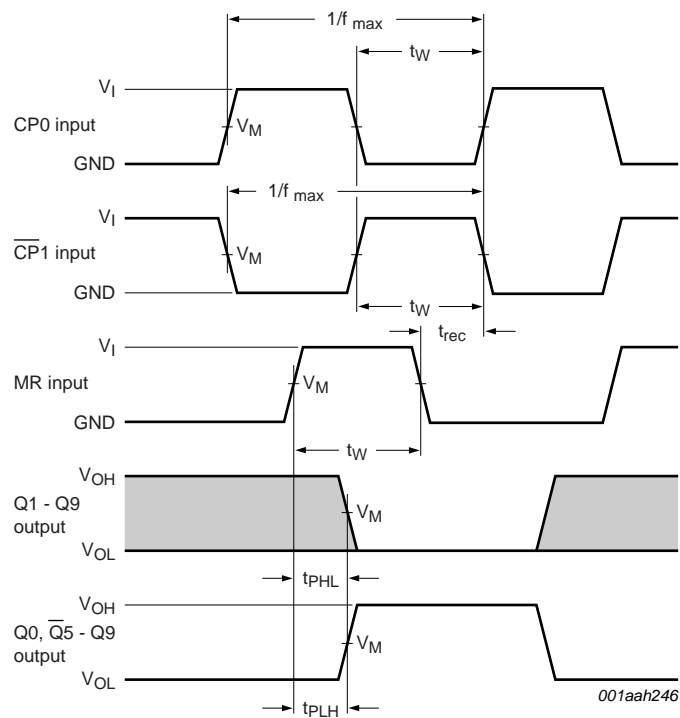
## 11. Waveforms



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

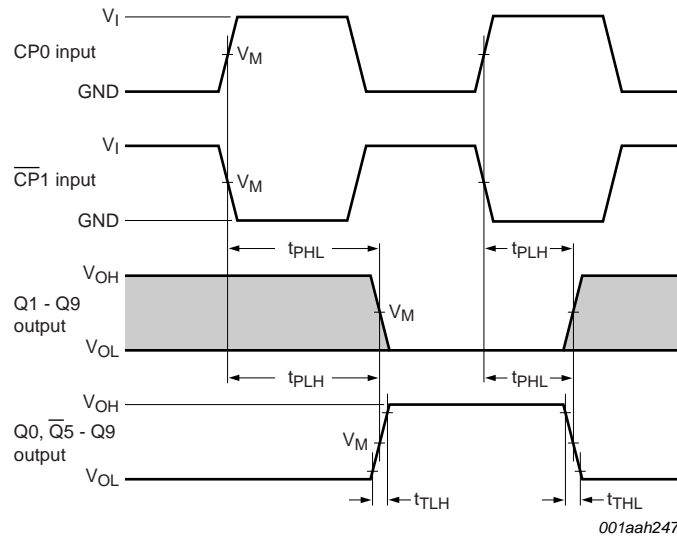
**Fig 8. Waveforms showing the set-up and hold times for CP0 to CP1 and CP1 to CP0**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 9. Waveforms showing minimum pulse widths, maximum CP input frequencies, recovery times and output propagation delays**



Measurement points are given in [Table 8](#).

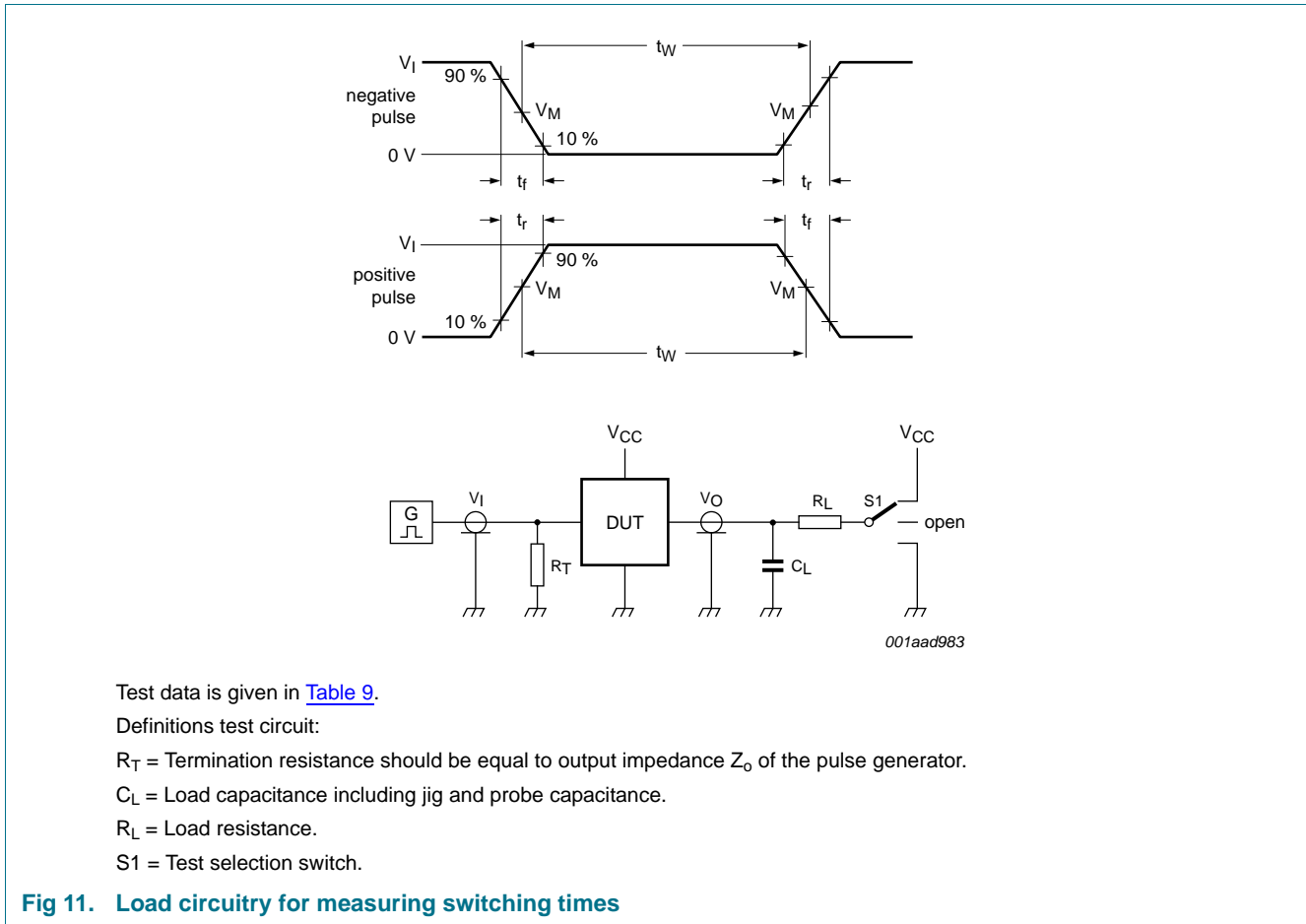
$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Conditions:  $\overline{CP1}$  = LOW while CP0 is triggered on a LOW-to-HIGH transition and CP0 = HIGH, while  $\overline{CP1}$  is triggered on a HIGH-to-LOW transition.

**Fig 10. Waveforms showing propagation delays for CP to Qn outputs and output transition times**

**Table 8. Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74HC4017-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT4017-Q100	1.3 V	1.3 V



**Fig 11. Load circuitry for measuring switching times**

**Table 9. Test data**

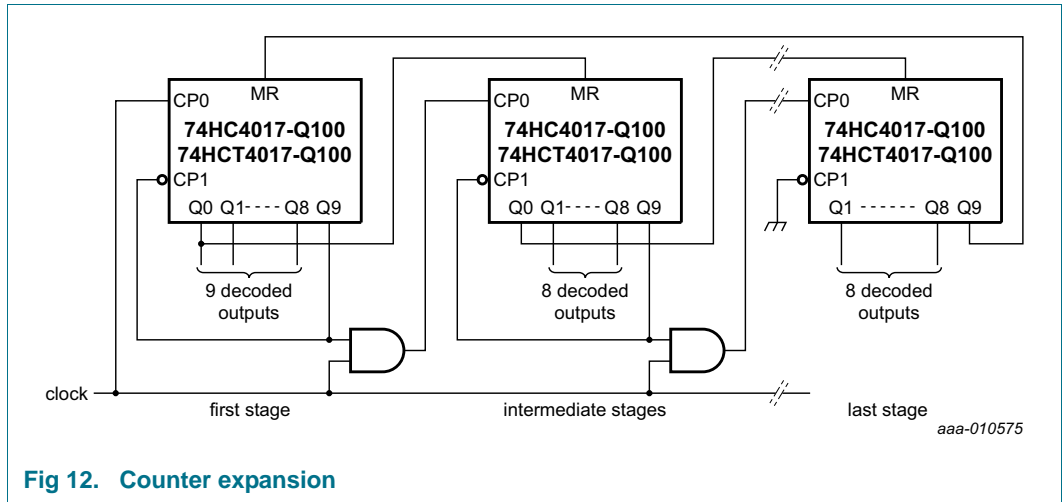
Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HC4017-Q100	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74HCT4017-Q100	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

## 12. Application information

Some examples of applications for the 74HC4017-Q100; 74HCT4017-Q100 are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer

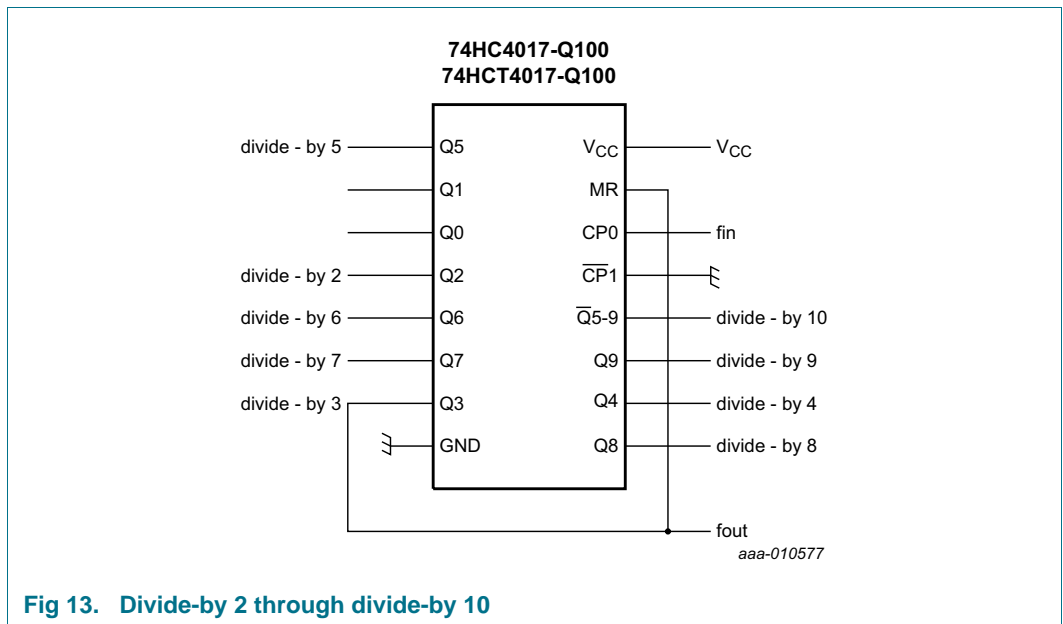
[Figure 12](#) shows a technique for extending the number of decoded output states for the 74HC4017-Q100; 74HCT4017-Q100. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).



**Fig 12. Counter expansion**

**Remark:** Do not enable the counter on  $\overline{CP1}$  when CP0 is HIGH, or on CP0 when  $\overline{CP1}$  is LOW. It causes an extra count.

Figure 13 shows an example of a divide-by 2 through divide-by 10 circuit using one 74HC4017-Q100; 74HCT4017-Q100. Since the 74HC4017-Q100; 74HCT4017-Q100 has an asynchronous reset, the output pulse widths are narrow (minimum expected pulse width is 6 ns). The output pulse widths can be enlarged by inserting an RC network at the MR input.



**Fig 13. Divide-by 2 through divide-by 10**

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

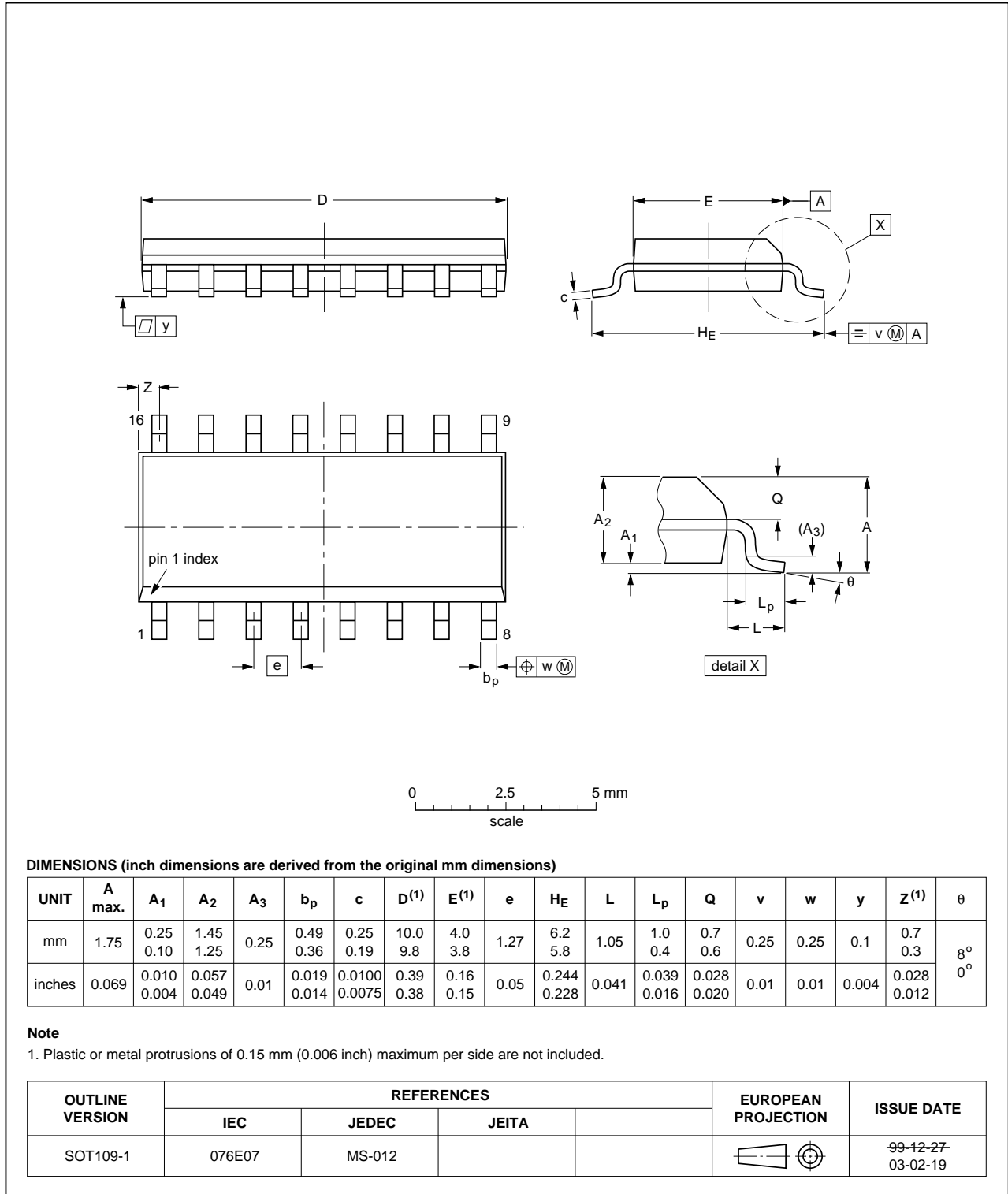


Fig 14. Package outline SOT109-1 (SO16)



TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

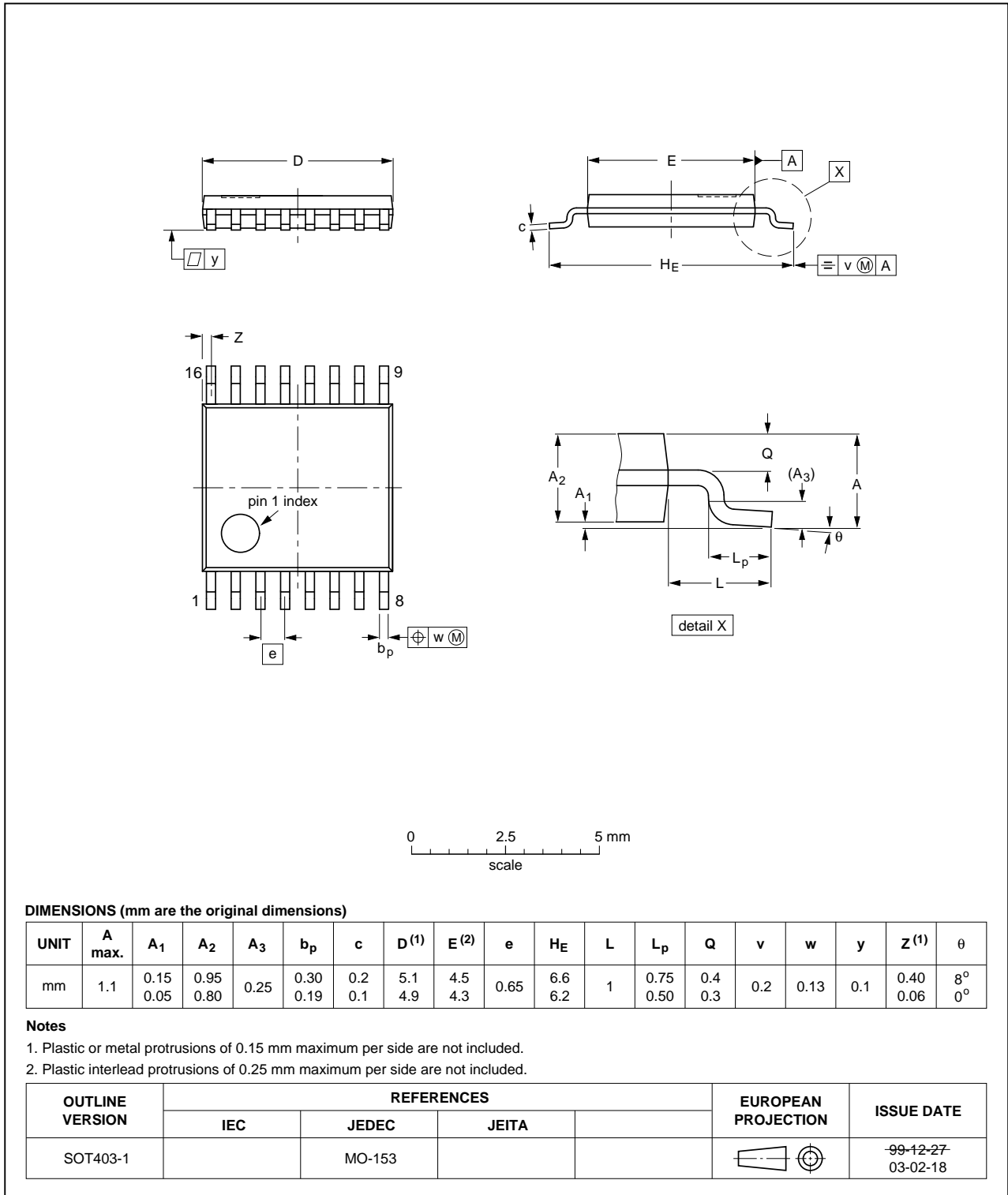
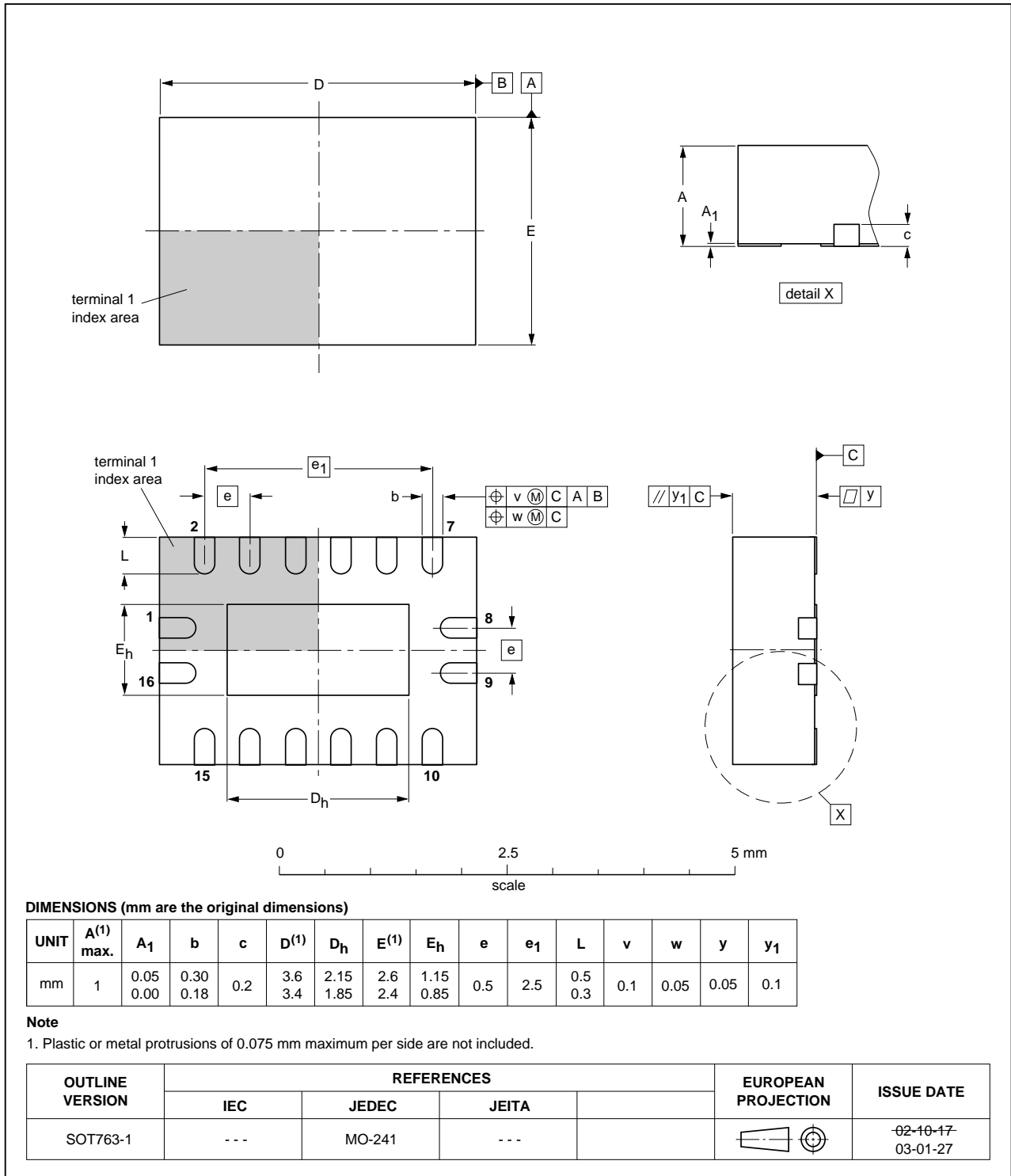


Fig 15. Package outline SOT403-1 (TSSOP16)

**DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm**

**SOT763-1**



**Fig 16. Package outline SOT763-1 (DHVQFN16)**

## 14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4017_Q100 v.1	20140324	Product data sheet	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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