FAN4803

8-Pin PFC and PWM Controller Combo

Features

- Internally synchronized PFC and PWM in one 8-pin IC
- Patented one-pin voltage error amplifier with advanced input current shaping technique
- Peak or average current, continuous boost, leading edge PFC (Input Current Shaping Technology)
- High efficiency trailing-edge current mode PWM
- Low supply currents; start-up: 150µA typ., operating: 2mA typ.
- Synchronized leading and trailing edge modulation
- Reduces ripple current in the storage capacitor between the PFC and PWM sections
- Overvoltage, UVLO, and brownout protection
- PFC V_{CC}OVP with PFC Soft Start

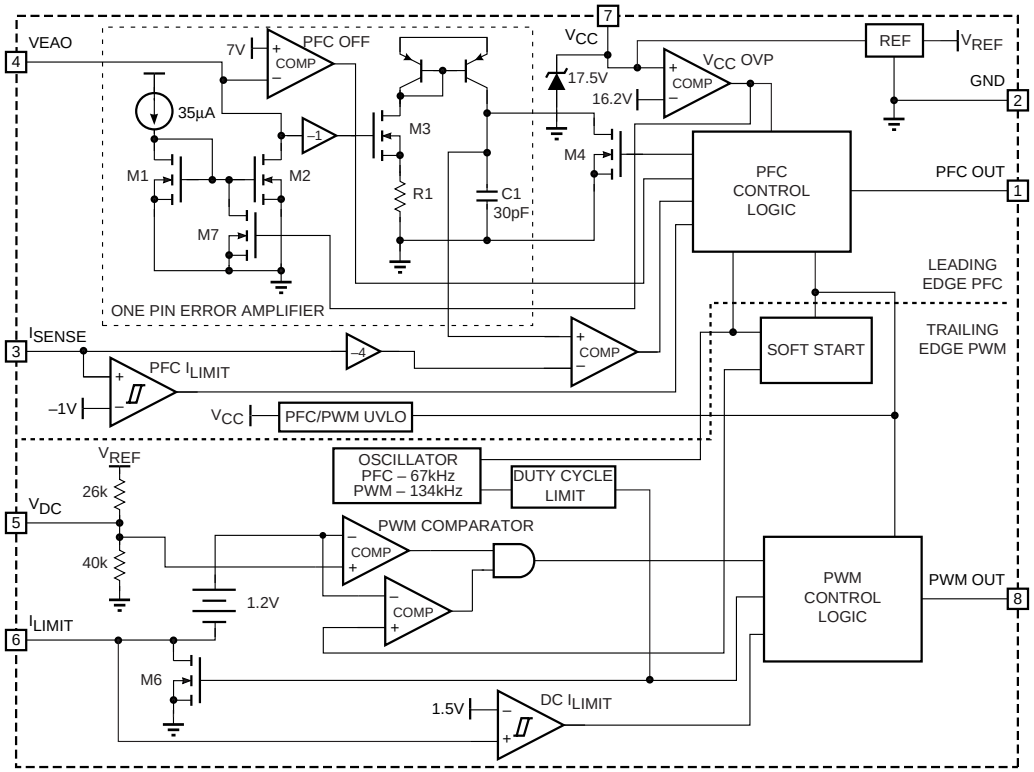
General Description

The FAN4803 is a space-saving controller for power factor corrected, switched mode power supplies that offers very low start-up and operating currents.

Power Factor Correction (PFC) offers the use of smaller, lower cost bulk capacitors, reduces power line loading and stress on the switching FETs, and results in a power supply fully compliant to IEC1000-3-2 specifications. The FAN4803 includes circuits for the implementation of a leading edge, average current "boost" type PFC and a trailing edge, PWM.

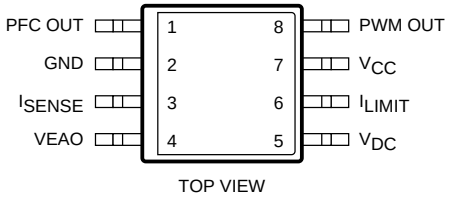
The FAN4803-1's PFC and PWM operate at the same frequency, 67kHz. The PFC frequency of the FAN4803-2 is automatically set at half that of the 134kHz PWM. This higher frequency allows the user to design with smaller PWM components while maintaining the optimum operating frequency for the PFC. An overvoltage comparator shuts down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting for enhanced system reliability.

Block Diagram



Pin Configuration

FAN4803
8-Pin PDIP (P08)
8-Pin SOIC (S08)



TOP VIEW

Pin Description

Pin	Name	Function
1	PFC OUT	PFC driver output
2	GND	Ground
3	I_{SENSE}	Current sense input to the PFC current limit comparator
4	VEAO	PFC one-pin error amplifier input
5	V_{DC}	PWM voltage feedback input
6	I_{LIMIT}	PWM current limit comparator input
7	V_{CC}	Positive supply (may require an external shunt regulator)
8	PWM OUT	PWM driver output

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Parameter	Min	Max	Unit
I_{CC} Current (average)		40	mA
V_{CC} MAX		18.3	V
I_{SENSE} Voltage	-5	1	V
Voltage on Any Other Pin	GND – 0.3	V_{CC} + 0.3	V
Peak PFC OUT Current, Source or Sink		1	A
Peak PWM OUT Current, Source or Sink		1	A
PFC OUT, PWM OUT Energy Per Cycle		1.5	µJ
Junction Temperature		150	°C
Storage Temperature Range	-65°	150	°C
Lead Temperature (Soldering, 10 sec)		260	°C
Thermal Resistance (θ_{JA})			
Plastic DIP		110	°C/W
Plastic SOIC		160	°C/W

Operating Conditions

Temperature Range	
FAN4803CS-X	0°C to 70°C
FAN4803CP-X	0°C to 70°C

Electrical Characteristics

Unless otherwise specified, V_{CC} = 15V, T_A = Operating Temperature Range (Note 1)

Symbol	Parameter	Conditions	Min	TYP	MAX	UNITS
One-pin Error Amplifier						
	V_{EAO} Output Current	T_A = 25°C, V_{EAO} = 6V	34.0	36.5	39.0	µA
	Line Regulation	10V < V_{CC} < 15V, V_{EAO} = 6V		0.1	0.3	µA
V_{CC} OVP Comparator						
	Threshold Voltage		15.5	16.3	16.8	V
PFC I_{LIMIT} Comparator						
	Threshold Voltage		-0.9	-1	-1.15	V
	Delay to Output			150	300	ns
DC I_{LIMIT} Comparator						
	Threshold Voltage		1.4	1.5	1.6	V
	Delay to Output			150	300	ns
Oscillator						
	Initial Accuracy	T_A = 25°C	60	67	74	kHz
	Voltage Stability	10V < V_{CC} < 15V		1		%
	Temperature Stability			2		%
	Total Variation	Over Line and Temp	60	67	74.5	kHz
	Dead Time	PFC Only	0.3	0.45	0.65	µs
PFC						
	Minimum Duty Cycle	V_{EAO} > 7.0V,I_{SENSE} = -0.2V			0	%
	Maximum Duty Cycle	V_{EAO} < 4.0V,I_{SENSE} = 0V	90	95		%
	Output Low Impedance			8	15	Ω
	Output Low Voltage	I_{OUT} = –100mA		0.8	1.5	V
		I_{OUT} = –10mA, V_{CC} = 8V		0.7	1.5	V
	Output High Impedance			8	15	Ω
	Output High Voltage	I_{OUT} = 100mA, V_{CC} = 15V	13.5	14.2		V
	Rise/Fall Time	C_L = 1000pF		50		ns
PWM						
	Duty Cycle Range	FAN4803-2	0-41	0-47	0-50	%
		FAN4803-1	0-49.5		0-50	%
	Output Low Impedance			8	15	Ω
	Output Low Voltage	I_{OUT} = –100mA		0.8	1.5	V
		I_{OUT} = –10mA, V_{CC} = 8V		0.7	1.5	V
	Output High Impedance			8	15	Ω
	Output High Voltage	I_{OUT} = 100mA, V_{CC} = 15V	13.5	14.2		V
	Rise/Fall Time	C_L = 1000pF		50		ns
Supply						
	V_{CC} Clamp Voltage (V_{CCZ})	I_{CC} = 10mA	16.7	17.5	18.3	V
	Start-up Current	V_{CC} = 11V, C_L = 0		0.2	0.4	mA
	Operating Current	V_{CC} = 15V, C_L = 0		2.5	4	mA
	Undervoltage Lockout Threshold		11.5	12	12.5	V
	Undervoltage Lockout Hysteresis		2.4	2.9	3.4	V

Note:

1. Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Functional Description

The FAN4803 consists of an average current mode boost Power Factor Corrector (PFC) front end followed by a synchronized Pulse Width Modulation (PWM) controller. It is distinguished from earlier combo controllers by its low pin count, innovative input current shaping technique, and very low start-up and operating currents. The PWM section is dedicated to peak current mode operation. It uses conventional trailing-edge modulation, while the PFC uses leading-edge modulation. This patented Leading Edge/Trailing Edge (LETE) modulation technique helps to minimize ripple current in the PFC DC buss capacitor.

The FAN4803 is offered in two versions. The FAN4803-1 operates both PFC and PWM sections at 67kHz, while the FAN4803-2 operates the PWM section at twice the frequency (134kHz) of the PFC. This allows the use of smaller PWM magnetics and output filter components, while minimizing switching losses in the PFC stage.

In addition to power factor correction, several protection features have been built into the FAN4803. These include soft start, redundant PFC over-voltage protection, peak current limiting, duty cycle limit, and under voltage lockout (UVLO). See Figure 12 for a typical application.

Detailed Pin Descriptions

V_{EAO}

This pin provides the feedback path which forces the PFC output to regulate at the programmed value. It connects to programming resistors tied to the PFC output voltage and is shunted by the feedback compensation network.

I_{SENSE}

This pin ties to a resistor or current sense transformer which senses the PFC input current. This signal should be negative with respect to the IC ground. It internally feeds the pulse-by-pulse current limit comparator and the current sense feedback signal. The I_{LIMIT} trip level is –1V. The I_{SENSE} feedback is internally multiplied by a gain of four and compared against the internal programmed ramp to set the PFC duty cycle. The intersection of the boost inductor current downslope with the internal programming ramp determines the boost off-time.

V_{DC}

This pin is typically tied to the feedback opto-collector. It is tied to the internal 5V reference through a 26kΩ resistor and to GND through a 40kΩ resistor.

I_{LIMIT}

This pin is tied to the primary side PWM current sense resistor or transformer. It provides the internal pulse-by-pulse current limit for the PWM stage (which occurs at 1.5V) and the peak current mode feedback path for the current mode control of the PWM stage. The current ramp is offset internally by 1.2V and then compared against the opto feedback voltage to set the PWM duty cycle.

PFC OUT and PWM OUT

PFC OUT and PWM OUT are the high-current power drivers capable of directly driving the gate of a power MOSFET with peak currents up to ±1A. Both outputs are actively held low when V_{CC} is below the UVLO threshold level.

V_{CC}

V_{CC} is the power input connection to the IC. The V_{CC} start-up current is 150µA . The no-load I_{CC} current is 2mA. V_{CC} quiescent current will include both the IC biasing currents and the PFC and PWM output currents. Given the operating frequency and the MOSFET gate charge (Qg), average PFC and PWM output currents can be calculated as I_{OUT} = Qg x F. The average magnetizing current required for any gate drive transformers must also be included. The V_{CC} pin is also assumed to be proportional to the PFC output voltage. Internally it is tied to the V_{CC}OVP comparator (16.2V) providing redundant high-speed over-voltage protection (OVP) of the PFC stage. V_{CC} also ties internally to the UVLO circuitry, enabling the IC at 12V and disabling it at 9.1V. V_{CC} must be bypassed with a high quality ceramic bypass capacitor placed as close as possible to the IC. Good bypassing is critical to the proper operation of the FAN4803.

V_{CC} is typically produced by an additional winding off the boost inductor or PFC Choke, providing a voltage that is proportional to the PFC output voltage. Since the V_{CC}OVP max voltage is 16.2V, an internal shunt limits V_{CC} overvoltage to an acceptable value. An external clamp, such as shown in Figure 1, is desirable but not necessary.

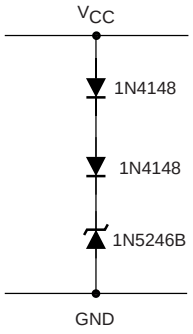


Figure 1. Optional V_{CC} Clamp

V_{CC} is internally clamped to 16.7V minimum, 18.3V maximum. This limits the maximum V_{CC} that can be applied to the IC while allowing a V_{CC} which is high enough to trip the V_{CC}OVP. The max current through this zener is 10mA. External series resistance is required in order to limit the current through this Zener in the case where the V_{CC} voltage exceeds the zener clamp level.

GND

GND is the return point for all circuits associated with this part. Note: a high-quality, low impedance ground is critical to the proper operation of the IC. High frequency grounding techniques should be used.

Power Factor Correction

Power factor correction makes a nonlinear load look like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with, and proportional to, the line voltage. This is defined as a unity power factor is (one). A common class of nonlinear load is the input of a most power supplies, which use a bridge rectifier and capacitive input filter fed from the line. Peak-charging effect, which occurs on the input filter capacitor in such a supply, causes brief high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such a supply presents a power factor to the line of less than one (another way to state this is that it causes significant current harmonics to appear at its input). If the input current drawn by such a supply (or any other nonlinear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the AC line and a unity power factor will be achieved.

To hold the input current draw of a device drawing power from the AC line in phase with, and proportional to, the input voltage, a way must be found to prevent that device from loading the line except in proportion to the instantaneous line voltage. The PFC section of the FAN4803 uses a boost-mode DC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage. No filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges, at twice line frequency, from zero volts to the peak value of the AC input and back to zero. By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current that the converter draws from the power line matches the instantaneous line voltage. One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is 385VDC, to allow for a high line of 270VAC$_{RMS}$. The other condition is that the current that the converter is allowed to draw from the line at any given instant must be proportional to the line voltage.

Since the boost converter topology in the FAN4803 PFC is of the current-averaging type, no slope compensation is required.

Leading/Trailing Modulation

Conventional Pulse Width Modulation (PWM) techniques employ trailing edge modulation in which the switch will turn ON right after the trailing edge of the system clock. The error amplifier output voltage is then compared with the modulating ramp. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned OFF. When the switch is ON, the inductor current will ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 2 shows a typical trailing edge control scheme.

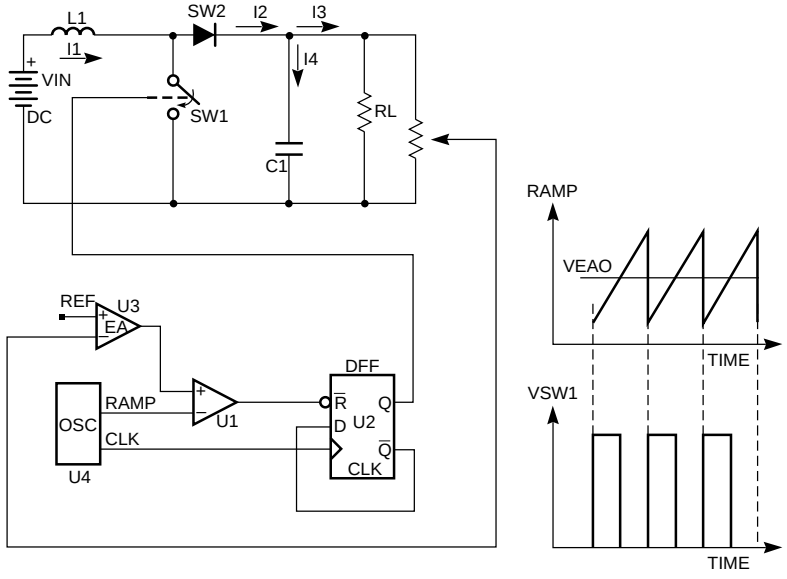


Figure 2. Typical Trailing Edge Control Scheme.

In the case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during the OFF time of the switch. Figure 3 shows a leading edge control scheme.

One of the advantages of this control technique is that it requires only one system clock. Switch 1 (SW1) turns OFF and Switch 2 (SW2) turns ON at the same instant to minimize the momentary “no-load” period, thus lowering ripple voltage generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC’s output ripple voltage can be reduced by as much as 30% using this method, substantially reducing dissipation in the high-voltage PFC capacitor.

Typical Applications

One Pin Error Amp

The FAN4803 utilizes a one pin voltage error amplifier in the PFC section (VEAO). The error amplifier is in reality a current sink which forces 35µA through the output programming resistor. The nominal voltage at the VEAO pin is 5V. The VEAO voltage range is 4 to 6V. For a 11.3MΩ resistor chain to the boost output voltage and 5V steady state at the VEAO, the boost output voltage would be 400V.

Programming Resistor Value

Equation 1 calculates the required programming resistor value.

$$Rp = \frac{V_{BOOST} - V_{EAO}}{I_{PGM}} = \frac{400V - 5.0V}{35\mu A} = 113M\Omega \quad (1)$$

PFC Voltage Loop Compensation

The voltage-loop bandwidth must be set to less than 120Hz to limit the amount of line current harmonic distortion. A typical crossover frequency is 30Hz. Equation 1, for simplicity, assumes that the pole capacitor dominates the error amplifier gain at the loop unity-gain frequency. Equation 2 places a pole at the crossover frequency, providing 45 degrees of phase margin. Equation 3 places a zero one decade prior to the pole. Bode plots showing the overall gain and phase are shown in Figures 5 and 6. Figure 4 displays a simplified model of the voltage loop.

$$C_{COMP} = \frac{Pin}{R_p \times V_{BOOST} \times \Delta VEAO \times C_{OUT} \times (2 \times \pi \times f)^2} \quad (2)$$

$$C_{COMP} = \frac{300W}{11.3M\Omega \times 400V \times 0.5V \times 220\mu F \times (2 \times \pi \times 30Hz)^2}$$

$$C_{COMP} = 16nF$$

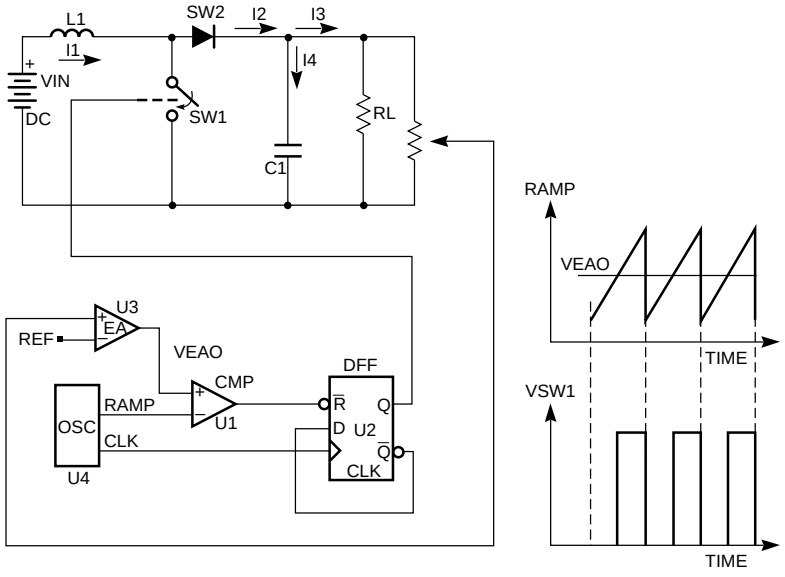


Figure 3. Typical Leading Edge Control Scheme.

$$R_{COMP} = \frac{1}{2 \times \pi \times f \times C_{COMP}} \quad (3)$$

$$R_{COMP} = \frac{1}{62\,8 \times 30Hz \times 16nF} = 330k\Omega$$

$$C_{ZERO} = \frac{1}{2 \times \pi \times \frac{f}{10} \times R_{COMP}} \quad (4)$$

$$C_{ZERO} = \frac{1}{6.28 \times 3Hz \times 330k\Omega} = 016\mu F$$

Internal Voltage Ramp

The internal ramp current source is programmed by way of the VEAO pin voltage. Figure 7 displays the internal ramp current vs. the VEAO voltage. This current source is used to develop the internal ramp by charging the internal 30pF +12/ –10% capacitor. See Figures 10 and 11. The frequency of the internal programming ramp is set internally to 67kHz.

PFC Current Sense Filtering

In DCM, the input current wave shaping technique used by the FAN4803 could cause the input current to run away. In order for this technique to be able to operate properly under DCM, the programming ramp must meet the boost inductor current down-slope at zero amps. Assuming the programming ramp is zero under light load, the OFF-time will be terminated once the inductor current reaches zero.

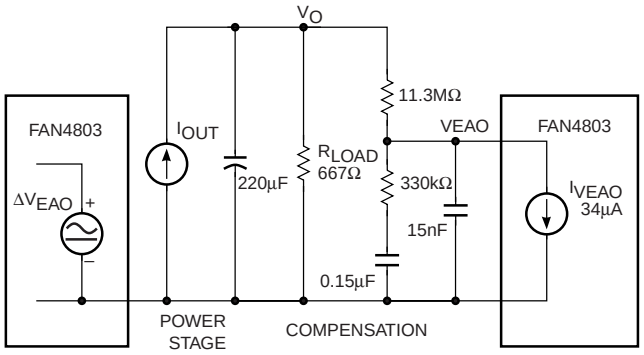


Figure 4. Voltage Control Loop

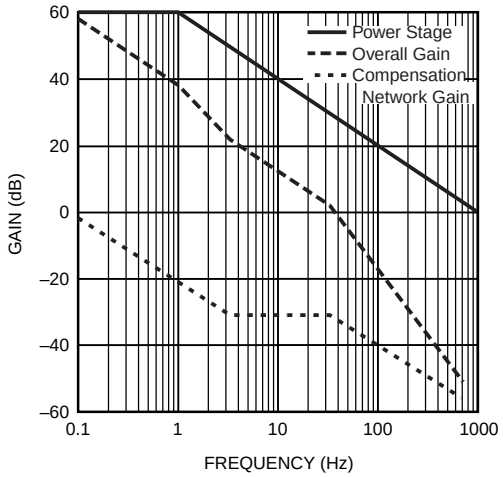


Figure 5. Voltage Loop Gain

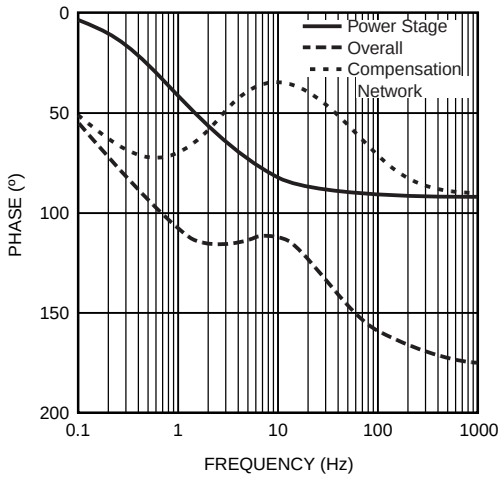


Figure 6. Voltage Loop Phase

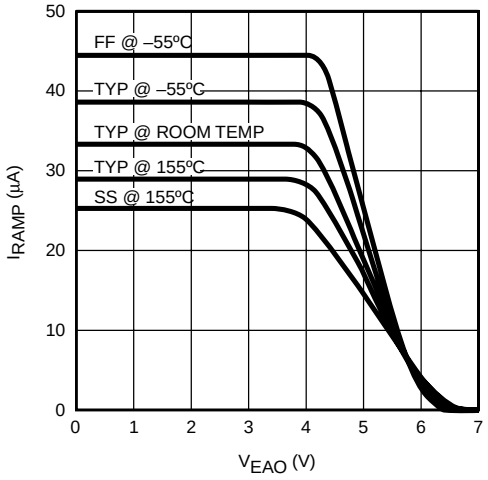


Figure 7. Internal Ramp Current vs. VEAO

Subsequently the PFC gate drive is initiated, eliminating the necessary dead time needed for the DCM mode. This forces the output to run away until the V_{CC} OVP shuts down the PFC. This situation is corrected by adding an offset voltage to the current sense signal, which forces the duty cycle to zero at light loads. This offset prevents the PFC from operating in the DCM and forces pulse-skipping from CCM to no-duty, avoiding DMC operation. External filtering to the current sense signal helps to smooth out the sense signal, expanding the operating range slightly into the DCM range, but this should be done carefully, as this filtering also reduces the bandwidth of the signal feeding the pulse-by-pulse current limit signal. Figure 9 displays a typical circuit for adding offset to I_{SENSE} at light loads.

PFC Start-Up and Soft Start

During steady state operation VEAO draws 35µA. At start-up the internal current mirror which sinks this current is defeated until V_{CC} reaches 12V. This forces the PFC error voltage to V_{CC} at the time that the IC is enabled. With leading edge modulation V_{CC} on the VEAO pin forces zero duty on the PFC output. When selecting external compensation components and V_{CC} supply circuits VEAO must not be prevented from reaching 6V prior to V_{CC} reaching 12V in the turn-on sequence. This will guarantee that the PFC stage will enter soft-start. Once V_{CC} reaches 12V the 35µA VEAO current sink is enabled. VEAO compensation components are then discharged by way of the 35µA current sink until the steady state operating point is reached. See Figure 8.

PFC Soft Recovery Following V_{CC} OVP

The FAN4803 assumes that V_{CC} is generated from a source that is proportional to the PFC output voltage. Once that source reaches 16.2V the internal current sink tied to the VEAO pin is disabled just as in the soft start turn-on sequence. Once disabled, the VEAO pin charges HIGH by way of the external components until the PFC duty cycle goes to zero, disabling the PFC. The V_{CC} OVP resets once the V_{CC} discharges below 16.2V, enabling the VEAO current sink and discharging the VEAO compensation components until the steady state operating point is reached. It should be noted that, as shown in Figure 8, once the VEAO pin exceeds 6.5V, the internal ramp is defeated. Because of this, an external Zener can be installed to reduce the maximum voltage to which the VEAO pin may rise in a shutdown condition. Clamping the VEAO pin externally to 7.4V will reduce the time required for the VEAO pin to recover to its steady state value.

UVLO

Once V_{CC} reaches 12V both the PFC and PWM are enabled. The UVLO threshold is 9.1V providing 2.9V of hysteresis.

Generating V_{CC}

An internal clamp limits overvoltage to V_{CC}. This clamp circuit ensures that the V_{CC} OVP circuitry of the FAN4803 will function properly over tolerance and temperature while protecting the part from voltage transients. This circuit allows the FAN4803 to deliver 15V nominal gate drive at PWM OUT and PFC OUT, sufficient to drive low-cost IGBTs.

It is important to limit the current through the Zener to avoid overheating or destroying it. This can be done with a single resistor in series with the V_{CC} pin, returned to a bias supply of typically 14V to 18V. The resistor value must be chosen to meet the operating current requirement of the FAN4803 itself (4.0mA max) plus the current required by the two gate driver outputs.

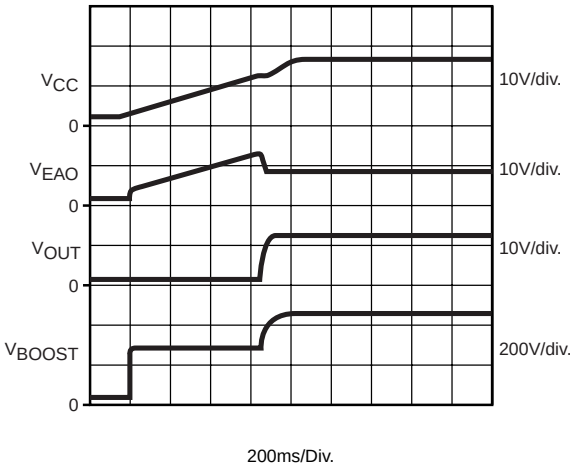


Figure 8. PFC Soft Start

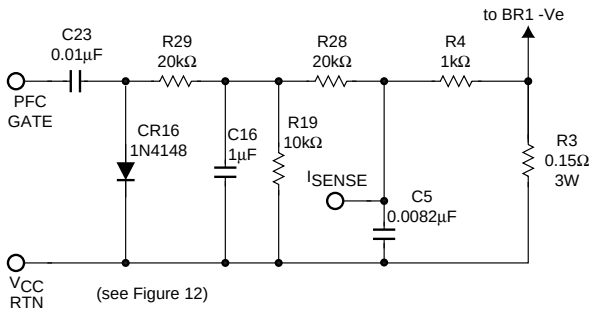


Figure 9. I_{SENSE} Offset for Light Load Conditions

V_{CC} OVP

V_{CC} is assumed to be a voltage proportional to the PFC output voltage, typically a bootstrap winding off the boost inductor. The V_{CC} OVP comparator senses when this voltage exceeds 16V, and terminates the PFC output drive while disabling the VEAO current sink. Once the VEAO current sink is disabled, the VEAO voltage will charge unabated, except for a diode clamp to V_{CC}, reducing the PFC pulse width. Once the V_{CC} rail has decreased to below 16.2V the VEAO sink will be enabled, discharging external VEAO compensation components until the steady state voltage is reached. Given that 15V on V_{CC} corresponds to 400V on the PFC output, 16V on V_{CC} corresponds to an OVP level of 426V.

Component Reduction

Components associated with the V_{RMS} and I_{RMS} pins of a typical PFC controller such as the ML4824 have been eliminated. The PFC power limit and bandwidth does vary with line voltage. Double the power can be delivered from a 220 V AC line versus a 110 V AC line. Since this is a combination PFC/PWM, the power to the load is limited by the PWM stage.

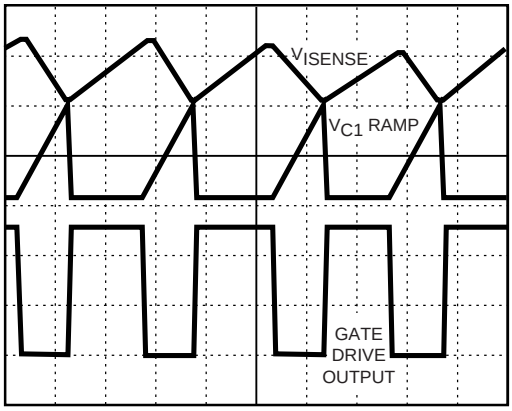


Figure 10. Typical Peak Current Mode Waveforms

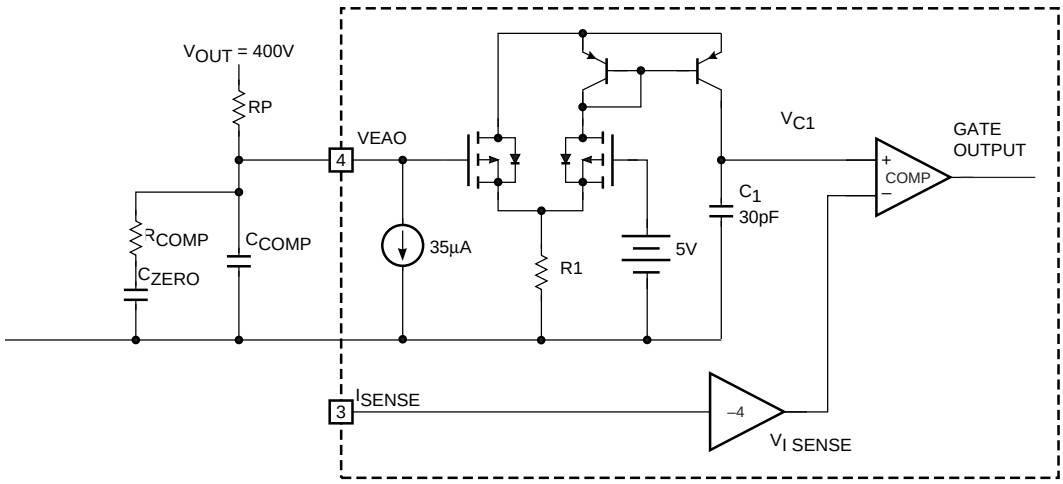


Figure 11. FAN4803 PFC Control

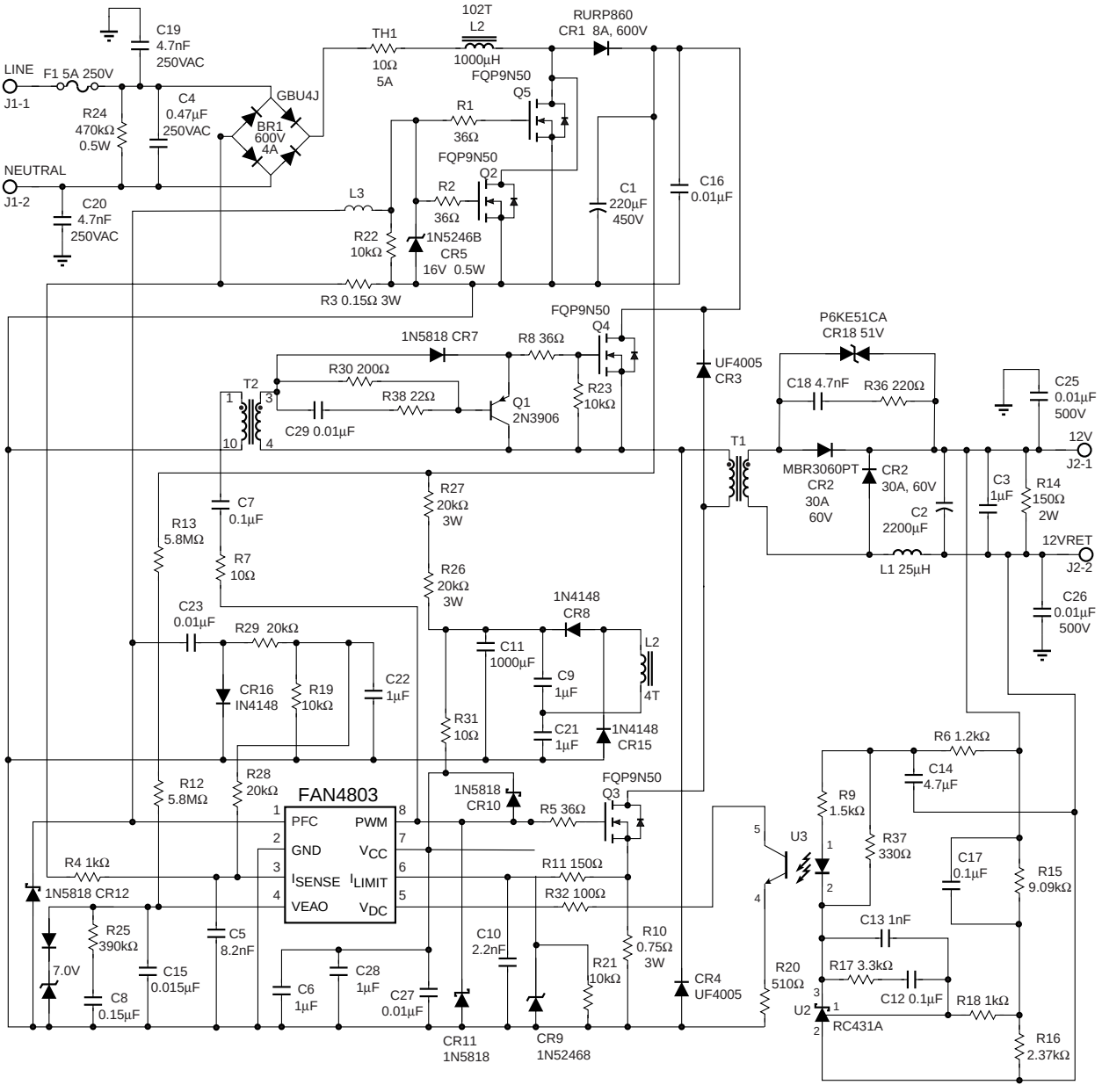
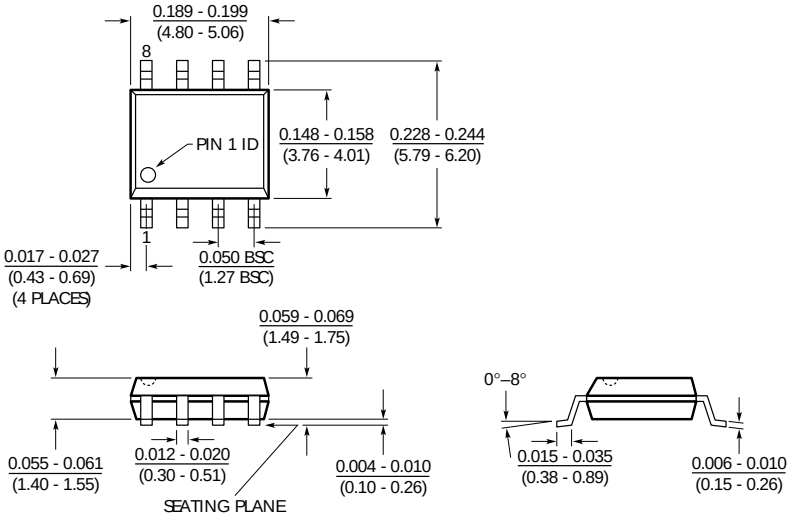


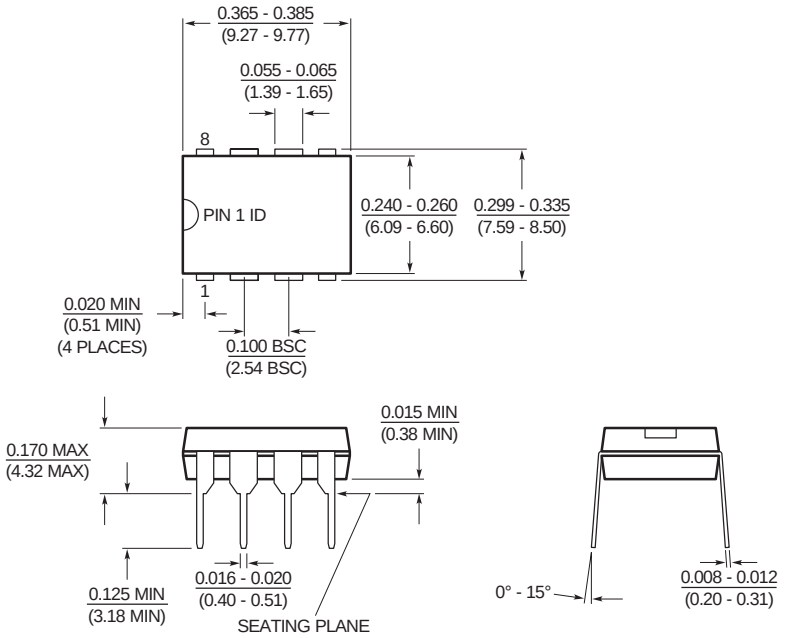
Figure 12. Typical Application Circuit. Universal Input 240W 12V DC Output

Mechanical Dimensions

Package: S08
8 Pin SOIC



Package: P08
8-Pin PDIP



Ordering Information

Part Number	PFC/PWM Frequency	Temperature Range	Package
FAN4803CS-1	67kHz / 67kHz	0°C to 70°C	8-Pin SOIC (S08)
FAN4803CS-2	67kHz / 134kHz	0°C to 70°C	8-Pin SOIC (S08)
FAN4803CP-1	67kHz / 67kHz	0°C to 70°C	8-Pin PDIP (P08)
FAN4803CP-2	67kHz / 134kHz	0°C to 70°C	8-Pin PDIP (P08)

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Стандарт Электрон Связь

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