

## FEATURES

- Guaranteed 0.4% Initial Voltage Tolerance
- 0.1 $\Omega$  Typical Dynamic Output Impedance
- Fast Turn-On
- Sink Current Capability, 1mA to 100mA
- Low Reference Pin Current

## APPLICATIONS

- Linear Regulators
- Adjustable Power Supplies
- Switching Power Supplies

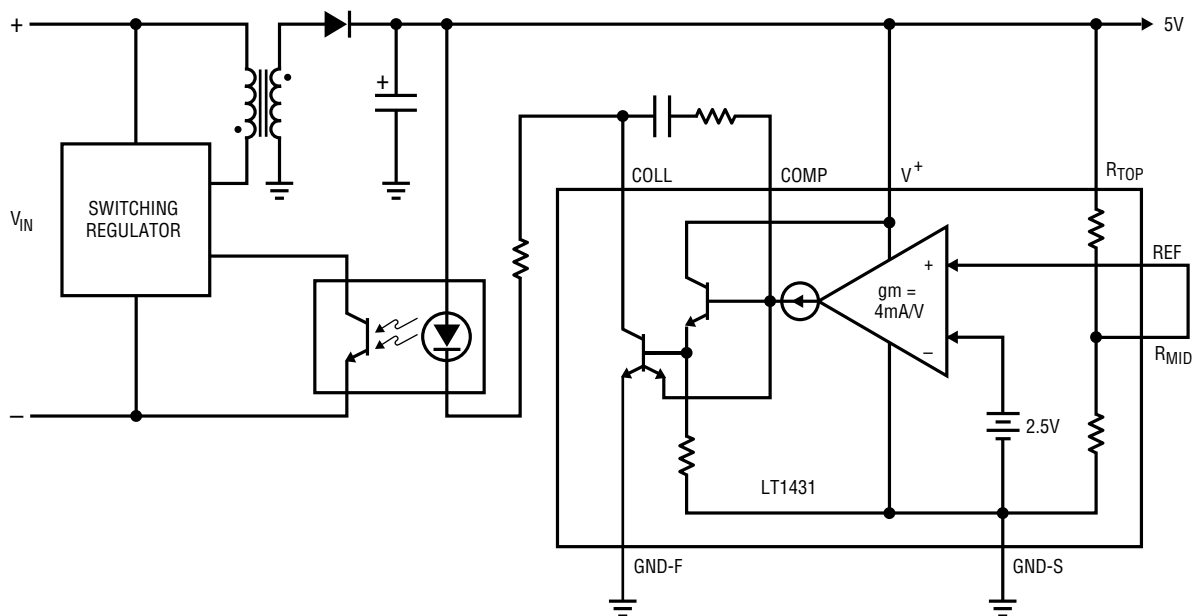
## DESCRIPTION

The LT1431 is an adjustable shunt voltage regulator with 100mA sink capability, 0.4% initial reference voltage tolerance, and 0.3% typical temperature stability. On-chip divider resistors allow the LT1431 to be configured as a 5V shunt regulator, with 1% initial voltage tolerance and requiring no additional external components. By adding two external resistors, the output voltage may be set to any value between 2.5V and 36V. The nominal internal current limit of 100mA may be decreased by including one external resistor.

A simplified three pin version, the LT1431Z/IZ, is available for applications as an adjustable reference and is pin compatible with the TL431.

## TYPICAL APPLICATION

Isolated 5V Regulator



LT1431 • TA01

# LT1431

## ABSOLUTE MAXIMUM RATINGS

V+, V <sub>COLLECTOR</sub> .....	36V
V <sub>COMP</sub> , R <sub>TOP</sub> , R <sub>MID</sub> , V <sub>REF</sub> .....	6V
GND-F to GND-S .....	0.7V
Ambient Temperature Range	
LT1431M .....	-55°C to 125°C
LT1431I .....	-40°C to 85°C
LT1431C .....	0°C to 70°C

Junction Temperature Range	
LT1431M .....	-55°C to 150°C
LT1431I .....	-40°C to 100°C
LT1431C .....	0°C to 100°C
Storage Temperature Range .....	
-65°C to 150°C	
Lead Temperature (Soldering, 10 sec) .....	
300°C	

## PACKAGE/ORDER INFORMATION

<p>J8 PACKAGE 8-LEAD CERAMIC DIP</p> <p>N8 PACKAGE 8-LEAD PLASTIC DIP</p> <p>T<sub>J</sub> MAX = 150°C, θ<sub>JA</sub> = 100°C/W (J) T<sub>J</sub> MAX = 100°C, θ<sub>JA</sub> = 130°C/W (N)</p>	ORDER PART NUMBER	<p>S8 PACKAGE 8-LEAD PLASTIC SOIC</p> <p>T<sub>J</sub> MAX = 100°C, θ<sub>JA</sub> = 170°C/W</p>	ORDER PART NUMBER	<p>Z PACKAGE 3-LEAD TO-92 PLASTIC</p> <p>T<sub>J</sub> MAX = 100°C, θ<sub>JA</sub> = 160°C/W</p>	ORDER PART NUMBER
	LT1431MJ8 LT1431CN8 LT1431IN8		LT1431CS8 LT1431IS8		PART MARKING LT1431 LT1431I

## ELECTRICAL CHARACTERISTICS T<sub>A</sub> = 25°C, I<sub>K</sub> = 10mA, unless otherwise specified (Note 1).

SYMBOL	PARAMETER	CONDITIONS	LT1431M/I			LT1431C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V <sub>REF</sub>	Reference Voltage	V <sub>KA</sub> = 5V, I <sub>K</sub> = 2mA, (Note 2)	● 2.490	2.500	2.510	2.490	2.500	2.510	V	
			● 2.465		2.535	2.480		2.520	V	
ΔV <sub>REF</sub> /ΔT	Reference Drift	V <sub>KA</sub> = 5V, I <sub>K</sub> = 2mA	●	50		30			ppm/°C	
ΔV <sub>REF</sub> /ΔV <sub>KA</sub>	Voltage Ratio, Reference to Cathode (Open-Loop Gain)	I <sub>K</sub> = 2mA, V <sub>KA</sub> = 3V to 36V	●	0.2	0.5	0.2	0.5		mV/V	
I <sub>REF</sub>	Reference Input Current	V <sub>KA</sub> = 5V, T <sub>A</sub> = 25°C	●	0.2	1.0	0.2	1.0		μA	
					1.5		1.2		μA	
I <sub>MIN</sub>	Minimum Operating Current	V <sub>KA</sub> = V <sub>REF</sub> to 36V		0.6	1.0	0.6	1.0		mA	
I <sub>OFF</sub>	Off-State Cathode Current	V <sub>KA</sub> = 36V, V <sub>REF</sub> = 0V	●		1	1			μA	
					15	2			μA	
I <sub>LEAK</sub>	Off-State Collector Leakage Current	V <sub>COLL</sub> = 36V, V <sup>+</sup> = 5V, V <sub>REF</sub> = 2.4V	●		1	1			μA	
					5	2			μA	
I <sub>ZKA</sub>	Dynamic Impedance	V <sub>KA</sub> = V <sub>REF</sub> , I <sub>K</sub> = 1mA to 100mA, f ≤ 1kHz			0.2	0.2			Ω	
I <sub>LIM</sub>	Collector Current Limit	V <sub>KA</sub> = V <sub>REF</sub> + 50mV	●	80	360	100	260		mA	
	5V Reference Output	Internal Divider Used, I <sub>K</sub> = 2mA		4.950	5.000	5.050	4.950	5.000	5.050	V

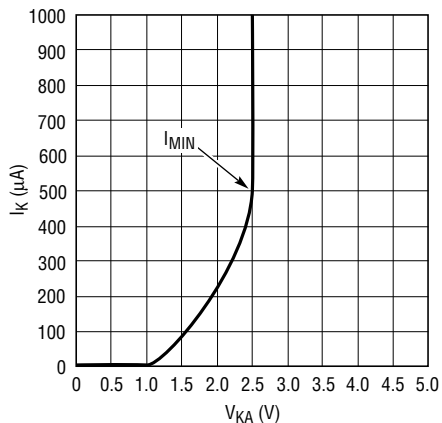
The ● denotes specifications which apply over the operating temperature range.

**Note 1:** V<sub>KA</sub> is the cathode voltage of the LT1431CZ/IZ and corresponds to V<sup>+</sup> of the LT1431CN8/MJ8. I<sub>K</sub> is the cathode current of the LT1431CZ/IZ and corresponds to I(V<sup>+</sup>) + I<sub>COLLECTOR</sub> of the LT1431CN8/MJ8/IN8.

**Note 2:** The LT1431 has bias current cancellation which is effective only for V<sub>KA</sub> ≥ 3V. A slight (≈2mV) shift in reference voltage occurs when V<sub>KA</sub> drops below 3V. For this reason, these tests are not performed at V<sub>KA</sub> = V<sub>REF</sub>.

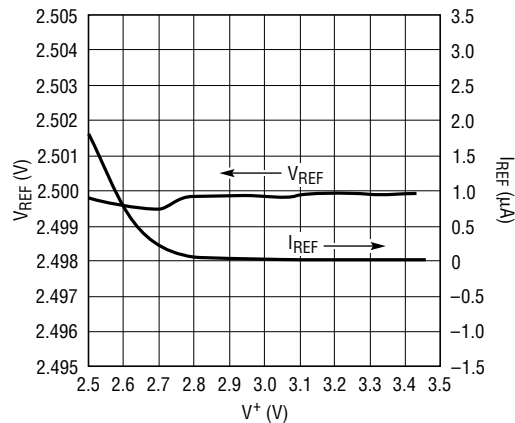
# TYPICAL PERFORMANCE CHARACTERISTICS

2.5V Reference  $I_K$  vs  $V_{KA}$



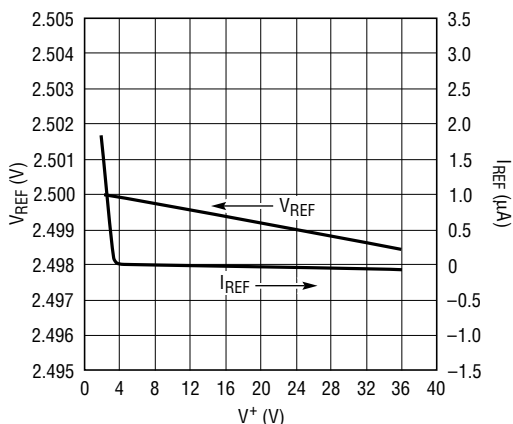
LT1431 • TPC01

$V_{REF}$  and  $I_{REF}$  vs  $V^+$



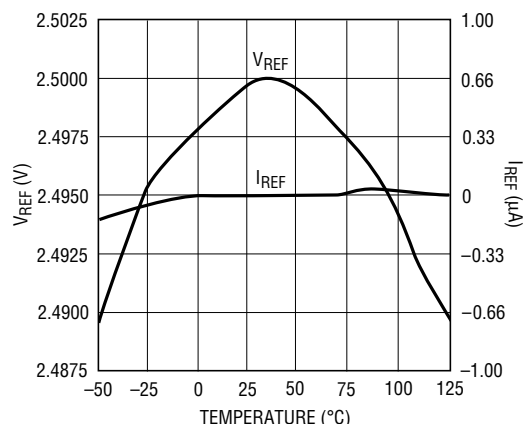
LT1431 • TPC02

$V_{REF}$  and  $I_{REF}$  vs  $V^+$



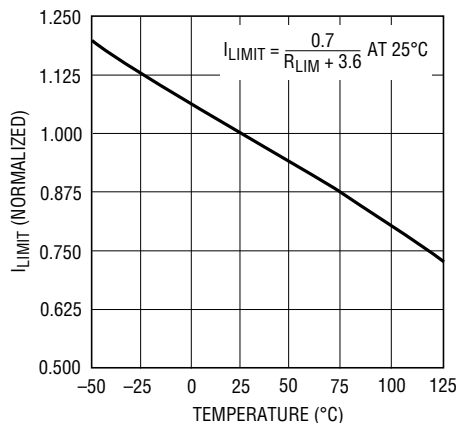
LT1431 • TPC03

$V_{REF}$  and  $I_{REF}$  vs Temperature



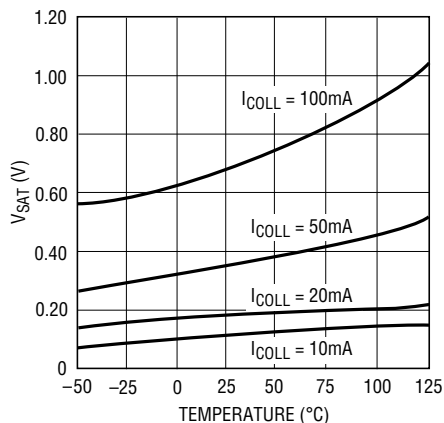
LT1027 • TPC04

$I_{LIMIT}$  vs Temperature with External Resistor



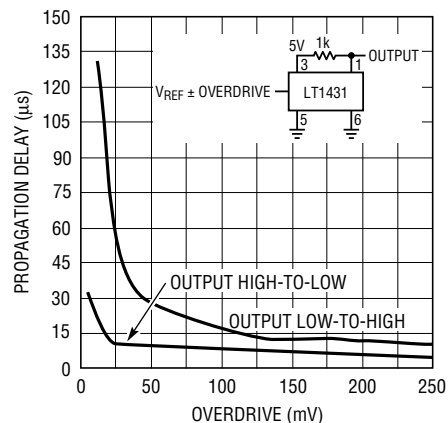
LT1431 • TPC05

COLLECTOR  $V_{SAT}$  vs Temperature vs Current



LT1431 • TPC06

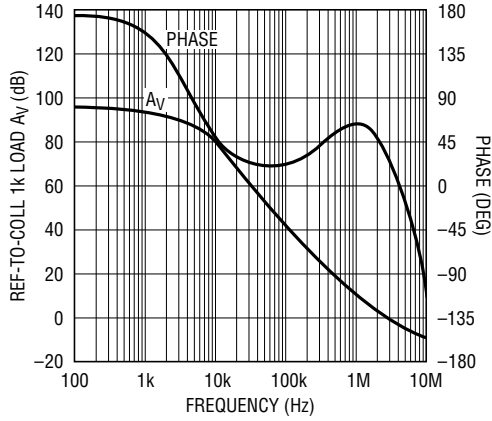
Propagation Delay vs Overdrive



LT1431 • TPC07

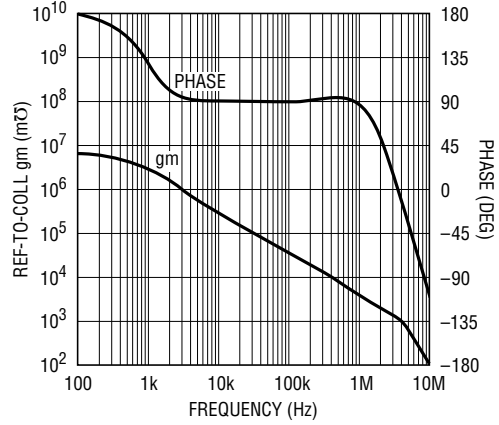
# TYPICAL PERFORMANCE CHARACTERISTICS

**Voltage Gain and Phase vs Frequency**



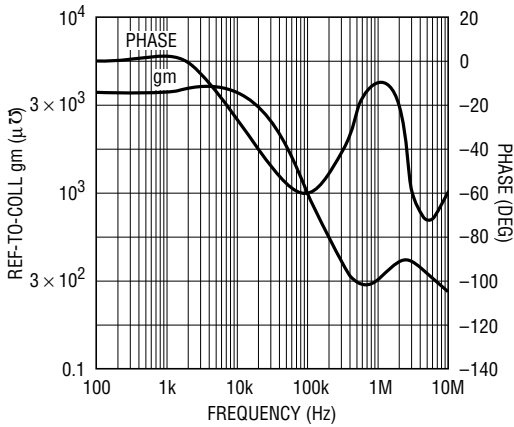
LT1431 • TPC08

**Transconductance and Phase vs Frequency (REF to COLL)**



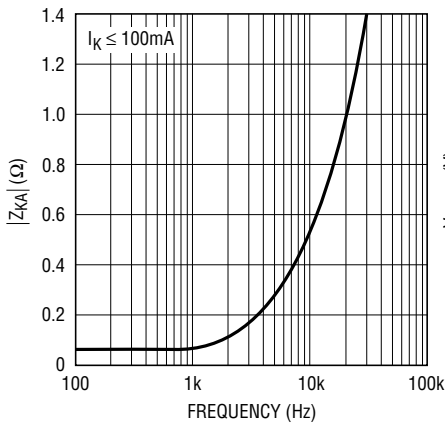
LT1431 • TPC09

**Transconductance and Phase vs Frequency (Ref to Comp)**



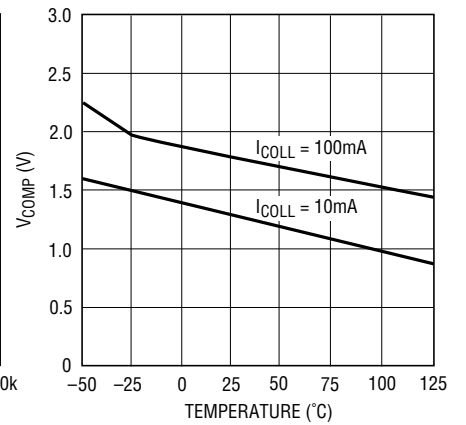
LT1431 • TPC10

**Dynamic Impedance vs Frequency**



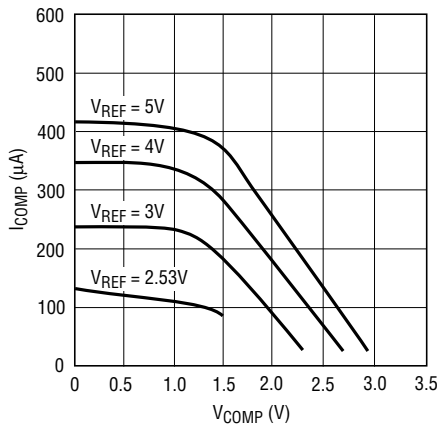
LT1431 • TPC11

**V<sub>COMP</sub> vs Temperature vs I<sub>COLL</sub>**



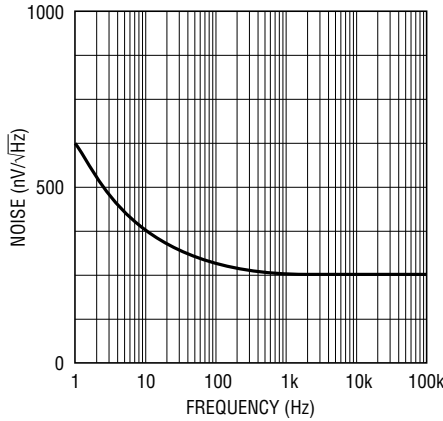
LT1431 • TPC12

**I<sub>COMP</sub> vs V<sub>COMP</sub> vs V<sub>REF</sub>**



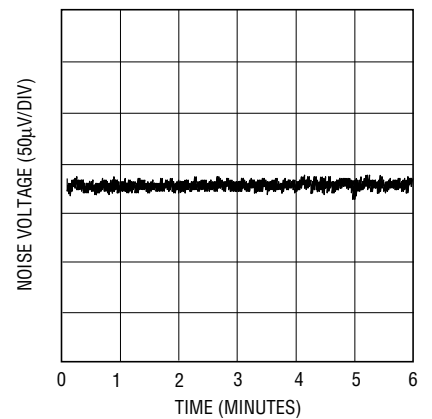
LT1431 • TPC13

**Noise vs Frequency**



LT1431 • G14

**0.1Hz to 10Hz Noise**



LT1431 • TPC15

## PIN FUNCTIONS

**COLL (Pin 1):** Open collector of the output transistor. The maximum pin voltage is 26V. The saturation voltage at 100mA is approximately 1V.

**COMP (Pin 2):** Base of the driver for the output transistor. This pin allows additional compensation for complex feedback systems and shutdown of the regulator. It must be left open if unused.

**V<sup>+</sup> (Pin 3):** Bias voltage for the entire shunt regulator. The maximum input voltage is 36V and the minimum to operate is equal to V<sub>REF</sub> (2.5V). The quiescent current is typically 0.6mA.

**R<sub>TOP</sub> (Pin 4):** Top of the on-chip 5k-5k resistive divider that guarantees 1% accuracy of operation as a 5V shunt regulator with no external trim. The pin is tied to COLL for self-contained 5V operation. It may be left open if unused. See note on parasitic diodes below.

**GND-S (Pin 5):** Ground reference for the on-chip resistive divider and shunt regulator circuitry except for the output transistor. This pin allows external current limit of the output transistor with one resistor between GND-F (force) and GND-S (sense).

**GND-F (Pin 6):** Emitter of the output transistor and substrate connection for the die.

**R<sub>MID</sub> (Pin 7):** Middle of the on-chip resistive divider string between R<sub>TOP</sub> and GND-S. The pin is tied to REF for self-contained 5V operation. It may be left open if unused.

**REF (Pin 8):** Control pin of the shunt regulator with a 2.5V threshold. If V<sup>+</sup> > 3V, input bias current cancellation reduces I<sub>B</sub> to 0.2μA typical.

COMP, R<sub>TOP</sub>, R<sub>MID</sub>, and REF have static discharge protection circuits that must not be activated on a continuous basis. Therefore, the absolute maximum DC voltage on these pins is 6V, well beyond the normal operating conditions.

As with all bipolar ICs, the LT1431 contains parasitic diodes which must not be forward biased or else anomalous behavior will result. Pin conditions to be avoided are R<sub>TOP</sub> below R<sub>MID</sub> in voltage and any pin below GND-F in voltage (except for GND-S).

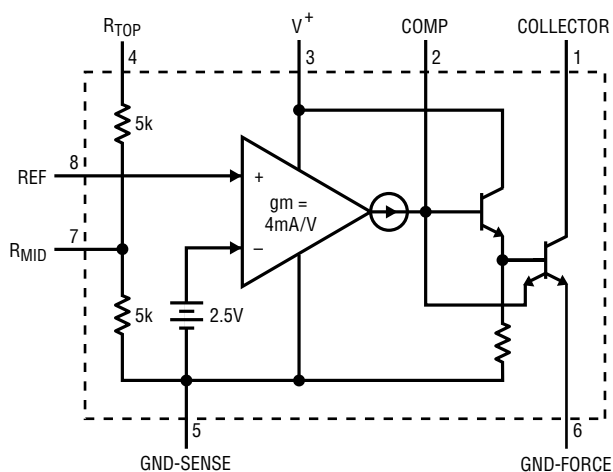
The following pin definitions apply to the Z package.

**CATHODE (Pin 1):** Corresponds to COLL and V<sup>+</sup> tied together.

**ANODE (Pin 2):** Corresponds to GND-S and GND-F tied together.

**REF (Pin 3):** Corresponds to REF.

## BLOCK DIAGRAM



LT1431 • BD01

## APPLICATIONS INFORMATION

### Frequency Compensation

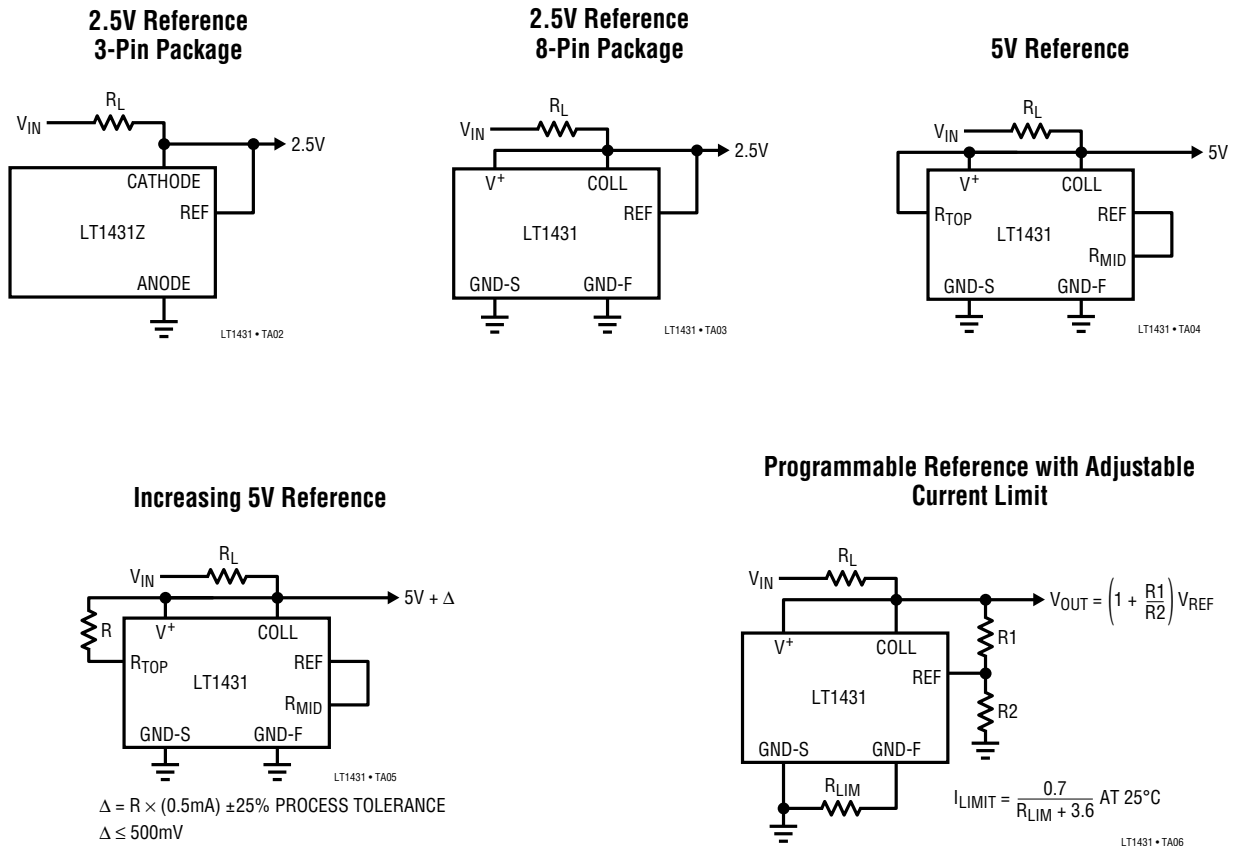
As a shunt regulator, the LT1431 is stable for all capacitive loads on the COLL pin. Capacitive loading between 0.01 $\mu$ F and 18 $\mu$ F causes reduced phase margin with some ringing under transient conditions. Output capacitors should not be used arbitrarily because output noise is not necessarily reduced.

Excess capacitance on the REF pin can introduce enough phase shift to induce oscillation when configured as a reference >2.5V. This can be compensated with capacitance between COLL and REF (phase lead). More complicated feedback loops may require shaping of the frequency response of the LT1431 with dominant pole or

pole-zero compensation. This can be accomplished with a capacitor or series resistor and capacitor between COLL and COMP.

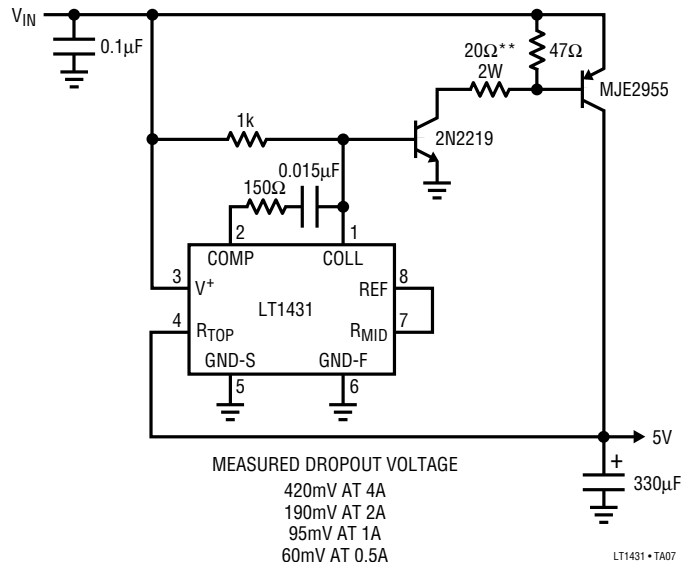
The compensation schemes mentioned above use voltage feedback to stabilize the circuits. There must be voltage gain at the COLL pin for them to be effective, so the COLL pin must see a reasonable AC impedance. Capacitive loading of the COLL pin reduces the AC impedance, voltage gain, and frequency response, thereby decreasing the effectiveness of the compensation schemes, but also decreasing their necessity.

## TYPICAL APPLICATIONS



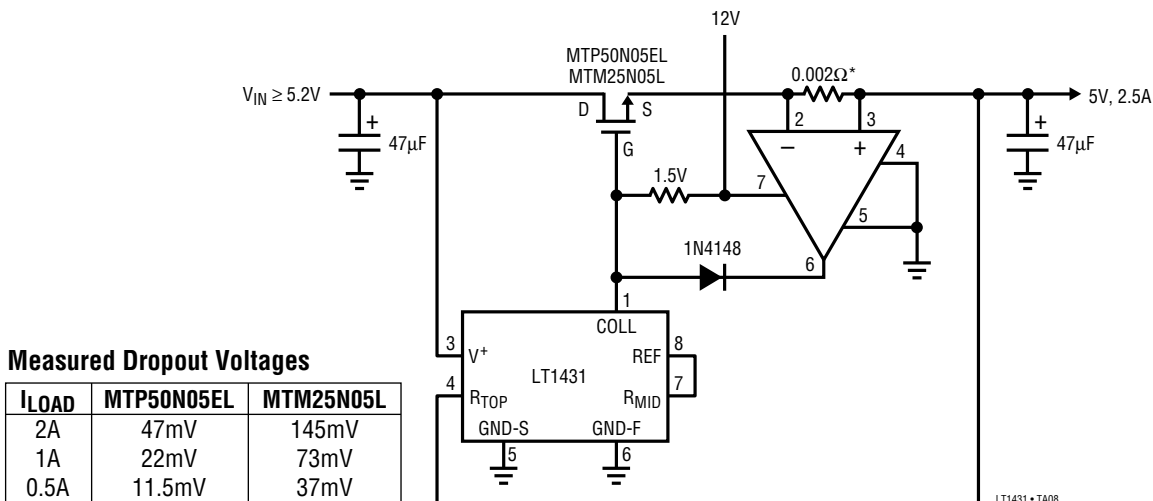
# TYPICAL APPLICATIONS

## PNP Low Dropout 5V Regulator\*



\*NO SHORT-CIRCUIT PROTECTION  
 \*\*MAY BE INCREASED AT LOWER WATTAGE  
 FOR LOWER OUTPUT CURRENTS

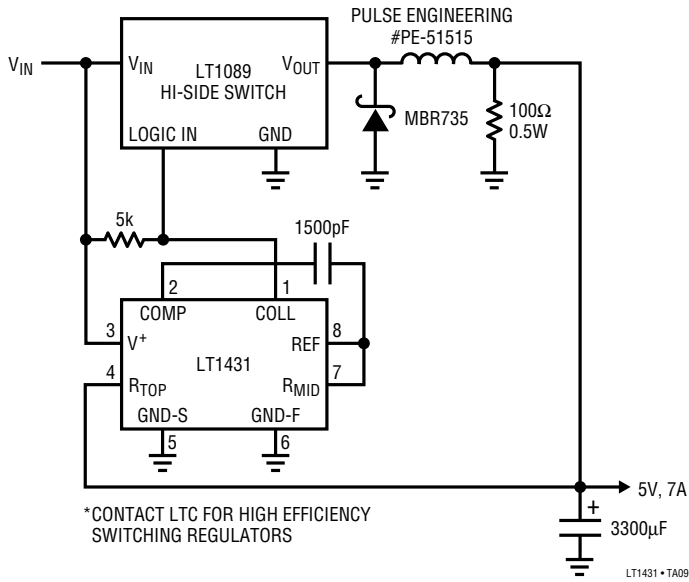
## FET Low Dropout 5V Regulator with Current Limit



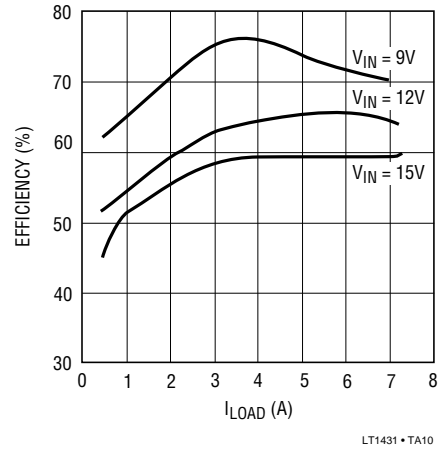
\*1.5" #23 SOLID COPPER WIRE  
 ~0.002Ω → 3A LIMIT

TYPICAL APPLICATIONS

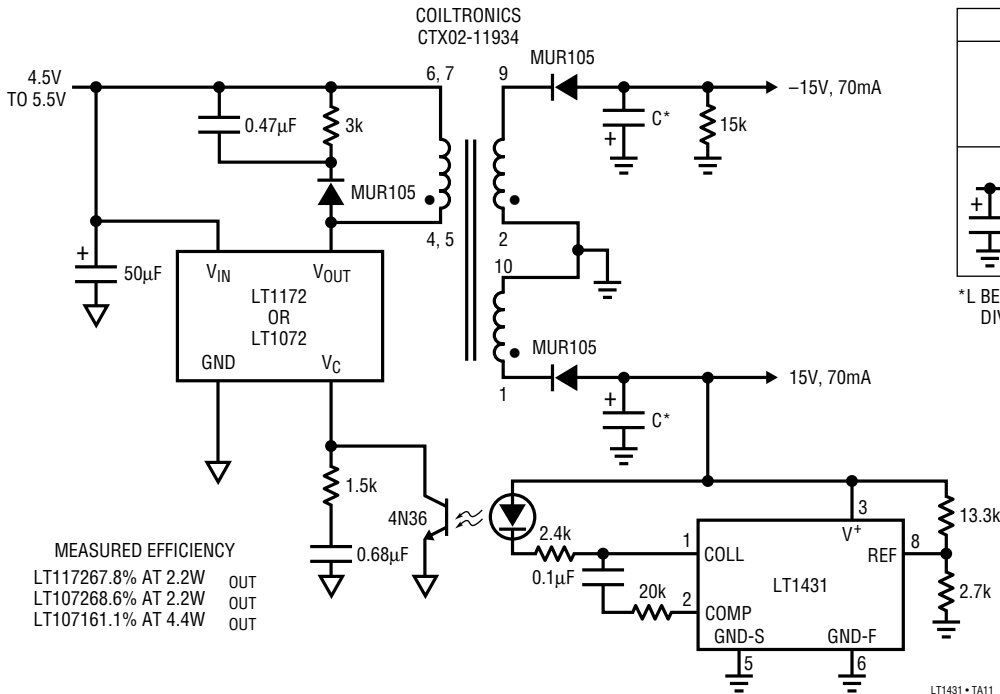
12V to 5V Buck Converter with Foldback Current Limit\*



Buck Converter Efficiency



Isolated 5V to ±15V Flyback Converter



Fully Loaded Output Ripple vs Filtering

	LT1172	LT1072
$C^+$ 	30mV <sub>p-p</sub>	40mV <sub>p-p</sub>
$L^+$ 	6mV <sub>p-p</sub>	8mV <sub>p-p</sub>

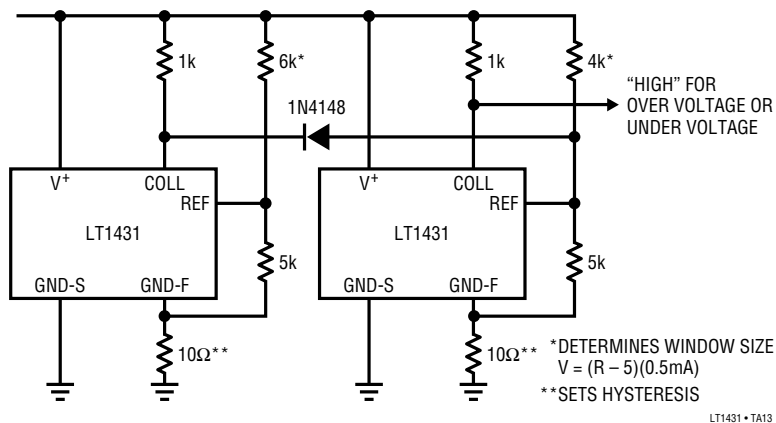
\*L BELL INDUSTRIES J.W. MILLER DIVISION 9310-36 10µH, 450mA

LT1431 • TA12

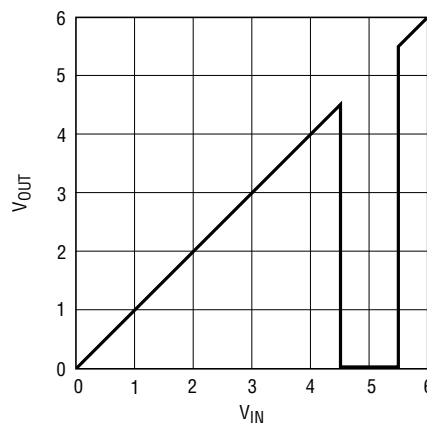


# TYPICAL APPLICATIONS

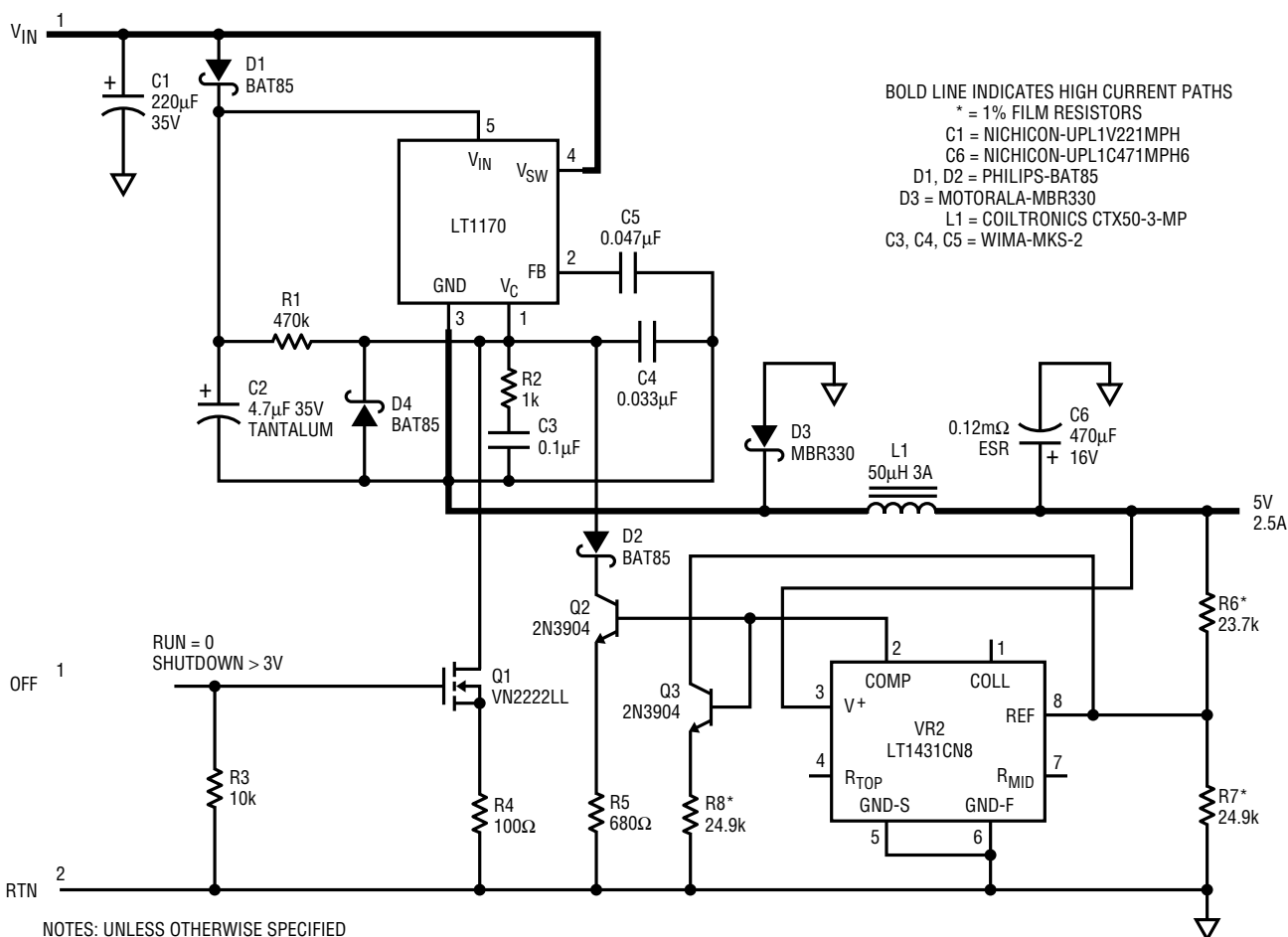
### 5V Power Supply Monitor with $\pm 500\text{mV}$ Window and 50mV Hysteresis



### Transfer Function

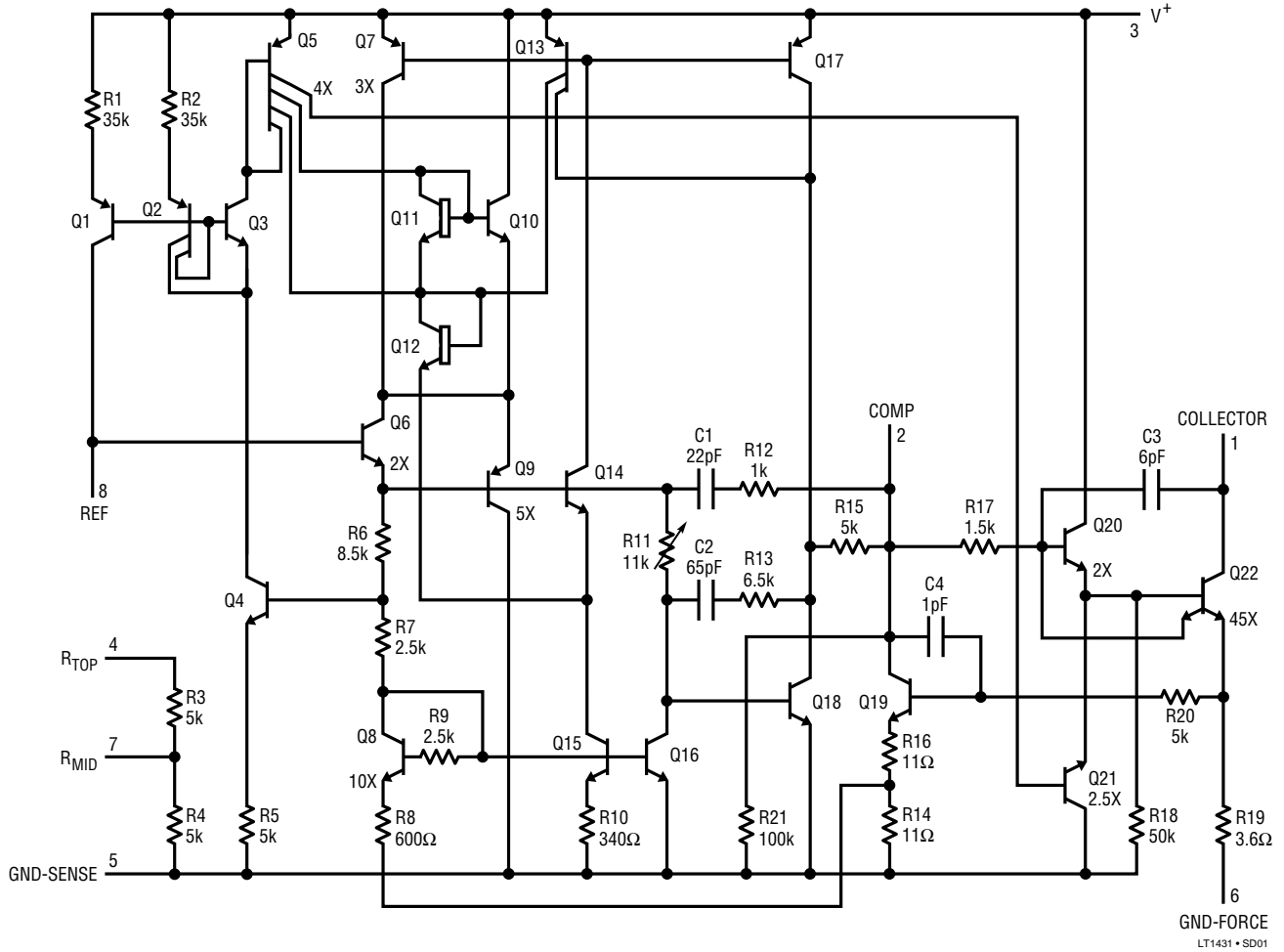


### High Efficiency Buck Converter E = 85% to 89%



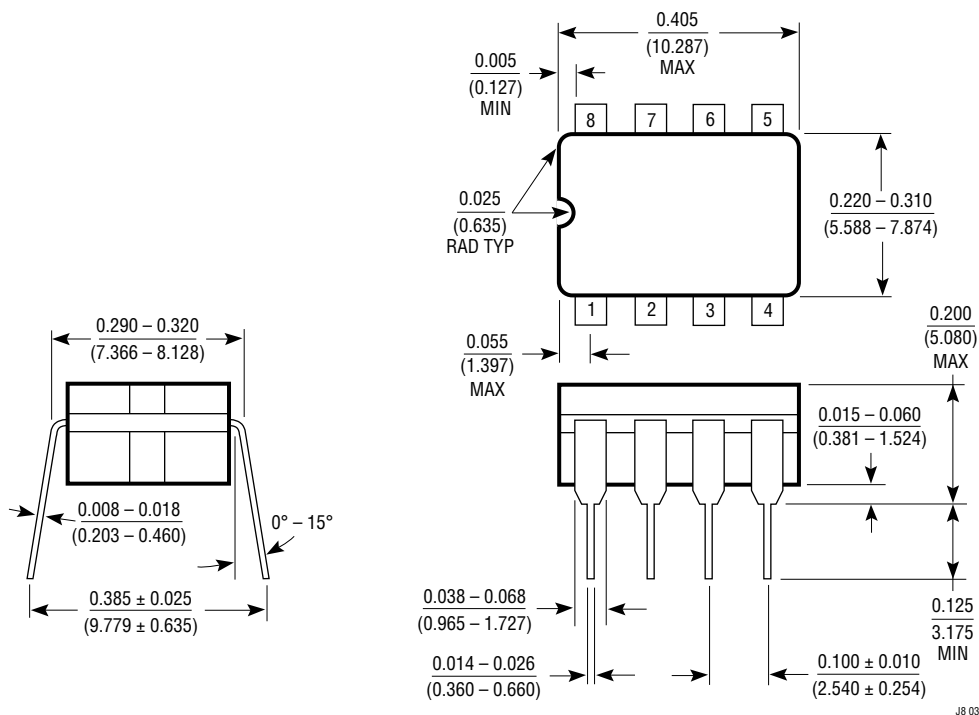
- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCES ARE IN  $\Omega$ , 0.25W, 5%
  2. ALL CAPACITANCES ARE IN  $\mu\text{F}$ , 50V, 10%
  3. SHUTDOWN LOGIC STATE MUST BE DEFINED BY A LOGIC GATE OR BY TYING TO GND

**SCHEMATIC DIAGRAM**



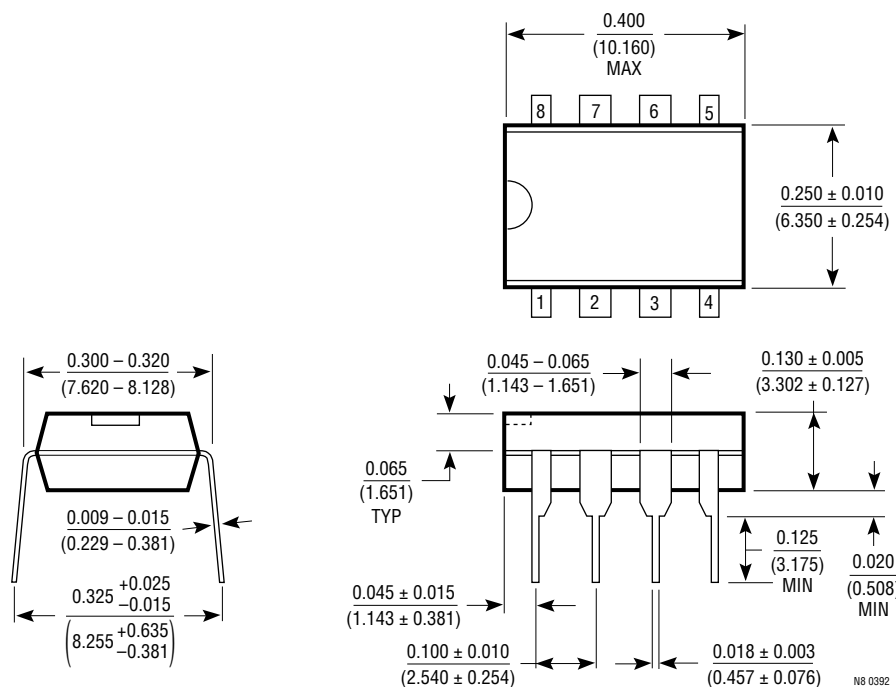
**PACKAGE DESCRIPTION** Dimensions in inches (millimeters) unless otherwise noted.

**J8 Package  
8-Lead Ceramic DIP**



J8 0392

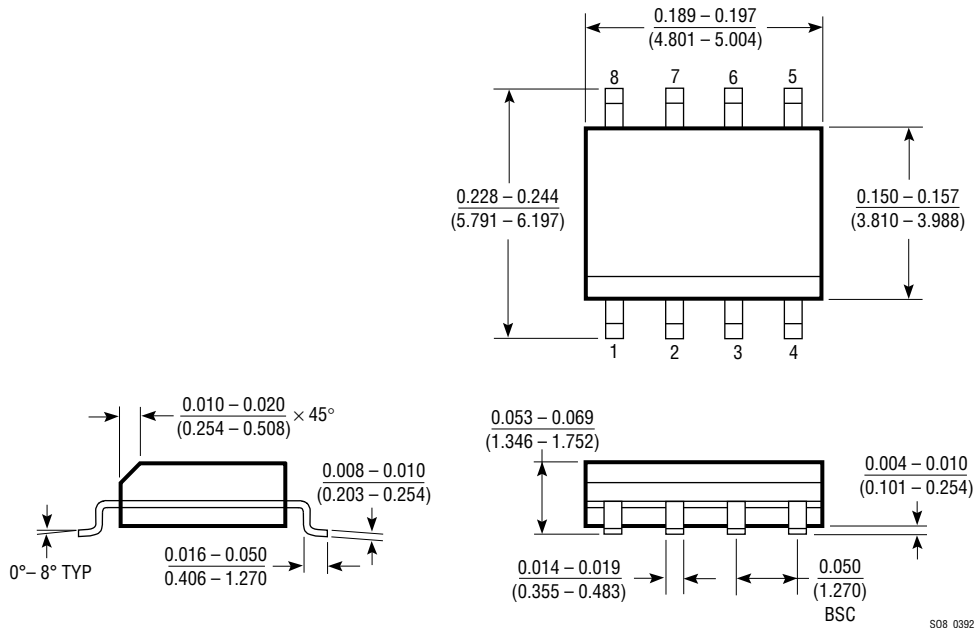
**N8 Package  
8-Lead Plastic DIP**



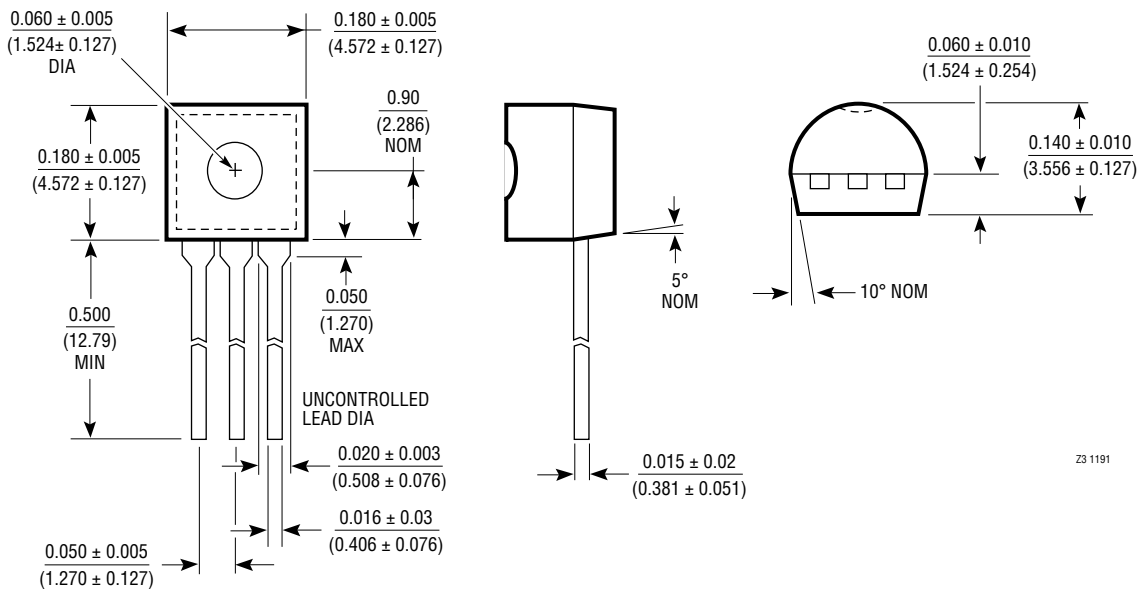
N8 0392

**PACKAGE DESCRIPTION** Dimensions in inches (millimeters) unless otherwise noted.

**S8 Package  
8-Lead Plastic SOIC**



**Z Package  
3-Lead TO-92**





## Стандарт Электрон Связь

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