PLL500-17B/27B/37B

Low Power CMOS Output VCXO Family (17MHz to 130MHz)

FEATURES

- VCXO output for the 17MHz to 130MHz range
  - PLL500-17B: 17MHz to 36MHz
  - PLL500-27B: 27MHz to 65MHz
  - PLL500-37B: 65MHz to 130MHz
- Low phase noise (-142 dBc @ 10kHz offset).
- CMOS output with OE tri-state control.
- Selectable output drive (Standard or High drive).
  - Standard: 8mA drive capability at TTL level.
  - High: 24mA drive capability at TTL level.
- Fundamental crystal input.
- Integrated high linearity variable capacitors.
- +/- 150 ppm pull range, max 5% linearity.
- Low jitter (RMS): 2.5ps period jitter.
- 2.5 to 3.3V operation.
- Available in 8-Pin SOIC or DIE.

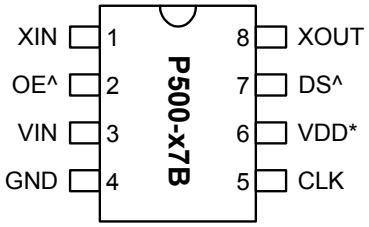
DESCRIPTION

The PLL500-17B/27B/37B are a low cost, high performance, low phase noise, and high linearity VCXO family for the 17 to 130MHz range, providing less than -130dBc at 10kHz offset. The very low jitter (2.5 ps RMS period jitter) makes these chips ideal for applications requiring voltage controlled frequency sources. The IC's are designed to accept fundamental resonant mode crystals.

FREQUENCY RANGE

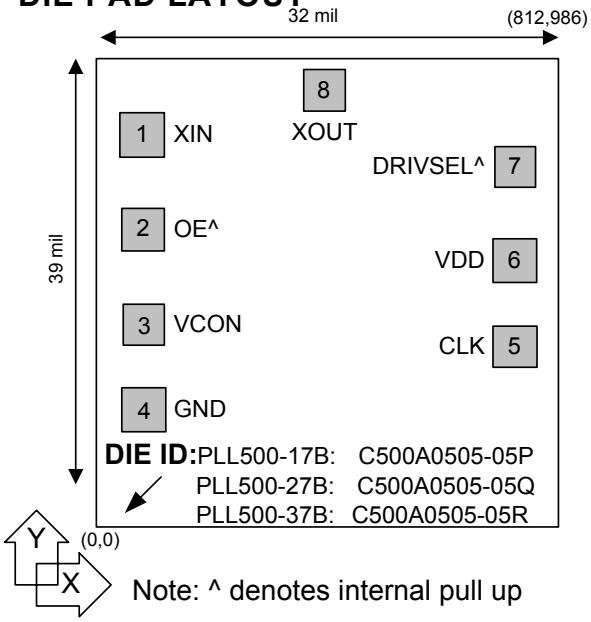
PART #	MULTIPLIER	FREQUENCY
PLL500-17B	No PLL	17 – 36 MHz
PLL500-27B	No PLL	27 – 65 MHz
PLL500-37B	No PLL	65 – 130 MHz

PIN CONFIGURATION



^: Denotes internal Pull-up

DIE PAD LAYOUT

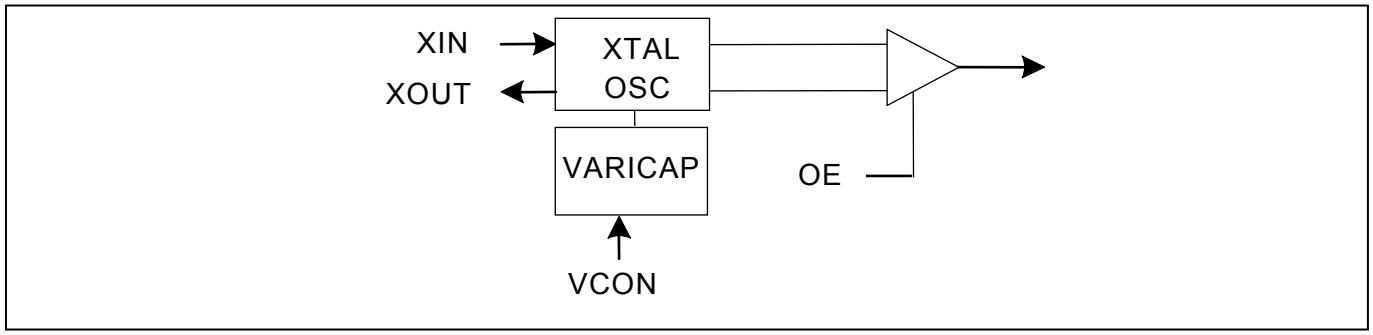


Note: ^ denotes internal pull up

DIE SPECIFICATIONS

Name	Value
Size	39 x 32 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

BLOCK DIAGRAM



PIN AND PAD DESCRIPTION

Name	Pin#	Die Pad Position		Type	Description
		X (μm)	Y (μm)		
XIN	1	94.183	768.599	I	Crystal input pin.
OE	2	94.157	605.029	I	Output Enable input pin. Disables the output when low. Internal pull-up enables output by default if pin is not connected low.
VCON	3	94.183	331.756	I	Frequency control voltage input pin.
GND	4	94.193	140.379	P	Ground pin.
CLK	5	715.472	203.866	O	Output clock pin.
VDD	6	715.307	455.726	P	VDD power supply pin.
DRIVSEL	7	715.472	626.716	I	Output drive select pin. High drive if set to '0'. Low drive if set to '1'. Internal pull-up.
XOUT	8	476.906	888.881	I	Crystal output pin. Ref clock input.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. AC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency		PLL500-17B	17		36	MHz
		PLL500-27B	27		65	
		PLL500-47B	65		130	
Output Clock Rise/Fall Time		0.8V ~ 2.0V with 10 pF load		0.8		ns
		0.3V ~ 3.0V with 15 pF load		2.5		
Output Clock Duty Cycle		Measured @ 1.4V	45	50	55	%
Short Circuit Current				±50		mA

3. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		F_{XIN} = 12 – 25MHz; XTAL C_0/C_1 < 250 0V ≤ VCON ≤ 3.3V		300		ppm
CLK output pullability		VCON=1.65V, ±1.65V	±150			ppm
VCXO Tuning Characteristic				100		ppm/V
Pull range linearity					5	%
Power Supply Rejection	PWSRR	Frequency change with VDD varied +/- 10%	-1		+1	ppm
VCON pin input impedance			2000			kΩ
VCON modulation BW		0V ≤ VCON ≤ 3.3V, -3dB	45			kHz

Note: Preliminary Specifications still to be characterized. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

4. Jitter and Phase Noise Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
RMS Period Jitter (1 sigma – 10,000 samples)	With capacitive decoupling between VDD and GND.		2.5		ps
Phase Noise relative to carrier	@100Hz offset		-100		dBc/Hz
Phase Noise relative to carrier	@1kHz offset		-125		dBc/Hz
Phase Noise relative to carrier	@10kHz offset		-142		dBc/Hz
Phase Noise relative to carrier	@100kHz offset		-150		dBc/Hz
Phase Noise relative to carrier	@1MHz offset		-150		dBc/Hz

5. DC Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	F_{XIN} = 27MHz, 15pF output load		2.8	4	mA
		F_{XIN} = 35MHz, 15pF output load		4.2	6	
		F_{XIN} = 78MHz, 15pF output load		7.2	9	
Allowable output load capacitance	C_L (Output)	PLL500-17B			30	pF
		PLL500-27B			20	pF
		PLL500-37B Std drive up to 100MHz			15	pF
		PLL500-37B High drive			10	pF
Operating Voltage	V_{DD}		2.25		3.63	V
Output High Voltage	V_{OH}	I_{OH} = -8mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Output High Voltage at CMOS level		I_{OH} = -4mA	V_{DD} – 0.4			V
Output drive current		Standard drive at TTL level	8	9.5		mA
		High drive at TTL level	24	27		
Short Circuit Current				±50		mA
VCXO Control Voltage	VCON		0		V_{DD}	V

6. Crystal Specifications

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Crystal Loading Rating (VCON = 1.65V)	$C_{L\ (xtal)}$		8.5		pF
Maximum Sustainable Drive Level				200	µW
Operating Drive Level			50		µW
Max C0 for PLL500-17B				5	pF
Max C0 for PLL500-27B				3.5	
Max C0 for PLL500-37B				2.5	
C0/C1				250	-
ESR	R_S			30	Ω

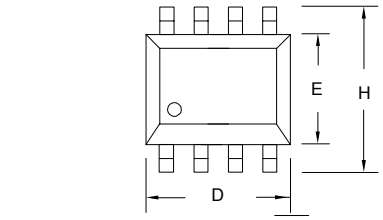
Note: The crystal must be such that it oscillates (parallel resonant) at nominal frequency when presented a C Load as specified above.
If the crystal requires more load to be at nominal frequency, the additional load must be added externally.
This however may reduce the pull range.

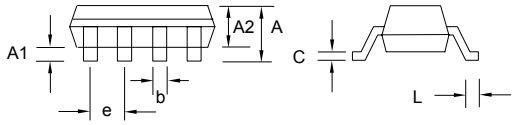
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PACKAGE INFORMATION

SOIC 8L (Dimensions in mm)

Symbol	Dimension in MM	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
B	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	





ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL500-X7B X X X X

PART NUMBER

NONE= TUBE
R=TAPE AND REEL

NONE=NORMAL PACKAGE
L=GREEN PACKAGE

PACKAGE TYPE
S=SSOP

TEMPERATURE
C=COMMERCIAL
I=INDUSTRIAL

Order Number	Marking	Package Option
PLL500-X7BDC	P500-X7BDC	Die (Waffle Pack)
PLL500-X7BSC	P500-X7BSC	8-Pin SOIC (Tube)
PLL500-X7BSC-R	P500-X7BSC	8-Pin SOIC (Tape and Reel)
PLL500-X7BSCL	P500-X7BSCL	8-Pin SOIC (Tube), GREEN
PLL500-X7BSCL-R	P500-X7BSCL	8-Pin SOIC (Tape and Reel) , GREEN

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