Variable Resolution, Monolithic Resolver-to-Digital Converters

AD2S81A/AD2S82A

FEATURES
Monolithic (BiMOS II) Tracking R/D Converter
Ratiometric Conversion
Low Power Consumption: 300 mW Typ
Dynamic Performance Set by User
Velocity Output
ESD Class 2 Protection (2,000 V Min)

AD2S81A
28-Lead DIP Package
Low Cost

AD2S82A
44-Lead PLCC Package
10-, 12-, 14- and 16-Bit Resolution Set by User
High Max Tracking Rate 1040 RPS (10 Bits)
VCO Output (Inter LSB Output)
Data Complement Facility
Industrial Temperature Range

APPLICATIONS
DC Brushless and AC Motor Control
Process Control
Numerical Control of Machine Tools
Robotics
Axis Control

GENERAL DESCRIPTION

The AD2S82A is a monolithic 10-, 12-, 14- or 16-bit tracking resolver-to-digital converter contained in a 44-lead J leaded PLCC package. Two extra functions are provided in the new surface mount package–COMPLEMENT and VCO output.

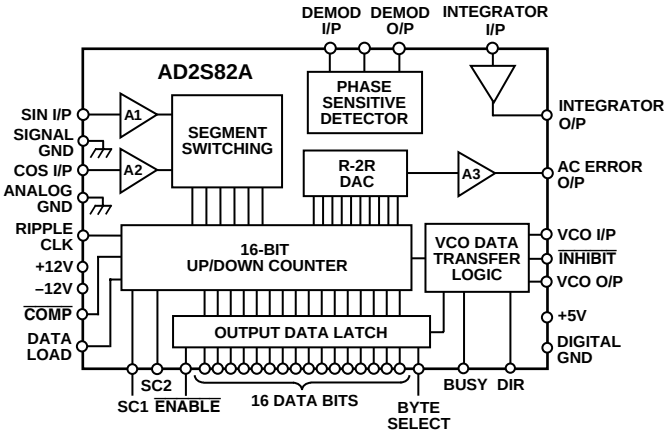
The AD2S81A is a monolithic 12-bit fixed resolution tracking resolver-to-digital converter packaged in a 28-lead DIP.

The converters allow users to *select their own dynamic performance with external components.* This allows the users great flexibility in defining the converter that best suits their system requirements. The AD2S82A allows users to select the resolution to be 10, 12, 14 or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

The AD2S81A and AD2S82A convert resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures high-noise immunity and tolerance of lead length when the converter is remote from the resolver.

The output word is in a three-state digital logic form available in two bytes on the 16 output data lines for the AD2S82A and on eight output data lines for the AD2S81A. BYTE SELECT, $\overline{\text{ENABLE}}$ and $\overline{\text{INHIBIT}}$ pins ensure easy data transfer to 8- and 16-bit data buses, and outputs are provided to allow for cycle or pitch counting in external counters.

AD2S82A FUNCTIONAL BLOCK DIAGRAM



An analog signal proportional to velocity is also available and can be used to replace a tachogenerator.

PRODUCT HIGHLIGHTS

Monolithic. A one-chip solution reduces the package size required and increases the reliability.

Resolution Set by User. Two control pins are used to select the resolution of the AD2S82A to be 10, 12, 14 or 16 bits allowing the user to use the AD2S82A with the optimum resolution for each application.

Ratiometric Tracking Conversion. Conversion technique provides continuous output position data without conversion delay and is insensitive to absolute signal levels. It also provides good noise immunity and tolerance to harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The external components required are all low cost, preferred value resistors and capacitors, and the component values are easy to select using the simple instructions given.

Velocity Output. An analog signal proportional to velocity is available and is linear to typically one percent. This can be used in place of a velocity transducer in many applications to provide loop stabilization in servo controls and velocity feedback data.

Low Power Consumption. Typically only 300 mW.

MODELS AVAILABLE

Information on the models available is given in the Ordering Guide.

REV. B

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703
© Analog Devices, Inc., 1998

AD2S81A/AD2S82A–SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Parameter	Conditions	AD2S81A Min	AD2S81A Typ	AD2S81A Max	AD2S82A Min	AD2S82A Typ	AD2S82A Max	Units
SIGNAL INPUTS								
Frequency		400		20,000	50		20,000	Hz
Voltage Level		1.8	2.0	2.2	1.8	2.0	2.2	V rms
Input Bias Current			60	150		60	150	nA
Input Impedance		1.0			1.0			MΩ
Maximum Voltage				±8			±8	V pk
REFERENCE INPUT								
Frequency		400		20,000	50		20,000	Hz
Voltage Level		1.0		8.0	1.0		8.0	V pk
Input Bias Current			60	150		60	150	nA
Input Impedance		1.0			1.0			MΩ
CONTROL DYNAMICS								
Repeatability				1			1	LSB
Allowable Phase Shift	(Signals to Reference)	–10		+10	–10		+10	Degrees
Tracking Rate	10 Bits						1040	rps
	12 Bits			260			260	rps
	14 Bits						65	rps
	16 Bits						16.25	rps
Bandwidth[1]	User Selectable							
ACCURACY								
Angular Accuracy	H						**±22 + 1 LSB**	arc min
	J			**±30 + 1 LSB**			**±8 + 1 LSB**	arc min
	K						**±4 + 1 LSB**	arc min
	L						**±2 + 1 LSB**	arc min
Monotonicity	Guaranteed Monotonic							
Missing Codes (16-Bit Resolution)	J, K						**4**	Codes
	L						**1**	Code
VELOCITY SIGNAL								
Linearity	Over Full Range		±1	**±3**		±1	**±3**	% FSD
Reversion Error				±2			±2	% FSD
DC Zero Offset[2]				**6**			**6**	mV
DC Zero Offset Tempco			–22			–22		µV/°C
Gain Scaling Accuracy				**±10**			**±10**	% FSD
Output Voltage	1 mA Load	±8	±9	±10.5	±8	±9	±10.5	V
Dynamic Ripple	Mean Value			1.5			1.5	% rms O/P
Output Load				1.0			1.0	kΩ
INPUT/OUTPUT PROTECTION								
Analog Inputs	Overvoltage Protection		±8			±8		V
Analog Outputs	Short Circuit O/P Protection	±5.6	±8	±10.4	±5.6	±8	±10.4	mA
DIGITAL POSITION								
Resolution	10, 12, 14 and 16							
Output Format	Bidirectional Natural Binary							
Load				3			3	LSTTL
$\overline{\text{INHIBIT}}$[3]								
Sense	Logic LO to Inhibit							
Time to Stable Data				600			600	ns
$\overline{\text{ENABLE}}$[3]	Logic LO Enables Position Output. Logic HI Outputs in High Impedance State							
$\overline{\text{ENABLE}}$/Disable Time		35		110	35		110	ns
BYTE SELECT[3]								
Sense								
Logic HI	MS Byte DB1–DB8, (LS Byte DB9–DB16)[4]							
Logic LO	LS Byte DB1–DB8, (LS Byte DB9–DB16)[4]							
Time to Data Available		60		140	60		140	ns
SHORT CYCLE INPUTS[4, 5]	Internally Pulled High (100 kΩ) to $+V_S$							
SC1 SC2								
0 0	10 Bit							
0 1	12 Bit							
1 0	14 Bit							
1 1	16 Bit							
DATA LOAD[4, 5]								
Sense	Internally Pulled High (100 kΩ) to $+V_S$; Logic LO Allows Data to Be Loaded into the Counters from the Data Lines					150	300	ns

Parameter	Conditions	AD2S81A Min	AD2S81A Typ	AD2S81A Max	AD2S82A Min	AD2S82A Typ	AD2S82A Max	Units
$\overline{\text{COMPLEMENT}}$[4, 5]	Internally Pulled High (100 kΩ) to $+V_S$; Logic LO to Activate; No Connect for Normal Operation							
BUSY[3]								
Sense	Logic HI When Position O/P Changing							
Width		**200**		**600**	**200**		**600**	ns
Load	Use Additional Pull-Up			1			1	LSTTL
DIRECTION[3]								
Sense	Logic HI Counting Up Logic LO Counting Down							
Max Load				3			3	LSTTL
RIPPLE CLOCK[3]								
Sense	Logic HI, All 1s to All 0s All 0s to All 1s							
Width	Dependent On Input Velocity	**300**			**300**			
Reset	Before Next Busy							
Load				3			3	LSTTL
DIGITAL INPUTS								
High Voltage, V_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 10.8$ V, $V_L = 5.0$ V	**2.0**			**2.0**			V
Low Voltage, V_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 13.2$ V, $V_L = 5.0$ V			**0.8**			**0.8**	V
DIGITAL INPUTS								
High Current, I_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16 $\pm V_S = \pm 13.2$ V, $V_L = 5.5$ V			**±100**			**±100**	µA
Low Current, I_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 13.2$ V, $V_L = 5.5$ V			**±100**			**±100**	µA
DIGITAL INPUTS								
Low Voltage, V_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, Data Load $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			**1.0**			**1.0**	V
Low Current, I_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, Data Load $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			**–400**			**–400**	µA
DIGITAL OUTPUTS								
High Voltage, V_{OH}	DB1–DB16; RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 4.5$ V $I_{OH} = 100$ µA	**2.4**			**2.4**			V
Low Voltage, V_{OL}	DB1–DB16, RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $I_{OL} = 1.2$ mA			**0.4**			**0.4**	V
THREE-STATE LEAKAGE	DB1–DB16 Only							
Current I_L	$+V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OL} = 0$ V			±100			±100	µA
	$+V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OH} = 5.0$ V			±100			±100	µA
POWER SUPPLIES								
Voltage Levels								
$+V_S$		**+10.8**		**+13.2**	**+10.8**		**+13.2**	V
$-V_S$		**–10.8**		**–13.2**	**–10.8**		**–13.2**	V
$+V_L$		**+5**		**+13.2**	**+5**		**+13.2**	V
Current								
$+I_S$	$\pm V_S$ @ ±12 V		**±12**	**±23**		**±12**	**±23**	mA
$+I_S$	$\pm V_S$ @ ±13.2 V		**±19**	**±30**		**±19**	**±30**	mA
$+I_L$	$\pm V_L$ @ ±5.0 V		**±0.5**	**±1.5**		**±0.5**	**±1.5**	mA

NOTES
[1]Refers to small signal bandwidth.
[2]Output offset dependent on value for R6.
[3]Refer to timing diagram.
[4]AD2S82A only.
[5]These pins are referenced to $+V_S$ (i.e., HI = +12 V, LO = 0 V).

Specifications subject to change without notice.
All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.

AD2S81A/AD2S82A–SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Parameter	Conditions	AD2S81A Min	AD2S81A Typ	AD2S81A Max	AD2S82A Min	AD2S82A Typ	AD2S82A Max	Units
RATIO MULTIPLIER								
AC Error Output Scaling	10 Bit					**177.6**		mV/Bit
	12 Bit		**44.4**			**44.4**		mV/Bit
	14 Bit					**11.1**		mV/Bit
	16 Bit					**2.775**		mV/Bit
PHASE SENSITIVE DETECTOR								
Output Offset Voltage				**12**		**12**		mV
Gain								
In Phase	w.r.t. REF	–0.882	–0.9	–0.918	–0.882	–0.9	–0.918	V rms/V dc
In Quadrature	w.r.t. REF			0.04			0.04	V rms/V dc
Input Bias Current			60	**150**		60	**150**	nA
Input Impedance		1			1			MΩ
Input Voltage				±8			±8	V
INTEGRATOR								
Open-Loop Gain	At 10 kHz	57		63	57		63	dB
Dead Zone Current (Hysteresis)			100			100		nA/LSB
Input Offset Voltage			1	5		1	5	mV
Input Bias Current			60	150		60	150	nA
Output Voltage Range	$\pm V_S = \pm 10.8$ V dc	±7						V
VCO	$\pm V_S = \pm 12$ V dc							
Maximum Rate		1.0	1.1		1.0	1.1		MHz
VCO Rate	Positive DIR	**7.1**	**7.9**	**8.7**	**7.1**	**7.9**	**8.7**	kHz/µA
	Negative DIR	**7.1**	**7.9**	**8.7**	**7.1**	**7.9**	**8.7**	kHz/µA
VCO Power Supply Sensitivity								
Increase	$+V_S$		+0.5			+0.5		%/V
	$-V_S$		–8.0			–8.0		%/V
Decrease	$+V_S$		–8.0			–8.0		%/V
	$-V_S$		+2.0			+2.0		%/V
Input Offset Voltage			1	5		1	5	mV
Input Bias Current			70	**380**		70	**380**	nA
Input Bias Current Tempco			–1.22			–1.22		nA/°C
Input Voltage Range				±8			±8	V
Linearity of Absolute Rate								
Full Range				**<2**			**<2**	% FSD
Over 0% to 50% of Full Range				**<1**			**<1**	% FSD
Reversion Error				1.5			1.5	% FSD
Sensitivity of Reversion Error to Symmetry of Power Supplies			±8			±8		%/V of Asymmetry
VCO Output[1, 2]					±2.7	±3.0	±3.3	V/LSB
POWER SUPPLIES								
Voltage Levels								
$+V_S$		**+10.8**		**+13.2**	**+10.8**		**+13.2**	V
$-V_S$		**–10.8**		**–13.2**	**–10.8**		**–13.2**	V
$+V_L$		**+5**		**+13.2**	**+5**		**+13.2**	V
Current								
$+I_S$	$\pm V_S$ @ ±12 V		**±12**	**±23**		**±12**	**±23**	mA
$+I_S$	$\pm V_S$ @ ±13.2 V		**±19**	**±30**		**±19**	**±30**	mA
$+I_L$	$\pm V_L$ @ ±5.0 V		**±0.5**	**±1.5**		**±0.5**	**±1.5**	mA

NOTES
[1]The VCO output swings between ±3 V depending on the resolver direction.
[2]AD2S82A only.

Specifications in **boldface** are tested on all production units at final electrical test. Specifications subject to change without notice.

ORDERING GUIDE

	Accuracy	Operating Temperature Ranges	Package Options*
AD2S81AJD	30 arc min	0°C to +70°C	D-28
AD2S82AHP	22 arc min	–40°C to +85°C	P-44A
AD2S82AJP	8 arc min	–40°C to +85°C	P-44A
AD2S82AKP	4 arc min	–40°C to +85°C	P-44A
AD2S82ALP	2 arc min	–40°C to +85°C	P-44A

*D = Ceramic DIP Package; P = Plastic Leaded Chip Carrier (PLCC) Package.

ESD SENSITIVITY

The AD2S81A and AD2S82A features an input protection circuit consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharge (Human Body Model) and fast, low energy pulses (Charges Device Model).

The AD2S81A and AD2S82A is ESD protection Class II (2000 V min). Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices ESD Prevention Manual.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($+V_S$ to $-V_S$) . . . . . ±12 V dc ±10%
Power Supply Voltage V_L . . . . . +5 V dc ±10%
Analog Input Voltage (SIN and COS) . . . . . 2 V rms ±10%
Analog Input Voltage (REF) . . . . . 1 V to 8 V peak
Signal and Reference Harmonic Distortion . . . . . 10% (max)
Phase Shift Between Signal and Reference . ±10 Degrees (max)
Ambient Operating Temperature Range
Commercial (JD) . . . . . 0°C to +70°C
Industrial (HP, JP, KP, LP) . . . . . –40°C to +85°C

PIN FUNCTION DESCRIPTIONS

Mnemonic	Description
REFERENCE I/P	Reference Signal Input
DEMOD I/P	Demodulator Input
AC ERROR O/P	Ratio Multiplier Output
COS I/P	Cosine Input
ANALOG GND	Power Ground
SIGNAL GND	Resolver Signal Ground
SIN I/P	Sine Input
$+V_S$	Positive Power Supply
DB1–DB16	Parallel Output Data
$+V_L$	Logic Power Supply
$\overline{\text{ENABLE}}$	Logic Hi-Output Data in High Impedance State Logic Lo Present Data to the Output Latches
BYTE SELECT	Logic Hi-Most Significant Byte to DB1–DB8 Logic Lo-Most Significant Byte to DB1–DB8
$\overline{\text{INHIBIT}}$	Logic Lo Inhibits Data Transfer to Output Latches
DIGITAL GND	Digital Ground
SC1–SC2*	Select Converter Resolution
DATA LOAD*	Logic Lo DB1–DB16 Inputs Logic Hi DB1–DB16 Outputs
BUSY	Converter Busy, Data Not Valid While Busy Hi
DIR	Logic State Defines Direction of Input Signal Rotation
RIPPLE CLK	Positive Pulse when Converter Output Changes from 1s to All 0s or Vice Versa
$-V_S$	Negative Power Supply
VCO I/P	VCO Input
INTEGRATOR I/P	Integrator Input
INTEGRATOR O/P	Integrator Output
DEMOD O/P	Demodulator Output
$\overline{\text{COMPLEMENT}}$*	Active Logic Lo
VCO O/P*	VCO Output

*AD2S82A Only.

Bit Weight Table

Binary Bits (N)	Resolution (2^N)	Degrees /Bit	Minutes /Bit	Seconds /Bit
0	1	360.0	21600.0	1296000.0
1	2	180.0	10800.0	648000.0
2	4	90.0	5400.0	324000.0
3	8	45.0	2700.0	162000.0
4	16	22.5	1350.0	81000.0
5	32	11.25	675.0	40500.0
6	64	5.625	337.5	20250.0
7	128	2.8125	168.75	10125.0
8	256	1.40625	84.375	5062.5
9	512	0.703125	42.1875	2531.25
10	1024	0.3515625	21.09375	1265.625
11	2048	0.1757813	10.546875	632.8125
12	4096	0.0878906	5.273438	316.40625
13	8192	0.0439453	2.636719	158.20313
14	16384	0.0219727	1.318359	79.10156
15	32768	0.0109836	0.659180	39.55078
16	65536	0.0054932	0.329590	19.77539
17	131072	0.0027466	0.164795	9.88770
18	262144	0.0013733	0.082397	4.94385

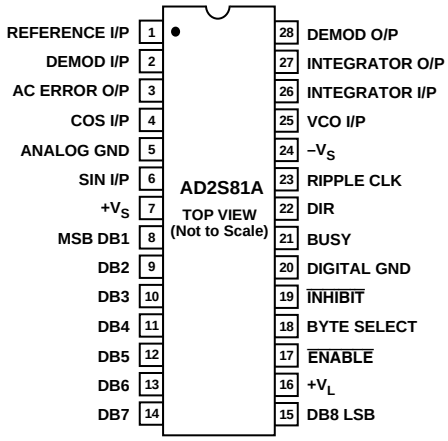
ABSOLUTE MAXIMUM RATINGS[1] (with respect to GND)

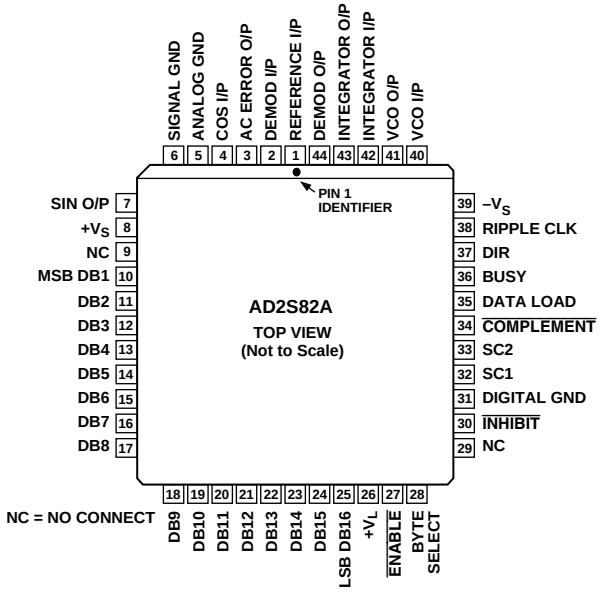
$+V_S$[2] . . . . . +14 V dc
$-V_S$ . . . . . –14 V dc
$+V_L$ . . . . . $+V_S$
Reference . . . . . +14 V to $-V_S$
SIN . . . . . +14 V to $-V_S$
COS . . . . . +14 V to $-V_S$
Any Logical Input . . . . . –0.4 V dc to $+V_L$ dc
Demodulator Input . . . . . +14 V to $-V_S$
Integrator Input . . . . . +14 V to $-V_S$
VCO Input . . . . . +14 V to $-V_S$
Power Dissipation . . . . . 860 mW
Operating Temperature
Commercial (JD) . . . . . 0°C to +70°C
Industrial (HP, JP, KP, LP) . . . . . –40°C to +85°C
Storage Temperature (All Grades) . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

CAUTION

1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

AD2S81A/AD2S82A PIN CONFIGURATIONS





CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be +12 V dc and –12 V dc and must not be reversed. The voltage applied to V_L can be +5 V dc to $+V_S$.

It is recommended that the decoupling capacitors are connected in parallel between the power lines $+V_S$, $-V_S$ and ANALOG GND adjacent to the converter. Recommended values are 100 nF (ceramic) and 10 µF (tantalum). Also capacitors of 100 nF and 10 µF should be connected between $+V_L$ and DIGITAL GND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

The resolver connections should be made to the SIN and COS inputs, REFERENCE I/P and SIGNAL GND as shown in Figure 7 and described in the Connecting the Resolver section.

The two signal ground wires from the resolver should be joined at the SIGNAL GROUND pin of the resolver to minimize the coupling between the sine and cosine signals. For this reason it is also recommended that the resolver is connected using individually screened twisted pair cables with the sine, cosine and reference signals twisted separately.

SIGNAL GND and ANALOG GND are connected internally. ANALOG GND and DIGITAL GND must be connected externally.

The external components required should be connected as shown in Figures 1a and 1b.

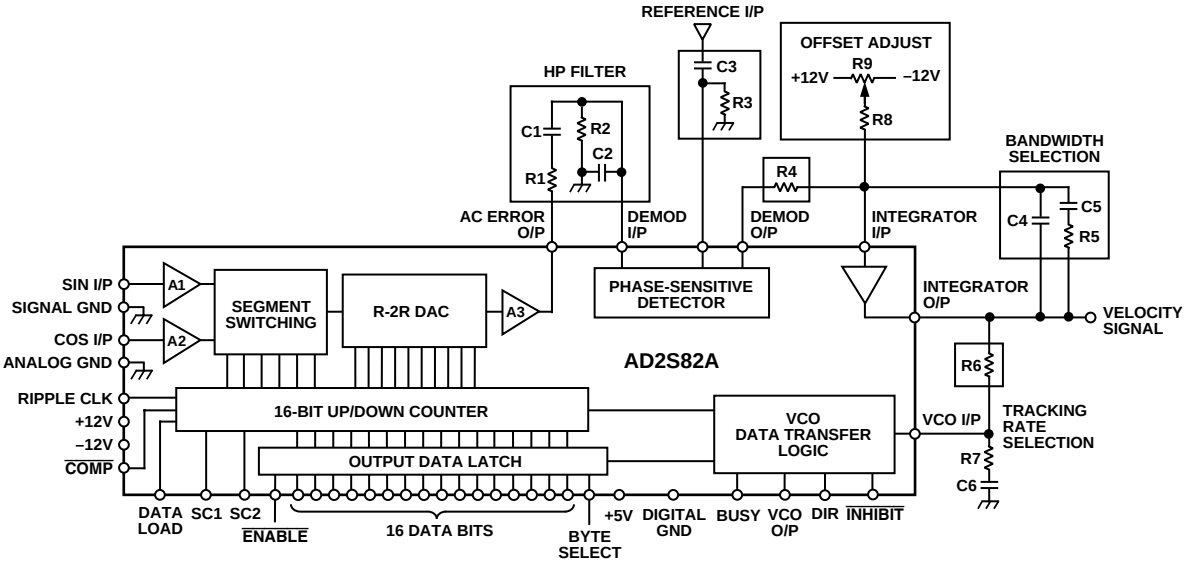


Figure 1a. AD2S82A Connection Diagram

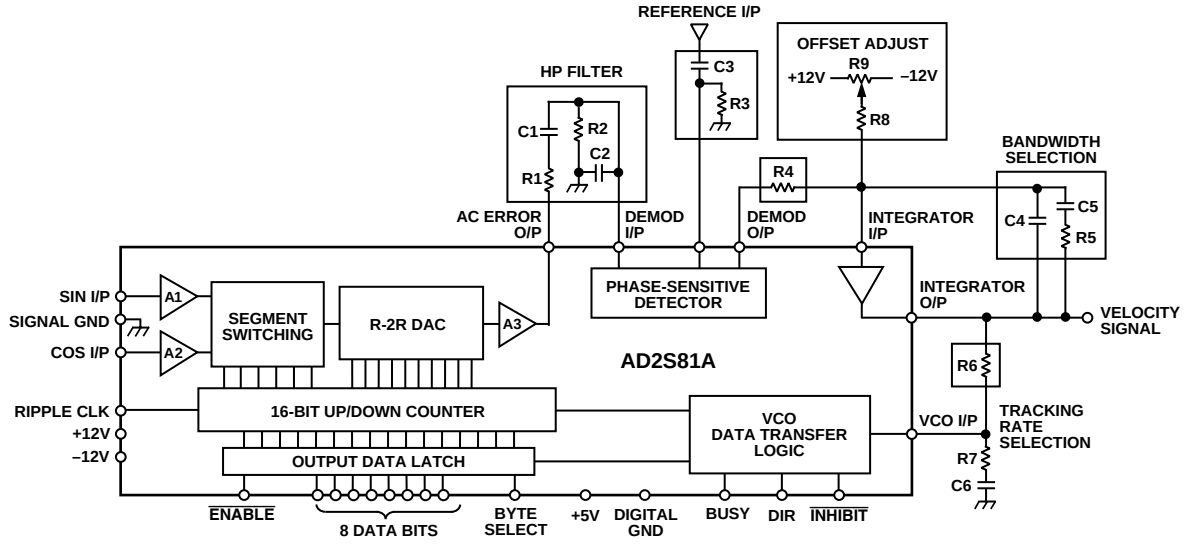


Figure 1b. AD2S81A Connection Diagram

CONVERTER RESOLUTION (AD2S82A ONLY)
Two major areas of the AD2S82A specification can be selected by the user to optimize the total system performance. The resolution of the digital output is set by the logic state of the inputs SC1 and SC2 to be 10, 12, 14 or 16 bits and the dynamic characteristics of bandwidth and tracking rate are selected by the choice of external components.

The choice of the resolution will affect the values of R4 and R6 which scale the inputs to the integrator and the VCO, respectively (see the Component Selection section). If the resolution is changed, then new values of R4 and R6 must be switched into the circuit.

Note: When changing resolution under dynamic conditions, do it when the BUSY is low, i.e., when Data is not changing.

CONVERTER OPERATION
When connected in a circuit such as shown in Figure 1, the AD2S81A/AD2S82A operates as a tracking resolver-to-digital converter and forms a type 2 closed loop system. The output will automatically follow the input for speeds up to the selected maximum tracking rate. No convert command is necessary as the conversion is automatically initiated by each LSB increment, or decrement, of the input. Each LSB change of the converter initiates a BUSY pulse.

The AD2S81A/AD2S82A is remarkably tolerant of input amplitude and frequency variation because the conversion depends only on the ratio of the input signals. Consequently there is no need for accurate, stable oscillator to produce the reference signal. The inclusion of the phase sensitive detector in the conversion loop ensures a high immunity to signals that are not coherent or are in quadrature with the reference signal.

SIGNAL CONDITIONING
The amplitude of the SINE and COSINE signal inputs should be maintained within 10% of the nominal values if full performance is required from the velocity signal.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a loss in accuracy due to internal overload. Reducing levels will result in a steady decline in accuracy. With the signal levels at 50% of the correct value, the angular error will increase to an amount equivalent to 1.3 LSB. At this level the repeatability will also degrade to 2 LSB and the dynamic response will also change, since the dynamic characteristics are proportional to the signal level.

The AD2S81A/AD2S82A will not be damaged if the signal inputs are applied to the converter without the power supplies and/or the reference.

REFERENCE INPUT
The amplitude of the reference signal applied to the converter's input is not critical, but care should be taken to ensure it is kept within the recommended operating limits.

The AD2S81A/AD2S82A will not be damaged if the reference is supplied to the converter without the power supplies and/or the signal inputs.

HARMONIC DISTORTION
The amount of harmonic distortion allowable on the signal and reference lines is 10%.

Square waveforms can be used but the input levels should be adjusted so that the average value is 1.9 V rms. (For example, a square wave should be 1.9 V peak). Triangular and sawtooth waveforms should have a amplitude of 2 V rms.

Note: The figure specified of 10% harmonic distortion is for calibration convenience only.

POSITION OUTPUT
The resolver shaft position is represented at the converter output by a natural binary parallel digital word.

As the digital position output of the converter passes through the major carries, i.e., all "1s" to all "0s" or the converse, a RIPPLE CLK logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is always valid in advance of a RIPPLE CLK pulse and, as it is internally latched, only changing state (1 LSB min change) with a corresponding change in direction.

Both the RIPPLE CLK pulse and the DIR data are unaffected by the application of the $\overline{\text{INHIBIT}}$.

The static positional accuracy quoted is the worst case error that can occur over the full operating temperature excluding the effects of offset signals at the INTEGRATOR I/P (which can be trimmed out–see Figures 1a and 1b), and with the following conditions: input signal amplitudes are within 10% of the nominal; phase shift between signal and reference is less than 10 degrees.

These operating conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice, the AD2S81A/AD2S82A can be used well outside these operating conditions providing the above points are observed.

VELOCITY SIGNAL
The tracking converter technique generates an internal signal at the output of the integrator (the INTEGRATOR O/P pin) that is proportional to the rate of change of the input angle. This is a dc analog output referred to as the VELOCITY signal.

In many applications it is possible to use the velocity signal of the AD2S81A/AD2S82A to replace a conventional tachogenerator.

DC ERROR SIGNAL
The signal at the output of the phase-sensitive detector (DEMOD O/P) is the signal to be nulled by the tracking loop and is, therefore, proportional to the error between the input angle and the output digital angle. This is the dc error of the converter; and as the converter is a type 2 servo loop, it will increase if the output fails to track the input for any reason. It is an indication that the input has exceeded the maximum tracking rate of the converter or, due to some internal malfunction, the converter is unable to reach a null. By connecting two external comparators, this voltage can be used as a "built-in test."

COMPONENT SELECTION

The following instructions describe how to select the external components for the converter in order to achieve the required bandwidth and tracking rate. In all cases the nearest "preferred value'' component should be used and a 5% tolerance will not degrade the overall performance of the converter. Care should be taken that the resistors and capacitors will function over the required operating temperature range. The components should be connected as shown in Figure 1.

PC compatible software is available to help users select the optimum component values for the AD2S81A and AD2S82A, and display the transfer gain, phase and small step response.

For more detailed information and explanation, see the Circuit Functions and Dynamic Performance section.

1. HF Filter (R1, R2, C1, C2)
   The function of the HF filter is to remove any dc offset and to reduce the amount of noise present on the signal inputs to the AD2S81A/AD2S82A, reaching the Phase Sensitive Detector and affecting the outputs. R1 and C2 may be omitted—in which case R2 = R3 and C1 = C3, calculated below—but their use is particularly recommended if noise from switch mode power supplies and brushless motor drive is present.

   Values should be chosen so that

$$15\ k\Omega \le R1 = R2 \le 56\ k\Omega$$

$$C1 = C2 \frac{1}{2\,\pi\, R1\, f_{REF}}$$

   and f_{REF} = Reference Frequency (Hz)

   This filter gives an attenuation of three times at the input to the phase sensitive detector.

2. Gain Scaling Resistor (R4)
   If R1, C2 are fitted, then:

$$R4 = \frac{E_{DC}}{100 \times 10^{-9}} \times \frac{1}{3}\ \Omega$$

   where 100×10^{-9} = current/LSB
   If R1, C2 are not fitted, then:

$$R4 = \frac{E_{DC}}{100 \times 10^{-9}}\ \Omega$$

   where E_{DC} = 160×10^{-3} for 10 bits resolution
   = 40×10^{-3} for 12 bits
   = 10×10^{-3} for 14 bits
   = 2.5×10^{-3} for 16 bits
   = Scaling of the DC ERROR in volts

3. AC Coupling of Reference Input (R3, C3)
   Select R3 and C3 so that there is no significant phase shift at the reference frequency. That is,

$$R3 = 100\ k\Omega$$

$$C3 > \frac{1}{R3 \times f_{REF}}\ F$$

   with $R3$ in Ω.

4. Maximum Tracking Rate (R6)
   The VCO input resistor R6 sets the maximum tracking rate of the converter, and hence the velocity scaling as at the max tracking rate, the velocity output will be 8 V.

   Decide on your maximum tracking rate, "T," in revolutions per second. Note that "T" must not exceed the maximum tracking rate or 1/16 of the reference frequency.

$$R6 = \frac{6.32 \times 10^{10}}{T \times n}\ \Omega$$

   where n = bits per revolution
   = 1,024 for 10 bits resolution
   = 4,096 for 12 bits
   = 16,384 for 14 bits
   = 65,536 for 16 bits

5. Closed-Loop Bandwidth Selection (C4, C5, R5)
   a. Choose the closed-loop bandwidth (f_{BW}) required ensuring that the ratio of reference frequency to bandwidth does exceed the following guidelines:

Resolution	Ratio of Reference Frequency/Bandwidth
10	2.5 : 1
12	4 : 1
14	6 : 1
16	7.5 : 1

   Typical values may be 100 Hz for a 400 Hz reference frequency and 500 Hz to 1000 Hz for a 5 kHz reference frequency.

   b. Select C4 so that

$$C4 = \frac{21}{R6 \times f_{BW}{}^{2}}\ F$$

   with $R6$ in Ω and f_{BW}, in Hz selected above.

   c. C5 is given by

$$C5 = 5 \times C4\ F$$

   d. R5 is given by

$$R5 = \frac{4}{2 \times \pi \times f_{BW} \times C5}\ \Omega$$

6. VCO Phase Compensation
   The following values of C6 and R7 should be fitted.

$$C6 = 470\ pF,\ R7 = 68\ \Omega$$

7. Offset Adjust
   Offsets and bias currents at the integrator input can cause an additional positional offset at the output of the converter of 1 arc minute typical, 5.3 arc minutes maximum. If this can be tolerated, then R8 and R9 can be omitted from the circuit.

   If fitted, the following values of R8 and R9 should be used:

$$R8 = 4.7\ M\Omega,\ R9 = 1\ M\Omega\ potentiometer$$

To adjust the zero offset, ensure the resolver is disconnected and all the external components are fitted. Connect the COS pin to the REFERENCE I/P and the SIN pin to the SIGNAL GND and with the power and reference applied, adjust the potentiometer to give all "0s" on the digital output bits.

The potentiometer may be replaced with select on test resistors if preferred.

DATA TRANSFER

To transfer data the $\overline{\text{INHIBIT}}$ input should be used. The data will be valid 600 ns after the application of a logic "LO" to the $\overline{\text{INHIBIT}}$. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied and allows time for an active BUSY to clear. By using the $\overline{\text{ENABLE}}$ input the two bytes of data can be transferred after which the $\overline{\text{INHIBIT}}$ should be returned to a logic "HI" state to enable the output latches to be updated.

BUSY Output

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses at TTL level. A BUSY pulse is initiated each time the input moves by the analog equivalent of one LSB and the internal counter is incremented or decremented.

$\overline{\text{INHIBIT}}$ Input

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and, therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

$\overline{\text{ENABLE}}$ Input

The $\overline{\text{ENABLE}}$ input determines the state of the output data. A logic "HI" maintains the output data pins in the high impedance condition, and the application of a logic "LO" presents the data in the latches to the output pins. The operation of the $\overline{\text{ENABLE}}$ has no effect on the conversion process.

BYTE SELECT Input

The BYTE SELECT input on the AD2S82A selects the byte of the position data to be presented at the data output DB1 to DB8. The least significant byte will be presented on data output DB9 to DB16 (with the $\overline{\text{ENABLE}}$ input taken to a logic "LO") regardless of the state of the BYTE SELECT pin. Note that when the AD2S82A is used with a resolution less than 16 bits, the unused data lines are pulled to a logic "LO." A logic "HI" on the BYTE SELECT input will present the eight most significant data bits on data output DB1 and DB8. A logic "LO" will present the least significant byte on data outputs 1 to 8, i.e., data outputs 1 to 8 will duplicate data outputs 9 to 16.

When the BYTE select pin is a logic "HI" on the AD2S81A, the most significant byte is presented on Pins 8 to 15 (with the $\overline{\text{ENABLE}}$ input taken to a logic "LO"). A logic "HI" presents the 4 least significant bits on Pins 8 to 11 and places a logic "LO" on Pins 12 to 15 (with the $\overline{\text{ENABLE}}$ input taken to a logic "LO").

The operation of the BYTE SELECT has no effect on the conversion process of the converter.

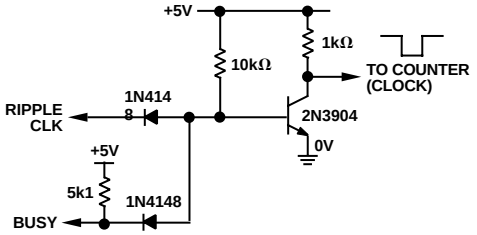
RIPPLE CLOCK

As the output of the converter passes through the major carry, i.e., all "1s" to all "0s" or the converse, a positive going edge on the RIPPLE CLK output is initiated indicating that a revolution, or a pitch, of the input has been completed.

The minimum pulsewidth of the ripple clock is 300 ns. RIPPLE CLK is normally set high before a BUSY pulse and resets before the next positive going edge of the next consecutive pulse.

The only exception to this is when DIR changes while the RIPPLE CLK is high. Resetting of the RIPPLE CLK will only occur if the DIR remains stable for two consecutive positive BUSY pulse edges.

If the AD2S81A/AD2S82A is being used in a pitch and revolution counting application, the ripple and busy will need to be gated to prevent false decrement or increment (see Figure 2). RIPPLE CLK is unaffected by $\overline{\text{INHIBIT}}$.



NOTE: DO NOT USE ABOVE CCT WHEN $\overline{\text{INHIBIT}}$ IS "LO."

Figure 2. Diode Transistor Logic Nand Gate

DIRECTION Output

The DIRECTION (DIR) logic output indicates the direction of the input rotation. Any change in the state of DIR precedes the corresponding BUSY, DATA, and RIPPLE CLK updates. DIR can be considered as an asynchronous output and can make multiple changes in state between two consecutive LSB update cycles. This corresponds to a change in input rotation direction but less than 1 LSB.

$\overline{\text{COMPLEMENT}}$ (AD2S82A Only)

The $\overline{\text{COMPLEMENT}}$ input is internally pulled to +12 V in the INACTIVE STATE. It is pulled down to DIGITAL GROUND (100 μA) to ACTIVATE.

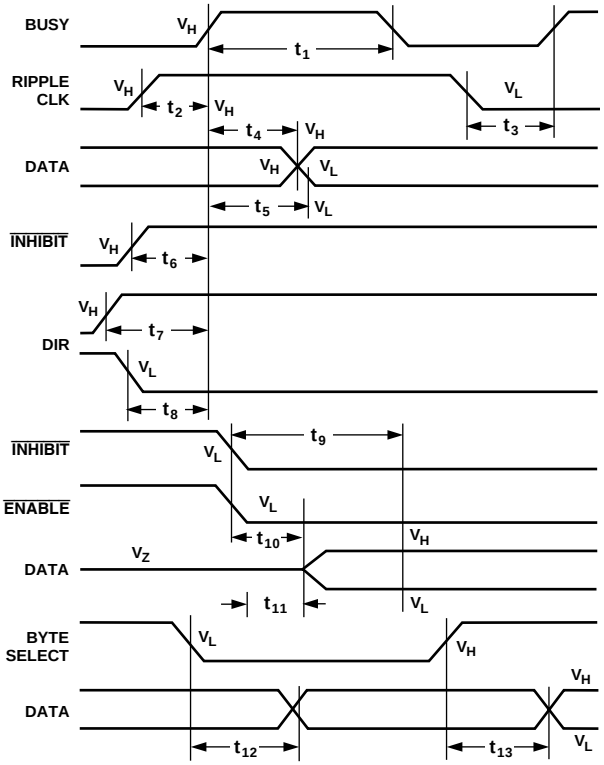
When used in conjunction with DATA LOAD, strobing DATA LOAD and $\overline{\text{COMPLEMENT}}$ pins to logic LO, will set the logic HIGH bits of the AD2S82A counter to a LO state. Those bits of the applied data which are logic LO will not change the corresponding bits in the AD2S82A counter:

For Example:

Initial Counter State	1 0 1 0 1
Applied Data Word	1 1 0 0 0
Counter State after Data Load	1 1 0 0 0
Initial Counter State	1 0 1 0 1
Applied Data Word	1 1 0 0 0
Counter State after Data Load and Complement	0 0 1 0 1

In order to read the output the following procedures should be followed:

1. Place Outputs in high impedance ($\overline{\text{ENABLE}}$ = HI).
2. Present data to pins.
3. Pull DATA LOAD and $\overline{\text{COMPLEMENT}}$ pins to ground.
4. Wait 100 ns.
5. Remove data from pins.
6. Remove outputs from high impedance state ($\overline{\text{ENABLE}}$ = LO).
7. Read outputs.



PARAMETER	T_{MIN}	T_{MAX}	CONDITION
t_1	200	600	BUSY WIDTH V_H–V_H
t_2	10	25	RIPPLE CLOCK V_H TO BUSY V_H
t_3	470	580	RIPPLE CLOCK V_L TO NEXT BUSY V_H
t_4	16	45	BUSY V_H TO DATA V_H
t_5	3	25	BUSY V_H TO DATA V_L
t_6	70	140	$\overline{\text{INHIBIT}}$ V_H TO BUSY V_H
t_7	485	625	MIN DIR V_H TO BUSY V_H
t_8	515	670	MIN DIR V_H TO BUSY V_H
t_9	–	600	$\overline{\text{INHIBIT}}$ V_L TO DATA STABLE
t_{10}	40	110	$\overline{\text{ENABLE}}$ V_L TO DATA V_H
t_{11}	35	110	$\overline{\text{ENABLE}}$ V_L TO DATA V_L
t_{12}	60	140	BYTE SELECT V_L TO DATA STABLE
t_{13}	60	125	BYTE SELECT V_H TO DATA STABLE

Figure 3. Digital Timing

CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE

The AD2S81A/AD2S82A allows the user greater flexibility in choosing the dynamic characteristics of the resolver-to-digital conversion to ensure the optimum system performance. The characteristics are set by the external components shown in Figure 1, and the Component Selection section explains how to select desired maximum tracking rate and bandwidth values. The following paragraphs explain in greater detail the circuit of the AD2S81A/AD2S82A and the variations in the dynamic performance available to the user.

Loop Compensation

The AD2S81A and AD2S82A (connected as shown in Figure 1a and 1b) operates as a type 2 tracking servo loop where the VCO/counter combination and integrator perform the two integration functions inherent in a type 2 loop.

Additional compensation in the form of a pole/zero pair is required to stabilize any type 2 loop to avoid the loop gain characteristic crossing the 0 dB axis with 180° of additional phase lag, as shown in Figure 6. This compensation is implemented by the integrator components (R4, C4, R5, C5).

The overall response of such a system is that of a unity gain second order low pass filter, with the angle of the resolver as the input and the digital position data as the output.

The AD2S81A/AD2S82A does not have to be connected as tracking converter, parts of the circuit can be used independently. This is particularly true of the Ratio Multiplier which can be used as a control transformer (see Application Note).

A block diagram of the AD2S81A/AD2S82A is given in Figure 4.

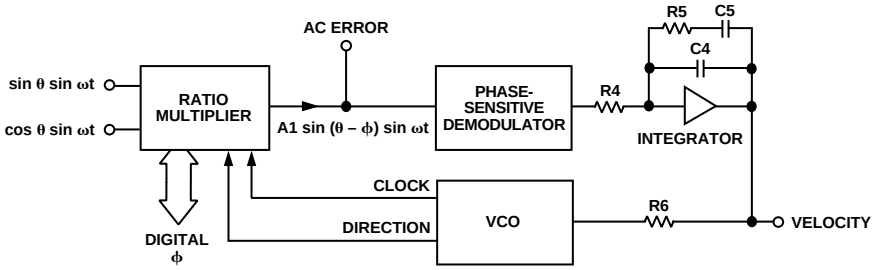


Figure 4. AD2S81A/AD2S82A Functional Diagram

Ratio Multiplier

The ratio multiplier is the input section of the AD2S81A/AD2S82A and compares the signal from the resolver input angle, θ, to the digital angle, ϕ, held in the counter. Any difference between these two angles results in an analog voltage at the AC ERROR OUTPUT. This circuit function has historically been called a "Control Transformer" as it was originally performed by an electromechanical device known by that name.

The AC ERROR signal is given by

$$A1 \sin(\theta - \phi) \sin \omega t$$

where $\omega = 2\pi f_{REF}$

f_{REF} = reference frequency

A1, the gain of the ratio multiplier stage is 14.5.

So for 2 V rms inputs signals
AC ERROR output in volts/(bit of error)

$$= 2 \times \sin\left(\frac{360}{n}\right) \times A1$$

Where n = bits per rev
= 1,024 for 10-bits resolution
= 4,096 for 12 bits
= 16,384 for 14 bits
= 65,536 for 16 bits

Giving an AC ERROR O/P
= 178 mV/bit @ 10-bits resolution
= 44.5 mV/bit @ 12 bits
= 11.125 mV/bit @ 14 bits
= 2.78 mV/bit @ 16 bits

The ratio multiplier will work in exactly the same way whether the AD2S81A/AD2S82A is connected as a tracking converter or as a control transformer, where data is preset into the counters using the DATA LOAD pin.

HF Filter

The AC ERROR OUTPUT may be fed to the PSD via a simple ac coupling network (R2, C1) to remove any dc offset at this point. Note, however, that the PSD of the AD2S81A/AD2S82A is a wideband demodulator and is capable of aliasing HF noise down to within the loop bandwidth. This is most likely to happen where the resolver is situated in particularly noisy environments, and the user is advised to fit a simple HF filter R1, C2 prior to the phase sensitive demodulator.

The attenuation and frequency response of a filter will affect the loop gain and must be taken into account in deriving the loop transfer function. The suggested filter (R1, C1, R2, C2) is shown in Figure 1 and gives an attenuation at the reference frequency (f_{REF}) of 3 times at the input to the phase sensitive demodulator.

Values of components used in the filter must be chosen to ensure that the phase shift at f_{REF} is within the allowable signal to reference phase shift of the converter.

Phase Sensitive Demodulator

The phase sensitive demodulator is effectively ideal and develops a mean dc output at the DEMODULATOR O/P pin of

$$\frac{\pm 2\sqrt{2}}{\pi} \times (DEMODULATOR\ I/P\ rms\ voltage)$$

for sinusoidal signals in phase or antiphase with the reference (for a square wave the DEMODULATOR O/P voltage will equal the DEMODULATOR I/P). This provides a signal at the DEMODULATOR O/P which is a dc level proportional to the positional error of the converter.

DC Error Scaling = 160 mV/bit (10-bits resolution)
= 40 mV/bit (12-bits resolution)
= 10 mV/bit (14-bits resolution)
= 2.5 mV/bit (16-bits resolution)

When the tracking loop is closed, this error is nulled to zero unless the converter input angle is accelerating.

Integrator

The integrator components (R4, C4, R5, C5) are external to the AD2S81A/AD2S82A to allow the user to determine the optimum dynamic characteristics for any given application. The Component Selection section explains how to select components for a chosen bandwidth.

Since the output from the integrator is fed to the VCO INPUT, it is proportional to velocity (rate of change of output angle) and can be scaled by selection of R6, the VCO input resistor. This is explained in the Voltage Controlled Oscillator (VCO) section below.

To prevent the converter from "flickering" (i.e., continually toggling by ±1 bit when the quantized digital angle, ϕ, is not an exact representation of the input angle, θ), feedback is internally applied from the VCO to the integrator input to ensure that the VCO will only update the counter when the error is greater than or equal to 1 LSB. In order to ensure that this feedback "hysteresis" is set to 1 LSB the input current to the integrator must be scaled to be 100 nA/bit. Therefore,

$$R4 = \frac{DC\ Error\ Scaling\ (mV/bit)}{100\ (nA/bit)}$$

Any offset at the input of the integrator will affect the accuracy of the conversion as it will be treated as an error signal and offset the digital output. One LSB of extra error will be added for each 100 nA of input bias current. The method of adjusting out this offset is given in the Component Selection section.

Voltage Controlled Oscillator (VCO)

The VCO is essentially a simple integrator feeding a pair of dc level comparators. Whenever the integrator output reaches one of the comparator threshold voltages, a fixed charge is injected into the integrator input to balance the input current. At the same time the counter is clocking either up or down, dependent on the polarity of the input current. In this way the counter is clocked at a rate proportional to the magnitude of the input current of the VCO.

During the reset period the input continues to be integrated, the reset period is constant at 400 ns.

The VCO rate is fixed for a given input current by the VCO scaling factor:

$$= 7.9\ kHz\ /\ \mu A$$

The tracking rate in rps per µA of VCO input current can be found by dividing the VCO scaling factor by the number of LSB changes per rev (i.e., 4096 for 12-bit resolution).

The input resistor R6 determines the scaling between the converter velocity signal voltage at the INTEGRATOR O/P pin and the VCO input current. Thus to achieve a 5 V output at 100 rps (6000 rpm) and 12-bit resolution the VCO input current must be:

$$(100 \times 4096)\,/\,(7900) = 51.8\ \mu A$$

Thus, R6 would be set to: $5/(51.8 \times 10^{-6}) = 96\ k\Omega$

The velocity offset voltage depends on the VCO input resistor, R6, and the VCO bias current and is given by

$$Velocity\ Offset\ Voltage = R6 \times (VCO\ bias\ current)$$

The temperature coefficient of this offset is given by

$$Velocity\ Offset\ Tempco = R6 \times (VCO\ bias\ current\ tempco)$$

where the VCO bias current tempco is typically –1.22 nA/°C.

The maximum recommended rate for the VCO is 1.1 MHz which sets the maximum possible tracking rate.

Since the minimum voltage swing available at the integrator output is ±8 V, this implies that the minimum value for R6 is 57 kΩ. As

$$Max\ Current = \frac{1.1 \times 10^{6}}{7.9 \times 10^{3}} = 139\ \mu A$$

$$Min\ Value\ R6 = \frac{8}{139 \times 10^{-6}} = 57\ k\Omega$$

VCO OUTPUT

In order to overcome the "freeplay" inherent in a servo system using digitized position feedback, an analog output voltage is available representing the resolver shaft position within the least significant bit of digital angle output.

The converter updates the output if the error is an LSB or greater and the VCO output gives the positional error smaller than 1 LSB.

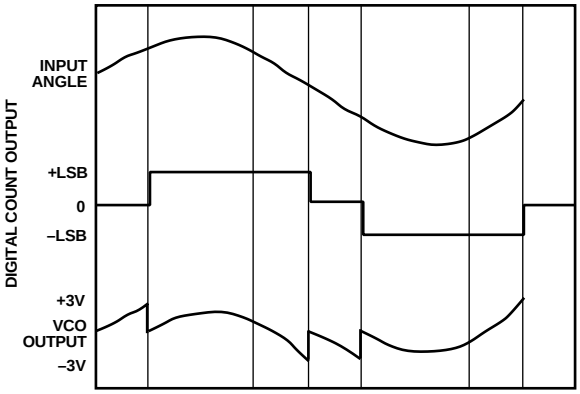


Figure 5.

Figure 5 illustrates how the VCO output compensates for instances where, due to hysteresis, there is no change in the digital count output for 1 LSB change in input angle. The sum of the digital count output and VCO output equals the actual input angle.

Transfer Function

By selecting components using the method outlined in the Component Selection section, the converter will have a critically damped time response and maximum phase margin. The Closed-Loop Transfer Function is given by:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{14\,(1+s_N)}{(s_N+2.4)(s_N^2+3.4\,s_N+5.8)}$$

where S_N, the normalized frequency variable, is:

$$S_N = \frac{2}{\pi}\frac{s}{f_{BW}}$$

and f_{BW} is the closed loop 3 dB bandwidth (selected by the choice of external components).

The acceleration constant, K_A, is given approximately by

$$K_A = 6 \times (f_{BW})^2\ \sec^{-2}$$

The normalized gain and phase diagrams are given in Figures 6 and 7.

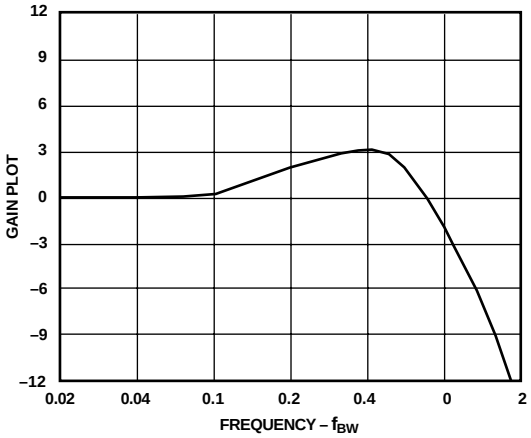


Figure 6. AD2S81A/AD2S82A Gain Plot

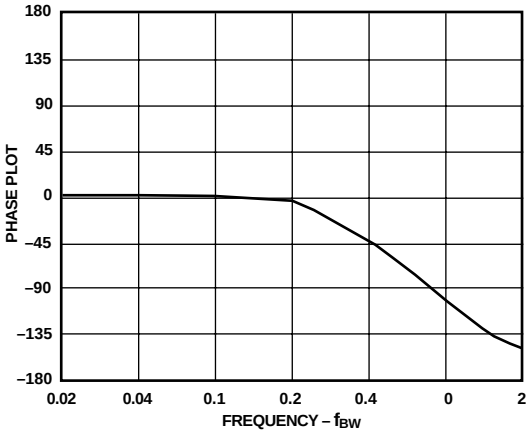


Figure 7. AD2S81A/AD2S82A Phase Plot

The small signal step response is shown in Figure 8. The time from the step to the first peak is t_1 and the t_2 is the time from the step until the converter is settled to 1 LSB. The times t_1 and t_2 are given approximately by

$$t_1 = \frac{1}{f_{BW}}$$

$$t_2 = \frac{5}{f_{BW}} \times \frac{R}{12}$$

where R = resolution, i.e., 10, 12, 14 or 16.

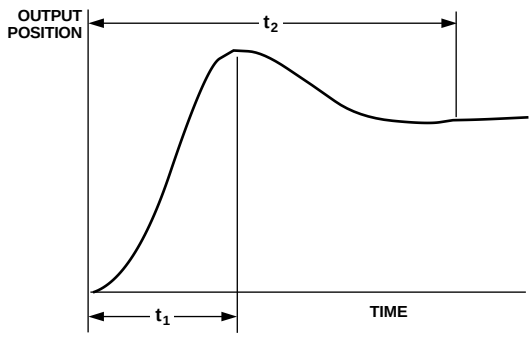


Figure 8. AD2S81A/AD2S82A Small Step Response

The large signal step response (for steps greater than 5 degrees) applies when the error voltage exceeds the linear range of the converter.

Typically the converter will take three times longer to reach the first peak for a 179 degrees step.

In response to a velocity step, the velocity output will exhibit the same time response characteristics as outlined above for the position output.

ACCELERATION ERROR

A tracking converter employing a type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_A of the converter.

$$K_A = \frac{Input\ Acceleration}{Error\ in\ Output\ Angle}$$

The numerator and denominator must have consistent angular units. For example, if K_A is in sec^{-2}, then the input acceleration may be specified in degrees/sec^2 and the error output in degrees. Angular measurement may also be specified using radians, minutes of arc, LSBs, etc.

K_A does not define maximum input acceleration, only the error due to it's acceleration. The maximum acceleration allowable before the converter loses track is dependent on the angular accuracy requirements of the system.

$$Angular\ Accuracy \times K_A = degrees/sec^2$$

K_A can be used to predict the output position error for a given input acceleration. For example for an acceleration of 100 revs/sec^2, $K_A = 2.7 \times 10^6\ sec^{-2}$ and 12-bit resolution.

$$Error\ in\ LSBs = \frac{Input\ Acceleration\,[LSB/sec^2]}{K_A[sec^{-2}]}$$

$$= \frac{100\,[rev/sec^2] \times 2^{12}}{2.7 \times 10^6} = 0.15\ LSBs\ or\ 47.5\ seconds\ of\ arc$$

To determine the value of K_A based on the passive components used to define the dynamics of the converter, the following should be used:

$$K_A = \frac{4.04 \times 10^{11}}{2^n \cdot R6 \cdot R4 \cdot (C4 + C5)}$$

Where n = resolution of the converter

$R4$, $R6$ in ohms

$C5$, $C4$ in farads

SOURCES OF ERRORS

Integrator Offset

Additional inaccuracies in the conversion of the resolver signals will result from an offset at the input to the integrator as it will be treated as an error signal. This error will typically be 1 arc minute over the operating temperature range.

A description of how to adjust from zero offset is given in the Component Selection section and the circuit required is shown in Figures 1a and 1b.

Differential Phase Shift

Phase shift between the sine and cosine signals from the resolver is known as differential phase shift and can cause static error. Some differential phase shift will be present on all resolvers as a result of coupling. A small resolver residual voltage (quadrature voltage) indicates a small differential phase shift. Additional phase shift can be introduced if the sine channel wires and the cosine channel wires are treated differently. For instance, different cable lengths or different loads could cause differential phase shift.

The additional error caused by differential phase shift on the input signals approximates to

Error = 0.53 a × b arc minutes
where a = differential phase shift (degrees).
b = signal to reference phase shift (degrees).

This error can be minimized by choosing a resolver with a small residual voltage, ensuring that the sine and cosine signals are handled identically and removing the reference phase shift (see Connecting the Resolver section). By taking these precautions the extra error can be made insignificant.

Under static operating conditions phase shift between the reference and the signal lines alone will not theoretically affect the converter's static accuracy.

However, most resolvers exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{Shaft\ Speed\ (rps) \times Phase\ Shift\ (Degrees)}{Reference\ Frequency}$$

For example, for a phase shift of 20 degrees, a shaft rotation of 22 rps and a reference frequency of 5 kHz, the converter will exhibit an additional error of:

$$\frac{22 \times 20}{5000} 0.088 \textit{ degrees}$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver (see Connecting the Resolver section).

Note: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.

VELOCITY ERRORS

The signal at the INTEGRATOR O/P pin relative to the ANALOG GND pin is an analog voltage proportional to the rate of change of the input angle. This signal can be used to stabilize servo loops or in the place of a velocity transducer. Although the conversion loop of the AD2S81A/AD2S82A includes a digital section, there is an additional analog feedback loop around the velocity signal. This ensures against flicker in the digital positional output in both dynamic and static states.

A better quality velocity signal will be achieved if the following points are considered:

1. Protection.
   The velocity signal should be buffered before use.
2. Reversion error*
   The reversion error can be nulled by varying one supply rail relative to the other.
3. Ripple and Noise.
   Noise on the input signals to the converter is the major cause of noise on the velocity signal. This can be reduced to a minimum if the following precautions are taken:

   The resolver is connected to the converter using separate twisted pair cable for the sine, cosine and reference signals.

   Care is taken to reduce the external noise wherever possible.

   An HF filter is fitted before the Phase-Sensitive Demodulator (as described in the section HF FILTER).

   A resolver is chosen that has low residual voltage, i.e., a small signal in quadrature with the reference.

   Components are selected to operate the AD2S81A/AD2S82A with the lowest acceptable bandwidth.

   Feedthrough of the reference frequency should be removed by a filter on the velocity signal.

   Maintenance of the input signal voltages at 2 V rms will prevent LSB flicker at the positional output. The analog feedback or hysteresis employed around the VCO and the integrator is a function of the input signal levels (see Integrator section).

*Reversion error, or side-to-side nonlinearity, is a result of differences in the up and down rates of the VCO.

Following the preceding precautions will allow the user to use the velocity signal in very noisy environments for example PWM motor drive applications. Resolver/converter error curves may exhibit apparent acceleration/deceleration at a constant velocity. This results in ripple on the velocity signal of frequency twice the input rotation.

CONNECTING THE RESOLVER

The recommended connection circuit is shown in Figure 9.

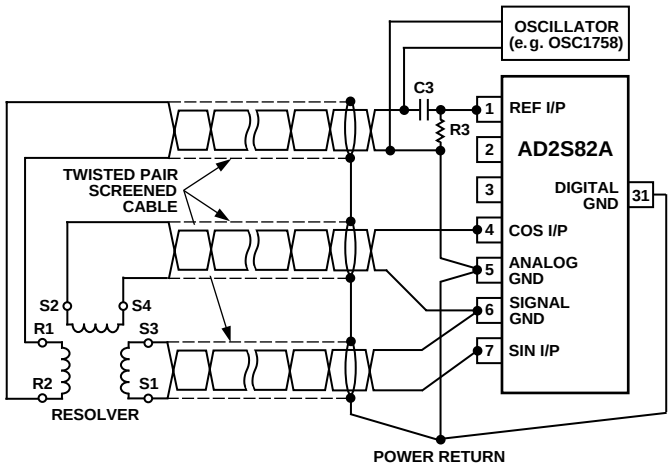


Figure 9. Connecting the AD2S82A to a Resolver

In cases where the reference phase relative to the input signals from the resolver requires adjustment, this can be easily achieved by varying the value of the resistor R2 of the HF filter (see Figures 1a and 1b).

Assuming that R1 = R2 = R and C1 = C2 = C

and Reference Frequency = $\frac{1}{2\pi RC}$

by altering the value of R2, the phase of the reference relative to the input signals will change in an approximately linear manner for phase shifts of up to 10 degrees.

Increasing R2 by 10% introduces a phase lag of 2 degrees. Decreasing R2 by 10% introduces a phase lead of 2 degrees.

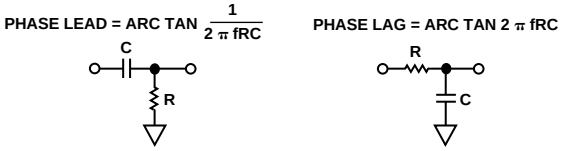


Figure 10. Phase Shift Circuits

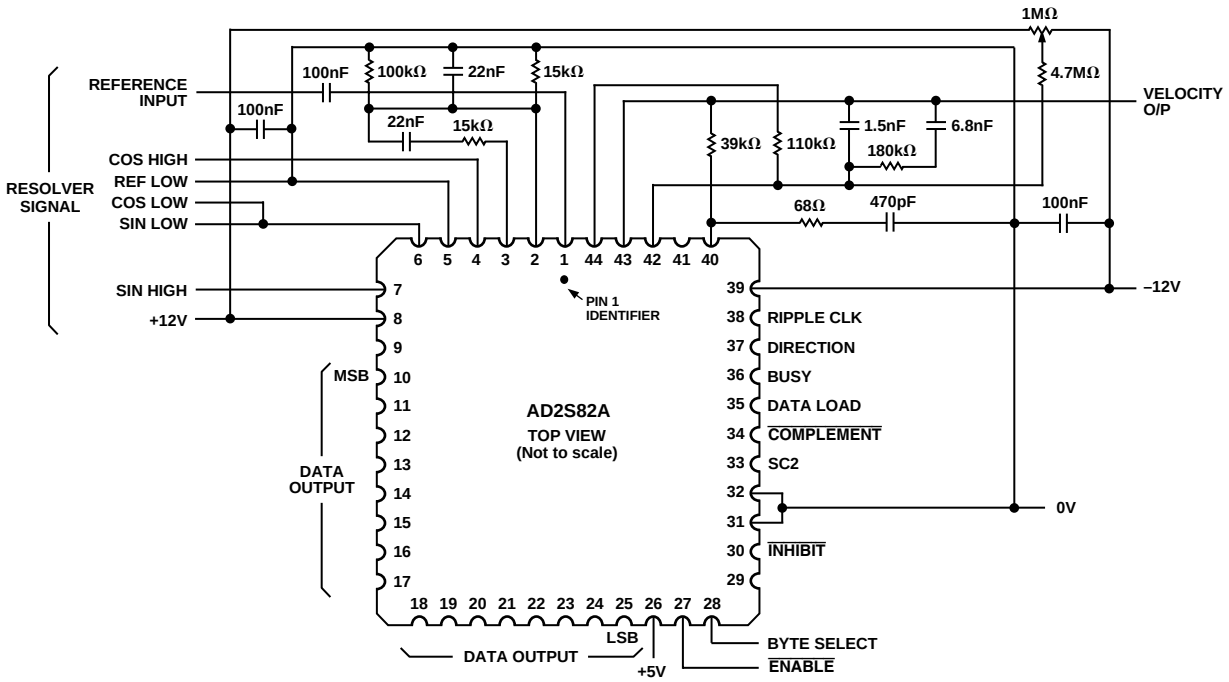


Figure 11. Typical Circuit Configuration

TYPICAL CIRCUIT CONFIGURATION

Figure 11 shows a typical circuit configuration for the AD2S81A/AD2S82A in a 12-bit resolution mode. Values of the external components have been chosen for a reference frequency of 5 kHz and a maximum tracking rate of 260 rps with a bandwidth of 520 Hz. Placing the values for R4, R6, C4 and C5 in the equation for K_A gives a value of 2.7×10^6. The resistors are 0.125 W, 5% tolerance preferred values. The capacitors are 100 V ceramic, 10% tolerance components.

For signal and reference voltages greater than 2 V rms a simple voltage divider circuit of resistors can be used to generate the correct signal level at the converter. Care should be taken to ensure that the ratios of the resistors between the sine signal line and ground and the cosine signal line and ground are the same. Any difference will result in an additional position error.

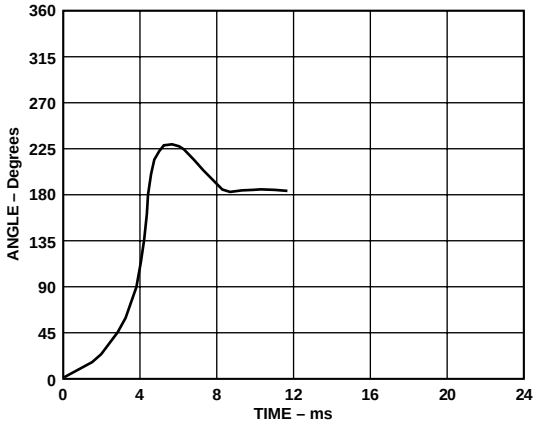


Figure 12. Large Step Response Curves for Typical Circuit Shown in Figure 11

For more information on resistive scaling of SIN, COS and REFERENCE converter inputs, refer to the application note "Circuit Applications of the 2S81 and 2S80 Resolver-to-Digital Converters."

APPLICATIONS

Control Transformer

The ratio multiplier of the AD2S82A can be used independently of the loop integrators as a *control transformer*. In this mode the resolver inputs θ are multiplied by a digital angle ϕ, any difference between and ϕ and θ will be represented by the AC ERROR output as SIN ωt sin (θ–ϕ) or the DEMOD output as sin (θ–ϕ). To use the AD2S81A/AD2S82A in this mode refer to the "Control Transformer" application note.

Dynamic Switching

In applications where the user requires wide band response from the converter, for example 100 rpm to 6000 rpm, superior performance is achieved if the converters control characteristics are switched dynamically. This reduces velocity offset levels at low tracking rates. For more information on the technique refer to "Dynamic Resolution Switching Using the Variable Resolution Monolithic Resolver-to-Digital Converters."

OTHER PRODUCTS

The AD2S80A is a monolithic resolver-to-digital converter offering 10–16 bits of resolution and user selectable dynamics. The AD2S80A is also available in 40-lead ceramic DIP, 44-lead LCC and is qualified to MIL-STD 883B Rev C.

The AD2S46 is a highly integrated hybrid resolver/synchro to digital converter packaged in a 28-lead ceramic DIP. The part offers the user 1.3 arc minutes of accuracy over the full military temperature range.

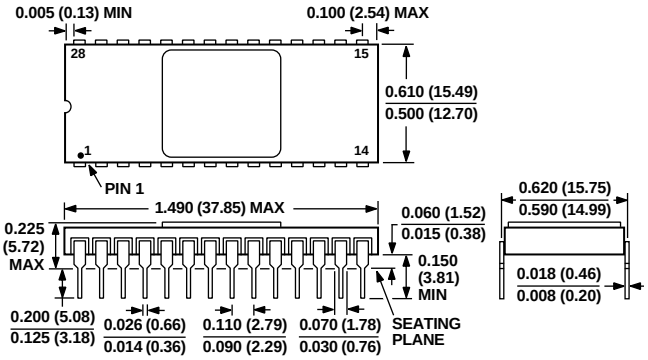
The AD2S34 is a dual channel 14-bit hybrid resolver-to-digital converter packaged in a 1 in^2 32-lead flatpack.

The 1740/41/42 are hybrid resolver/synchro to digital converters which incorporate pico-transformer isolated input signal conditioning.

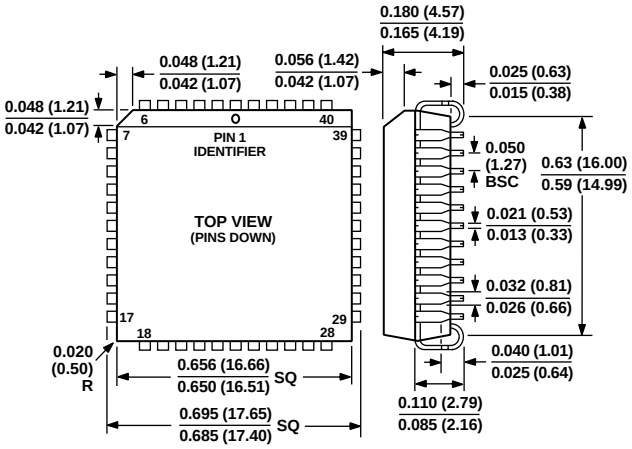
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Ceramic DIP (D) Package (D-28)



Plastic Leaded Chip Carrier (P) Package (P-44A)



C1453b–2.5–11/98

PRINTED IN U.S.A.

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331