# Precision 1-13 Clock Buffer

## Features

- High-speed, low-noise, non-inverting, 1-13 buffer
- Supports up to four SDRAM DIMMs
- Low skew (< 250ps) between any two output clocks
- $I^2C$ Serial Configuration interface
- Multiple $V_{DD}$, $V_{SS}$ pins for noise reduction
- 3.3V power supply voltage
- Separate Hi-Z pin for testing
- Packaging (Pb-free & Green available):
  - 28-pin SSOP (H)

## Description

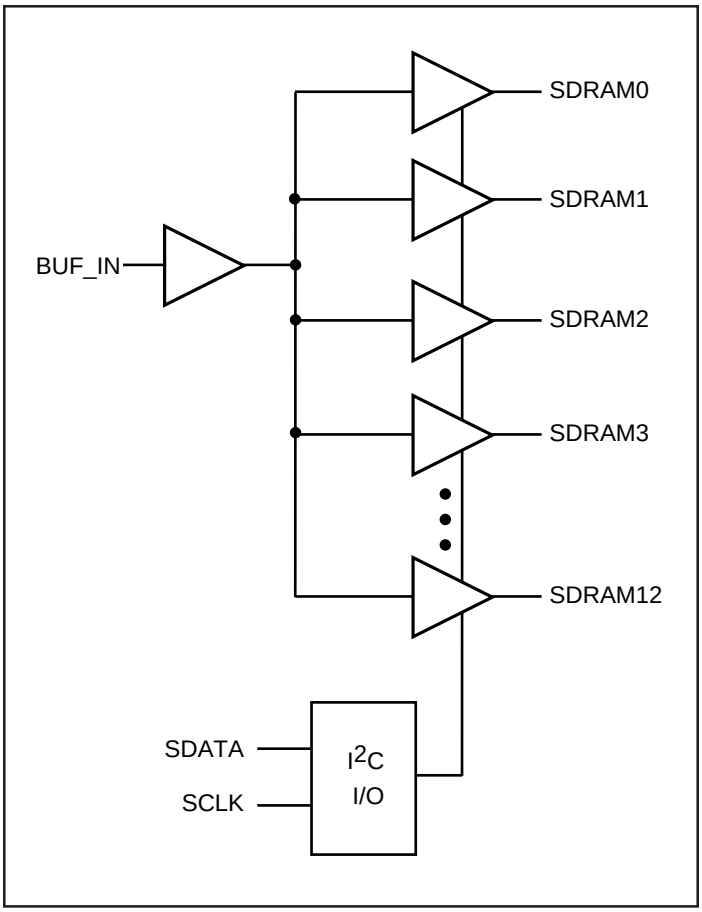
The PI6C184 is a high-speed low-noise 1-13 non-inverting buffer designed for SDRAM clock buffer applications.

This buffer is intended to be used with the PI6C104 clock generator for Intel Architecture for both desktop and mobile systems.

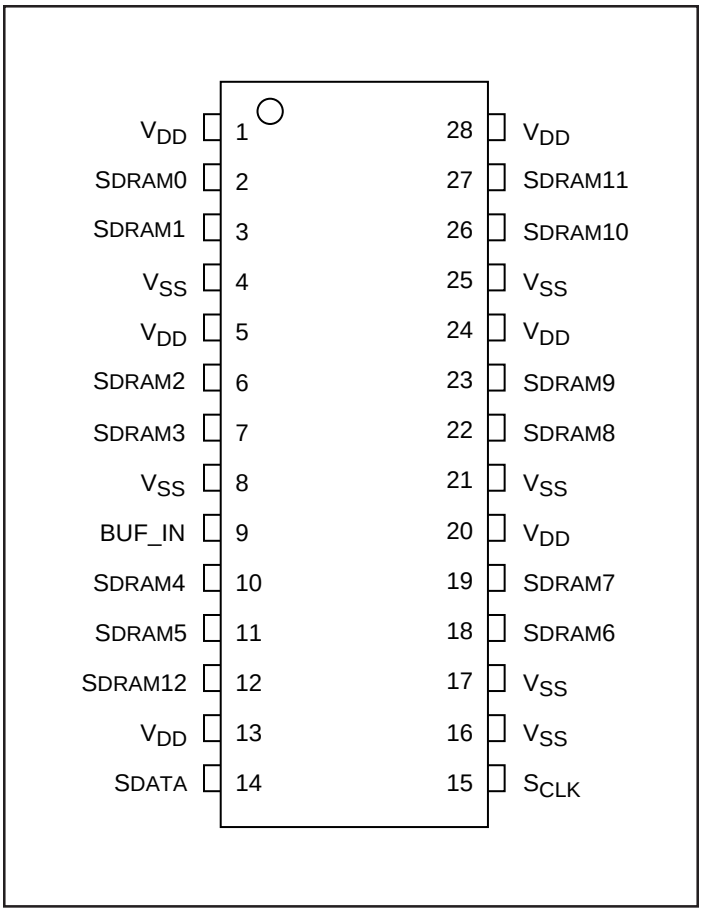
At power-up, all SDRAM outputs are enabled and active. The $I^2C$ Serial control may be used to individually activate/deactivate any of the 13 output drivers.

**Note:**
Purchase of $I^2C$ components from Pericom conveys a license to use them in an $I^2C$ system as defined by Philips®.

## Block Diagram




## Pin Configuration



## Pin Description

| Pin | Symbol | Type | Quantity | Description |
|---|---|---|---|---|
| 2,3,6,7,10,11,18,19 | SDRAM [0.7] | 0 | 8 | SDRAM Byte 0 clock output |
| 26,27,12 | SDRAM [10.12] | 0 | 3 | SDRAM Byte 1 clock output |
| 22,23 | SDRAM [8.9] | 0 | 2 | SDRAM Byte 2 clock output |
| 9 | BUF_IN | 1 | 1 | Input for 1-13-buffer |
| 14 | SDATA | I/O | 1 | Data pin for $I^2C$ circuitry. Has a 100k Internal pull-up resistor |
| 15 | SCLK | I/O | 1 | Clock pin for $I^2C$ circuitry. Has a 100k Internal pull-up resistor |
| 1,5,13,20,24,28 | $V_{DD}$ | Power | 6 | 3.3V power supply for SDRAM buffer |
| 4,8,16,17,21,25 | $V_{SS}$ | Ground | 6 | Ground for SDRAM Buffers |

## Serial Configuration Map

**Byte0: SDRAM Active/Inactive Register**
**(1 = enable, 0 = disable)**

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | 19 | SDRAM7 (Active/Inactive) |
| Bit 6 | 18 | SDRAM6 (Active/Inactive) |
| Bit 5 | 11 | SDRAM5 (Active/Inactive) |
| Bit 4 | 10 | SDRAM4 (Active/Inactive) |
| Bit 3 | 7 | SDRAM3 (Active/Inactive) |
| Bit 2 | 6 | SDRAM2 (Active/Inactive) |
| Bit 1 | 3 | SDRAM1 (Active/Inactive) |
| Bit 0 | 2 | SDRAM0 (Active/Inactive) |

**Note:**
Inactive means outputs are held LOW and are disabled from switching

## $I^2C$ Address Assignment

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |

## 2-Wire I²C Control

The I²C interface permits individual enable/disable of each clock output and test mode enable.

The PI6C184 is a slave receiver device. It can not be read back. Sub addressing is not supported. All preceding bytes must be sent in order to change one of the control bytes.

Every bite put on the SDATA line must be 8-bits long (MSB first), followed by an acknowledge bit generated by the receiving device. During normal data transfers SDATA changes only when SCLK is LOW. Exceptions: A HIGH-to-LOW transition on SDATA while SCLK is HIGH indicates a "start" condition. A LOW-to-HIGH transition on SDATA while SCLK is HIGH is a "stop" condition and indicates the end of a data transfer cycle.

Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always a 7-bit address byte followed by a read/write bit. (HIGH = read from addressed device, LOW= write to addressed device). If the device's own address is detected, PI6C184 generates an acknowledge by pulling SDATA line LOW during ninth clock pulse, then accepts the following data bytes until another start or stop condition is detected.

Following acknowledgement of the address byte (D2), two more bytes must be sent:

1. "Command Code" byte, and

2. "Byte Count" byte.

Although the data bits on these two bytes are "don't care," they must be sent and acknowledged.

**Byte1: SDRAM Active/Inactive Register (1 = enable, 0 = disable)**

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | | NC (Initialize to 0) |
| Bit 6 | | NC (Initialize to 0) |
| Bit 5 | | NC (Initialize to 0) |
| Bit 4 | | NC (Initialize to 0) |
| Bit 3 | | NC (Initialize to 0) |
| Bit 2 | 12 | SDRAM12 (Active/Inactive) |
| Bit 1 | 27 | SDRAM11(Active/Inactive) |
| Bit 0 | 26 | SDRAM10 (Active/Inactive) |

**Byte2: Optional Register for Possible Future Requirements (1 = enable, 0 = disable)**

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | 23 | SDRAM9 (Active/Inactive) |
| Bit 6 | 22 | SDRAM8 (Active/Inactive) |
| Bit 5 | - | (Reserved) |
| Bit 4 | - | (Reserved) |
| Bit 3 | - | (Reserved) |
| Bit 2 | - | (Reserved) |
| Bit 1 | - | (Reserved) |
| Bit 0 | - | (Reserved) |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Ambient Temperature with Power Applied ..... –0°C to +70°C
3.3V Supply Voltage to Ground Potential ..... –0.5V to +4.6V
DC Input Voltage ..... –0.5V to +4.6V

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Supply Current ($V_{DD}$=+3.465V, $C_{LOAD}$=Max.)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply Current | BUF_IN = 0 MHz | | | 3 | mA |
| $I_{DD}$ | Supply Current | BUF_IN = 66.66 MHz | | | 230 | |
| $I_{DD}$ | Supply Current | BUF_IN = 100.0 MHz | | | 360 | |

## DC Operating Specifications ($V_{DD}$ = +3.3V ±5%, $T_A$ = 0°C - 70°C)

| Symbol | Parameter | Test Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| Input Voltage | | | | | |
| $V_{IH}$ | Input high voltage | $V_{DD}$ | 2.0 | $V_{DD}$ +0.3 | V |
| $V_{IL}$ | Input low voltage | | $V_{SS}$ –0.3 | 0.8 | |
| $I_{IL}$ | Input leakage current | 0 < $V_{IN}$ < $V_{DD}$ | –5 | +5 | mA |
| $V_{DD}$[0-9] = 3.3V ±5% | | | | | |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = -1mA | 2.4 | | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 1mA | | 0.4 | |
| $C_{OUT}$ | Output pin capacitance | | | 6 | pF |
| $C_{IN}$ | Input pin capacitance | | | 5 | |
| $L_{PIN}$ | Pin Inductance | | | 7 | nH |
| $T_A$ | Ambient Temperature | No Airflow | 0 | 70 | °C |

## SDRAM Clock Buffer Operating Specification

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{OHMIN}$ | Pull-up current | $V_{OUT}$ = 2.0V | –54 | | | mA |
| $I_{OHMAX}$ | Pull-up current | $V_{OUT}$ = 3.135V | | | –46 | |
| $I_{OLMIN}$ | Pull-down current | $V_{OUT}$ = 1.0V | 54 | | | |
| $I_{OLMAX}$ | Pull-down current | $V_{OUT}$ = 0.4V | | | 53 | |
| $t_{RH}$SDRAM | Output rise edge rate SDRAM only | 3.3V ±5% @ 04V-2.4V | 1.5 | | 4 | V/ns |
| $t_{TH}$SDRAM | Output fall edge rate SDRAM only | 3.3V ±5% @ 2.4V-0.4V | 1.5 | | 4 | |

## AC Timing

| Symbol | Parameter | 66 MHz | | 100 MHz | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $T_{DSKP}$ | SDRAM CLK period | 15.0 | 15.5 | 10.0 | 10.5 | ns |
| $T_{SDKH}$ | SDRAM CLK high time | 5.6 | | 3.3 | | ns |
| $T_{SDKL}$ | SDRAM CLK low time | 5.3 | | 3.1 | | ns |
| $T_{SDRISE}$ | SDRAM CLK rise time | 1.5 | 4.0 | 1.5 | 4.0 | V/ns |
| $T_{SDFALL}$ | SDRAM CLK fall time | 1.5 | 4.0 | 1.5 | 4.0 | V/ns |
| $t_{PLH}$ | SDRAM Buffer LH prop delay | 1.0 | 5.5 | 1.0 | 5.0 | ns |
| $t_{PHL}$ | SDRAM Buffer HL prop delay | 1.0 | 5.5 | 1.0 | 5.0 | ns |
| DutyCycle | Measured at 1.5V | 45 | 55 | 45 | 55 | % |
| tSDSKW | SDRAM Output to Output Skew | | 250 | | 250 | ps |

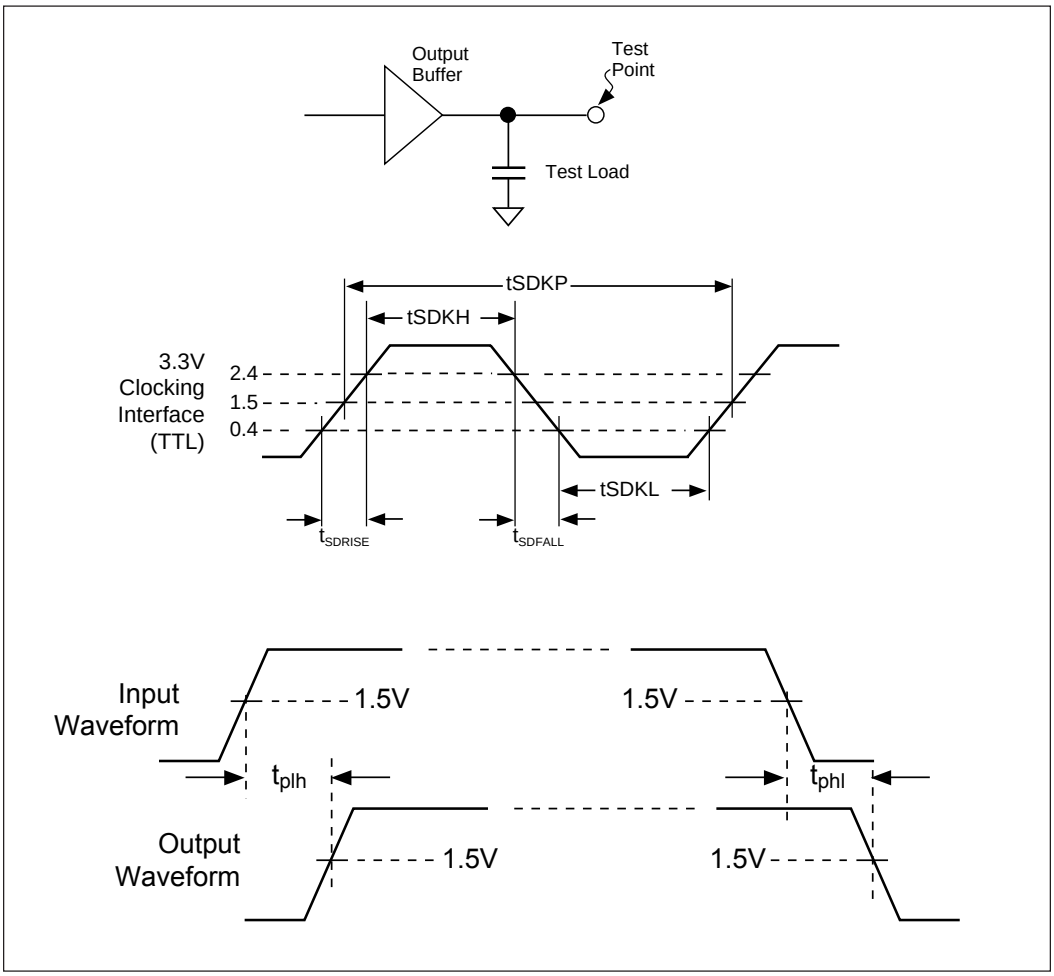



**Figure 1. Clock Waveforms**

## Minimum and Maximum Expected Capacitive Loads

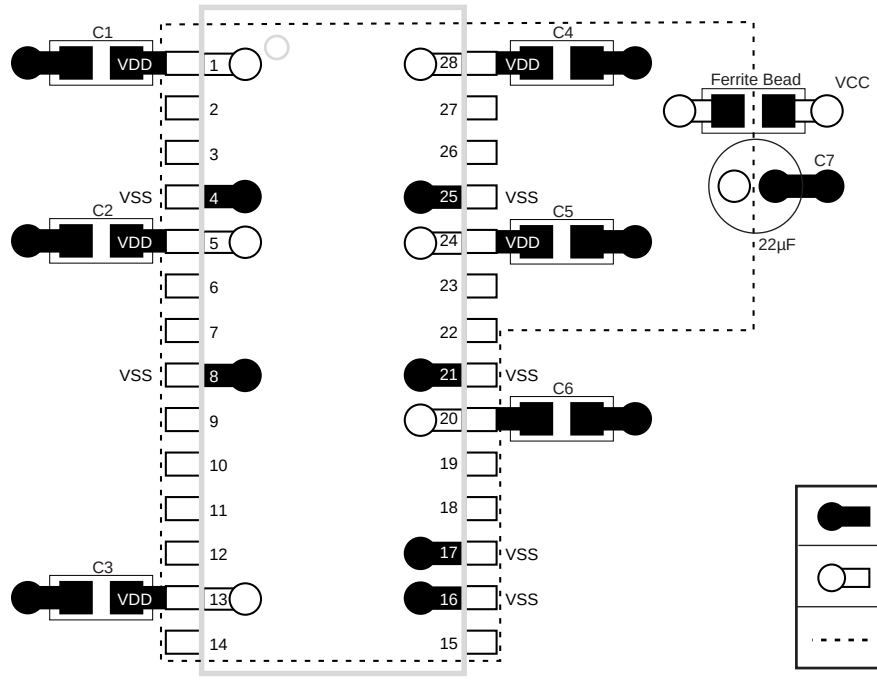
| Clock | Min. Load | Max. Load | Units | Notes |
|---|---|---|---|---|
| SDRAM | 20 | 30 | pF | SDRAM DIMM Specification |

**Notes:**
1. Maximum rise/fall times are guaranteed at maximum specified load.
2. Minimum rise/fall times are guaranteed at minimum specified load.
3. Rise/fall times are specified with pure capacitive load as shown. Testing is done with an additional 500Ω resistor in parallel.

## Design Guidelines to Reduce EMI

1. Place series resistors and CI capacitors as close as possible to the respective clock pins. Typical value for CI is 10pF. Series resistor value can be increased to reduce EMI provided that the rise and fall time are still within the specified values.
2. Minimize the number of "vias" of the clock traces.
3. Route clock traces over a continuous ground plane or over a continuous power plane. Avoid routing clock traces from plane to plane (refer to rule #2).
4. Position clock signals away from signals that go to any cables or any external connectors.

## PCB Layout Suggestion




**Note:**
This is only a suggested layout. There may be alternate solutions depending on actual PCB design and layout.
As a general rule, C1-C7 should be placed as close as possible to their respective $V_{DD}$.

Recommended capacitor values:
C1-C7 ..... 0.1µF, ceramic
C8 ..... 22µF

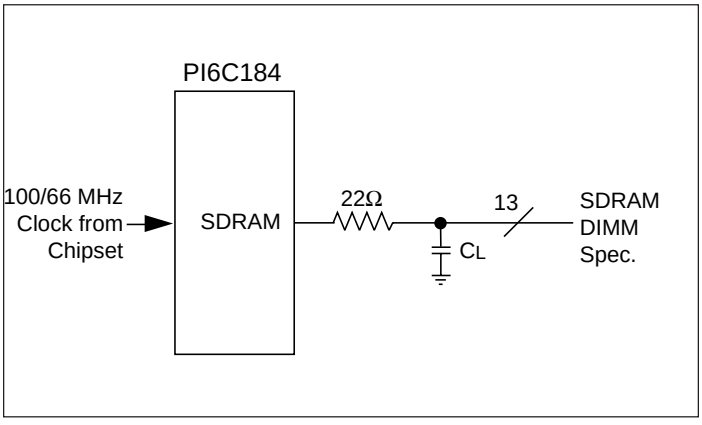
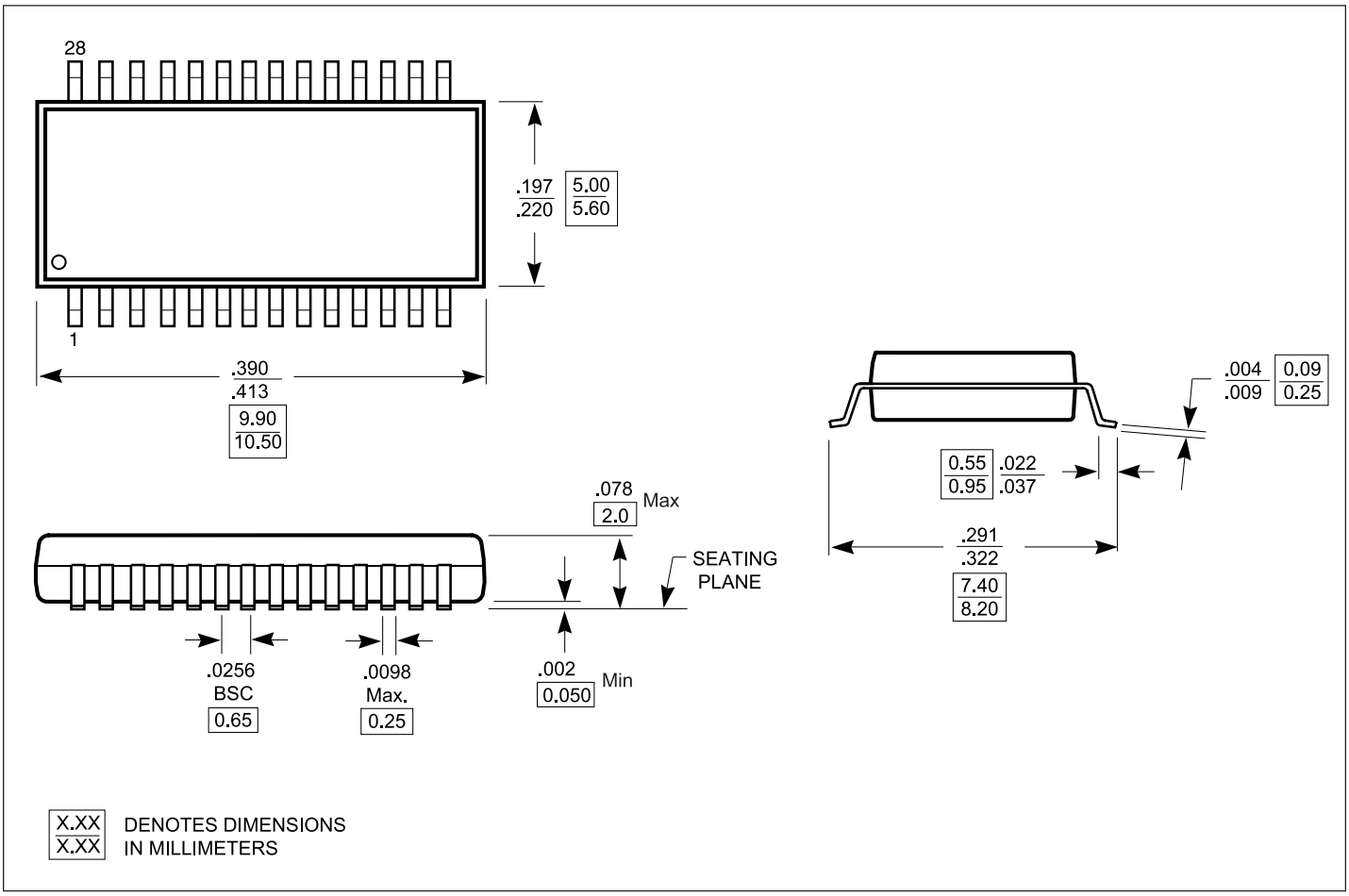



**Figure 2. Design Guidelines**

## Packaging Mechanical: 28-pin SSOP (H)




## Ordering Information

| Ordering Code | Package Code | Package Type |
|---|---|---|
| PI6C184H | H | 28-pin SSOP |
| PI6C184HE | H | Pb-free & Green, 28-pin SSOP |

**Notes:**
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

Стандарт Электрон Связь

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