

74LVC2G74

Single D-type flip-flop with set and reset; positive edge trigger

Rev. 06 — 23 December 2009

Product data sheet

1. General description

The 74LVC2G74 is a single positive-edge triggered D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set (\overline{SD}) and reset (\overline{RD}) inputs, and complementary Q and \overline{Q} outputs.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing damaging backflow current through the device when it is powered down.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable, one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------|-------------------|--------|--|----------|
| | Temperature range | Name | Description | |
| 74LVC2G74DP | -40 °C to +125 °C | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm | SOT505-2 |
| 74LVC2G74DC | -40 °C to +125 °C | VSSOP8 | plastic very thin shrink small outline package; 8 leads; body width 2.3 mm | SOT765-1 |
| 74LVC2G74GT | -40 °C to +125 °C | XSON8 | plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm | SOT833-1 |
| 74LVC2G74GF | -40 °C to +125 °C | XSON8 | extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm | SOT1089 |
| 74LVC2G74GD | -40 °C to +125 °C | XSON8U | plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 × 2 × 0.5 mm | SOT996-2 |
| 74LVC2G74GM | -40 °C to +125 °C | XQFN8U | plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 × 1.6 × 0.5 mm | SOT902-1 |

4. Marking

Table 2. Marking codes

| Type number | Marking code ^[1] |
|-------------|-----------------------------|
| 74LVC2G74DP | V74 |
| 74LVC2G74DC | V74 |
| 74LVC2G74GT | V74 |
| 74LVC2G74GF | Y4 |
| 74LVC2G74GD | V74 |
| 74LVC2G74GM | V74 |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

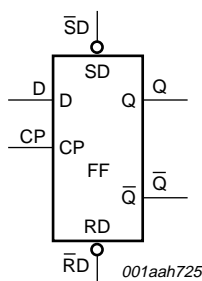


Fig 1. Logic symbol

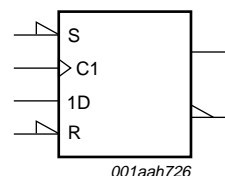


Fig 2. IEC logic symbol

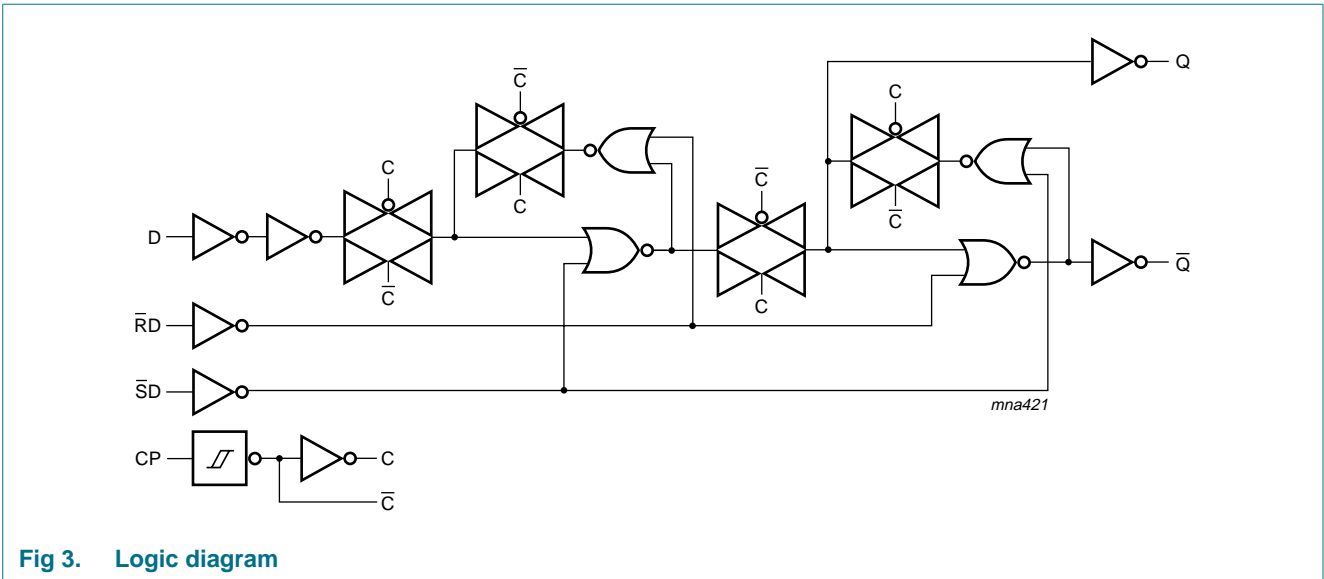


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

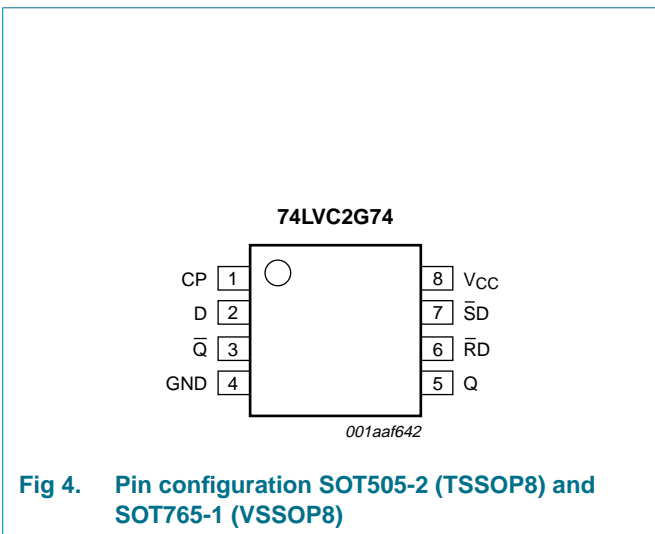


Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

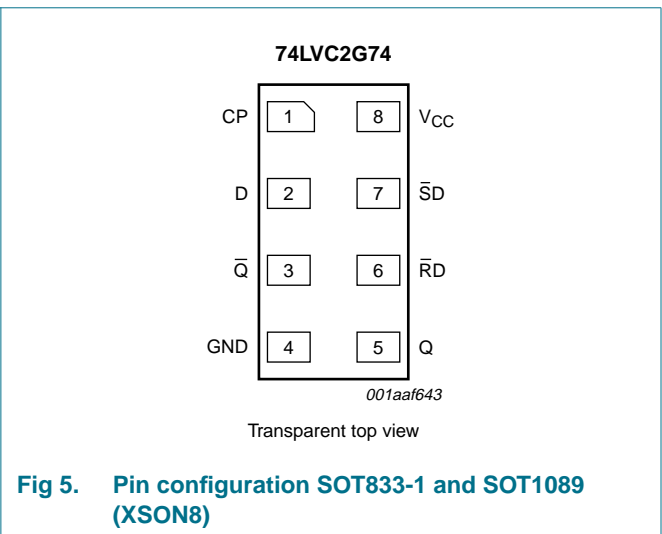
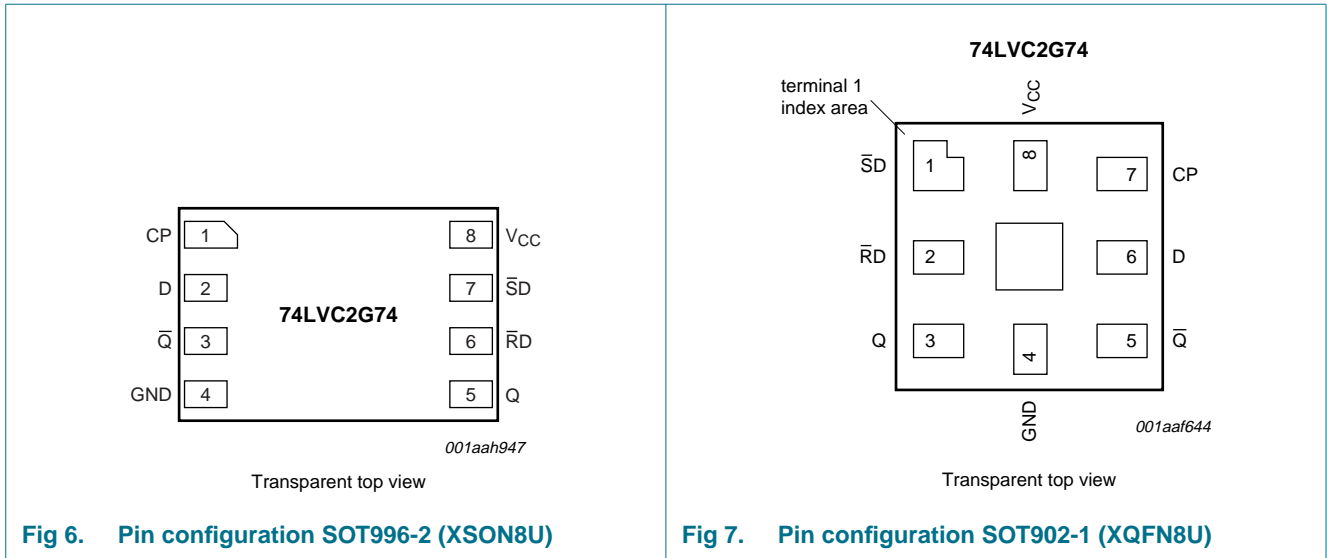


Fig 5. Pin configuration SOT833-1 and SOT1089 (XSON8)



6.2 Pin description

Table 3. Pin description

| Symbol | Pin | | Description |
|-----------------|--|----------|--|
| | SOT505-2, SOT765-1, SOT833-1, SOT996-2 and SOT1089 | SOT902-1 | |
| CP | 1 | 7 | clock input (LOW-to-HIGH, edge-triggered) |
| D | 2 | 6 | data input |
| \bar{Q} | 3 | 5 | complement output |
| GND | 4 | 4 | ground (0 V) |
| Q | 5 | 3 | true output |
| \bar{RD} | 6 | 2 | asynchronous reset-direct input (active LOW) |
| \bar{SD} | 7 | 1 | asynchronous set-direct input (active LOW) |
| V _{CC} | 8 | 8 | supply voltage |

7. Functional description

Table 4. Function table for asynchronous operation^[1]

| Input | | | | Output | |
|------------|------------|----|---|--------|-----------|
| \bar{SD} | \bar{RD} | CP | D | Q | \bar{Q} |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |

[1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care.

Table 5. Function table for synchronous operation^[1]

| Input | | | | Output | |
|-------|----|----|---|------------------|----------------------|
| SD | RD | CP | D | Q _{n+1} | \overline{Q}_{n+1} |
| H | H | ↑ | L | L | H |
| H | H | ↑ | H | H | L |

- [1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|--|-------------|-----------------------|------|
| V _{CC} | supply voltage | | -0.5 | +6.5 | V |
| I _{IK} | input clamping current | V _I < 0 V | -50 | - | mA |
| V _I | input voltage | | [1] -0.5 | +6.5 | V |
| I _{OK} | output clamping current | V _O > V _{CC} or V _O < 0 V | - | ±50 | mA |
| V _O | output voltage | Active mode | [1][2] -0.5 | V _{CC} + 0.5 | V |
| | | Power-down mode | [1][2] -0.5 | +6.5 | V |
| I _O | output current | V _O = 0 V to V _{CC} | - | ±50 | mA |
| I _{CC} | supply current | | - | 100 | mA |
| I _{GND} | ground current | | -100 | - | mA |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +125 °C | [3] - | 300 | mW |
| T _{stg} | storage temperature | | -65 | +150 | °C |

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.
- [3] For TSSOP8 packages: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
For XSON8, XSON8U and XQFN8U packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 7. Operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------------------|--|------|-----------------|------|
| V _{CC} | supply voltage | | 1.65 | 5.5 | V |
| V _I | input voltage | | 0 | 5.5 | V |
| V _O | output voltage | Active mode | 0 | V _{CC} | V |
| | | Power-down mode; V _{CC} = 0 V | 0 | 5.5 | V |
| T _{amb} | ambient temperature | | -40 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 1.65 V to 2.7 V | - | 20 | ns/V |
| | | V _{CC} = 2.7 V to 5.5 V | - | 10 | ns/V |

10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|---|---------------------------|--|------------------------|--------------------|------------------------|------|
| T_{amb} = -40 °C to +85 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | - | - | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | V |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.65 V to 1.95 V | - | - | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | V |
| | | V _{CC} = 4.5 V to 5.5 V | - | - | 0.3 × V _{CC} | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -100 μA; V _{CC} = 1.65 V to 5.5 V | V _{CC} - 0.1 | - | - | V |
| | | I _O = -4 mA; V _{CC} = 1.65 V | 1.2 | 1.54 | - | V |
| | | I _O = -8 mA; V _{CC} = 2.3 V | 1.9 | 2.15 | - | V |
| | | I _O = -12 mA; V _{CC} = 2.7 V | 2.2 | 2.50 | - | V |
| | | I _O = -24 mA; V _{CC} = 3.0 V | 2.3 | 2.62 | - | V |
| | | I _O = -32 mA; V _{CC} = 4.5 V | 3.8 | 4.11 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V | - | - | 0.10 | V |
| | | I _O = 4 mA; V _{CC} = 1.65 V | - | 0.07 | 0.45 | V |
| | | I _O = 8 mA; V _{CC} = 2.3 V | - | 0.12 | 0.30 | V |
| | | I _O = 12 mA; V _{CC} = 2.7 V | - | 0.17 | 0.40 | V |
| | | I _O = 24 mA; V _{CC} = 3.0 V | - | 0.33 | 0.55 | V |
| | | I _O = 32 mA; V _{CC} = 4.5 V | - | 0.39 | 0.55 | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | ±0.1 | ±5 | μA |
| I _{OFF} | power-off leakage current | V _I or V _O = 5.5 V; V _{CC} = 0 V | - | ±0.1 | ±10 | μA |
| I _{CC} | supply current | V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A | - | 0.1 | 10 | μA |
| ΔI _{CC} | additional supply current | per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V | - | 5 | 500 | μA |
| C _I | input capacitance | | - | 4.0 | - | pF |

Table 8. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--|---------------------------|--|------------------------|--------------------|------------------------|------|
| T_{amb} = -40 °C to +125 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | - | - | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | V |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.65 V to 1.95 V | - | - | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | V |
| | | V _{CC} = 4.5 V to 5.5 V | - | - | 0.3 × V _{CC} | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -100 μA; V _{CC} = 1.65 V to 5.5 V | V _{CC} - 0.1 | - | - | V |
| | | I _O = -4 mA; V _{CC} = 1.65 V | 0.95 | - | - | V |
| | | I _O = -8 mA; V _{CC} = 2.3 V | 1.7 | - | - | V |
| | | I _O = -12 mA; V _{CC} = 2.7 V | 1.9 | - | - | V |
| | | I _O = -24 mA; V _{CC} = 3.0 V | 2.0 | - | - | V |
| | | I _O = -32 mA; V _{CC} = 4.5 V | 3.4 | - | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V | - | - | 0.10 | V |
| | | I _O = 4 mA; V _{CC} = 1.65 V | - | - | 0.70 | V |
| | | I _O = 8 mA; V _{CC} = 2.3 V | - | - | 0.45 | V |
| | | I _O = 12 mA; V _{CC} = 2.7 V | - | - | 0.60 | V |
| | | I _O = 24 mA; V _{CC} = 3.0 V | - | - | 0.80 | V |
| | | I _O = 32 mA; V _{CC} = 4.5 V | - | - | 0.80 | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | ±20 | μA |
| I _{OFF} | power-off leakage current | V _I or V _O = 5.5 V; V _{CC} = 0 V | - | - | ±20 | μA |
| I _{CC} | supply current | V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A | - | - | 40 | μA |
| ΔI _{CC} | additional supply current | per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V | - | - | 5000 | μA |

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 10](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|----------------------------------|-------------------|--|------------------|--------------------|------|-------------------|------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| t _{pd} | propagation delay | CP to Q, \bar{Q} ; see Figure 8 ^[2] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.5 | 6.0 | 13.4 | 1.5 | 13.4 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 3.5 | 7.1 | 1.0 | 7.1 | ns |
| | | V _{CC} = 2.7 V | 1.0 | 3.5 | 7.1 | 1.0 | 7.1 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 3.5 | 5.9 | 1.0 | 5.9 | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 1.0 | 2.5 | 4.1 | 1.0 | 4.1 | ns |
| | | $\bar{S}D$ to Q, \bar{Q} ; see Figure 9 ^[2] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.5 | 6.0 | 12.9 | 1.5 | 12.9 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 3.5 | 7.0 | 1.0 | 7.0 | ns |
| | | V _{CC} = 2.7 V | 1.0 | 3.5 | 7.0 | 1.0 | 7.0 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 3.0 | 5.9 | 1.0 | 5.9 | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 1.0 | 2.5 | 4.1 | 1.0 | 4.1 | ns |
| | | $\bar{R}D$ to Q, \bar{Q} ; see Figure 9 ^[2] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.5 | 5.0 | 12.9 | 1.5 | 12.9 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 3.5 | 7.0 | 1.0 | 7.0 | ns |
| V _{CC} = 2.7 V | 1.0 | 3.5 | 7.0 | 1.0 | 7.0 | ns | | |
| V _{CC} = 3.0 V to 3.6 V | 1.0 | 3.0 | 5.9 | 1.0 | 5.9 | ns | | |
| V _{CC} = 4.5 V to 5.5 V | 1.0 | 2.5 | 4.1 | 1.0 | 4.1 | ns | | |
| t _w | pulse width | CP HIGH or LOW; see Figure 8 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 6.2 | - | - | 6.2 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 2.7 | - | - | 2.7 | - | ns |
| | | V _{CC} = 2.7 V | 2.7 | - | - | 2.7 | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 2.7 | 1.3 | - | 2.7 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | ns |
| | | $\bar{S}D$ and $\bar{R}D$ LOW; see Figure 9 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 6.2 | - | - | 6.2 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 2.7 | - | - | 2.7 | - | ns |
| | | V _{CC} = 2.7 V | 2.7 | - | - | 2.7 | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 2.7 | 1.6 | - | 2.7 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | ns |

Table 9. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 10](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|--|------------------|--------------------|-----|-------------------|-----|------|
| | | | Min | Typ ^[1] | Max | Min | Max | |
| t _{rec} | recovery time | SD or \overline{RD} ; see Figure 9 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.9 | - | - | 1.9 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.4 | - | - | 1.4 | - | ns |
| | | V _{CC} = 2.7 V | 1.3 | - | - | 1.3 | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | +1.2 | -3.0 | - | +1.2 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 1.0 | - | - | 1.0 | - | ns |
| t _{su} | set-up time | D to CP; see Figure 8 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 2.9 | - | - | 2.9 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | ns |
| | | V _{CC} = 2.7 V | 1.7 | - | - | 1.7 | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.3 | 0.5 | - | 1.3 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 1.1 | - | - | 1.1 | - | ns |
| t _h | hold time | D to CP; see Figure 8 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.5 | - | - | 1.5 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | - | - | 1.0 | - | ns |
| | | V _{CC} = 2.7 V | 1.0 | - | - | 1.0 | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 0.6 | - | 1.0 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 1.0 | - | - | 1.0 | - | ns |
| f _{max} | maximum frequency | CP; see Figure 8 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 80 | - | - | 80 | - | MHz |
| | | V _{CC} = 2.3 V to 2.7 V | 175 | - | - | 175 | - | MHz |
| | | V _{CC} = 2.7 V | 175 | - | - | 175 | - | MHz |
| | | V _{CC} = 3.0 V to 3.6 V | 175 | 280 | - | 175 | - | MHz |
| | | V _{CC} = 4.5 V to 5.5 V | 200 | - | - | 200 | - | MHz |
| C _{PD} | power dissipation capacitance | V _I = GND to V _{CC} ; V _{CC} = 3.3 V | ^[3] | - | 15 | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

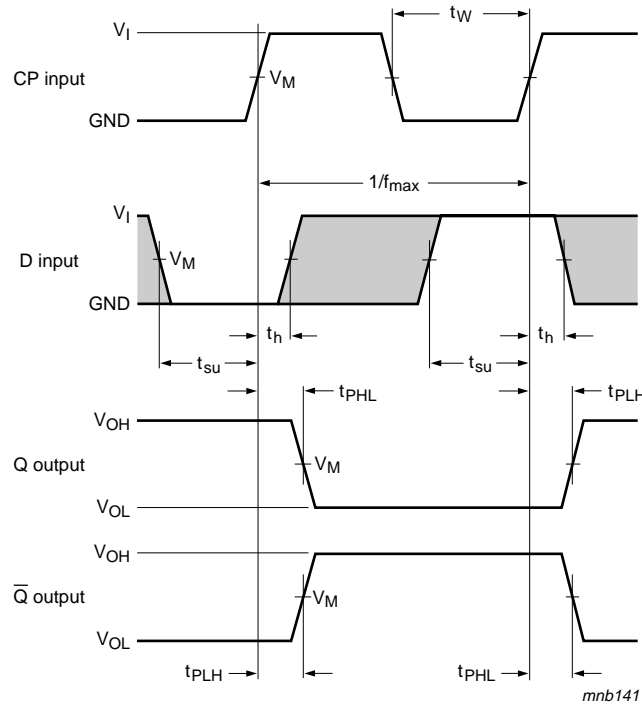
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

∑(C_L × V_{CC}² × f_o) = sum of outputs.

12. Waveforms



Measurement points are given in [Table 10](#).

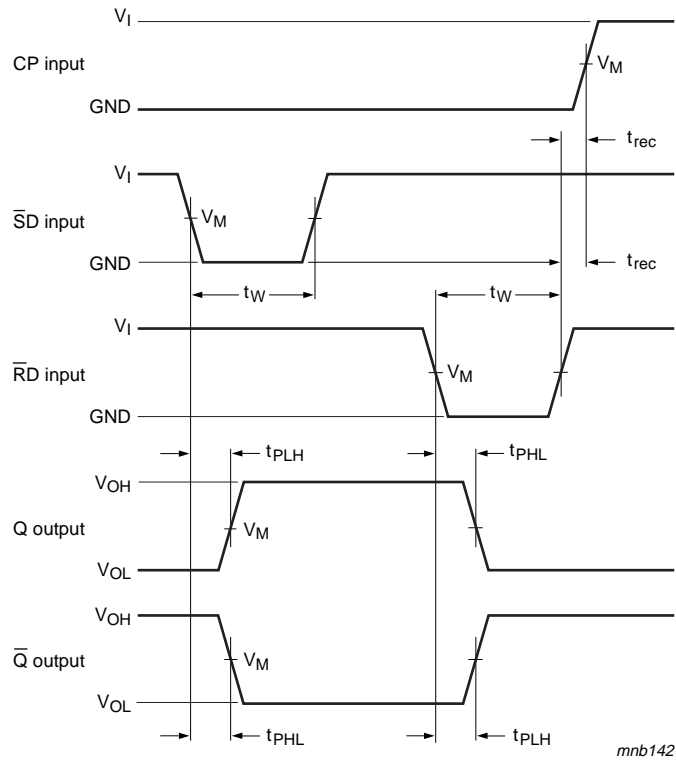
The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. The clock input (CP) to output (Q, Q̄) propagation delays, the clock pulse width, the D to CP set-up, the CP to D hold times and the CP maximum frequency

Table 10. Measurement points

| Supply voltage | Input | Output |
|------------------|---------------------|---------------------|
| V_{CC} | V_M | V_M |
| 1.65 V to 1.95 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 2.3 V to 2.7 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 2.7 V | 1.5 V | 1.5 V |
| 3.0 V to 3.6 V | 1.5 V | 1.5 V |
| 4.5 V to 5.5 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |

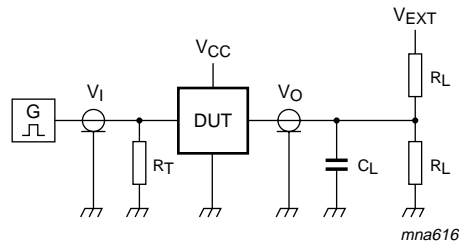


mnb142

Measurement points are given in [Table 10](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. The set (\overline{SD}) and reset (\overline{RD}) input to output (Q , \overline{Q}) propagation delays, the set and reset pulse widths and the \overline{RD} to CP recovery time



Test data is given in [Table 11](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 10. Test circuit for measuring switching times

Table 11. Test data

| Supply voltage | Input | | Load | | V_{EXT} | | |
|------------------|----------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| V_{CC} | V_I | t_r, t_f | C_L | R_L | t_{PLH}, t_{PHL} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 1.65 V to 1.95 V | V_{CC} | ≤ 2.0 ns | 30 pF | 1 k Ω | open | GND | $2V_{CC}$ |
| 2.3 V to 2.7 V | V_{CC} | ≤ 2.0 ns | 30 pF | 500 Ω | open | GND | $2V_{CC}$ |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | 6 V |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | 6 V |
| 4.5 V to 5.5 V | V_{CC} | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | $2V_{CC}$ |

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

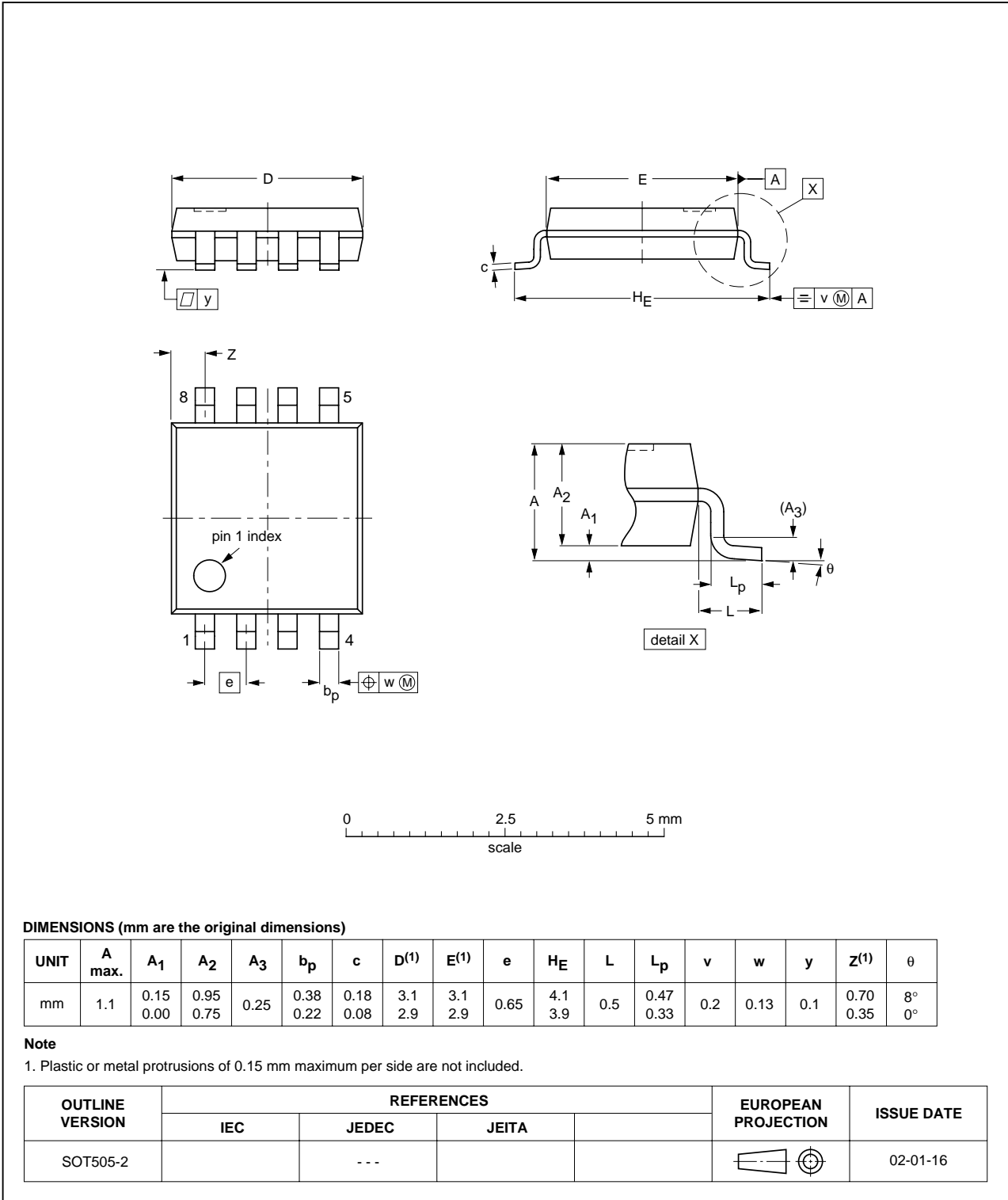


Fig 11. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

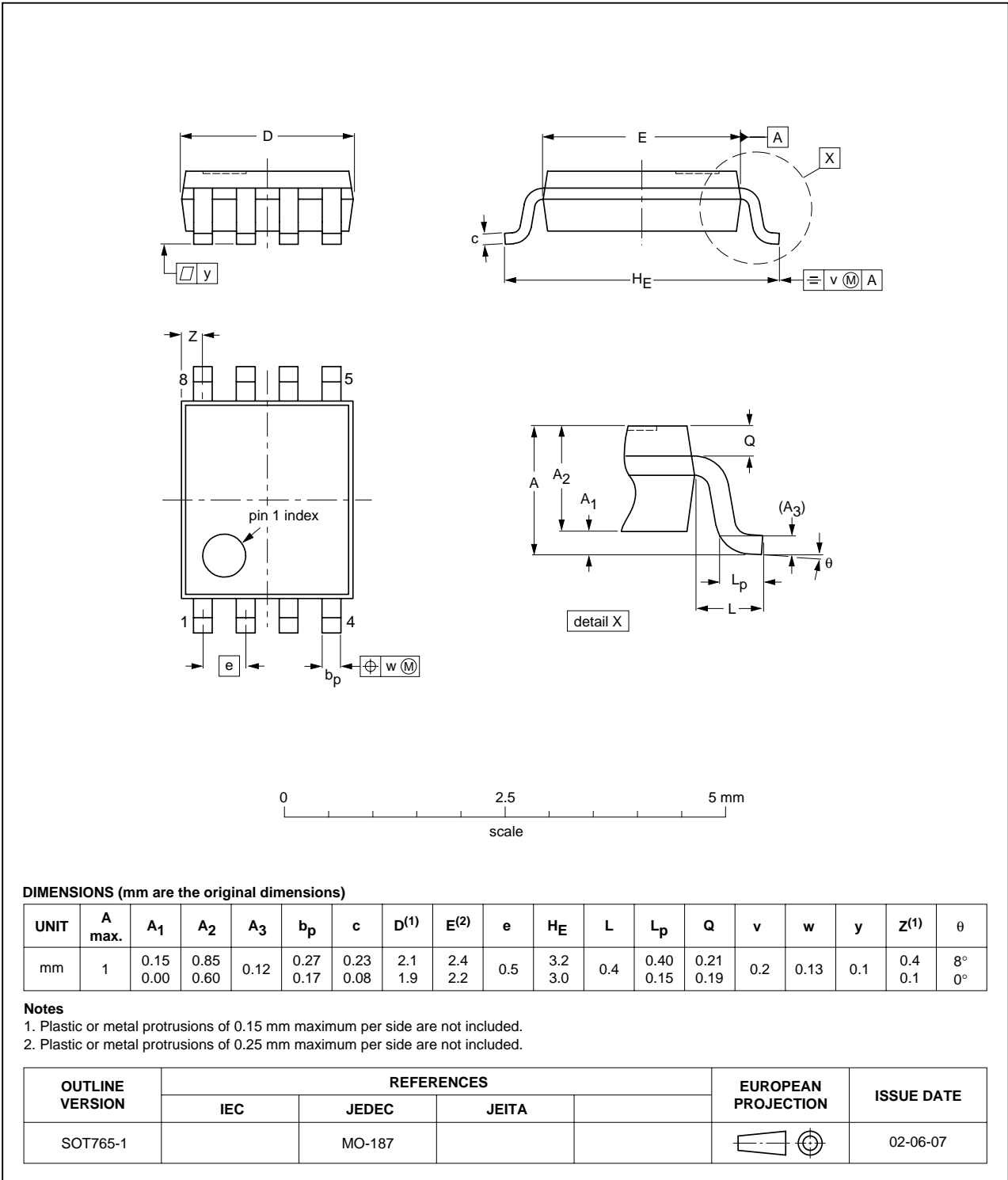


Fig 12. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

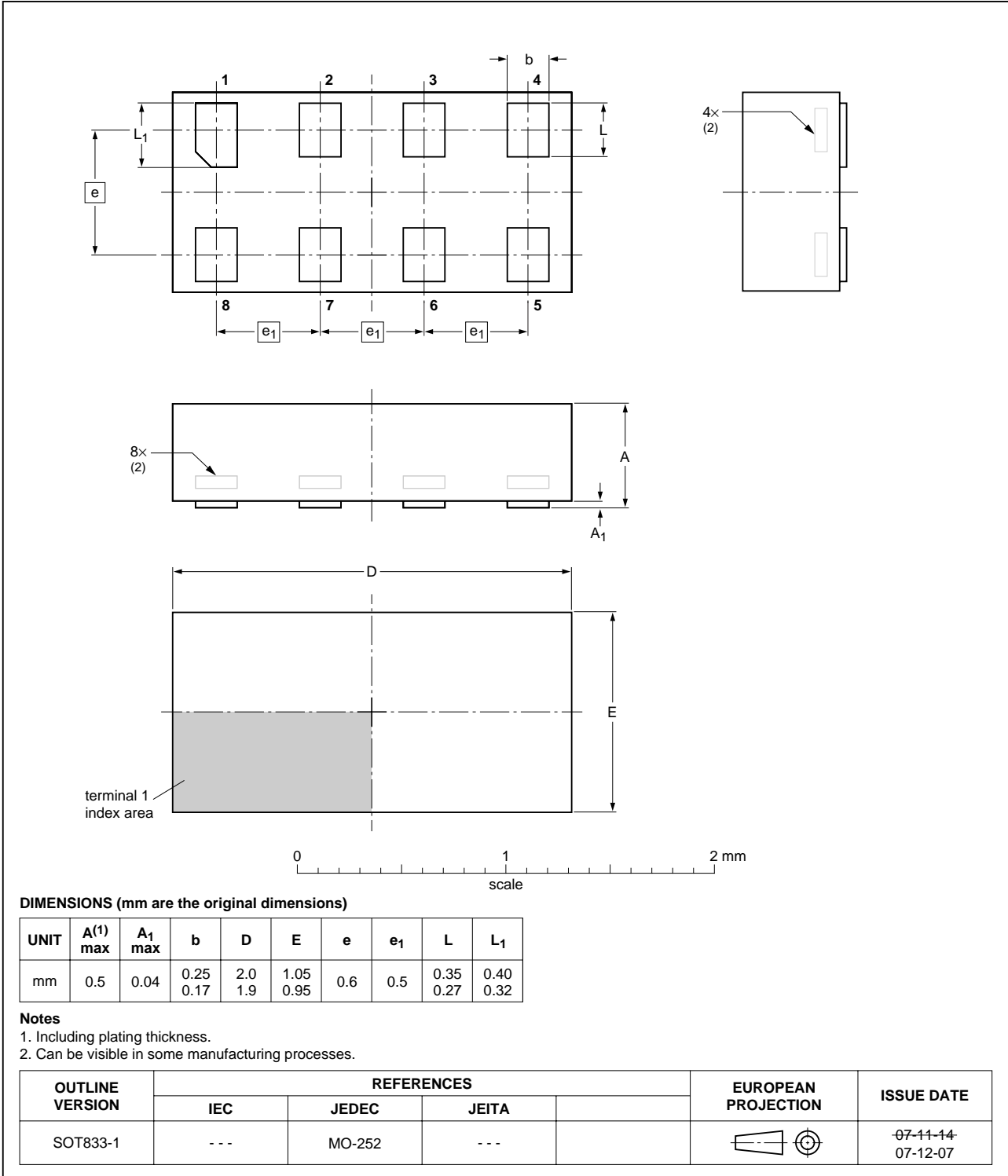


Fig 13. Package outline SOT833-1 (XSON8)

**XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1 x 0.5 mm**

SOT1089

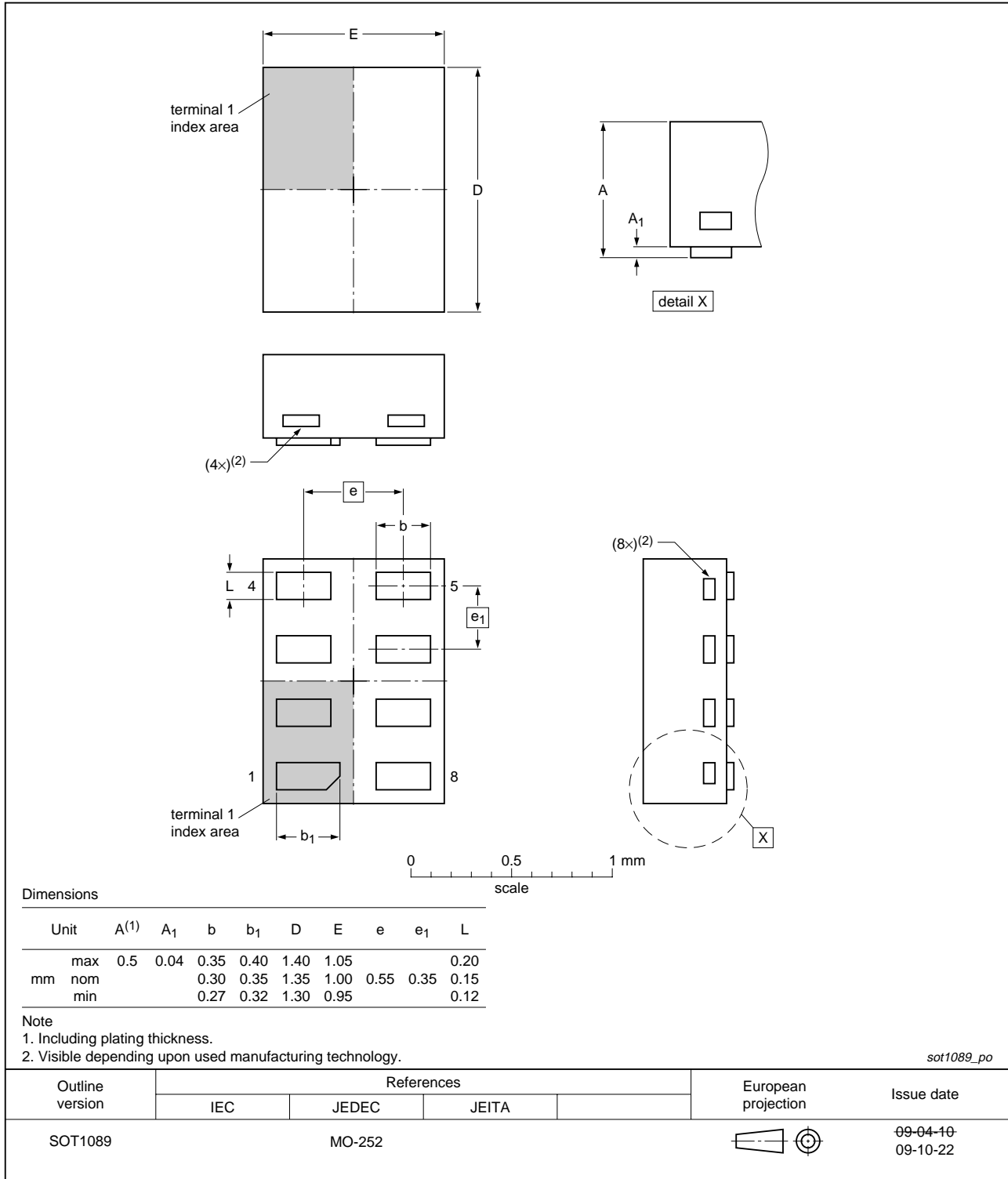


Fig 14. Package outline SOT1089 (XSON8)

XSON8U: plastic extremely thin small outline package; no leads;
8 terminals; UTLP based; body 3 x 2 x 0.5 mm

SOT996-2

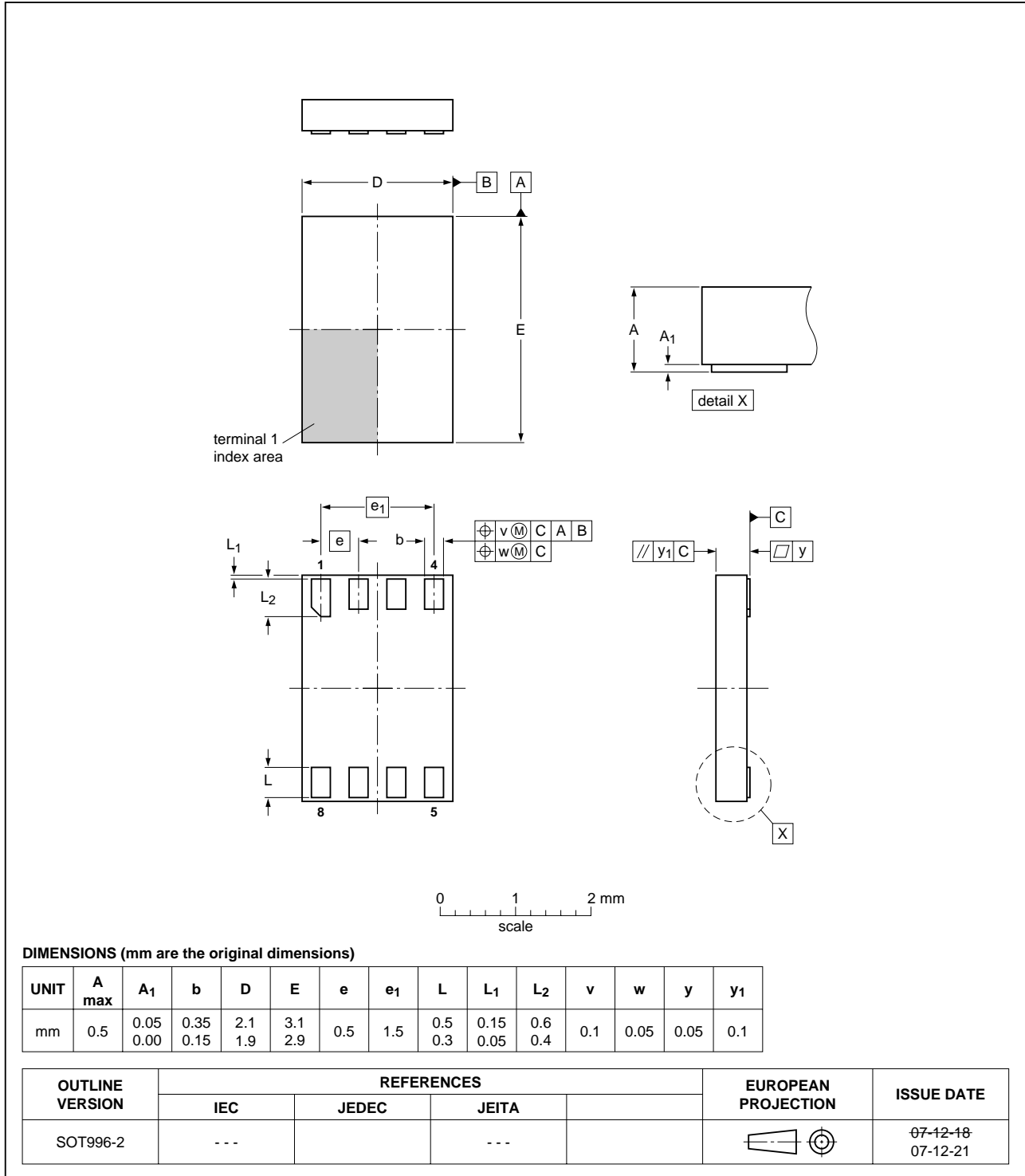


Fig 15. Package outline SOT996-2 (XSON8U)

XQFN8U: plastic extremely thin quad flat package; no leads;
8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm

SOT902-1

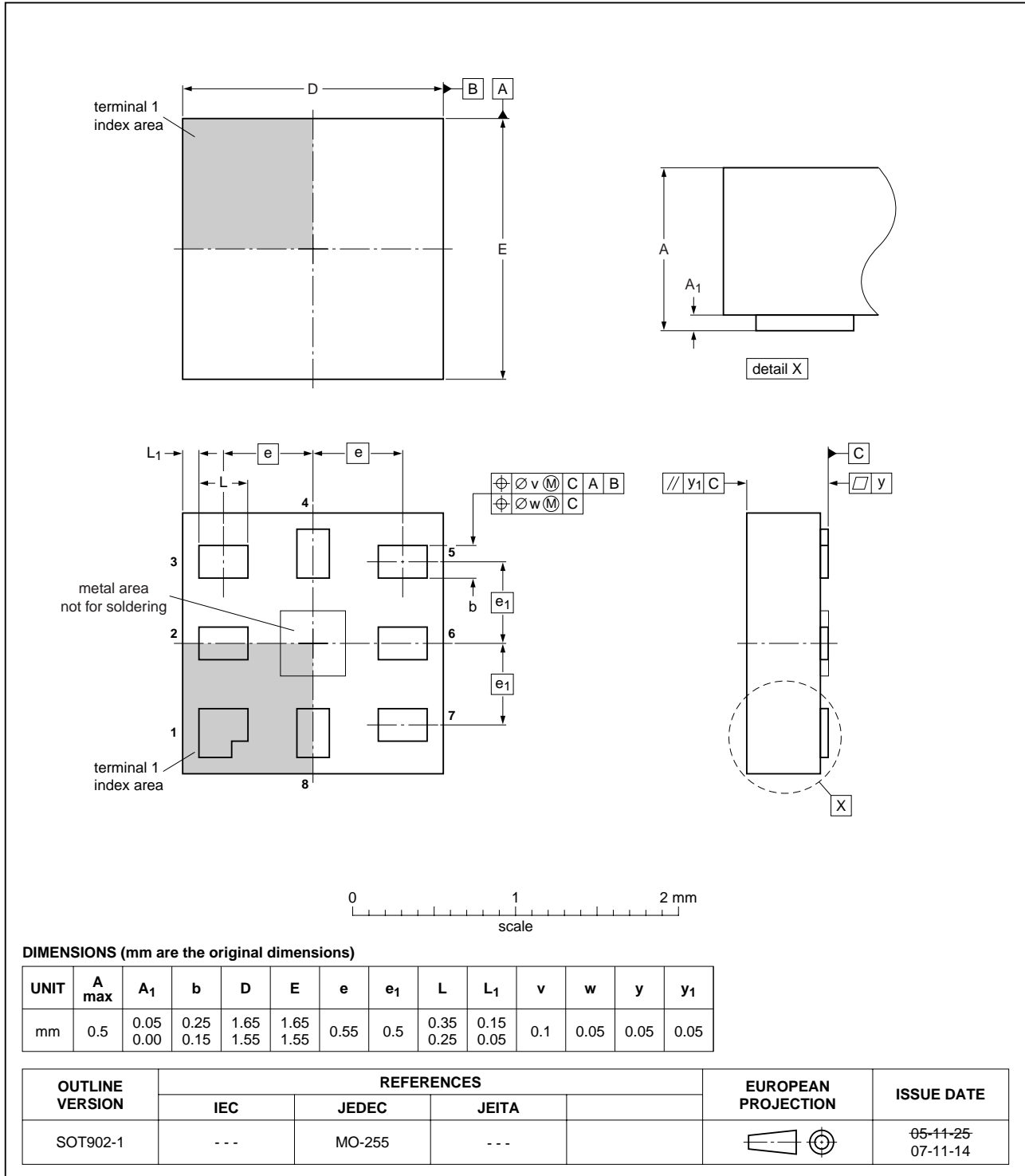


Fig 16. Package outline SOT902-1 (XQFN8U)

14. Abbreviations

Table 12. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| HBM | Human Body Model |
| ESD | ElectroStatic Discharge |
| MM | Machine Model |
| DUT | Device Under Test |

15. Revision history

Table 13. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|--------------------|---------------|-------------|
| 74LVC2G74_6 | 20091223 | Product data sheet | - | 74LVC2G74_5 |
| Modifications: | <ul style="list-style-type: none"> Added type number 74LVC2G74GF (XSON8 package) | | | |
| 74LVC2G74_5 | 20080630 | Product data sheet | - | 74LVC2G74_4 |
| 74LVC2G74_4 | 20080207 | Product data sheet | - | 74LVC2G74_3 |
| 74LVC2G74_3 | 20070809 | Product data sheet | - | 74LVC2G74_2 |
| 74LVC2G74_2 | 20061214 | Product data sheet | - | 74LVC2G74_1 |
| 74LVC2G74_1 | 20051103 | Product data sheet | - | - |

16. Legal information

16.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

16.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1 **General description** 1

2 **Features** 1

3 **Ordering information** 2

4 **Marking** 2

5 **Functional diagram** 2

6 **Pinning information** 3

6.1 Pinning 3

6.2 Pin description 4

7 **Functional description** 4

8 **Limiting values** 5

9 **Recommended operating conditions** 5

10 **Static characteristics** 6

11 **Dynamic characteristics** 8

12 **Waveforms** 10

13 **Package outline** 13

14 **Abbreviations** 19

15 **Revision history** 19

16 **Legal information** 20

16.1 Data sheet status 20

16.2 Definitions 20

16.3 Disclaimers 20

16.4 Trademarks 20

17 **Contact information** 20

18 **Contents** 21

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.





Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331