6 GHz Fractional-N Frequency Synthesizer

ADF4156

FEATURES

- RF bandwidth to 6 GHz
- 2.7 V to 3.3 V power supply
- Separate V_P allows extended tuning voltage
- Programmable fractional modulus
- Programmable charge pump currents
- 3-wire serial interface
- Digital lock detect
- Power-down mode
- Pin compatible with ADF4110/ADF4111/ADF4112/ADF4113/ADF4106/ ADF4153 and ADF4154 frequency synthesizers
- Programmable RF output phase
- Loop filter design possible with ADISimPLL
- Cycle slip reduction for faster lock times

APPLICATIONS

- CATV equipment
- Base stations for mobile radio (WiMAX, GSM, PCS, DCS, SuperCell 3G, CDMA, WCDMA)
- Wireless handsets (GSM, PCS, DCS, CDMA, WCDMA)
- Wireless LANs, PMR
- Communications test equipment

GENERAL DESCRIPTION

The ADF4156 is a 6 GHz fractional-N frequency synthesizer that implements local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, and a programmable reference divider. There is a sigma-delta (Σ-Δ) based fractional interpolator to allow programmable fractional-N division. The INT, FRAC, and MOD registers define an overall N divider ($N = (INT + (FRAC/MOD))$). The RF output phase is programmable for applications that require a particular phase relationship between the output and the reference. The ADF4156 also features cycle slip reduction circuitry leading to faster lock times without the need for modifications to the loop filter.

Control of all on-chip registers is via a simple 3-wire interface. The device operates with a power supply ranging from 2.7 V to 3.3 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

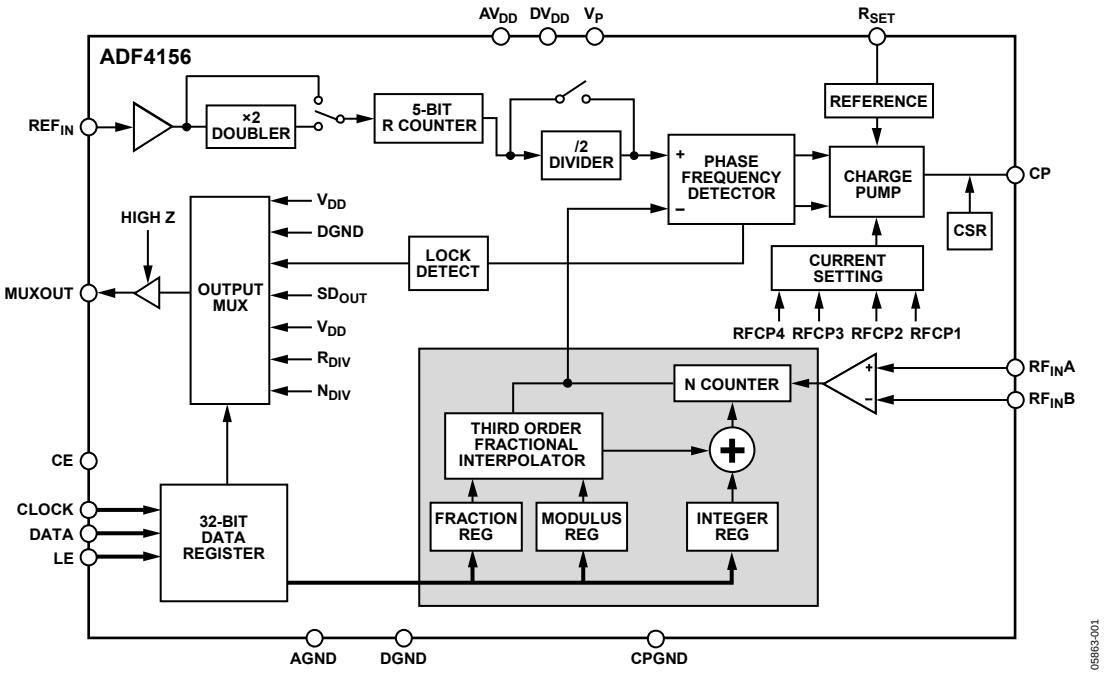

Figure 1.

Rev. 0

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REVISION HISTORY

5/06—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = 2.7 V to 3.3 V, V_P = AV_{DD} to 5.5 V, AGND = DGND = 0 V, T_A = T_{MIN} to T_{MAX}, dBm referred to 50 Ω, unless otherwise noted.

Table 1.

Parameter	B Version	Unit	Test Conditions/Comments[1]
RF CHARACTERISTICS			
RF Input Frequency (RF_{IN})	0.5/6.0	GHz min/max	−10 dBm min to 0 dBm max; for lower frequencies, ensure slew rate (SR) > 400 V/µs
REFERENCE CHARACTERISTICS			
REF_{IN} Input Frequency	10/250	MHz min/max	For f < 10 MHz, use a dc-coupled CMOS-compatible square wave, slew rate > 25 V/µs
REF_{IN} Input Sensitivity	0.4/AV_{DD}	V p-p min/max	Biased at AV_{DD}/2[2]
REF_{IN} Input Capacitance	10	pF max	
REF_{IN} Input Current	±100	µA max	
PHASE DETECTOR			
Phase Detector Frequency[3]	32	MHz max	
CHARGE PUMP			
I_{CP} Sink/Source			Programmable
High Value	5	mA typ	With R_{SET} = 5.1 kΩ
Low Value	312.5	µA typ	
Absolute Accuracy	2.5	% typ	With R_{SET} = 5.1 kΩ
R_{SET} Range	2.7/10	kΩ min/max	
I_{CP} Three-State Leakage Current	1	nA typ	Sink and source current
Matching	2	% typ	0.5 V < V_{CP} < V_P − 0.5
I_{CP} vs. V_{CP}	2	% typ	0.5 V < V_{CP} < V_P − 0.5
I_{CP} vs. Temperature	2	% typ	V_{CP} = V_P/2
LOGIC INPUTS			
V_{INH}, Input High Voltage	1.4	V min	
V_{INL}, Input Low Voltage	0.6	V max	
I_{INH}/I_{INL}, Input Current	±1	µA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	1.4	V min	Open-drain output chosen; 1 kΩ pull-up to 1.8 V
V_{OH}, Output High Voltage	V_{DD} − 0.4	V min	CMOS output chosen
I_{OH}	100	µA max	
V_{OL}, Output Low Voltage	0.4	V max	I_{OL} = 500 µA
POWER SUPPLIES			
AV_{DD}	2.7/3.3	V min/V max	
DV_{DD}	AV_{DD}		
V_P	AV_{DD}/5.5	V min/V max	
I_{DD}	32	mA max	26 mA typical
NOISE CHARACTERISTICS			
Normalized Phase Noise Floor[4]	−211	dBc/Hz typ	
Phase Noise Performance[5]			@ VCO output
5800 MHz Output[6]	−89	dBc/Hz typ	@ 5 kHz offset, 25 MHz PFD frequency

[1] Operating temperature for B version: −40°C to +85°C.
[2] AC coupling ensures AV_{DD}/2 bias.
[3] Guaranteed by design. Sample tested to ensure compliance.
[4] This figure can be used to calculate phase noise for any application. Use the formula −213 + 10log(f_{PFD}) + 20logN to calculate in-band phase noise performance as seen at the VCO output. The value given is the lowest noise mode.
[5] The phase noise is measured with the EVAL-ADF4156EB1 evaluation board and the Agilent E5500 phase noise system.
[6] f_{REFIN} = 100 MHz; f_{PFD} = 25 MHz; offset frequency = 5 kHz; RF_{OUT} = 5800 MHz; N = 232; loop B/W = 20 kHz, I_{CP} = 313 µA; lowest noise mode.

TIMING SPECIFICATIONS

AV_{DD} = DV_{DD} = 2.7 V to 3.3 V, V_P = AV_{DD} to 5.5 V, AGND = DGND = 0 V, T_A = T_{MIN} to T_{MAX}, dBm referred to 50 Ω, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLOCK setup time
t_3	10	ns min	DATA to CLOCK hold time
t_4	25	ns min	CLOCK high duration
t_5	25	ns min	CLOCK low duration
t_6	10	ns min	CLOCK to LE setup time
t_7	20	ns min	LE pulse width

Timing Diagram

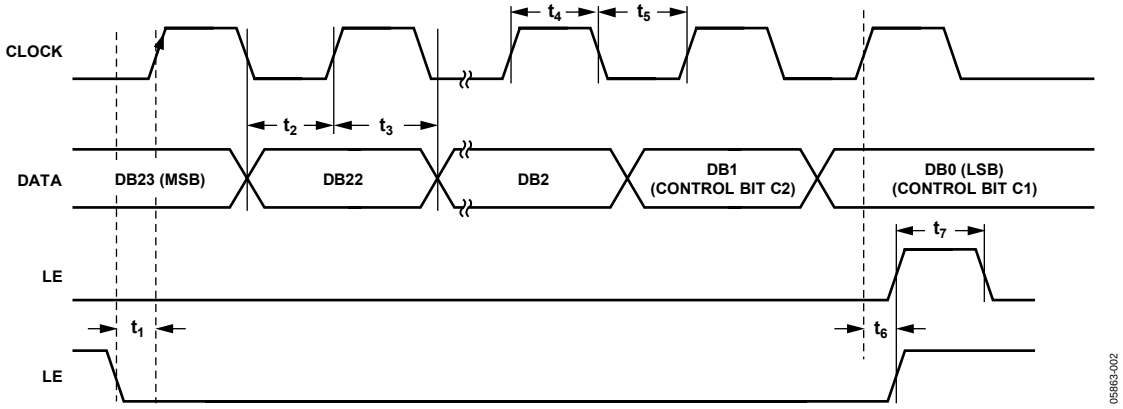


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, GND = AGND = DGND = 0 V, V_{DD} = AV_{DD} = DV_{DD}, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +4 V
V_{DD} to V_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +5.8 V
V_P to V_{DD}	−0.3 V to +5.8 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
REF_{IN}, RF_{IN} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Maximum Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

THERMAL IMPEDANCE

Table 4. Thermal Impedance

Package Type	θ_{JA}	Unit
TSSOP	112	°C/W
LFCSP_VQ (Paddle Soldered)	30.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

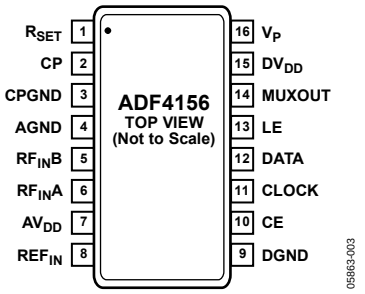


Figure 3. TSSOP Pin Configuration

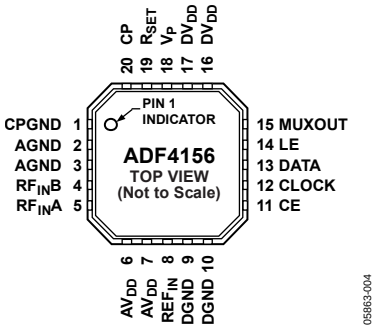


Figure 4. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

TSSOP	LFCSP	Mnemonic	Description
1	19	R_{SET}	Connecting a resistor between this pin and ground sets the maximum charge pump output current. The relationship between I_{CP} and R_{SET} is $$I_{CPmax} = \frac{25.5}{R_{SET}}$$ where: R_{SET} = 5.1 kΩ. $I_{CP\,max}$ = 5 mA.
2	20	CP	Charge Pump Output. When enabled, this provides ±I_{CP} to the external loop filter, which in turn, drives the external VCO.
3	1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
5	4	$RF_{IN}B$	Complementary Input to the RF Prescaler. Decouple this point to the ground plane with a small bypass capacitor, typically 100 pF.
6	5	$RF_{IN}A$	Input to the RF Prescaler. This small-signal input is normally ac-coupled from the VCO.
7	6, 7	AV_{DD}	Positive Power Supply for the RF Section. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. AV_{DD} has a value of 3 V ± 10%. AV_{DD} must have the same voltage as DV_{DD}.
8	8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of V_{DD}/2 and an equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode.
11	12	CLOCK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first with the three LSBs serving as the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE is high, the data stored in the shift registers is loaded into one of the five latches. The control bits are used to select the latch.
14	15	MUXOUT	Multiplexer Output. This multiplexer output allows either the RF lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	16, 17	DV_{DD}	Positive Power Supply for the Digital Section. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} has a value of 3 V ± 10%. DV_{DD} must have the same voltage as AV_{DD}.
16	18	V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range of up to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

PFD = 25 MHz, loop bandwidth = 20 kHz, reference = 100 MHz, I_{CP} = 313 µA, phase noise measurements taken on the Agilent E5500 phase noise system.

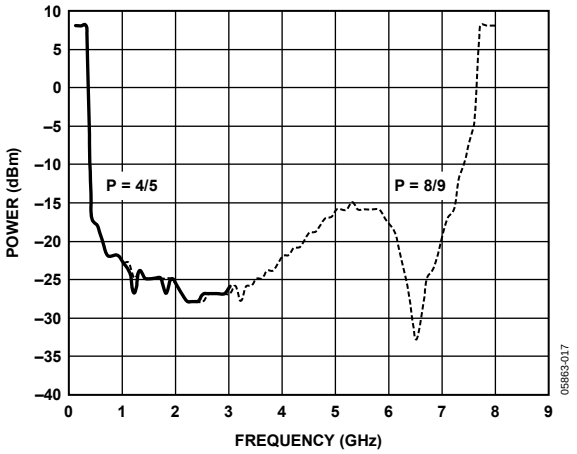


Figure 5. RF Input Sensitivity

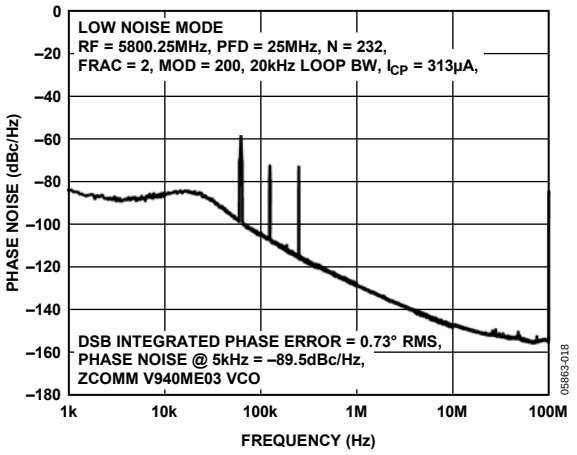


Figure 6. Phase Noise and Spurs, Low Noise Mode

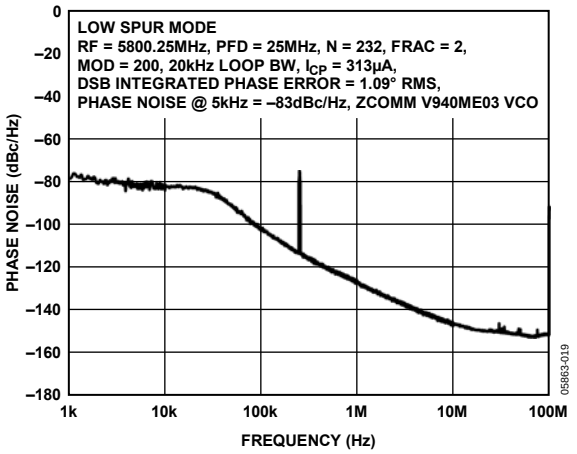


Figure 7. Phase Noise and Spurs, Low Spur Mode. (Note that fractional spurs are removed and only the integer boundary spur remains in low spur mode.)

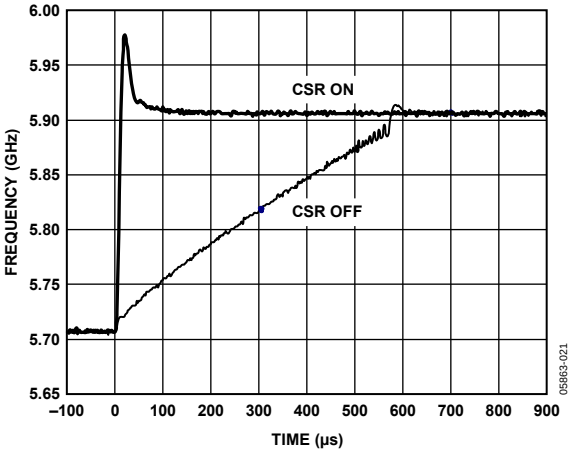


Figure 8. Lock Time for 200 MHz Jump from 5705 MHz to 5905 MHz with CSR On and Off

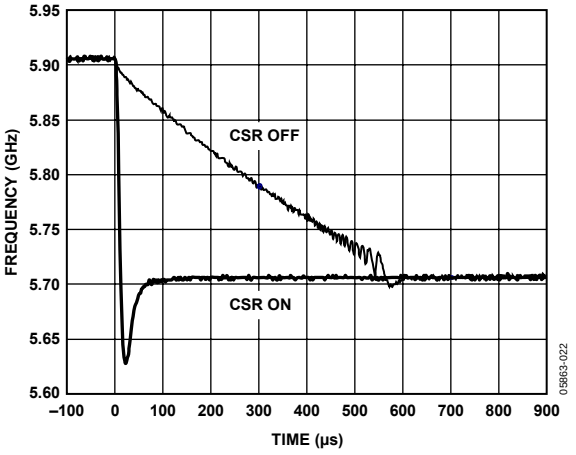


Figure 9. Lock Time for 200 MHz Jump from 5905 MHz to 57905 MHz with CSR On and Off

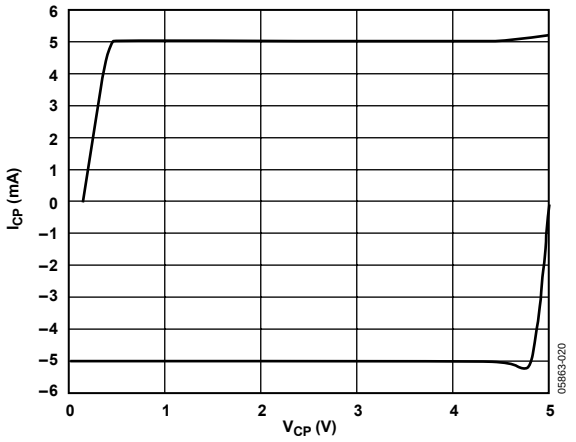


Figure 10. Charge Pump Output Characteristics

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 11. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

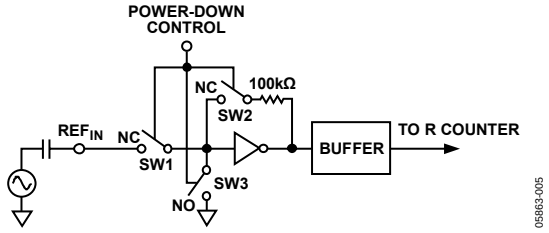


Figure 11. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 12. It is followed by a 2-stage limiting amplifier to generate the current-mode logic (CML) clock levels needed for the prescaler.

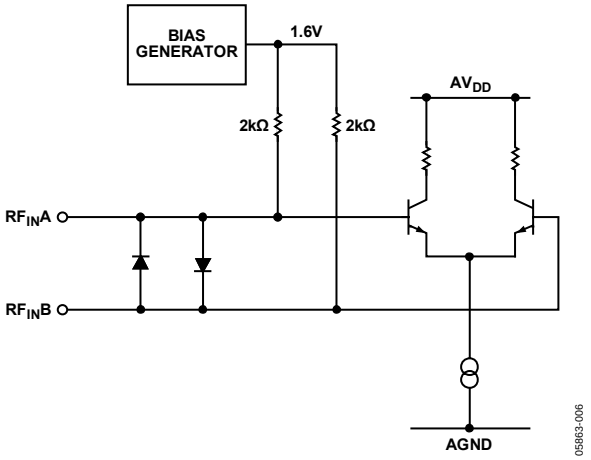


Figure 12. RF Input Stage

RF INT DIVIDER

The RF INT counter allows a division ratio in the PLL feedback counter. Division ratios from 23 to 4095 are allowed.

INT, FRAC, MOD, AND R RELATIONSHIP

The INT, FRAC, and MOD values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the phase frequency detector (PFD). See the RF Synthesizer: A Worked Example section for more information. The RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = F_{PFD} \times (INT + (FRAC/MOD)) \quad (1)$$

where RF_{OUT} is the output frequency of external voltage controlled oscillator (VCO).

$$F_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (2)$$

where:

REF_{IN} is the reference input frequency.

D is the REF_{IN} doubler bit.

T is the REF_{IN} divide-by-2 bit (0 or 1).

R is the preset divide ratio of binary 5-bit programmable reference counter (1 to 32).

INT is the preset divide ratio of binary 12-bit counter (23 to 4095).

MOD is the preset fractional modulus (2 to 4095).

$FRAC$ is the numerator of the fractional division (0 to MOD−1).

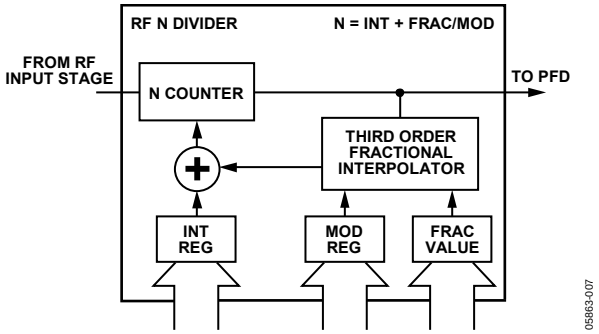


Figure 13. RF INT Divider

RF R COUNTER

The 5-bit RF R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 14 is a simplified schematic of the phase frequency detector. The PFD includes a fixed delay element that sets the width of the antibacklash pulse, which is typically 3 ns. This pulse ensures that there is no dead zone in the PFD transfer function, and gives a consistent reference spur level.

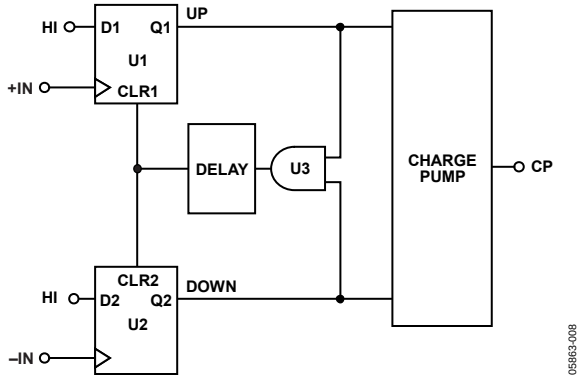


Figure 14. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4156 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M4, M3, M2, and M1 (for details, see Figure 16). Figure 15 shows the MUXOUT section in block diagram form.

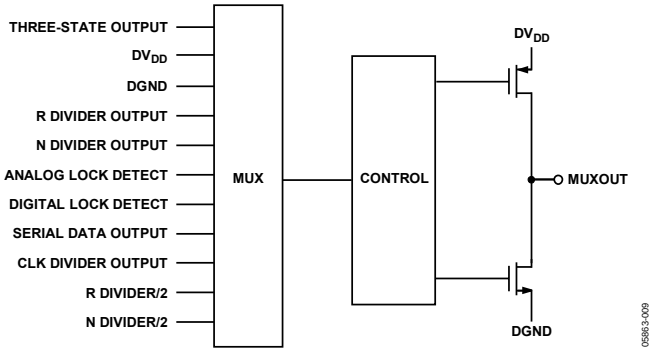


Figure 15. MUXOUT Schematic

INPUT SHIFT REGISTERS

The ADF4156 digital section includes a 5-bit RF R counter, a 12-bit RF N counter, a 12-bit FRAC counter, and a 12-bit modulus counter. Data is clocked into the 32-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of five latches on the rising edge of LE. The destination latch is determined by the state of the three control bits (C3, C2 and C1) in the shift register. These are the 3 LSBs, DB2, DB1, and DB0, as shown in Figure 2. The truth table for these bits is shown in Table 6. Figure 16 shows a summary of how the latches are programmed.

PROGRAM MODES

Table 6 and Figure 16 through Figure 20 show how to set up the program modes in the ADF4156.

A number of settings in the ADF4156 are double buffered. These include the modulus value, phase value, R counter value, reference doubler, reference divide-by-2, and current setting. This means that two events have to occur before the part uses a new value of any of the double buffered settings. First, the new value is latched into the device by writing to the appropriate register. Second, a new write must be performed on Register R0. For example, any time that the modulus value has been updated, Register R0 must be written to after this, to ensure that the modulus value is loaded correctly.

Table 6. C3, C2, and C1 Truth Table

Control Bits			
C3	**C2**	**C1**	**Register**
0	0	0	Register R0
0	0	1	Register R1
0	1	0	Register R2
0	1	1	Register R3
1	0	0	Register R4

REGISTER MAPS

FRAC/INT REGISTER (R0)

RE-SERVED	MUXOUT CONTROL				12-BIT INTEGER VALUE (INT)												12-BIT FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	M4	M3	M2	M1	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3(0)	C2(0)	C1(0)

PHASE REGISTER (R1)

RESERVED																	12-BIT PHASE VALUE (PHASE) (DB)											DBB[1]	CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C3(0)	C2(0)	C1(1)

MOD/R REGISTER (R2)

RESERVED	NOISE MODE		CSR EN	CURRENT SETTING				RESERVED	PRESCALER	RDIV2 DBB[1]	REFERENCE DOUBLER DBB[1]	5-BIT R COUNTER					12-BIT MODULUS WORD (DB)											DBB[1]	CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	L2	L1	C1	CPI4	CPI3	CPI2	CPI1	0	P1	U2	U1	R5	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C3(0)	C2(1)	C1(0)

FUNCTION REGISTER (R3)

RESERVED																	SD RESET	RESERVED						LDP	PD POLARITY	PD	CP THREE-STATE	COUNTER RESET	CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	U12	0	0	0	0	0	0	U7	U6	U5	U4	U3	C3(0)	C2(1)	C1(1)

CLKDIV REGISTER (R4)

RESERVED											CLK DIV MODE		12-BIT CLOCK DIVIDER VALUE											RESERVED				CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	M2	M1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	0	0	0	0	C3(1)	C2(0)	C1(0)

05863-010

[1]DBB = DOUBLE BUFFERED BIT.

Figure 16. Register Summary

FRAC/INT REGISTER, R0

With R0[2, 1, 0] set to [0, 0, 0], the on-chip FRAC/INT register is programmed. Figure 17 shows the input data format for programming this register.

12-Bit INT Value

These twelve bits control what is loaded as the INT value. This determines the overall feedback division factor. It is used in Equation 1 (see the INT, FRAC, MOD, and R Relationship section).

12-Bit FRAC Value

These twelve bits control what is loaded as the FRAC value into the fractional interpolator. This is part of what determines the overall feedback division factor. It is also used in Equation 1. The FRAC value must be less than the value loaded into the MOD register.

MUXOUT

The on-chip multiplexer is controlled by DB30, DB29, DB28, and DB27 on the ADF4156. See Figure 17 for the truth table.

RE-SERVED	MUXOUT CONTROL				12-BIT INTEGER VALUE (INT)												12-BIT FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	M4	M3	M2	M1	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3(0)	C2(0)	C1(0)

M4	M3	M2	M1	OUTPUT
0	0	0	0	THREE-STATE OUTPUT
0	0	0	1	DV_{DD}
0	0	1	0	DGND
0	0	1	1	R DIVIDER OUTPUT
0	1	0	0	N DIVIDER OUTPUT
0	1	0	1	ANALOG LOCK DETECT
0	1	1	0	DIGITAL LOCK DETECT
0	1	1	1	SERIAL DATA OUTPUT
1	0	0	0	RESERVED
1	0	0	1	RESERVED
1	0	1	0	CLK DIVIDER
1	0	1	1	RESERVED
1	1	0	0	RESERVED
1	1	0	1	R DIVIDER/2
1	1	1	0	N DIVIDER/2
1	1	1	1	RESERVED

F12	F11	.....	F2	F1	FRACTIONAL VALUE (FRAC)
0	0	.....	0	0	0
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	4092
1	1	.....	0	1	4093
1	1	.....	1	0	4094
1	1	.....	1	1	4095

N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	INTEGER VALUE (INT)
0	0	0	0	0	0	0	1	0	1	1	1	23
0	0	0	0	0	0	0	1	1	0	0	0	24
0	0	0	0	0	0	0	1	1	0	0	1	25
0	0	0	0	0	0	0	1	1	0	1	0	26
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	0	1	4093
1	1	1	1	1	1	1	1	1	1	1	0	4094
1	1	1	1	1	1	1	1	1	1	1	1	4095

05883-011

Figure 17. FRAC/INT Register (R0) Map

PHASE REGISTER, R1

With R1[2, 1, 0] set to [0, 0, 1], the on chip PHASE register is programmed. Figure 18 shows the input data format for programming this register.

12-Bit PHASE Value

These twelve bits control what is loaded as the PHASE word. The word must be less than the MOD value programmed in the MOD/R register (R2). The word is used to program the RF output phase from 0° to 360 ° with a resolution of 360°/MOD.

See the PHASE RESYNC section for more information. In most applications, the phase relationship between the RF signal and the reference is not important. In such applications, the PHASE value can be used to optimize the fractional and subfractional spur levels. See the section, Spur Consistency and Fractional Spur Optimization, for more information.

If neither the PHASE resync nor the spurious optimization functions are being used, it is recommended that the PHASE word be set to 1.

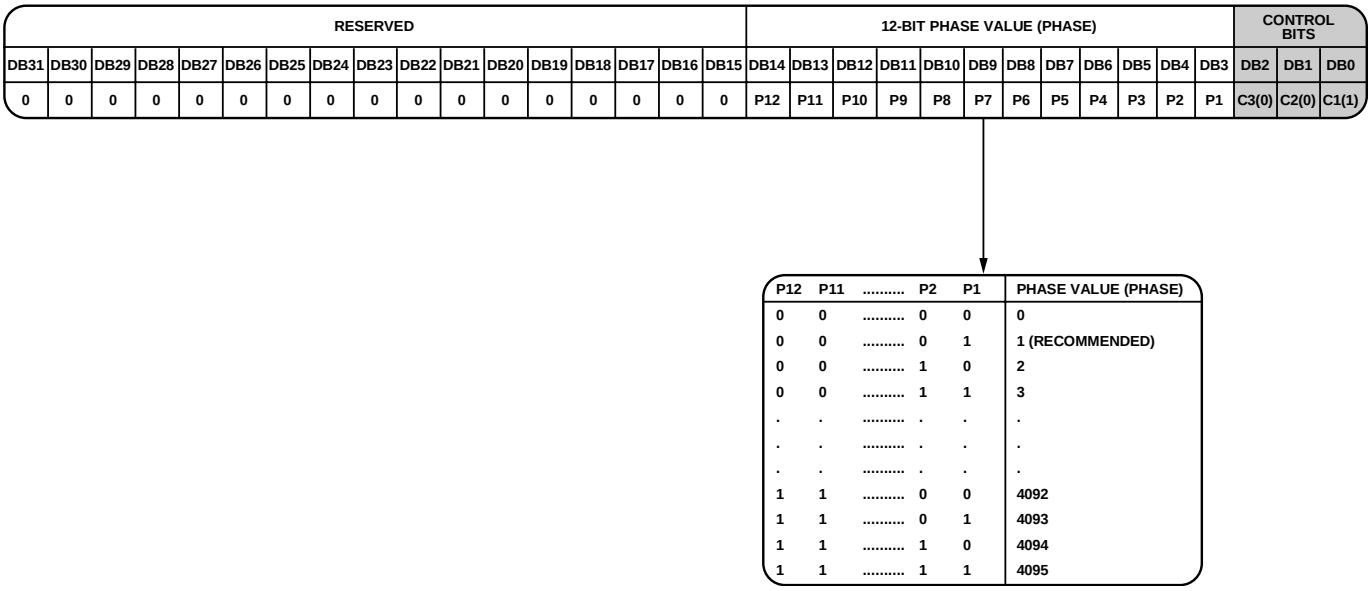


Figure 18. PHASE Register (R1) Map

MOD/R REGISTER, R2

With R1[2, 1, 0] set to [0, 1, 0], the on-chip MOD/R register is programmed. Figure 19 shows the input data format for programming this register.

Noise and Spur Mode

The noise modes on the ADF4156 are controlled by DB30 and DB29 in the MOD/R register. See Figure 19 for the truth table. The noise modes allow the user to optimize a design either for improved spurious performance or for improved phase noise performance.

When the lowest spur setting is chosen, dither is enabled. This randomizes the fractional quantization noise so that it resembles white noise rather than spurious noise. As a result, the part is optimized for improved spurious performance. This operation would normally be used when the PLL closed-loop bandwidth is wide, for fast-locking applications. (Wide loop bandwidth is seen as a loop bandwidth greater than 1/10 of the RF_{OUT} channel step resolution (f_{RES})). A wide loop filter does not attenuate the spurs to the same level as a narrow loop bandwidth.

For best noise performance, use the lowest noise setting option. As well as disabling the dither, it also ensures that the charge pump is operating in an optimum region for noise performance. This setting is extremely useful where a narrow loop filter bandwidth is available. The synthesizer ensures extremely low noise and the filter attenuates the spurs. The typical performance characteristics give the user an idea of the trade-off in a typical WCDMA setup for the different noise and spur settings.

CSR Enable

Setting this bit to 1 enables cycle slip reduction. This is a method for improving lock times. Note that the signal at the phase frequency detector (PFD) must have a 50% duty cycle in order for cycle slip reduction to work. The charge pump current setting must also be set to a minimum. See the section, Cycle Slip Reduction for Faster Lock Times, for more information.

Charge Pump Current Setting

DB27, DB26, DB25, and DB24 set the charge pump current setting. This should be set to the charge pump current that the loop filter is designed with (see Figure 19).

Prescaler (P/P + 1)

The dual modulus prescaler (P/P + 1), along with the INT, FRAC, and MOD counters, determines the overall division ratio from the RF_{IN} to the PFD input.

Operating at CML levels, it takes the clock from the RF input stage and divides it down for the counters. It is based on a synchronous 4/5 core. When set to 4/5, the maximum RF frequency allowed is 3 GHz. Therefore, when operating the ADF4156 above 3 GHz, this must be set to 8/9. The prescaler limits the INT value.

With $P = 4/5$, $N_{MIN} = 23$.
With $P = 8/9$, $N_{MIN} = 75$.

RDIV/2

Setting this bit to 1 inserts a divide-by-2 toggle flip-flop between the R counter and PFD, which extends the maximum REF_{IN} input rate.

Reference Doubler

Setting DB20 to 0 feeds the REF_{IN} signal directly to the 5-bit RF R counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding into the 5-bit R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising and falling edges of REF_{IN} become active edges at the PFD input.

When the doubler is enabled and the lowest spur mode is chosen, the in-band phase noise performance is sensitive to the REF_{IN} duty cycle. The phase noise degradation can be as much as 5 dB for the REF_{IN} duty cycles outside a 45% to 55% range. The phase noise is insensitive to the REF_{IN} duty cycle in the lowest noise mode. The phase noise is insensitive to REF_{IN} duty cycle when the doubler is disabled.

The maximum allowable REF_{IN} frequency when the doubler is enabled is 30 MHz.

5-Bit R Counter

The 5-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 32 are allowed.

12-Bit Interpolator MOD Value

This programmable register sets the fractional modulus. This is the ratio of the PFD frequency to the channel step resolution on the RF output. Refer to the RF Synthesizer: A Worked Example section for more information.

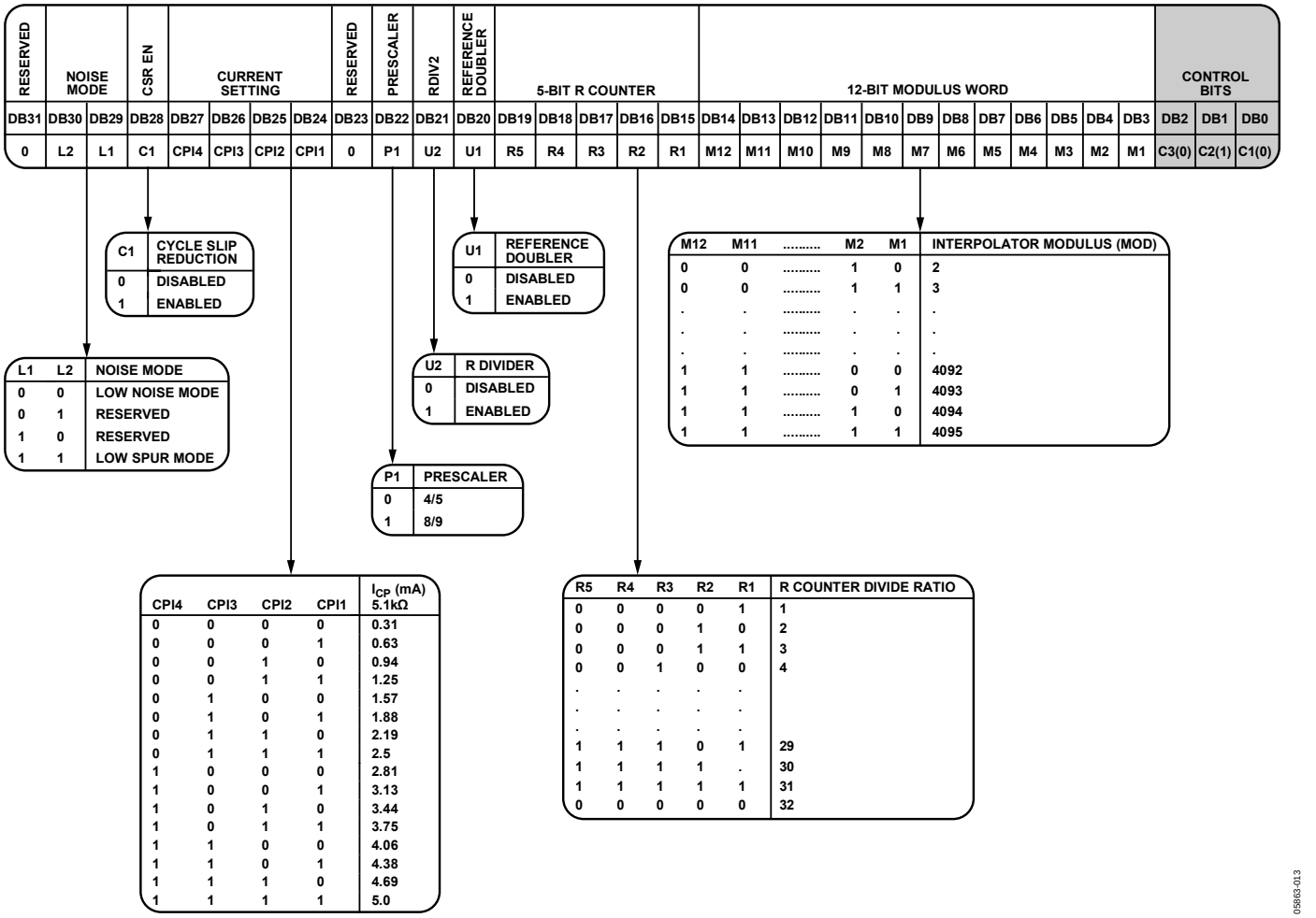


Figure 19. MOD/R Register (R2) Map

FUNCTION REGISTER, R3

With R2[2, 1, 0] set to [0, 1, 1], the on-chip function register is programmed. Figure 20 shows the input data format for programming this register.

RF Counter Reset

DB3 is the RF counter reset bit for the ADF4156. When this is 1, the RF synthesizer counters are held in reset. For normal operation, this bit should be 0.

RF Charge Pump Three-State

DB4 puts the charge pump into three-state mode when programmed to 1. It should be set to 0 for normal operation.

RF Power-Down

DB5 on the ADF4156 provides the programmable power-down mode. Setting this bit to 1 performs a power-down. Setting this bit to 0 returns the synthesizer to normal operation. While in software power-down mode, the part retains all information in its registers. Only when supplies are removed are the register contents lost.

When a power-down is activated, the following events occur:

1. The synthesizer counters are forced to their load state conditions.
2. The charge pump is forced into three-state mode.
3. The digital lock detect circuitry is reset.
4. The RF_{IN} input is debiased.
5. The input register remains active and capable of loading and latching data.

Phase Detector Polarity

DB6 in the ADF4156 sets the phase detector polarity. When the VCO characteristics are positive, this should be set to 1. When they are negative, it should be set to 0.

Lock Detect Precision (LDP)

When DB7 is programmed to 0, 40 consecutive PFD cycles of 10 ns must occur before digital lock detect is set. When this bit is programmed to 1, 40 consecutive reference cycles of 6 ns must occur before digital lock detect is set.

Sigma-Delta (SD) Reset

For most applications, DB14 should be programmed to 0. When DB14 is programmed to 0, the sigma-delta is reset and seeded with the PHASE word on every write to Register 0. This has the effect of producing consistent spur levels.

If it is not required that the sigma-delta be reset on each write to Register 0, this bit should be set to 1.

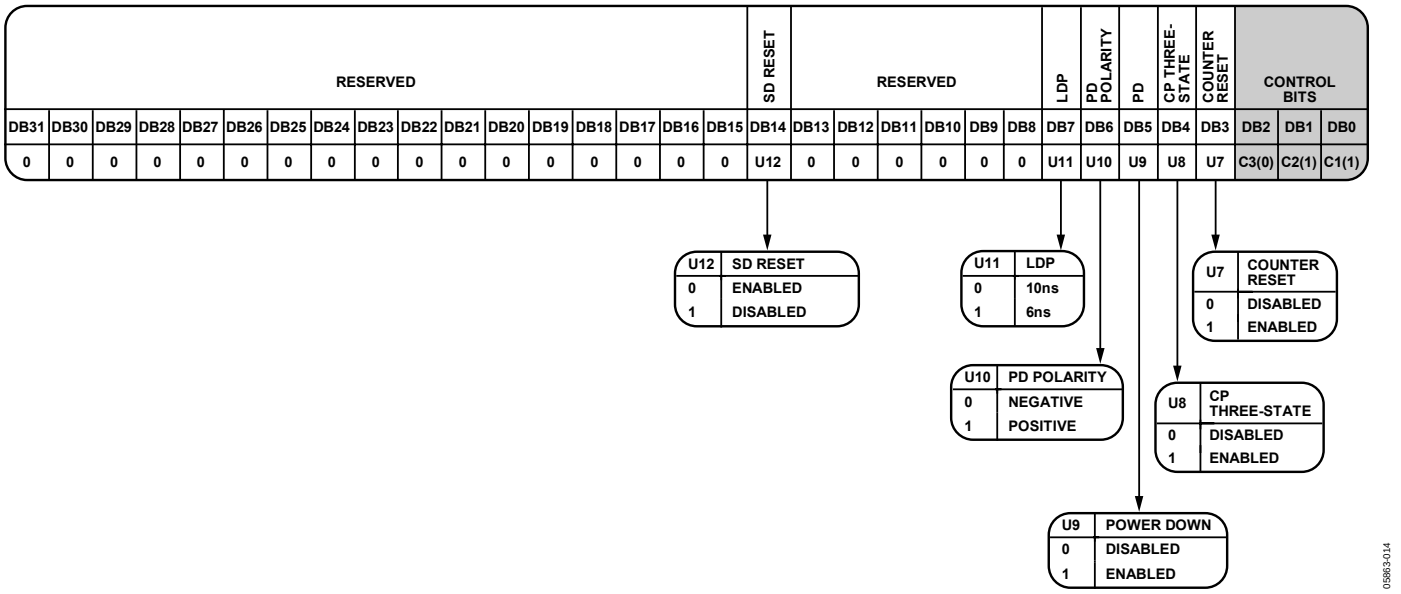


Figure 20. Function Register (R3) Map

CLK DIV REGISTER, R4

With R3[2,1, 0] set to [1, 0, 0], the on-chip clock divider register (R4) is programmed. Figure 21 shows the input data format for programming this register.

12-Bit Clock Divider Value

The 12-bit clock divider value sets the timeout counter for activation of PHASE Resync. See the PHASE RESYNC section for more information.

Clock Divider Mode

These bits must be set to DB[20, 19] = [1, 0] in order to activate PHASE resync, and 0 otherwise.

RESERVED BITS

All reserved bits should be set to 0 for normal operation.

INITIALIZATION SEQUENCE

After powering up the part, the correct register programming sequence is:

1. CLK/DIV register (R4)
2. FUNCTION register (R3)
3. MOD/R register (R2)
4. PHASE register (R1)
5. FRAC/INT register (R0)

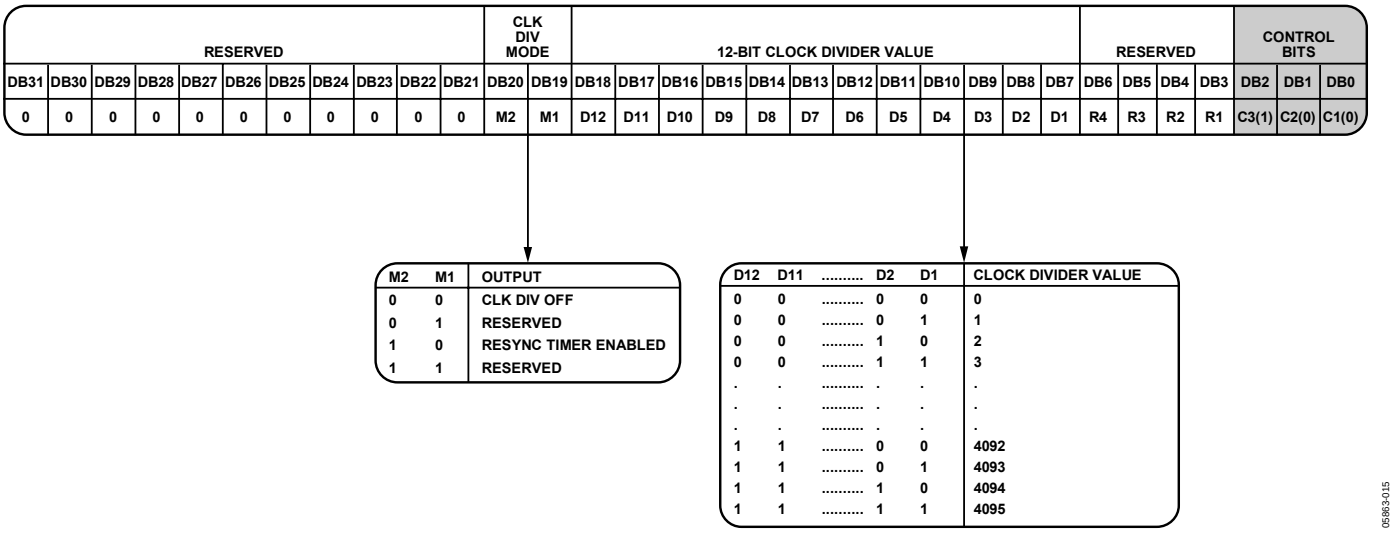


Figure 21. CLK DIV Register (R4) Map

RF SYNTHESIZER: A WORKED EXAMPLE

The following equation governs how the synthesizer should be programmed:

$$RF_{OUT} = [INT + (FRAC/MOD)] \times [F_{PFD}] \quad (3)$$

where:

RF_{OUT} is the RF frequency output.
INT is the integer division factor.
FRAC is the fractionality.
MOD is the modulus.

$$F_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1+T))] \quad (4)$$

where:

REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit.
T is the reference divide-by-2 Bit(0 or 1).
R is the RF reference division factor. For example, in a GSM 1800 system, where 1.8 GHz RF frequency output (RF_{OUT}) is required, a 13 MHz reference frequency input (REF_{IN}) is available, and a 200 kHz channel resolution (f_{RES}) is required, on the RF output.

$$MOD = REF_{IN}/f_{RES}$$
$$MOD = 13 \text{ MHz}/200 \text{ kHz} = 65$$

From Equation 4

$$F_{PFD} = [13 \text{ MHz} \times (1 + 0)/1] = 13 \text{ MHz} \quad (5)$$

$$1.8 \text{ GHz} = 13 \text{ MHz} \times (INT + FRAC/65) \quad (6)$$

where *INT* = 138; *FRAC* = 30.

MODULUS

The choice of modulus (MOD) depends on the reference signal (REF_{IN}) available and the channel resolution (f_{RES}) required at the RF output. For example, a GSM system with 13 MHz REF_{IN} sets the modulus to 65. This means that the RF output resolution (f_{RES}) is the 200 kHz (13 MHz/65) necessary for GSM. With dither off, the fractional spur interval depends on the modulus values chosen. See Table 7 for more information.

REFERENCE DOUBLER AND REFERENCE DIVIDER

The reference doubler on-chip allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually improves noise performance by 3 dB. It is important to note that the PFD cannot be operated above 32 MHz due to a limitation in the speed of the Σ-Δ circuit of the N-divider.

The reference divide-by-2 divides the reference signal by 2, resulting in a 50% duty cycle PFD frequency. This is necessary for the correct operation of the cycle slip reduction (CSR) function. See the Cycle Slip Reduction for Faster Lock Times section for more information.

12-BIT PROGRAMMABLE MODULUS

Unlike most other fractional-N PLLs, the ADF4156 allows the user to program the modulus over a 12-bit range. This means that the user can set up the part in many different configurations for the application, when combined with the reference doubler and the 5-bit R counter.

The following is an example of an application that requires 1.75 GHz RF and 200 kHz channel step resolution. The system has a 13 MHz reference signal.

One possible setup is feeding the 13 MHz directly to the PFD and programming the modulus to divide by 65. This results in the required 200 kHz resolution.

Another possible setup is using the reference doubler to create 26 MHz from the 13 MHz input signal. This 26 MHz is then fed into the PFD programming the modulus to divide by 130. This also results in 200 kHz resolution and offers superior phase noise performance over the previous setup.

The programmable modulus is also very useful for multi-standard applications. If a dual-mode phone requires PDC and GSM 1800 standards, the programmable modulus is a great benefit. PDC requires 25 kHz channel step resolution, whereas GSM 1800 requires 200 kHz channel step resolution.

A 13 MHz reference signal can be fed directly to the PFD and the modulus can be programmed to 520 when in PDC mode (13 MHz/520 = 25 kHz).

The modulus needs to be reprogrammed to 65 for GSM 1800 operation (13 MHz/65 = 200 kHz).

It is important that the PFD frequency remains constant (13 MHz). This allows the user to design one loop filter that can be used in both setups without running into stability issues. It is the ratio of the RF frequency to the PFD frequency that affects the loop design. By keeping this relationship constant, the same loop filter can be used in both applications.

CYCLE SLIP REDUCTION FOR FASTER LOCK TIMES

As mentioned in the Noise and Spur Mode section, the ADF4156 can be optimized for noise performance. However, in fast-locking applications, the loop bandwidth needs to be wide, and therefore, the filter does not provide much attenuation of the spurs. The cycle slip reduction function on the ADF4156 can be used to get around this issue. Using cycle slip reduction, the loop bandwidth can be kept narrow to attenuate spurs and still obtain fast lock times.

Cycle Slips

Cycle slips occur in integer-N/fractional-N synthesizers when the loop bandwidth is narrow compared to the PFD frequency. The phase error at the PFD inputs accumulates too fast for the PLL to correct, and the charge pump temporarily pumps in the wrong direction. This slows down the lock time dramatically. The ADF4156 contains a cycle slip reduction circuit to extend the linear range of the PFD allowing faster lock times without loop filter changes.

When the ADF4156 detects that a cycle slip is about to occur, it turns on an extra charge pump current cell. This outputs a constant current to the loop filter, or removes a constant current from the loop filter (depending on whether the VCO tuning voltage needs to increase or decrease to acquire the new frequency). The effect is that the linear range of the PFD is increased. Stability is maintained because the current is constant and is not a pulsed current.

If the phase error increases again to a point where another cycle slip is likely, the ADF4156 turns on another charge pump cell. This continues until the ADF4156 detects that the VCO frequency has gone past the desired frequency. It then begins to turn off the extra charge pump cells one by one until they have all been turned off and the frequency is settled.

Up to seven extra charge pump cells can be turned on. In most applications, it is enough to eliminate cycle slips altogether, giving much faster lock times.

Setting Bit DB28 in the MOD/R register (R2) to 1 enables cycle slip reduction. Note that a 45% to 55% duty cycle is needed on the signal at the PFD in order for CSR to operate correctly.

SPUR MECHANISMS

This section describes the three different spur mechanisms that arise with a fractional-N synthesizer and how to minimize them in the ADF4156.

Fractional Spurs

The fractional interpolator in the ADF4156 is a third order Σ-Δ modulator (SDM) with a modulus (MOD) that is programmable to any integer value from 2 to 4095. In low spur mode (dither enabled) the minimum allowable value of MOD is 50. The SDM is clocked at the PFD reference rate (f_{PFD}) that allows PLL output frequencies to be synthesized at a channel step resolution of f_{PFD}/MOD.

In low noise mode (dither off), the quantization noise from the Σ-Δ modulator appears as fractional spurs. The interval between spurs is f_{PFD}/L, where L is the repeat length of the code sequence in the digital Σ-Δ modulator. For the third-order modulator used in the ADF4156, the repeat length depends on the value of MOD, as listed in Table 7.

Table 7. Fractional Spurs with Dither Off

Condition (Dither Off)	Repeat Length	Spur Interval
If MOD is divisible by 2, but not 3	2 × MOD	Channel step/2
If MOD is divisible by 3, but not 2	3 × MOD	Channel step/3
If MOD is divisible by 6	6 × MOD	Channel step/6
Otherwise	MOD	Channel step

In low spur mode (dither enabled), the repeat length is extended to 2^{21} cycles, regardless of the value of MOD, which makes the quantization error spectrum look like broadband noise. This can degrade the in-band phase noise at the PLL output by as much as 10 dB. Therefore, for lowest noise, dither off is a better choice, particularly when the final loop BW is low enough to attenuate even the lowest frequency fractional spur.

Integer Boundary Spurs

Another mechanism for fractional spur creation are interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related (which is the whole point of a fractional-N synthesizer) spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or difference frequency between an integer multiple of the reference and the VCO frequency.

These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference where the difference frequency can be inside the loop bandwidth, hence the name integer boundary spurs.

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers as the reference offset is far outside the loop bandwidth. However, any reference feed-through mechanism that bypasses the loop can cause a problem. One such mechanism is feed through of low levels of on-chip reference switching noise out through the RF_{IN} pin back to the VCO, resulting in reference spur levels as high as –90 dBc. Care should be taken in the PCB layout to ensure that the VCO is well separated from the input reference to avoid a possible feed through path on the board.

SPUR CONSISTENCY AND FRACTIONAL SPUR OPTIMIZATION

With dither off, the fractional spur pattern due to the quantization noise of the SDM also depends on the particular PHASE word with which the modulator is seeded. Setting the SD reset bit to zero (DB14 in Register 3) ensures that the SDM is seeded with the PHASE word on every write to Register 0.

The PHASE word can be varied to optimize the fractional and subfractional spur levels on any particular frequency. Thus, a look-up table of PHASE values corresponding to each frequency can be constructed for use when programming the ADF4156.

The evaluation software has a sweep function to sweep the PHASE word so that the user can observe the spur levels on a spectrum analyzer.

If a look-up table is not used, keep the PHASE word at a constant value to ensure consistent spur levels on any particular frequency.

PHASE RESYNC

The output of a fractional-N PLL can settle to any one of MOD phase offsets with respect to the input reference; where MOD is the fractional modulus. The PHASE resync feature in the ADF4156 is used to produce a consistent output phase offset with respect to the input reference. This is necessary in applications where the output phase and frequency are important, such as digital beam forming. See the section, PHASE Programmability, for how to program a specific RF output phase when using PHASE resync.

PHASE resync is enabled by setting Bit DB20 and Bit DB19 in Register R4 to [1, 0]. When PHASE resync is enabled, an internal timer generates sync signals at intervals of T_{SYNC} given by the following formula:

$$T_{SYNC} = CLK\_DIV\_VALUE \times MOD \times T_{PFD}$$

where:

T_{PFD} is the PFD reference period.

CLK_DIV_VALUE is the decimal value programmed in Bit DB[18:7] of Register R4, and can be any integer in the range of 1 to 4095.

MOD is the modulus value programmed in Bit DB[14:3] of Register R1.

When a new frequency is programmed, the second sync pulse after the LE rising edge is used to resynchronize the output phase to the reference. The T_{SYNC} time should be programmed to a value that is as least as long as the worst-case lock time. Doing so guarantees that the PHASE resync occurs after the last cycle slip in the PLL settling transient.

In the example shown in Figure 22, the PFD reference is 25 MHz and MOD = 125 for a 200 kHz channel spacing. T_{SYNC} is set to 400 µs by programming CLK_DIV_VALUE = 80.

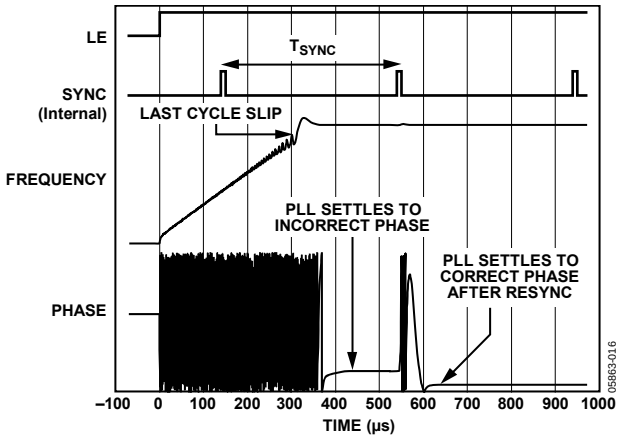


Figure 22. PHASE Resync Example

PHASE Programmability

In order to program a specific RF output phase, the PHASE word in Register R1 should be changed. As this word is swept from 0 to MOD, the RF output phase sweeps over a 360°/MOD range in steps of 360°/MOD.

LOW FREQUENCY APPLICATIONS

The specification on the RF input is 0.5 GHz minimum, however, RF frequencies lower than this can be used providing the minimum slew rate specification of 400 V/µs is met. An appropriate LVDS driver can be used to square up the RF signal before it is fed back to the ADF4156 RF input. The FIN1001 from Fairchild Semiconductor is one such LVDS driver.

FILTER DESIGN—ADIsimPLL

A filter design and analysis program is available to help the user to implement PLL design. Visit www.analog.com/pll for a free download of the ADIsimPLL software. The software designs, simulates, and analyzes the entire PLL frequency domain and time domain response. Various passive and active filter architectures are allowed. In designing the loop filter, the ratio of PFD frequency to loop bandwidth should be kept >200:1. This is to attenuate the SDM noise.

INTERFACING

The ADF4156 has a simple SPI®-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When latch enable (LE) is high, the 29 bits that have been clocked into the input register on each rising edge of SCLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 6 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz.

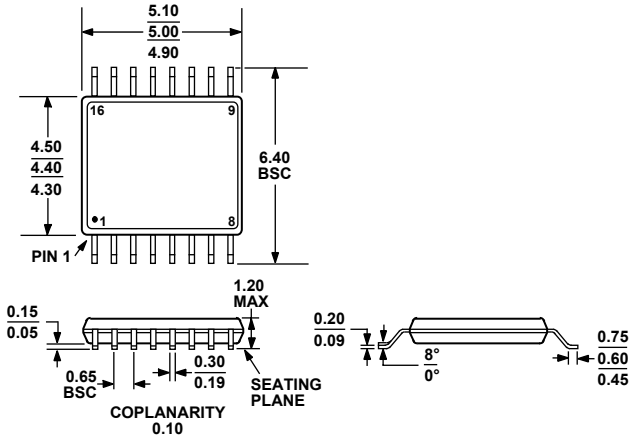
PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The lands on the lead frame chip scale package (CP-20-1) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

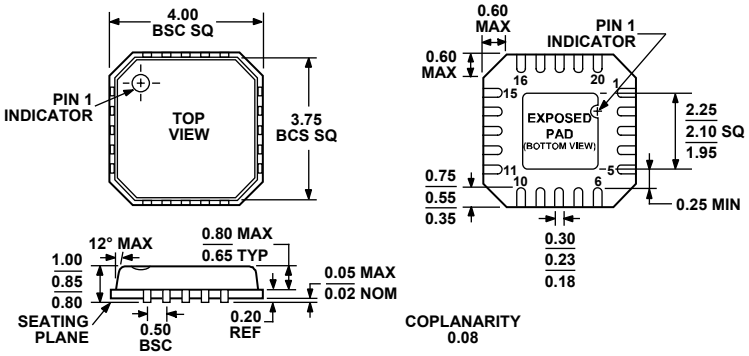
Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 ounce of copper to plug the via. The user should connect the printed circuit board thermal pad to AGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 23. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 24. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF4156BRUZ[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4156BRUZ-RL[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4156BRUZ-RL7[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4156BCPZ[1]	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-1
ADF4156BCPZ-RL[1]	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-1
ADF4156BCPZ-RL7[1]	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-1
EVAL-ADF4156EB1		Evaluation Board	

[1] Z = Pb-free part.

NOTES

NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

D05863-0-5/06(0)

Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

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