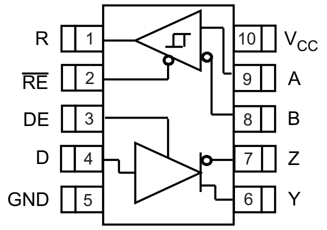
LOW-POWER RS-485 FULL-DUPLEX DRIVERS/RECEIVERS

Check for Samples: SN65HVD3080E, SN65HVD3083E, SN65HVD3086E

FEATURES

- **Low Quiescent Power**
  - **375 μA (Typical) Enabled Mode**
  - **2 nA (Typical) Shutdown Mode**
- **Small MSOP Package**
- **1/8 Unit-Load—Up to 256 Nodes per Bus**
- **16 kV Bus-Pin ESD Protection, 6 kV All Pins**
- **Failsafe Receiver (Bus Open, Short, Idle)**
- **TIA/EIA-485A Standard Compliant**
- **RS-422 Compatible**
- **Power-Up, Power-Down Glitch-Free Operation**

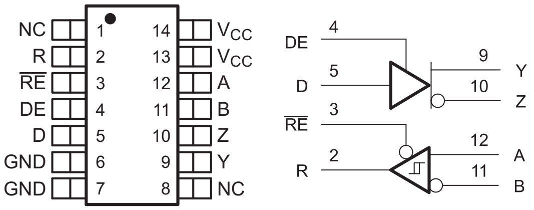
DGS PACKAGE
(TOP VIEW)



APPLICATIONS

- **Motion Controllers**
- **Point-of-Sale (POS) Terminals**
- **Rack-to-Rack Communications**
- **Industrial Networks**
- **Power Inverters**
- **Battery-Powered Applications**
- **Building Automation**

D PACKAGE
(TOP VIEW)



NC - No internal connection
Pins 6 and 7 are connected together internally
Pins 13 and 14 are connected together internally

DESCRIPTION

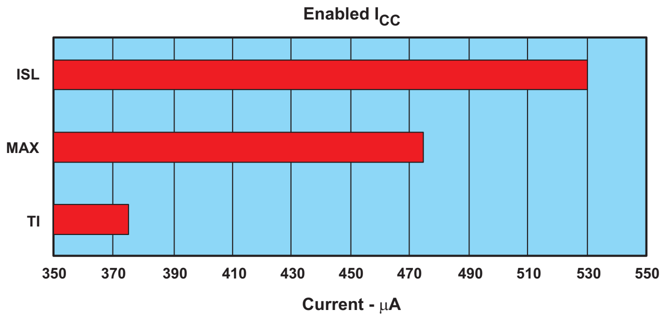
Each of these devices is a balanced driver and receiver designed for full-duplex RS-485 or RS-422 data bus networks. Powered by a 5-V supply, they are fully compliant with the TIA/EIA-485A standard.

With controlled bus output transition times, the devices are suitable for signaling rates from 200 kbps to 20 Mbps.

The devices are designed to operate with a low supply current, less than 1 mA (typical), exclusive of the load. When in the inactive shutdown mode, the supply current drops to a few nanoamps, making these devices ideal for power-sensitive applications.

The wide common-mode range and high ESD protection levels of these devices make them suitable for demanding applications such as motion controllers, electrical inverters, industrial networks, and cabled chassis interconnects where noise tolerance is essential.

These devices are characterized for operation over the temperature range -40°C to 85°C



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PART NUMBER	SIGNALING RATE	PACKAGE[1]	MARKED AS
SN65HVD3080E	200 kbps	DGS, DGSR 10-pin MSOP [2]	BTT
SN65HVD3083E	1 Mbps		BTU
SN65HVD3086E	20 Mbps		BTF
		D 14-pin SOIC	HVD3086

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The R suffix indicated tape and reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

		UNIT
V_{CC}	Supply voltage range[2]	–0.3 V to 7 V
$V_{(A)}$, $V_{(B)}$, $V_{(Y)}$, $V_{(Z)}$	Voltage range at any bus terminal (A, B, Y, Z)	–9 V to 14 V
$V_{(TRANS)}$	Voltage input, transient pulse through 100 Ω. See Figure 10 (A, B, Y, Z)	–50 to 50 V
V_I	Input voltage range (D, DE, $\overline{RE}$)	-0.3 V to V_{CC}+0.3 V
P_D	Continuous total power dissipation	See the dissipation rating table
T_J	Junction temperature	170°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

POWER DISSIPATION RATINGS

PACKAGE	T_A < 25°C	DERATING FACTOR[1] ABOVE T_A < 25°C	T_A = 85°C
10-pin MSOP (DGS)	463 mW	3.71 mW/°C	241 mW
14-pin SOIC (D)	765 mW	6.1 mW/°C	400 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

ELECTROSTATIC DISCHARGE PROTECTION

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Human Body Model[1]	A,B,Y,Z, and GND		16		kV
	All pins		6		kV
Charged Device Mode[2]	All pins		1.5		kV
Machine Model[3]	All pins		400		V

(1) Tested in accordance JEDEC Standard 22, Test Method A114-A. Bus pin stressed with respect to a common connection of GND and V_{CC}.
(2) Tested in accordance JEDEC Standard 22, Test Method C101.
(3) Tested in accordance JEDEC Standard 22, Test Method A115.

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SUPPLY CURRENT

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	$\overline{RE}$ at 0 V, D and DE at V_{CC}, No load	Receiver enabled, Driver enabled		375	750	µA
		$\overline{RE}$ at 0 V, D and DE at 0 V, No load	Receiver enabled, Driver disabled		300	680	µA
		$\overline{RE}$ at V_{CC}, D and DE at V_{CC}, No load	Receiver disabled, Driver enabled		240	600	µA
		$\overline{RE}$ and D at V_{CC}, DE at 0 V, No load	Receiver disabled, Driver disabled		2	1000	nA

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–7[1]		12	
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	
V_{ID}	Differential input voltage		–12		12	V
		Dynamic , See Figure 11				V
I_{OH}	High-level output current	Driver	–60			mA
		Receiver	–10			
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			10	
T_J	Junction temperature				150	°C
T_A	Ambient still-air temperature		–40		85	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

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DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage	No load, I_O = 0	3	4.3	V_{CC}	V
		R_L = 54 Ω, See Figure 1	1.5	2.3		
		V_{test} = –7 V to 12 V, See Figure 2	1.5			
		R_L = 100 Ω, See Figure 1	2			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage	R_L = 54 Ω, See Figure 1 and Figure 2	–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1	2.6	3	V
$\Delta V_{OC(SS)}$	Common-mode output voltage (Dominant)		-0.1	0	0.1	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			0.5		
$I_{Z(Y)}$ or $I_{Z(Z)}$	High-impedance state output current	V_{CC} = 0 V, $V_{(Z)}$ or $V_{(Y)}$ = 12 V Other input at 0 V			1	μA
		V_{CC} = 0 V, $V_{(Z)}$ or $V_{(Y)}$ = -7 V Other input at 0 V	-1			
		V_{CC} = 5 V, $V_{(Z)}$ or $V_{(Y)}$ = 12 V Other input at 0 V			1	
		V_{CC} = 5 V, $V_{(Z)}$ or $V_{(Y)}$ = -7 V Other input at 0 V	-1			
I_I	Input current	D, DE	-100		100	μA
I_{OS}	Short-circuit output current	–7 V ≤ V_O ≤ 12 V	-250		250	mA

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	HVD3080E	R_L = 54 Ω, C_L = 50 pF, See Figure 4		0.7	1.3	μs
		HVD3083E			150	500	ns
		HVD3086E			12	20	ns
t_r, t_f	Differential output signal rise time Differential output signal fall time	HVD3080E		0.5	0.9	1.5	μs
		HVD3083E			200	300	ns
		HVD3086E			7	15	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)	HVD3080E			20	200	ns
		HVD3083E			5	50	ns
		HVD3086E			1.4	5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	HVD3080E	R_L = 110 Ω, $\overline{RE}$ at 0 V, See Figure 5		2.5	7	μs
		HVD3083E			1	2.5	μs
		HVD3086E			13	30	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD3080E			80	200	ns
		HVD3083E			60	100	ns
		HVD3086E			12	30	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	HVD3080E	R_L = 110 Ω, $\overline{RE}$ at 0 V, See Figure 6		2.5	7	μs
		HVD3083E			1	2.5	μs
		HVD3086E			13	30	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD3080E			80	200	ns
		HVD3083E			60	100	ns
		HVD3086E			12	30	ns
t_{PZH}, t_{PZL}	Propagation delay time, standby-to-high-level output (See Figure 5) Propagation delay time, standby-to-low-level output (See Figure 6)		R_L = 110 Ω, $\overline{RE}$ at 3 V		3.5	7	μs

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RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage		I_O = –10 mA		-0.08	–0.01	V
V_{IT-}	Negative-going differential input threshold voltage		I_O = 10 mA	–0.2	-0.1		
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})				30		mV
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = –10 mA, See Figure 7 and Figure 8	4	4.6		V
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, I_{OH} = 10 mA, See Figure 7 and Figure 8		0.15	0.4	V
I_{OZ}	High-impedance-state output current		V_O = 0 or V_{CC}	–1		1	µA
I_I	Bus input current	Other input at 0V	V_A or V_B = 12 V		0.04	0.11	mA
			V_A or V_B = 12 V, V_{CC} = 0 V		0.06	0.13	
			V_A or V_B = -7 V	–0.1	–0.04		
			V_A or V_B = -7 V, V_{CC} = 0 V	–0.05	–0.03		
I_{IH}	High-level input current		V_{IH} = 2 V	–60	-30		µA
I_{IL}	Low-level input current		V_{IL} = 0.8 V	-60	-30		µA
C_{ID}	Differential input capacitance		V_I = 0.4 sin (4E6πt) + 0.5 V		7		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, See Figure 8			75	100	ns
t_{PHL}	Propagation delay time, high-to-low-level output				79	100	
$t_{sk(p)}$	Pulse skew (|t_{PHL} – t_{PLH}|)				4	10	
t_r	Output signal rise time				1.5	3	
t_f	Output signal fall time				1.8	3	
t_{PZH}, t_{PZL}	Output enable time		DE at V_{CC}, See Figure 9		10	50	ns
		From standby	DE at GND, See Figure 9		1.7	3.5	µs
t_{PHZ}, t_{PLZ}	Output disable time	DE at GND or V_{CC}, See Figure 9			7	50	ns

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PARAMETER MEASUREMENT INFORMATION

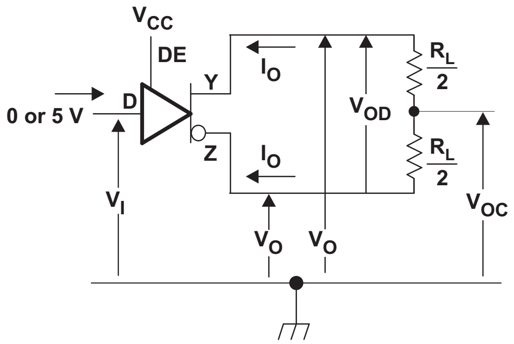


Figure 1. Driver V_{OD} Test Circuit and Current Definitions

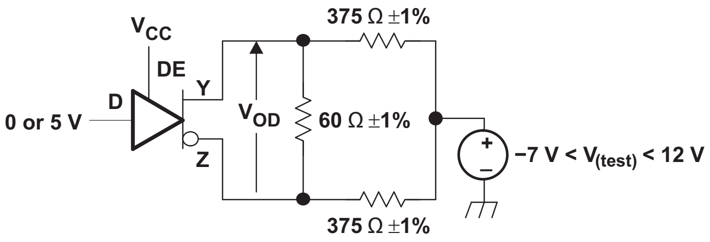
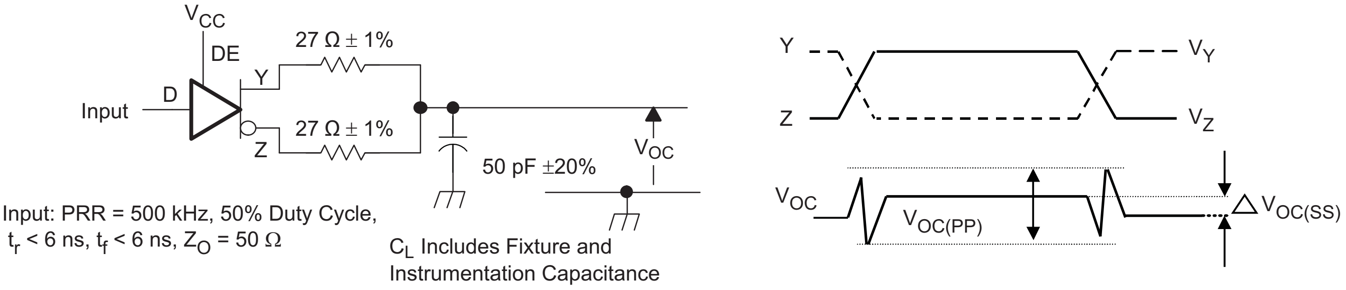


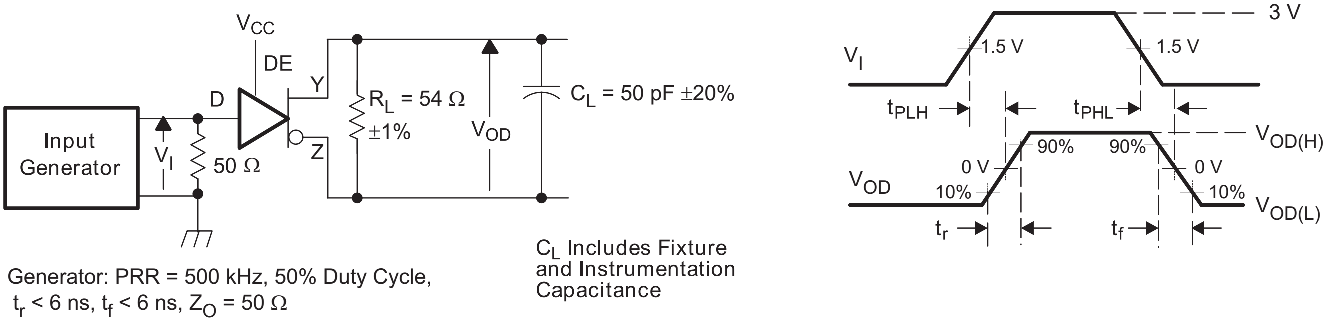
Figure 2. Driver V_{OD} With Common-Mode Loading Test Circuit



Input: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

C_L Includes Fixture and Instrumentation Capacitance

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

C_L Includes Fixture and Instrumentation Capacitance

Figure 4. Driver Switching Test Circuit and Voltage Waveforms

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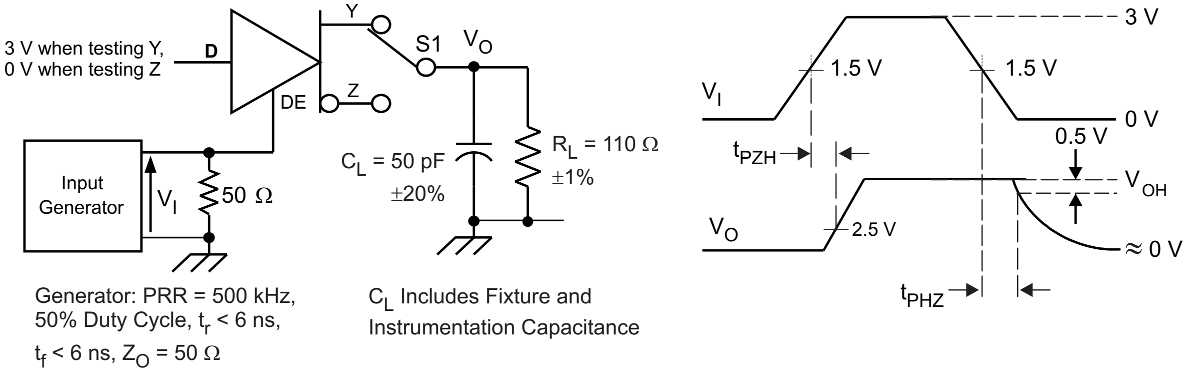
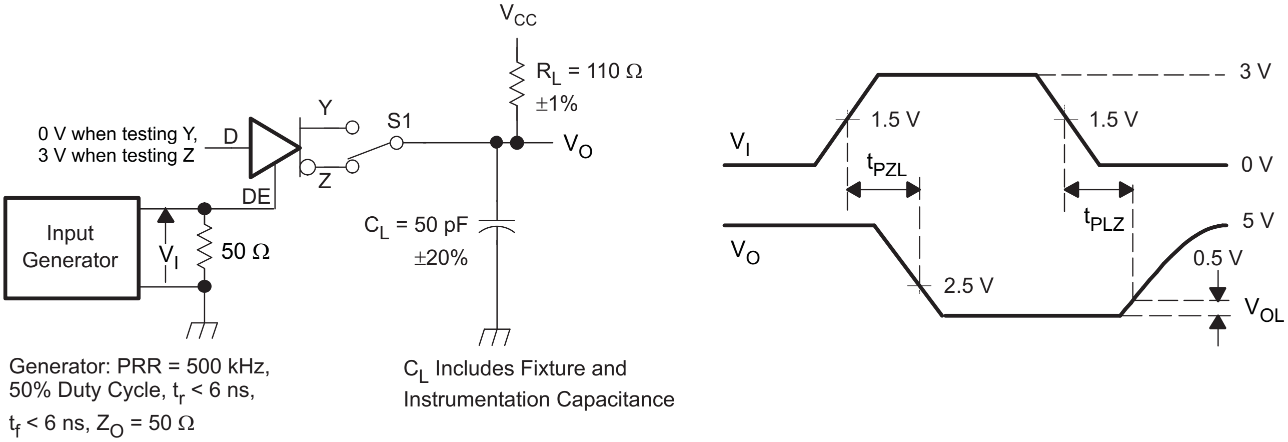
PARAMETER MEASUREMENT INFORMATION (continued)



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

C_L Includes Fixture and Instrumentation Capacitance

Figure 5. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

C_L Includes Fixture and Instrumentation Capacitance

Figure 6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

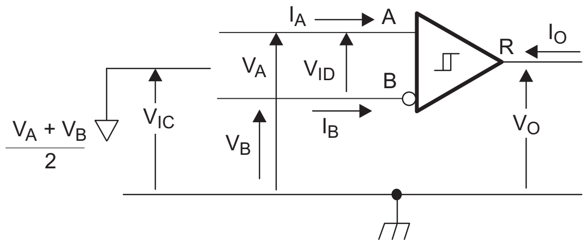
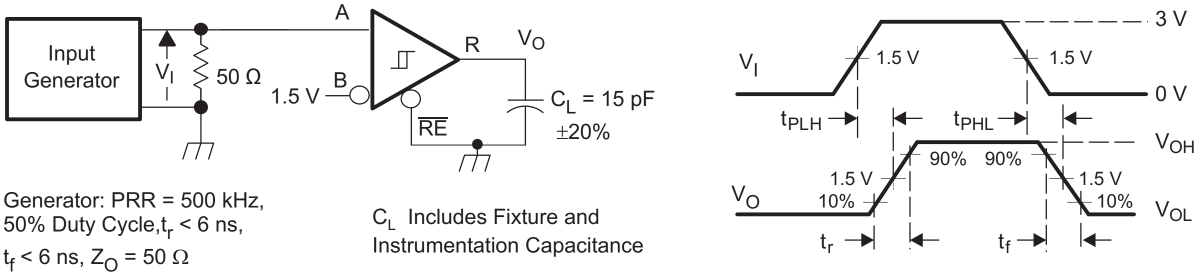


Figure 7. Receiver Voltage and Current Definitions



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

C_L Includes Fixture and Instrumentation Capacitance

Figure 8. Receiver Switching Test Circuit and Voltage Waveforms

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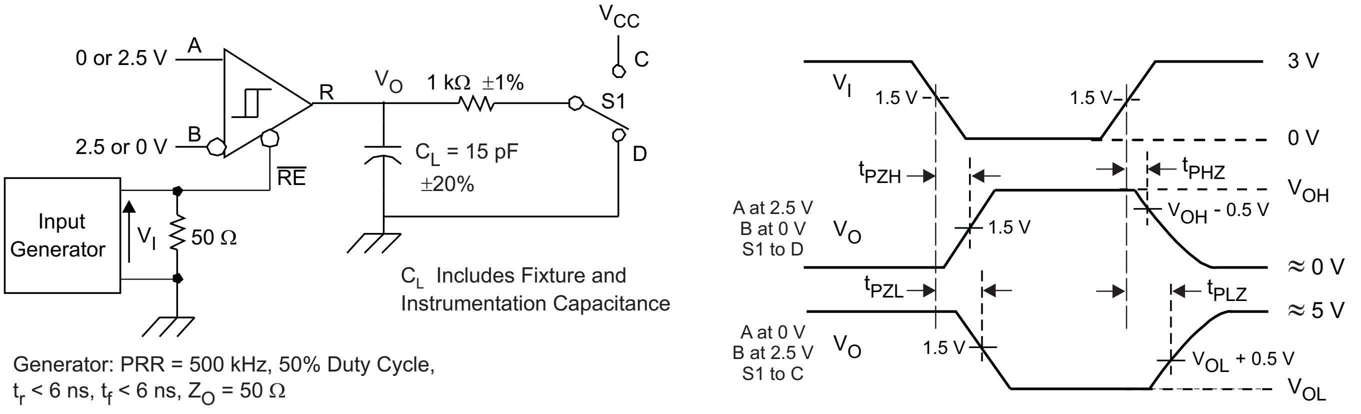
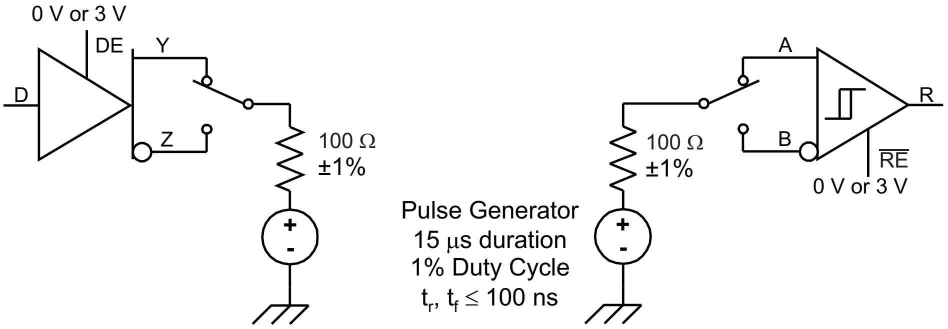
PARAMETER MEASUREMENT INFORMATION (continued)



Generator: PRR = 500 kHz, 50% Duty Cycle,
t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

Figure 9. Receiver Enable and Disable Test Circuit and Voltage Waveforms



Pulse Generator
15 µs duration
1% Duty Cycle
t_r, t_f ≤ 100 ns

A. This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 10. Transient Overvoltage Test Circuit

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DEVICE INFORMATION

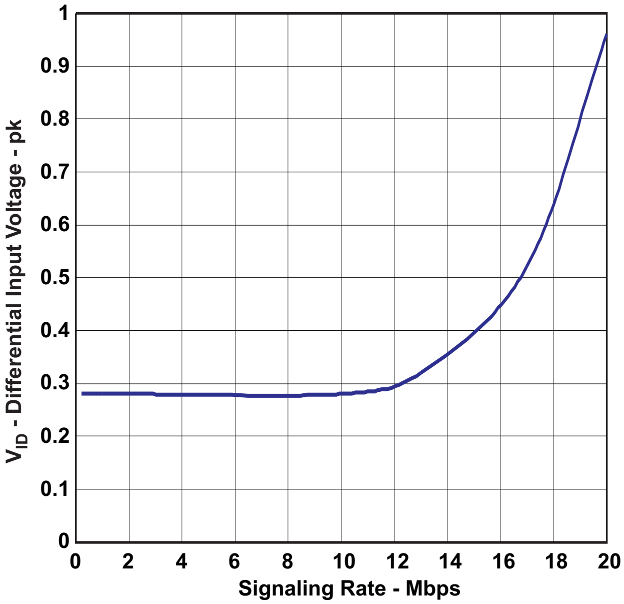

Figure 11. Recommended Minimum Differential Input Voltage vs Signaling Rate

FUNCTION TABLES

DRIVER(1)

INPUT	ENABLE	OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L or OPEN	Z	Z
Open	H	H	L

(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

RECEIVER(1)

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \leq -0.2$ V	L	L
-0.2 V $< V_{ID} < -0.01$ V	L	?
-0.01 V $\leq V_{ID}$	L	H
X	H or OPEN	Z
Open Circuit	L	H
BUS Idle	L	H
Short Circuit	L	H

(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

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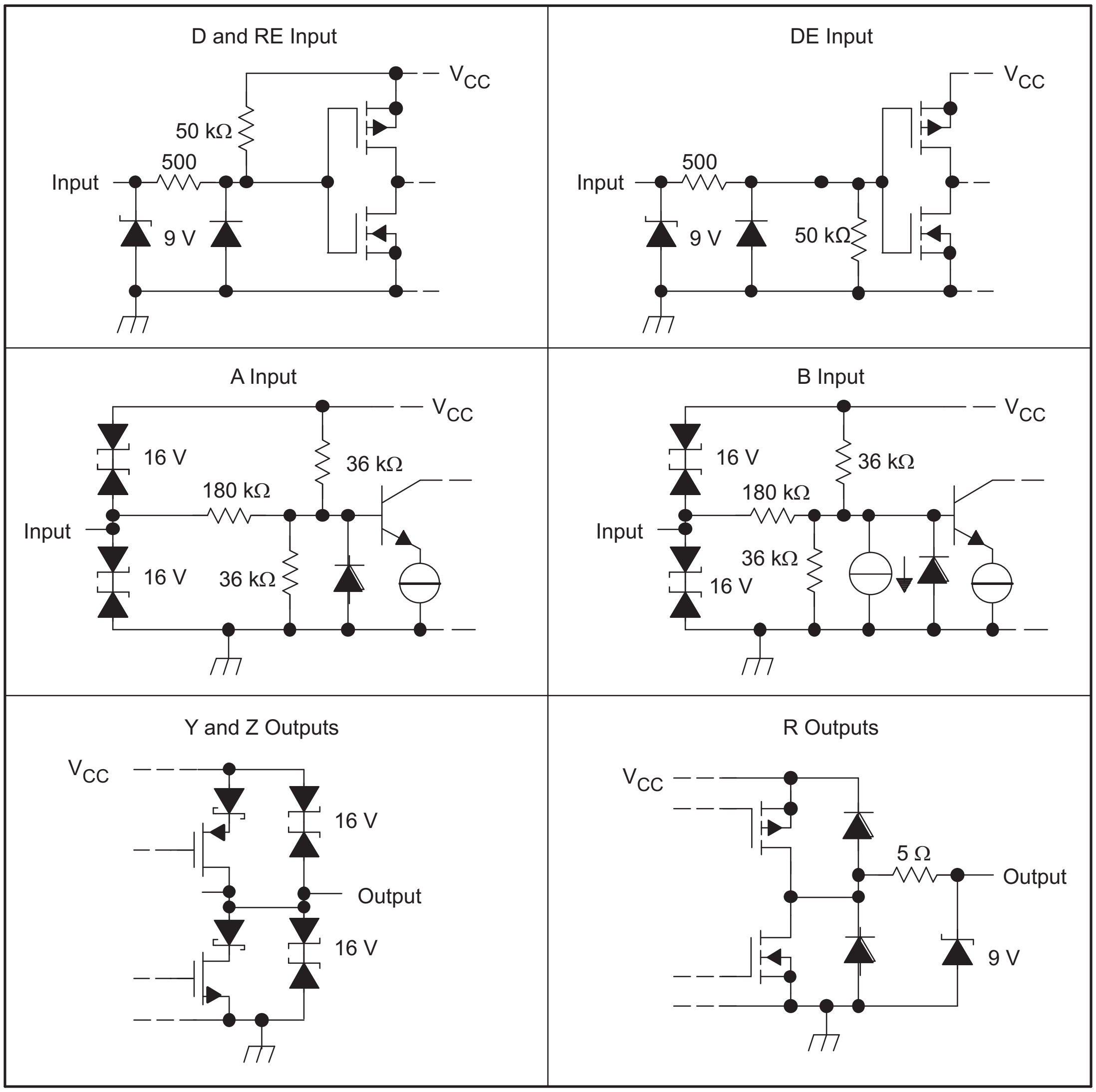
DEVICE ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

	PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{(AVG)}$	Average power dissipation	R_L = 60 Ω, Input to D a 500-kHz 50% duty cycle square-wave	85	109	136	mW

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



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TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
BUS INPUT VOLTAGE

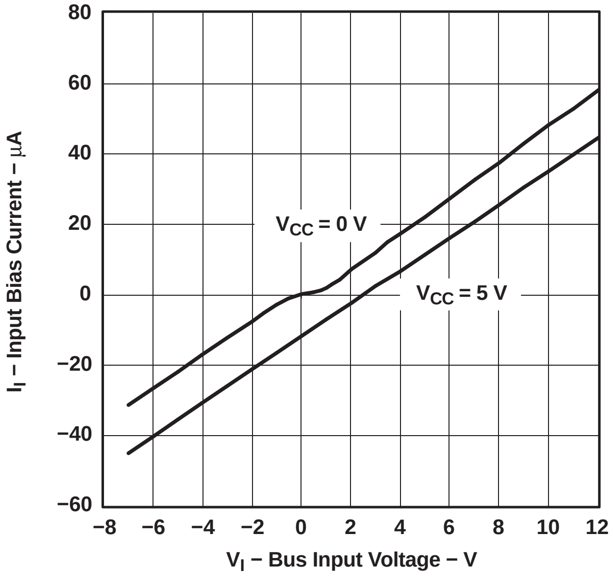

Figure 12.

HVD3080E
SUPPLY CURRENT
vs
SIGNALING RATE

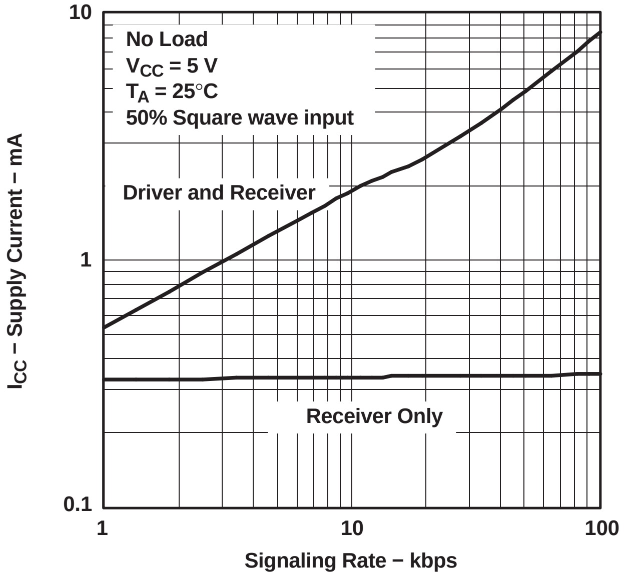

Figure 13.

HVD3083E
SUPPLY CURRENT
vs
SIGNALING RATE

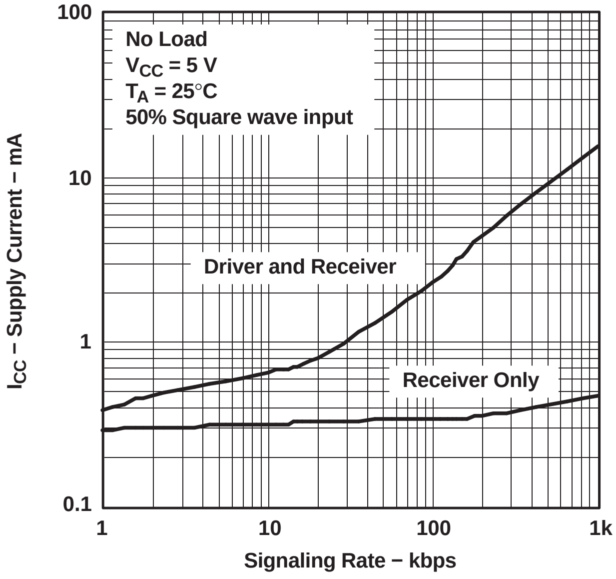

Figure 14.

HVD3086E
SUPPLY CURRENT
vs
SIGNALING RATE

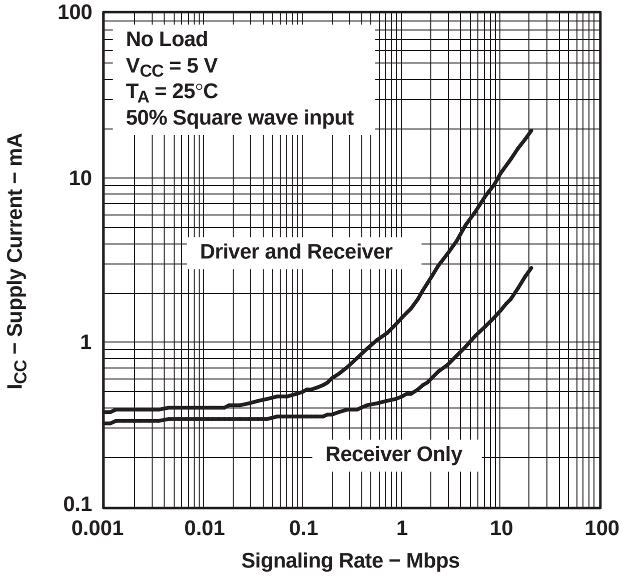

Figure 15.

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TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL OUTPUT VOLTAGE
vs
DIFFERENTIAL OUTPUT CURRENT

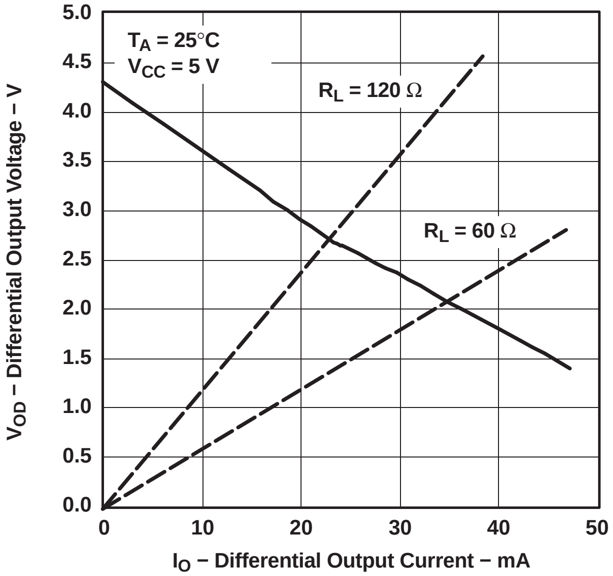

Figure 16.

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

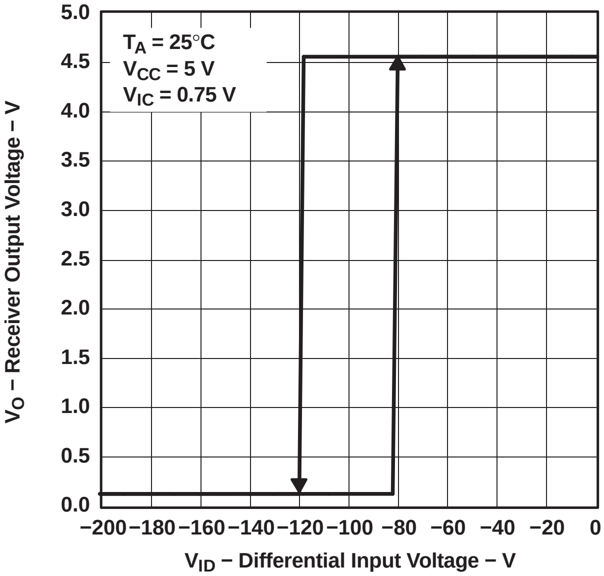

Figure 17.

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APPLICATION INFORMATION

Hot-Plugging

These devices are designed to operate in “hot swap” or “hot pluggable” applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. An internal Power-On Reset circuit keeps the outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in the device FUNCTION TABLES, the ENABLE inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

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REVISION HISTORY

Changes from Revision B (March 2007) to Revision C — Page

- Added D package ... 1
- Added D package and information to Ordering Information ... 2
- Added D package information to Power Dissipation Ratings ... 2
- Changed Electrostatic Discharge Protection ... 2
- Changed Supply Current information ... 3
- Changed Receiver Switching Characteristics ... 5
- Changed Figure 5 ... 7
- Changed Figure 6 ... 7

Changes from Revision C (December 2009) to Revision D — Page

- Added Differential input voltage dynamic to RECOMMENDED OPERATING CONDITIONS ... 3
- Added Figure 11 ... 9

Changes from Revision D (January 2011) to Revision E — Page

- Added Power-Up, Power-Down Glitch-Free Operation to FEATURES ... 1
- Changed ENABLE in DRIVER FUNCTION TABLE from L to L or OPEN ... 9
- Changed ENABLE in RECEIVER FUNCTION TABLE from H to H or OPEN ... 9
- Added APPLICATION INFORMATION section ... 13

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN65HVD3080EDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN65HVD3080EDGSG4	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN65HVD3080EDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN65HVD3080EDGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN65HVD3083EDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN65HVD3083EDGSG4	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN65HVD3083EDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN65HVD3083EDGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN65HVD3086ED	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3086EDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN65HVD3086EDGSG4	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN65HVD3086EDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN65HVD3086EDGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN65HVD3086EDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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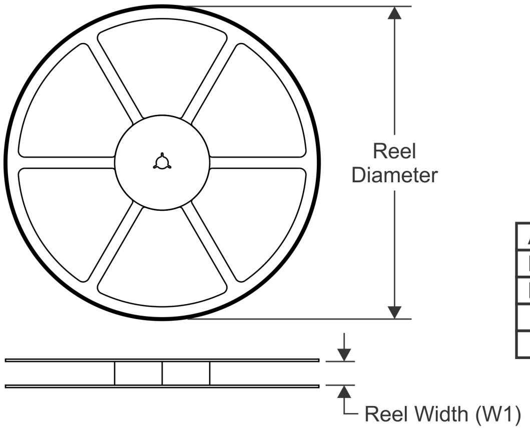
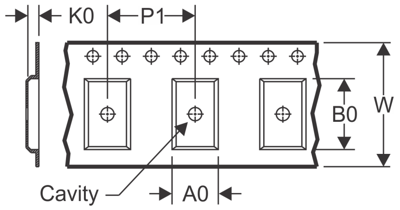
TAPE AND REEL INFORMATION

REEL DIMENSIONS

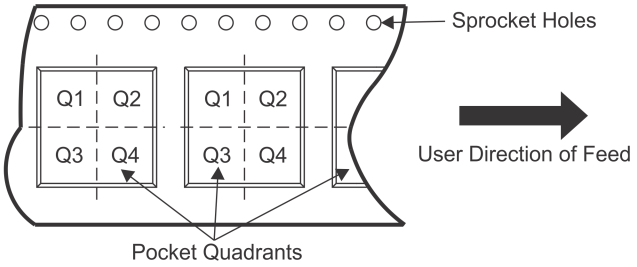


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

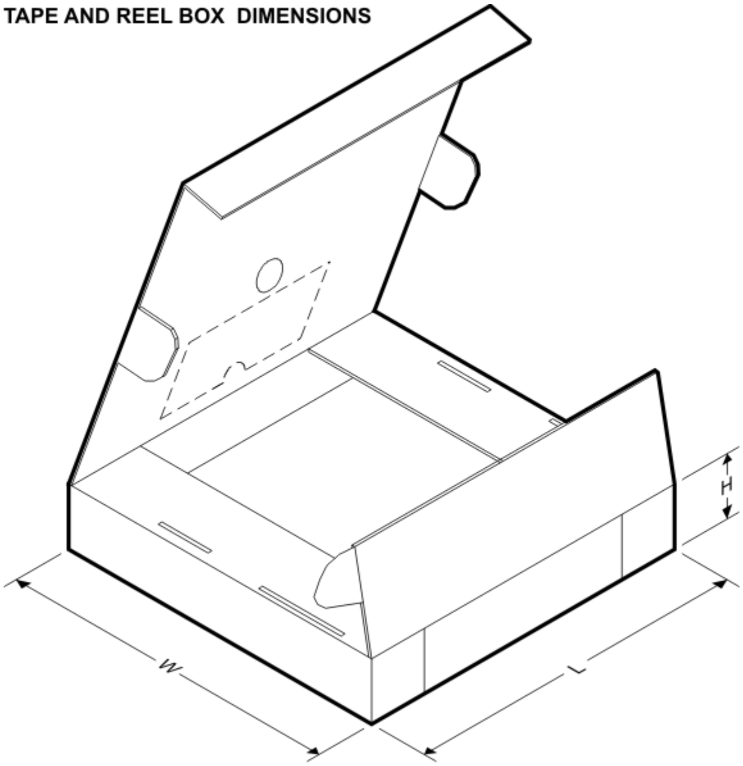
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD3080EDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD3083EDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD3086EDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD3086EDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

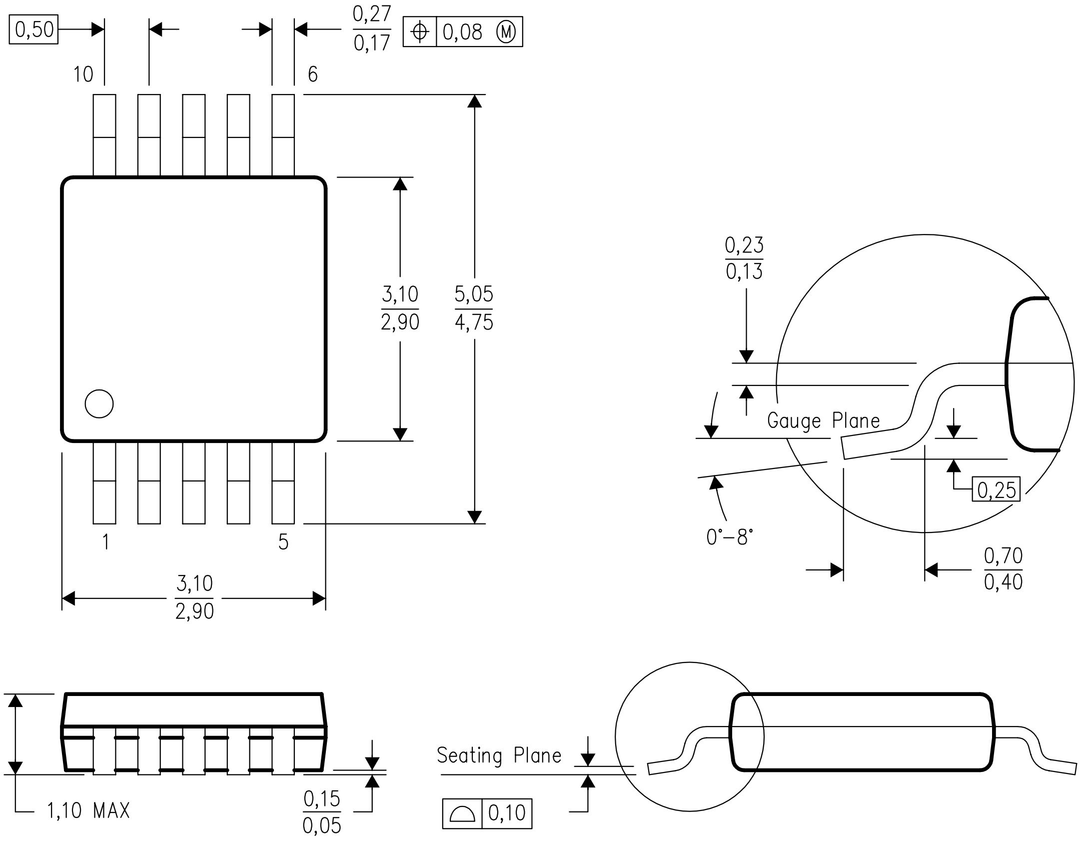
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD3080EDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
SN65HVD3083EDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
SN65HVD3086EDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
SN65HVD3086EDR	SOIC	D	14	2500	367.0	367.0	38.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



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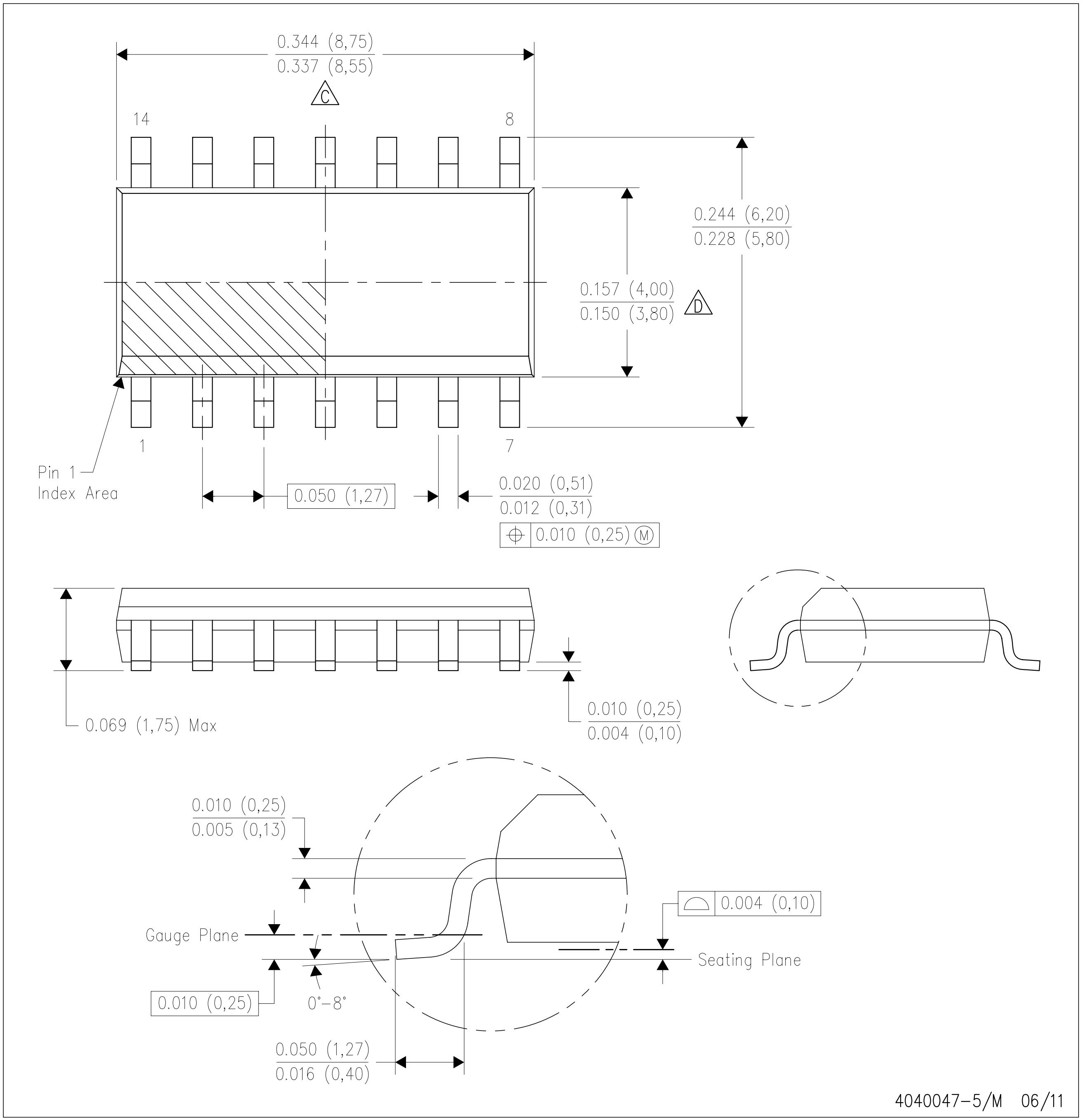
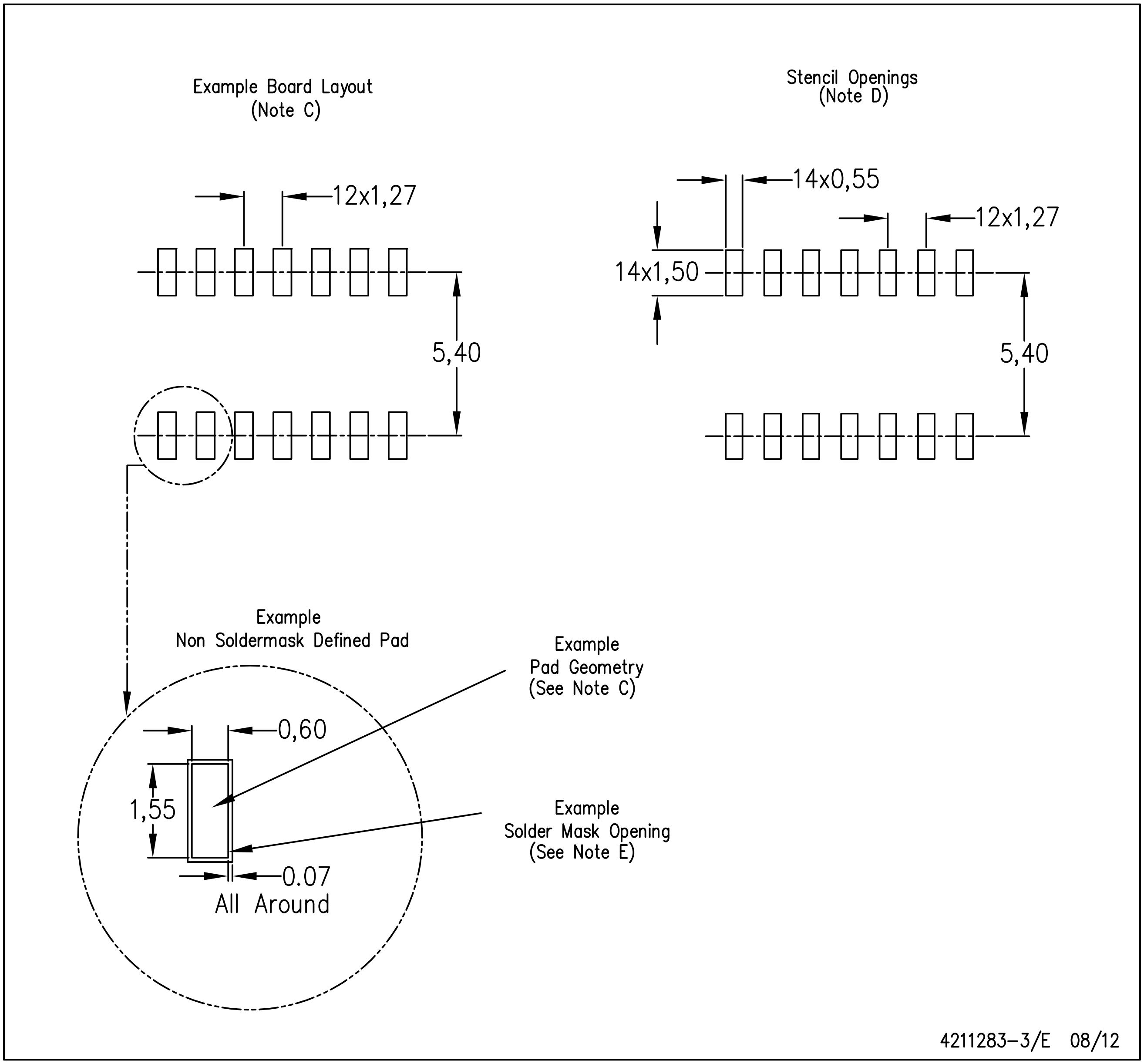
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO–187 variation BA.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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