

To all our customers

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## **Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.**

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The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.)

Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003



## Description

**Pin Configuration**

Figures 1.1 to 1.2 show the pin configurations (top view).

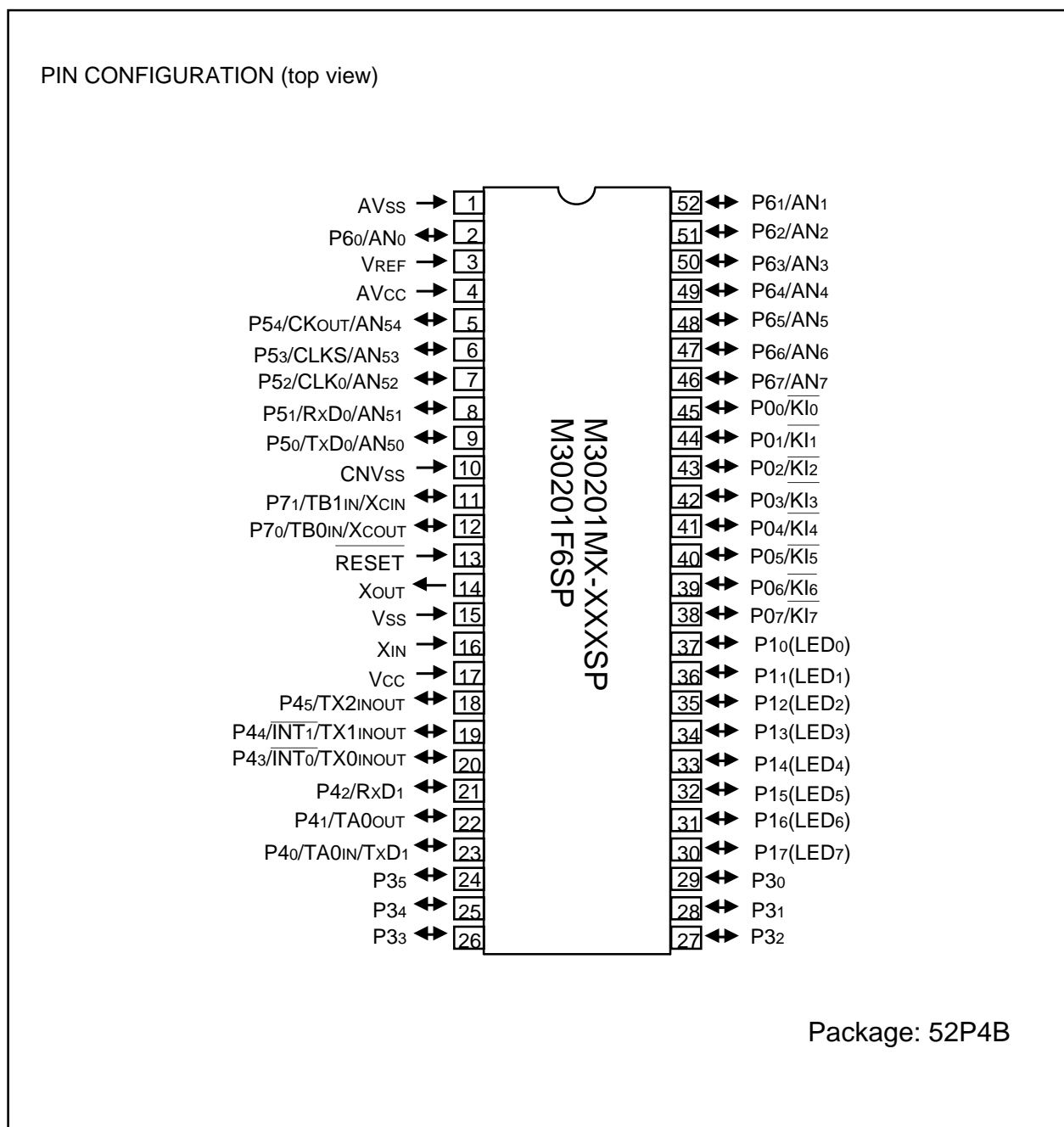


Figure 1.1. Pin configuration for the M30201 group (shrink DIP product) (top view)

## Description

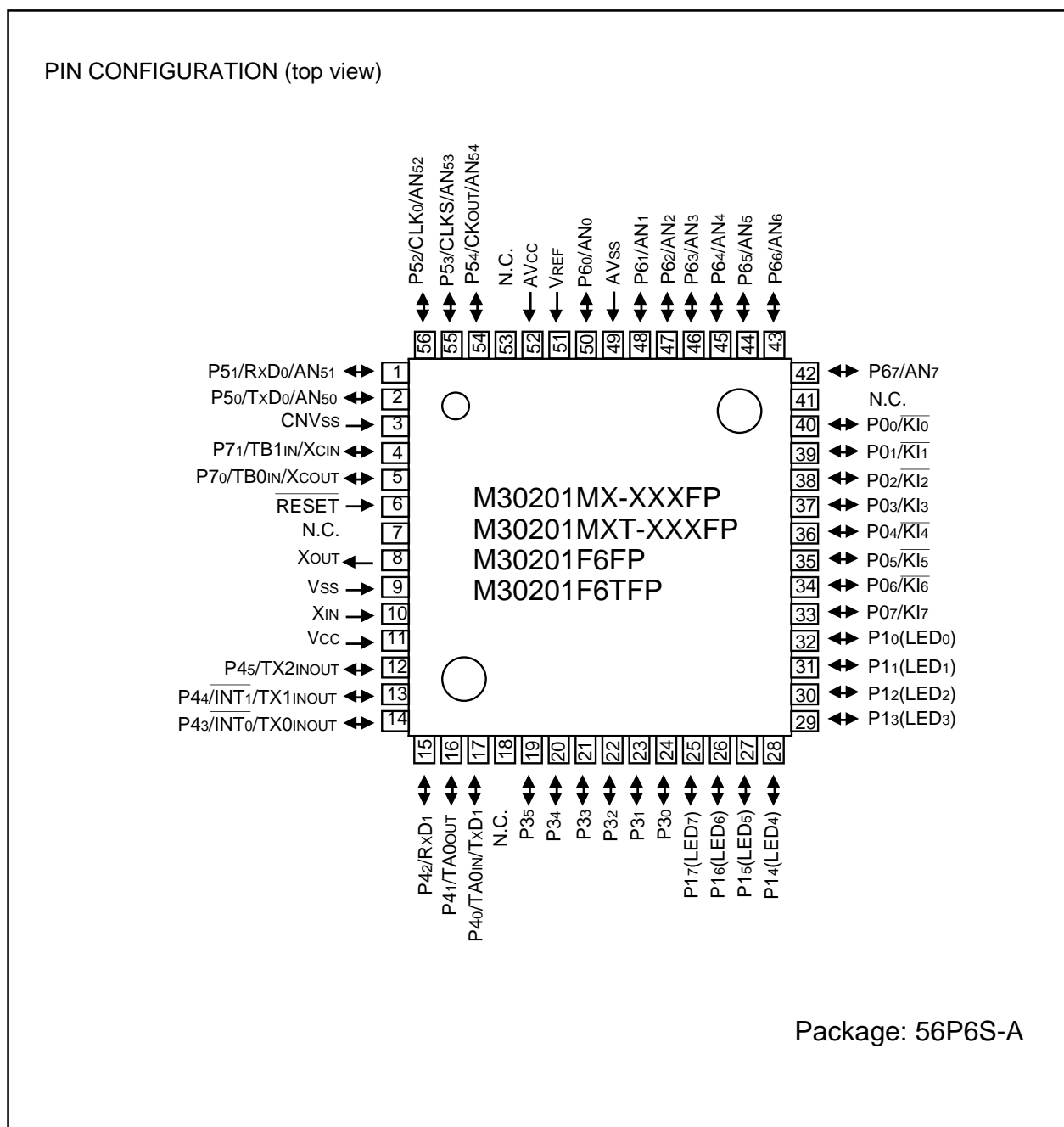
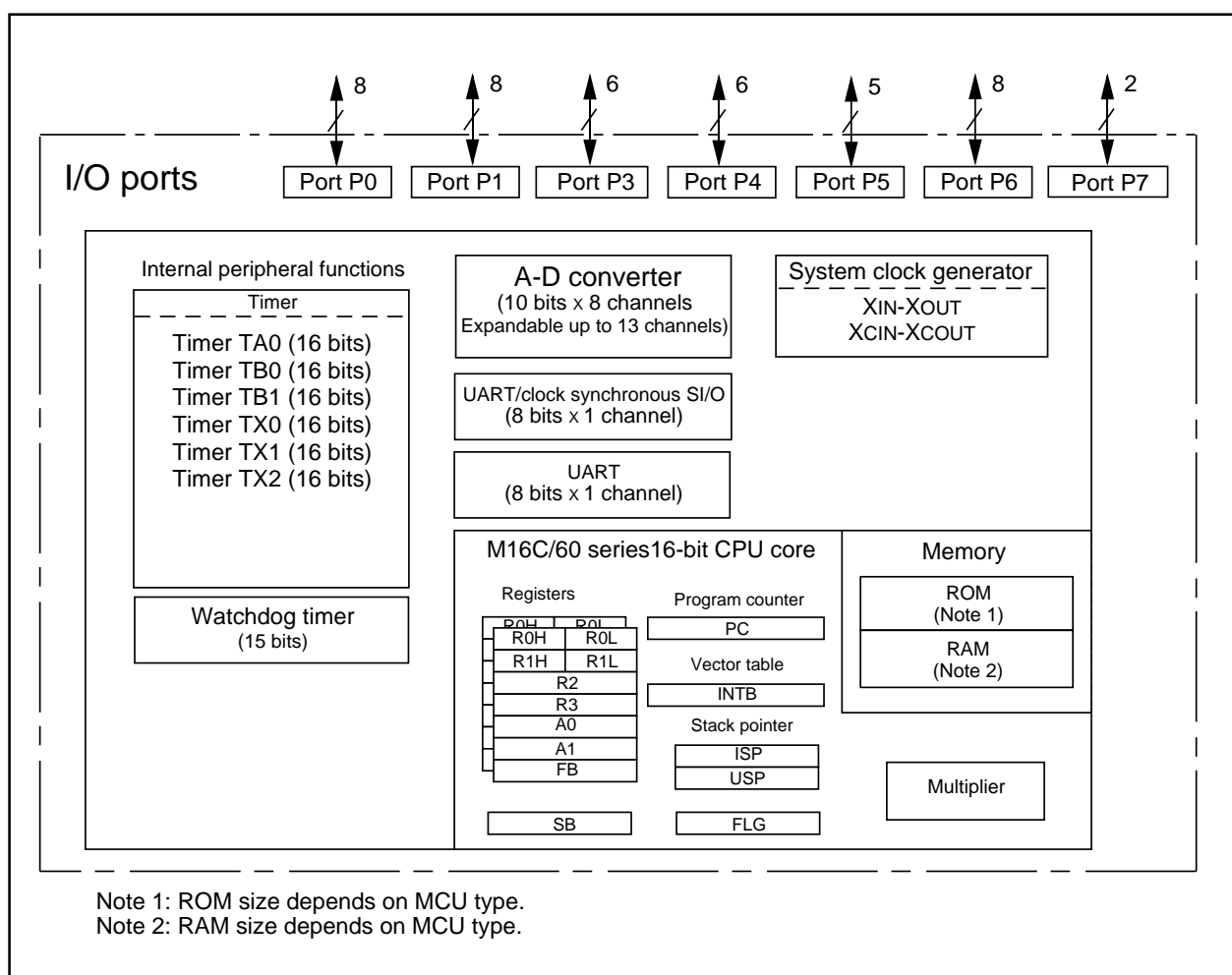


Figure 1.2. Pin configuration for the M30201 group (QFP product) (top view)

## Description

**Block Diagram**

Figure 1.3 is a block diagram of the M30201 group.



**Figure 1.3. Block diagram for the M30201 group**

## Description

### Performance Outline

Table 1.1 is performance outline of M30201 group.

**Table 1.1. Performance outline of M30201 group**

| Item                                |                       | Performance   |
|-------------------------------------|-----------------------|---|
| Number of basic instructions        |                       | 91 instructions   |
| Shortest instruction execution time |                       | 100ns (f(XIN)=10MHz)  |
| Memory capacity                     | ROM                   | (See figure 4. ROM expansion.)  |
|                                     | RAM                   | (See figure 4. ROM expansion.)  |
| I/O port                            | P0 to P7              | 43 lines  |
| Multifunction timer                 | TA0                   | 16 bits x 1   |
|                                     | TB0, TB1              | 16 bits x 2   |
|                                     | TX0, TX1, TX2         | 16 bits x 3   |
| Serial I/O                          | UART0                 | (UART or clock synchronous) x 1   |
|                                     | UART1                 | UART x 1  |
| A-D converter                       |                       | 10 bits x 8 channels (Expandable up to 13 channels)   |
| Watchdog timer                      |                       | 15 bits x 1 (with prescaler)  |
| Interrupt                           |                       | 13 internal and 3 external sources, 4 software sources  |
| Clock generating circuit            |                       | 2 built-in clock generation circuits<br>(built-in feedback resistor, and external ceramic or quartz oscillator)                                   |
| Supply voltage                      |                       | 4.0 to 5.5V (f(XIN)=10MHz) :mask ROM version<br>2.7 to 5.5V (f(XIN)=3.5MHz) :mask ROM version<br>4.0 to 5.5V (f(XIN)=10MHz) :flash memory version |
| Power consumption                   |                       | 11mW (f(XIN)=3.5MHz, Vcc=3V) :mask ROM version<br>95mW (f(XIN)=10MHz, Vcc=5V) :flash memory version   |
| I/O characteristics                 | I/O withstand voltage | 5V  |
|                                     | Output current        | 5mA (15mA:LED drive port)   |
| Device configuration                |                       | CMOS silicon gate   |
| Package                             |                       | 52-pin plastic mold SDIP<br>56-pin plastic mold QFP   |

## Description

Mitsubishi plans to release the following products in the M30201 group:

(1) Support for mask ROM version and flash memory version

(2) ROM capacity

(3) Package

52P4B : Plastic molded SDIP (mask ROM version and flash memory version)

56P6S-A : Plastic molded QFP (mask ROM version and flash memory version)

Apr. 2001

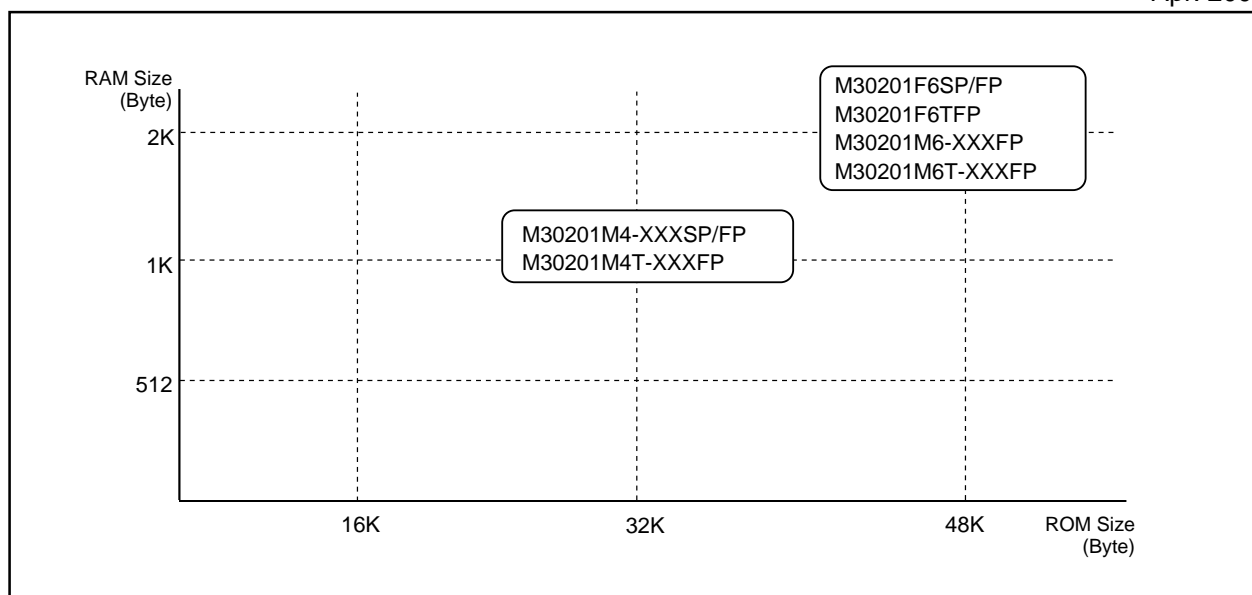


Figure 1.4. ROM expansion

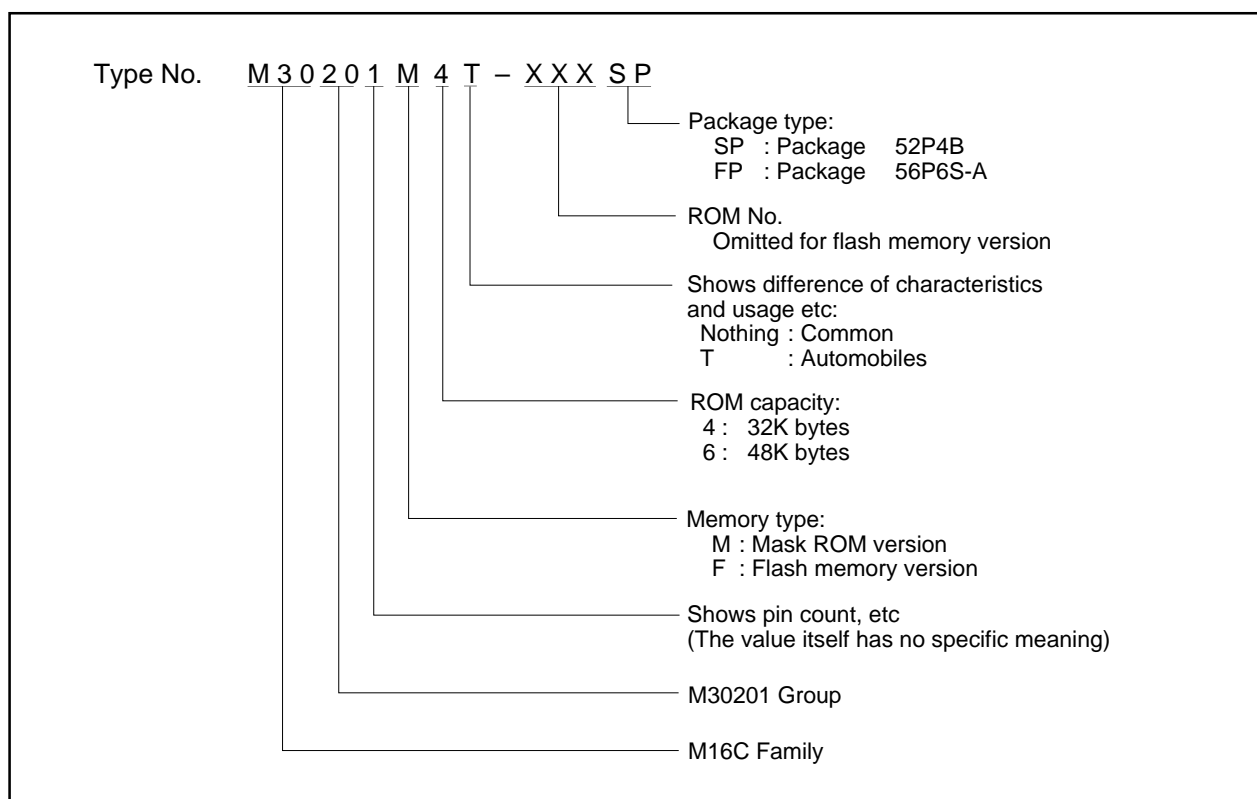


Figure 1.5. Type No., memory size, and package

## Pin Description

### Pin Description

| Pin name    | Signal name                 | I/O type        | Function  |
|-------------|-----------------------------|-----------------|---|
| Vcc, Vss    | Power supply input          |                 | Supply 2.7 to 5.5 V to the Vcc pin. Supply 0 V to the Vss pin.  |
| CNVss       | CNVss                       | Input           | Connect it to the Vss pin.  |
| RESET       | Reset input                 | Input           | A "L" on this input resets the microcomputer.   |
| XIN<br>XOUT | Clock input<br>Clock output | Input<br>Output | These pins are provided for the main clock generating circuit. Connect a ceramic resonator or crystal between the XIN and the XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.   |
| AVCC        | Analog power supply input   |                 | This pin is a power supply input for the A-D converter. Connect it to Vcc.  |
| AVss        | Analog power supply input   |                 | This pin is a power supply input for the A-D converter. Connect it to Vss.  |
| VREF        | Reference voltage input     | Input           | This pin is a reference voltage input for the A-D converter.  |
| P00 to P07  | I/O port P0                 | Input/output    | This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When set for input, the user can specify in units of four bits via software whether or not they are tied to a pull-up resistor.   |
| P10 to P17  | I/O port P1                 | Input/output    | This is an 8-bit I/O port equivalent to P0.   |
| P30 to P35  | I/O port P3                 | Input/output    | This is a 6-bit I/O port equivalent to P0.  |
| P40 to P45  | I/O port P4                 | Input/output    | This is a 6-bit I/O port equivalent to P0. The P40 pin is shared with timer A0 input and serial I/O output TxD1. The P41 pin is shared with timer A0 output. The P42 pin is shared with serial I/O input RxD1. The P43 pin is shared with external interrupt INT0 and timer X0 input/output TX0INOUT. The P44 pin is shared with external interrupt INT1 and timer X1 input/output TX1INOUT. The P45 pin is shared with timer X2 input/output TX2INOUT. |
| P50 to P54  | I/O port P5                 | Input/output    | This is a 5-bit I/O port equivalent to P0. The P50, P51, P52, and P53 pins are shared with serial I/O pins TxD0, RxD0, CLK0, and CLKS. The P54 pin is shared with clock output CLKOUT. Also, these pins are shared with analog input pins AN50 through AN54.  |
| P60 to P67  | I/O port P6                 | Input/output    | This is an 8-bit I/O port equivalent to P0. These pins are shared with analog input pins AN0 through AN7.   |
| P70 to P71  | I/O port P7                 | Input/output    | This is a 2-bit I/O port equivalent to P0. These pins are used for input/output to and from the oscillator circuit for the clock. Connect a crystal oscillator between the XCIN and the XOUT pins.  |



## Memory

### Operation of Functional Blocks

The M30201 accommodates certain units in a single chip. These units include ROM and RAM to store instructions and data and the central processing unit (CPU) to execute arithmetic/logic operations. Also included are peripheral units such as timers, serial I/O, A-D converter, and I/O ports.

The following explains each unit.

### Memory

Figure 1.6 is a memory map of the M30201. The address space extends the 1M bytes from address  $00000_{16}$  to  $FFFFFF_{16}$ . From  $FFFFFF_{16}$  down is ROM. For example, in the M30201M4-XXXSP, there is 32K bytes of internal ROM from  $F8000_{16}$  to  $FFFFFF_{16}$ . The vector table for fixed interrupts such as the reset are mapped to  $FFFDC_{16}$  to  $FFFFFF_{16}$ . The starting address of the interrupt routine is stored here. The address of the vector table for timer interrupts, etc., can be set as desired using the internal register (INTB). See the section on interrupts for details.

From  $00400_{16}$  up is RAM. For example, in the M30201M4-XXXSP, there is 1K byte of internal RAM from  $00400_{16}$  to  $007FF_{16}$ . In addition to storing data, the RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SFR area is mapped to  $00000_{16}$  to  $003FF_{16}$ . This area accommodates the control registers for peripheral devices such as I/O ports, A-D converter, serial I/O, and timers, etc. Any part of the SFR area that is not occupied is reserved and cannot be used for other purposes.

The special page vector table is mapped to  $FFE00_{16}$  to  $FFFD_{16}$ . If the starting addresses of subroutines or the destination addresses of jumps are stored here, subroutine call instructions and jump instructions can be used as 2-byte instructions, reducing the number of program steps.

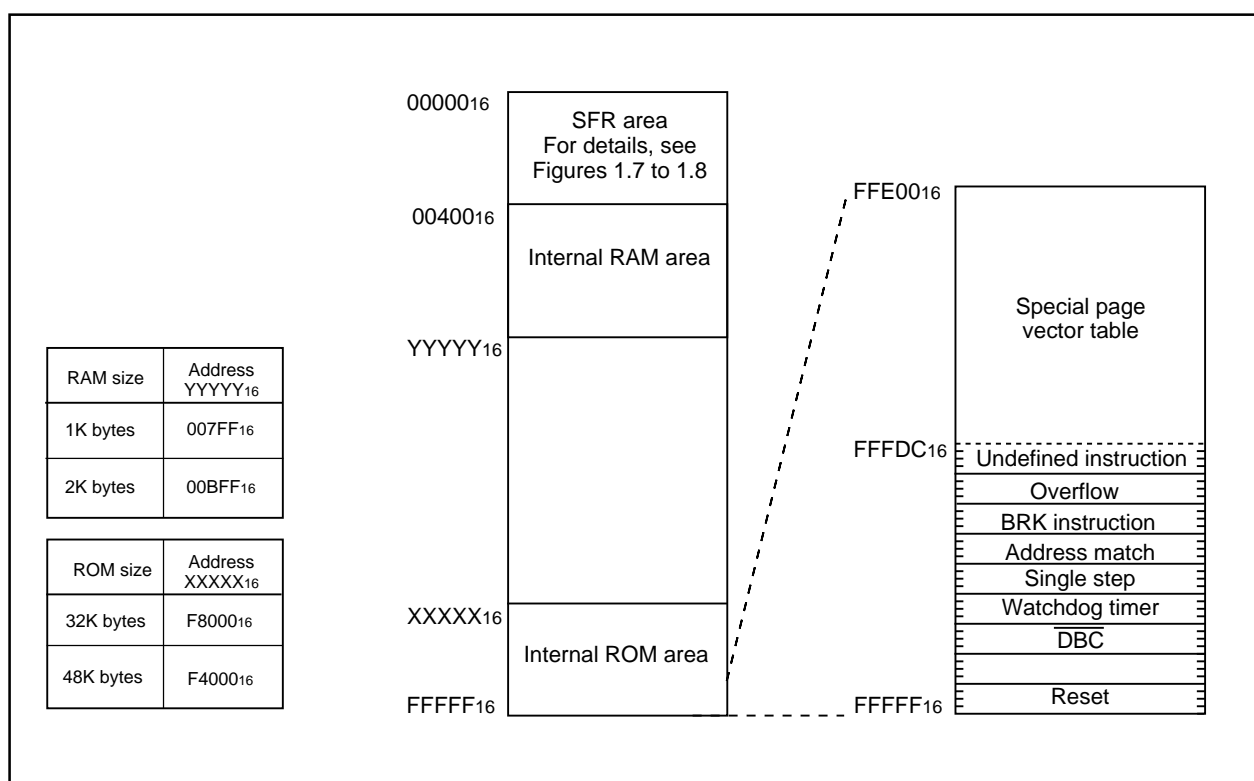


Figure 1.6. Memory map

## Memory

|                    |  |                    |   |
|--------------------|--|--------------------|---|
| 0000 <sub>16</sub> |  | 0040 <sub>16</sub> |   |
| 0001 <sub>16</sub> |  | 0041 <sub>16</sub> |   |
| 0002 <sub>16</sub> |  | 0042 <sub>16</sub> |   |
| 0003 <sub>16</sub> |  | 0043 <sub>16</sub> |   |
| 0004 <sub>16</sub> | Processor mode register 0 (PM0)                | 0044 <sub>16</sub> |   |
| 0005 <sub>16</sub> | Processor mode register 1 (PM1)                | 0045 <sub>16</sub> |   |
| 0006 <sub>16</sub> | System clock control register 0 (CM0)          | 0046 <sub>16</sub> |   |
| 0007 <sub>16</sub> | System clock control register 1 (CM1)          | 0047 <sub>16</sub> |   |
| 0008 <sub>16</sub> |  | 0048 <sub>16</sub> |   |
| 0009 <sub>16</sub> | Address match interrupt enable register (AIER) | 0049 <sub>16</sub> |   |
| 000A <sub>16</sub> | Protect register (PRCR)                        | 004A <sub>16</sub> |   |
| 000B <sub>16</sub> |  | 004B <sub>16</sub> |   |
| 000C <sub>16</sub> |  | 004C <sub>16</sub> |   |
| 000D <sub>16</sub> |  | 004D <sub>16</sub> | Key input interrupt control register (KUPIC)      |
| 000E <sub>16</sub> | Watchdog timer start register (WDTS)           | 004E <sub>16</sub> | A-D conversion interrupt control register (ADIC)  |
| 000F <sub>16</sub> | Watchdog timer control register (WDC)          | 004F <sub>16</sub> |   |
| 0010 <sub>16</sub> |  | 0050 <sub>16</sub> |   |
| 0011 <sub>16</sub> | Address match interrupt register 0 (RMAD0)     | 0051 <sub>16</sub> | UART0 transmit interrupt control register (S0TIC) |
| 0012 <sub>16</sub> |  | 0052 <sub>16</sub> | UART0 receive interrupt control register (S0RIC)  |
| 0013 <sub>16</sub> |  | 0053 <sub>16</sub> | UART1 transmit interrupt control register (S1TIC) |
| 0014 <sub>16</sub> |  | 0054 <sub>16</sub> | UART1 receive interrupt control register (S1RIC)  |
| 0015 <sub>16</sub> | Address match interrupt register 1 (RMAD1)     | 0055 <sub>16</sub> | Timer A0 interrupt control register (TA0IC)       |
| 0016 <sub>16</sub> |  | 0056 <sub>16</sub> | Timer X0 interrupt control register (TX0IC)       |
| 0017 <sub>16</sub> |  | 0057 <sub>16</sub> | Timer X1 interrupt control register (TX1IC)       |
| 0018 <sub>16</sub> |  | 0058 <sub>16</sub> | Timer X2 interrupt control register (TX2IC)       |
| 0019 <sub>16</sub> |  | 0059 <sub>16</sub> |   |
| 001A <sub>16</sub> |  | 005A <sub>16</sub> | Timer B0 interrupt control register (TB0IC)       |
| 001B <sub>16</sub> |  | 005B <sub>16</sub> | Timer B1 interrupt control register (TB1IC)       |
| 001C <sub>16</sub> |  | 005C <sub>16</sub> |   |
| 001D <sub>16</sub> |  | 005D <sub>16</sub> | INT0 interrupt control register (INT0IC)          |
| 001E <sub>16</sub> |  | 005E <sub>16</sub> | INT1 interrupt control register (INT1IC)          |
| 001F <sub>16</sub> |  | 005F <sub>16</sub> |   |
| 0020 <sub>16</sub> |  |                    |   |
| 0021 <sub>16</sub> |  |                    |   |
| 0022 <sub>16</sub> |  |                    |   |
| 0023 <sub>16</sub> |  |                    |   |
| 0024 <sub>16</sub> |  |                    |   |
| 0025 <sub>16</sub> |  |                    |   |
| 0026 <sub>16</sub> |  |                    |   |
| 0027 <sub>16</sub> |  |                    |   |
| 0028 <sub>16</sub> |  |                    |   |
| 0029 <sub>16</sub> |  |                    |   |
| 002A <sub>16</sub> |  |                    |   |
| 002B <sub>16</sub> |  |                    |   |
| 002C <sub>16</sub> |  |                    |   |
| 002D <sub>16</sub> |  |                    |   |
| 002E <sub>16</sub> |  |                    |   |
| 002F <sub>16</sub> |  |                    |   |
| 0030 <sub>16</sub> |  |                    |   |
| 0031 <sub>16</sub> |  |                    |   |
| 0032 <sub>16</sub> |  |                    |   |
| 0033 <sub>16</sub> |  |                    |   |
| 0034 <sub>16</sub> |  |                    |   |
| 0035 <sub>16</sub> |  |                    |   |
| 0036 <sub>16</sub> |  |                    |   |
| 0037 <sub>16</sub> |  |                    |   |
| 0038 <sub>16</sub> |  |                    |   |
| 0039 <sub>16</sub> |  |                    |   |
| 003A <sub>16</sub> |  |                    |   |
| 003B <sub>16</sub> |  |                    |   |
| 003C <sub>16</sub> |  |                    |   |
| 003D <sub>16</sub> |  |                    |   |
| 003E <sub>16</sub> |  |                    |   |
| 003F <sub>16</sub> |  |                    |   |

Note: Locations in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

Figure 1.7. Location of peripheral unit control registers (1)

## Memory

|                    |  |                    |   |
|--------------------|--|--------------------|---|
| 0380 <sub>16</sub> | Count start flag (TABSR)                         | 03C0 <sub>16</sub> | A-D register 0 (AD0)                        |
| 0381 <sub>16</sub> | Clock prescaler reset flag (CPSRF)               | 03C1 <sub>16</sub> |   |
| 0382 <sub>16</sub> | One-shot start flag (ONSF)                       | 03C2 <sub>16</sub> | A-D register 1 (AD1)                        |
| 0383 <sub>16</sub> | Trigger select register (TRGSR)                  | 03C3 <sub>16</sub> |   |
| 0384 <sub>16</sub> | Up-down flag (UDF)                               | 03C4 <sub>16</sub> | A-D register 2 (AD2)                        |
| 0385 <sub>16</sub> |  | 03C5 <sub>16</sub> |   |
| 0386 <sub>16</sub> | Timer A0 (TA0)                                   | 03C6 <sub>16</sub> | A-D register 3 (AD3)                        |
| 0387 <sub>16</sub> |  | 03C7 <sub>16</sub> |   |
| 0388 <sub>16</sub> | Timer X0 (TX0)                                   | 03C8 <sub>16</sub> | A-D register 4 (AD4)                        |
| 0389 <sub>16</sub> |  | 03C9 <sub>16</sub> |   |
| 038A <sub>16</sub> | Timer X1 (TX1)                                   | 03CA <sub>16</sub> | A-D register 5 (AD5)                        |
| 038B <sub>16</sub> |  | 03CB <sub>16</sub> |   |
| 038C <sub>16</sub> | Timer X2 (TX2)                                   | 03CC <sub>16</sub> | A-D register 6 (AD6)                        |
| 038D <sub>16</sub> |  | 03CD <sub>16</sub> |   |
| 038E <sub>16</sub> | Clock divided counter (CDC)                      | 03CE <sub>16</sub> | A-D register 7 (AD7)                        |
| 038F <sub>16</sub> |  | 03CF <sub>16</sub> |   |
| 0390 <sub>16</sub> | Timer B0 (TB0)                                   | 03D0 <sub>16</sub> |   |
| 0391 <sub>16</sub> |  | 03D1 <sub>16</sub> |   |
| 0392 <sub>16</sub> | Timer B1 (TB1)                                   | 03D2 <sub>16</sub> |   |
| 0393 <sub>16</sub> |  | 03D3 <sub>16</sub> |   |
| 0394 <sub>16</sub> |  | 03D4 <sub>16</sub> | A-D control register 2 (ADCON2)             |
| 0395 <sub>16</sub> |  | 03D5 <sub>16</sub> |   |
| 0396 <sub>16</sub> | Timer A0 mode register (TA0MR)                   | 03D6 <sub>16</sub> | A-D control register 0 (ADCON0)             |
| 0397 <sub>16</sub> | Timer X0 mode register (TX0MR)                   | 03D7 <sub>16</sub> | A-D control register 1 (ADCON1)             |
| 0398 <sub>16</sub> | Timer X1 mode register (TX1MR)                   | 03D8 <sub>16</sub> |   |
| 0399 <sub>16</sub> | Timer X2 mode register (TX2MR)                   | 03D9 <sub>16</sub> |   |
| 039A <sub>16</sub> |  | 03DA <sub>16</sub> |   |
| 039B <sub>16</sub> | Timer B0 mode register (TB0MR)                   | 03DB <sub>16</sub> |   |
| 039C <sub>16</sub> | Timer B1 mode register (TB1MR)                   | 03DC <sub>16</sub> |   |
| 039D <sub>16</sub> |  | 03DD <sub>16</sub> |   |
| 039E <sub>16</sub> |  | 03DE <sub>16</sub> |   |
| 039F <sub>16</sub> |  | 03DF <sub>16</sub> |   |
| 03A0 <sub>16</sub> | UART0 transmit/receive mode register (U0MR)      | 03E0 <sub>16</sub> | Port P0 (P0)                                |
| 03A1 <sub>16</sub> | UART0 bit rate generator (U0BRG)                 | 03E1 <sub>16</sub> | Port P1 (P1)                                |
| 03A2 <sub>16</sub> | UART0 transmit buffer register (U0TB)            | 03E2 <sub>16</sub> | Port P0 direction register (PD0)            |
| 03A3 <sub>16</sub> |  | 03E3 <sub>16</sub> | Port P1 direction register (PD1)            |
| 03A4 <sub>16</sub> | UART0 transmit/receive control register 0 (U0C0) | 03E4 <sub>16</sub> | Port P2 (P2) (Reserved)                     |
| 03A5 <sub>16</sub> | UART0 transmit/receive control register 1 (U0C1) | 03E5 <sub>16</sub> | Port P3 (P3)                                |
| 03A6 <sub>16</sub> | UART0 receive buffer register (U0RB)             | 03E6 <sub>16</sub> | Port P2 direction register (PD2) (Reserved) |
| 03A7 <sub>16</sub> |  | 03E7 <sub>16</sub> | Port P3 direction register (PD3)            |
| 03A8 <sub>16</sub> | UART1 transmit/receive mode register (U1MR)      | 03E8 <sub>16</sub> | Port P4 (P4)                                |
| 03A9 <sub>16</sub> | UART1 bit rate generator (U1BRG)                 | 03E9 <sub>16</sub> | Port P5 (P5)                                |
| 03AA <sub>16</sub> | UART1 transmit buffer register (U1TB)            | 03EA <sub>16</sub> | Port P4 direction register (PD4)            |
| 03AB <sub>16</sub> |  | 03EB <sub>16</sub> | Port P5 direction register (PD5)            |
| 03AC <sub>16</sub> | UART1 transmit/receive control register 0 (U1C0) | 03EC <sub>16</sub> | Port P6 (P6)                                |
| 03AD <sub>16</sub> | UART1 transmit/receive control register 1 (U1C1) | 03ED <sub>16</sub> | Port P7 (P7)                                |
| 03AE <sub>16</sub> | UART1 receive buffer register (U1RB)             | 03EE <sub>16</sub> | Port P6 direction register (PD6)            |
| 03AF <sub>16</sub> |  | 03EF <sub>16</sub> | Port P7 direction register (PD7)            |
| 03B0 <sub>16</sub> | UART transmit/receive control register 2 (UCON)  | 03F0 <sub>16</sub> |   |
| 03B1 <sub>16</sub> |  | 03F1 <sub>16</sub> |   |
| 03B2 <sub>16</sub> |  | 03F2 <sub>16</sub> |   |
| 03B3 <sub>16</sub> |  | 03F3 <sub>16</sub> |   |
| 03B4 <sub>16</sub> | Flash memory control register 0 (FCON0) (Note1)  | 03F4 <sub>16</sub> |   |
| 03B5 <sub>16</sub> | Flash memory control register 1 (FCON1) (Note1)  | 03F5 <sub>16</sub> |   |
| 03B6 <sub>16</sub> | Flash command register (FCMD) (Note)             | 03F6 <sub>16</sub> |   |
| 03B7 <sub>16</sub> |  | 03F7 <sub>16</sub> |   |
| 03B8 <sub>16</sub> |  | 03F8 <sub>16</sub> |   |
| 03B9 <sub>16</sub> |  | 03F9 <sub>16</sub> |   |
| 03BA <sub>16</sub> |  | 03FA <sub>16</sub> |   |
| 03BB <sub>16</sub> |  | 03FB <sub>16</sub> |   |
| 03BC <sub>16</sub> |  | 03FC <sub>16</sub> | Pull-up control register 0 (PUR0)           |
| 03BD <sub>16</sub> |  | 03FD <sub>16</sub> | Pull-up control register 1 (PUR1)           |
| 03BE <sub>16</sub> |  | 03FE <sub>16</sub> | Port P1 drive control register (DRR)        |
| 03BF <sub>16</sub> |  | 03FF <sub>16</sub> |   |

Note 1: This register is only exist in flash memory version.  
Note 2: Locations in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

Figure 1.8. Location of peripheral unit control registers (2)

## CPU

## Central Processing Unit (CPU)

The CPU has a total of 13 registers shown in Figure 1.9. Seven of these registers (R0, R1, R2, R3, A0, A1, and FB) come in two sets; therefore, these have two register banks.

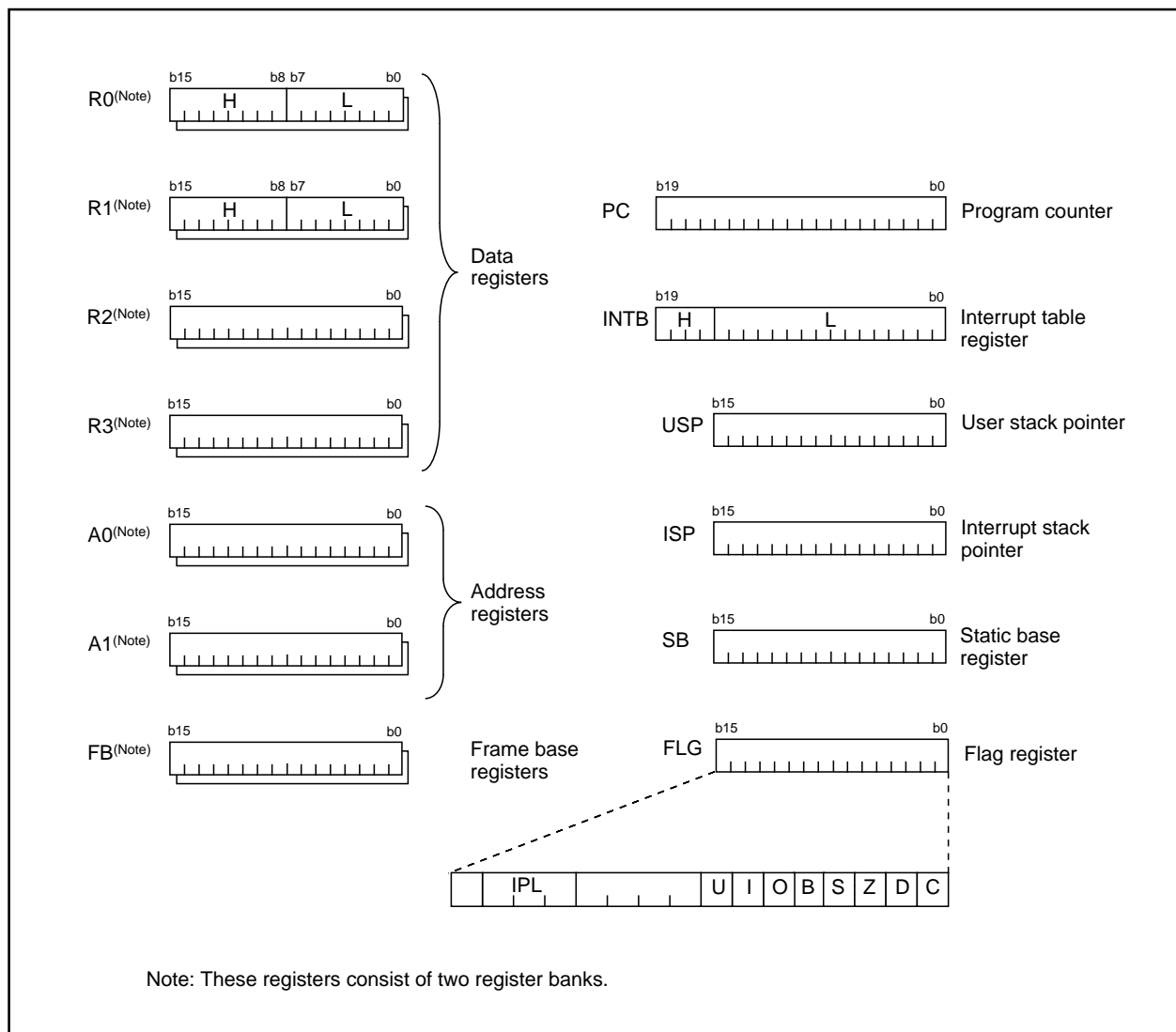


Figure 1.9. Central processing unit register

### (1) Data registers (R0, R0H, R0L, R1, R1H, R1L, R2, and R3)

Data registers (R0, R1, R2, and R3) are configured with 16 bits, and are used primarily for transfer and arithmetic/logic operations.

Registers R0 and R1 each can be used as separate 8-bit data registers, high-order bits as (R0H, R1H), and low-order bits as (R0L, R1L). In some instructions, registers R2 and R0, as well as R3 and R1 can use as 32-bit data registers (R2R0, R3R1).

### (2) Address registers (A0 and A1)

Address registers (A0 and A1) are configured with 16 bits, and have functions equivalent to those of data registers. These registers can also be used for address register indirect addressing and address register relative addressing.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

**(3) Frame base register (FB)**

Frame base register (FB) is configured with 16 bits, and is used for FB relative addressing.

**(4) Program counter (PC)**

Program counter (PC) is configured with 20 bits, indicating the address of an instruction to be executed.

**(5) Interrupt table register (INTB)**

Interrupt table register (INTB) is configured with 20 bits, indicating the start address of an interrupt vector table.

**(6) Stack pointer (USP/ISP)**

Stack pointer comes in two types: user stack pointer (USP) and interrupt stack pointer (ISP), each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by a stack pointer select flag (U flag).

This flag is located at the position of bit 7 in the flag register (FLG).

**(7) Static base register (SB)**

Static base register (SB) is configured with 16 bits, and is used for SB relative addressing.

**(8) Flag register (FLG)**

Flag register (FLG) is configured with 11 bits, each bit is used as a flag. Figure 1.10 shows the flag register (FLG). The following explains the function of each flag:

- **Bit 0: Carry flag (C flag)**

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

- **Bit 1: Debug flag (D flag)**

This flag enables a single-step interrupt.

When this flag is "1", a single-step interrupt is generated after instruction execution. This flag is cleared to "0" when the interrupt is acknowledged.

- **Bit 2: Zero flag (Z flag)**

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, cleared to "0".

- **Bit 3: Sign flag (S flag)**

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, cleared to "0".

- **Bit 4: Register bank select flag (B flag)**

This flag chooses a register bank. Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

- **Bit 5: Overflow flag (O flag)**

This flag is set to "1" when an arithmetic operation resulted in overflow; otherwise, cleared to "0".

- **Bit 6: Interrupt enable flag (I flag)**

This flag enables a maskable interrupt.

An interrupt is disabled when this flag is "0", and is enabled when this flag is "1". This flag is cleared to "0" when the interrupt is acknowledged.

- **Bit 7: Stack pointer select flag (U flag)**

Interrupt stack pointer (ISP) is selected when this flag is “0” ; user stack pointer (USP) is selected when this flag is “1”.

This flag is cleared to “0” when a hardware interrupt is acknowledged or an INT instruction of software interrupt Nos. 0 to 31 is executed.

- **Bits 8 to 11: Reserved area**

- **Bits 12 to 14: Processor interrupt priority level (IPL)**

Processor interrupt priority level (IPL) is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than the processor interrupt priority level (IPL), the interrupt is enabled.

- **Bit 15: Reserved area**

The C, Z, S, and O flags are changed when instructions are executed. See the software manual for details.

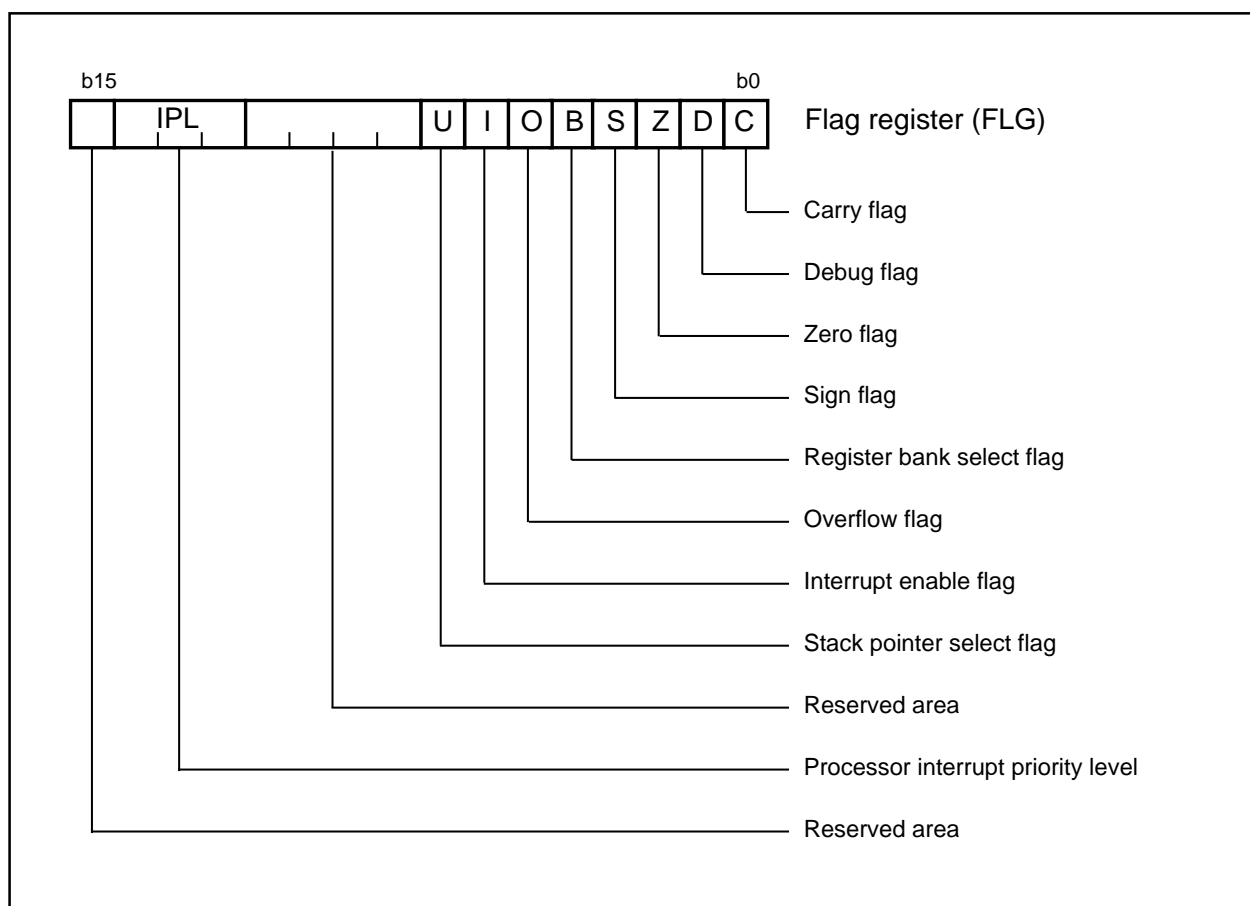


Figure 1.10. Flag register (FLG)

## Reset

### Reset

There are two kinds of resets; hardware and software. In both cases, operation is the same after the reset. (See "Software Reset" for details of software resets.) This section explains on hardware resets.

When the supply voltage is in the range where operation is guaranteed, a reset is effected by holding the reset pin level "L" (0.2V<sub>CC</sub> max.) for at least 20 cycles. When the reset pin level is then returned to the "H" level while main clock is stable, the reset status is cancelled and program execution resumes from the address in the reset vector table.

Figure 1.11 shows the example reset circuit. Figure 1.12 shows the reset sequence.

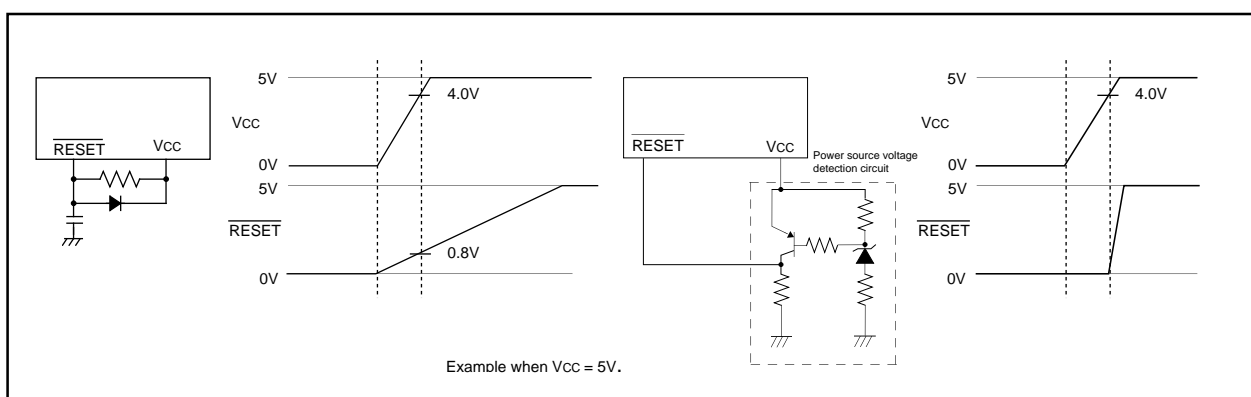


Figure 1.11. Example reset circuit

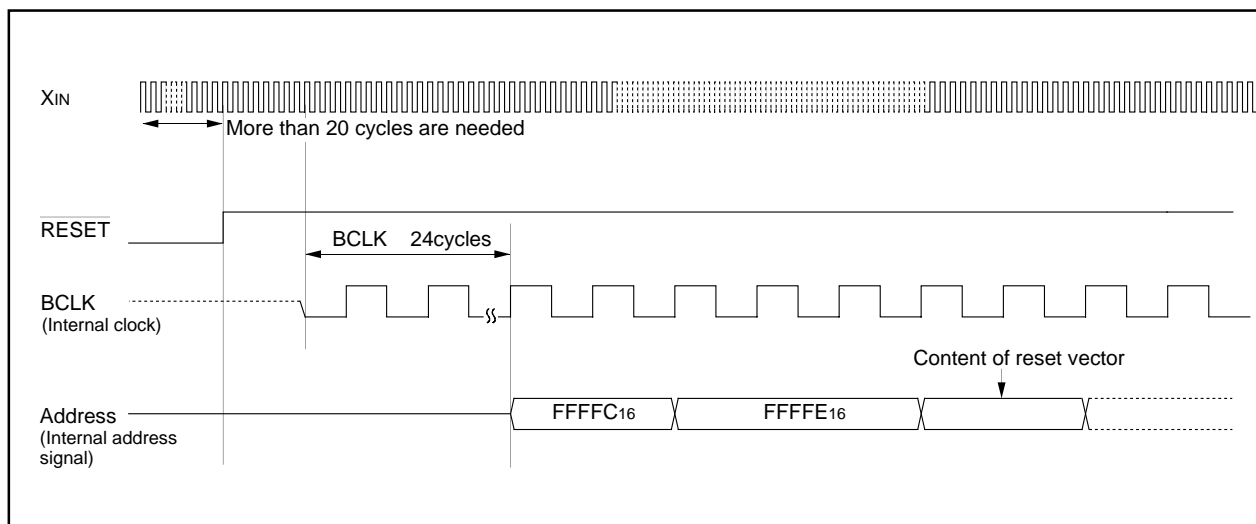


Figure 1.12. Reset sequence

## Reset

|  |                          |  |  |                          |  |
|--|--------------------------|--|--|--------------------------|--|
| (1) Processor mode register 0                  | (0004 <sub>16</sub> )... |  | (33) Timer B0 mode register                    | (039B <sub>16</sub> )... |  |
| (2) Processor mode register 1                  | (0005 <sub>16</sub> )... |  | (34) Timer B1 mode register                    | (039C <sub>16</sub> )... |  |
| (3) System clock control register 0            | (0006 <sub>16</sub> )... |  | (35) UART0 transmit/receive mode register      | (03A0 <sub>16</sub> )... |  |
| (4) System clock control register 1            | (0007 <sub>16</sub> )... |  | (36) UART0 transmit/receive control register 0 | (03A4 <sub>16</sub> )... |  |
| (5) Address match interrupt enable register    | (0009 <sub>16</sub> )... |  | (37) UART0 transmit/receive control register 1 | (03A5 <sub>16</sub> )... |  |
| (6) Protect register                           | (000A <sub>16</sub> )... |  | (38) UART1 transmit/receive mode register      | (03A8 <sub>16</sub> )... |  |
| (7) Watchdog timer control register            | (000F <sub>16</sub> )... |  | (39) UART1 transmit/receive control register 0 | (03AC <sub>16</sub> )... |  |
| (8) Address match interrupt register 0         | (0010 <sub>16</sub> )... |  | (40) UART1 transmit/receive control register 1 | (03AD <sub>16</sub> )... |  |
|  | (0011 <sub>16</sub> )... |  | (41) UART transmit/receive control register 2  | (03B0 <sub>16</sub> )... |  |
|  | (0012 <sub>16</sub> )... |  | (42) Flash memory control register 0 (Note)    | (03B4 <sub>16</sub> )... |  |
| (9) Address match interrupt register 1         | (0014 <sub>16</sub> )... |  | (43) Flash memory control register 1 (Note)    | (03B5 <sub>16</sub> )... |  |
|  | (0015 <sub>16</sub> )... |  | (44) Flash command register                    | (03B6 <sub>16</sub> )... |  |
|  | (0016 <sub>16</sub> )... |  | (45) A-D control register 2                    | (03D4 <sub>16</sub> )... |  |
| (10) Key input interrupt control register      | (004D <sub>16</sub> )... |  | (46) A-D control register 0                    | (03D6 <sub>16</sub> )... |  |
| (11) A-D conversion interrupt control register | (004E <sub>16</sub> )... |  | (47) A-D control register 1                    | (03D7 <sub>16</sub> )... |  |
| (12) UART0 transmit interrupt control register | (0051 <sub>16</sub> )... |  | (48) Port P0 direction register                | (03E2 <sub>16</sub> )... |  |
| (13) UART0 receive interrupt control register  | (0052 <sub>16</sub> )... |  | (49) Port P1 direction register                | (03E3 <sub>16</sub> )... |  |
| (14) UART1 transmit interrupt control register | (0053 <sub>16</sub> )... |  | (50) Port P2 direction register                | (03E6 <sub>16</sub> )... |  |
| (15) UART1 receive interrupt control register  | (0054 <sub>16</sub> )... |  | (51) Port P3 direction register                | (03E7 <sub>16</sub> )... |  |
| (16) Timer A0 interrupt control register       | (0055 <sub>16</sub> )... |  | (52) Port P4 direction register                | (03EA <sub>16</sub> )... |  |
| (17) Timer X0 interrupt control register       | (0056 <sub>16</sub> )... |  | (53) Port P5 direction register                | (03EB <sub>16</sub> )... |  |
| (18) Timer X1 interrupt control register       | (0057 <sub>16</sub> )... |  | (54) Port P6 direction register                | (03EE <sub>16</sub> )... |  |
| (19) Timer X2 interrupt control register       | (0058 <sub>16</sub> )... |  | (55) Port P7 direction register                | (03EF <sub>16</sub> )... |  |
| (20) Timer B0 interrupt control register       | (005A <sub>16</sub> )... |  | (56) Pull-up control register 0                | (03FC <sub>16</sub> )... |  |
| (21) Timer B1 interrupt control register       | (005B <sub>16</sub> )... |  | (57) Pull-up control register 1                | (03FD <sub>16</sub> )... |  |
| (22) INT0 interrupt control register           | (005D <sub>16</sub> )... |  | (58) Port P1 drive capacity control register   | (03FE <sub>16</sub> )... |  |
| (23) INT1 interrupt control register           | (005E <sub>16</sub> )... |  | (59) Data registers (R0/R1/R2/R3)              |                          |  |
| (24) Count start flag                          | (0380 <sub>16</sub> )... |  | (60) Address registers (A0/A1)                 |                          |  |
| (25) Clock prescaler reset flag                | (0381 <sub>16</sub> )... |  | (61) Frame base register (FB)                  |                          |  |
| (26) One-shot start flag                       | (0382 <sub>16</sub> )... |  | (62) Interrupt table register (INTB)           |                          |  |
| (27) Trigger select flag                       | (0383 <sub>16</sub> )... |  | (63) User stack pointer (USP)                  |                          |  |
| (28) Up-down flag                              | (0384 <sub>16</sub> )... |  | (64) Interrupt stack pointer (ISP)             |                          |  |
| (29) Timer A0 mode register                    | (0396 <sub>16</sub> )... |  | (65) Static base register (SB)                 |                          |  |
| (30) Timer X0 mode register                    | (0397 <sub>16</sub> )... |  | (66) Flag register (FLG)                       |                          |  |
| (31) Timer X1 mode register                    | (0398 <sub>16</sub> )... |  |  |                          |  |
| (32) Timer X2 mode register                    | (0399 <sub>16</sub> )... |  |  |                          |  |

x : Nothing is mapped to this bit  
? : Undefined

The content of other registers and RAM is undefined when the microcomputer is reset. The initial values must therefore be set.

Note: This register is only exist in flash memory version.

Figure 1.13. Device's internal status after a reset is cleared



## Software Reset

## Software Reset

Writing "1" to bit 3 of the processor mode register 0 (address 0004<sub>16</sub>) applies a (software) reset to the microcomputer. A software reset has almost the same effect as a hardware reset. The contents of internal RAM are preserved.

Figure 1.14 shows the processor mode register 0 and 1.

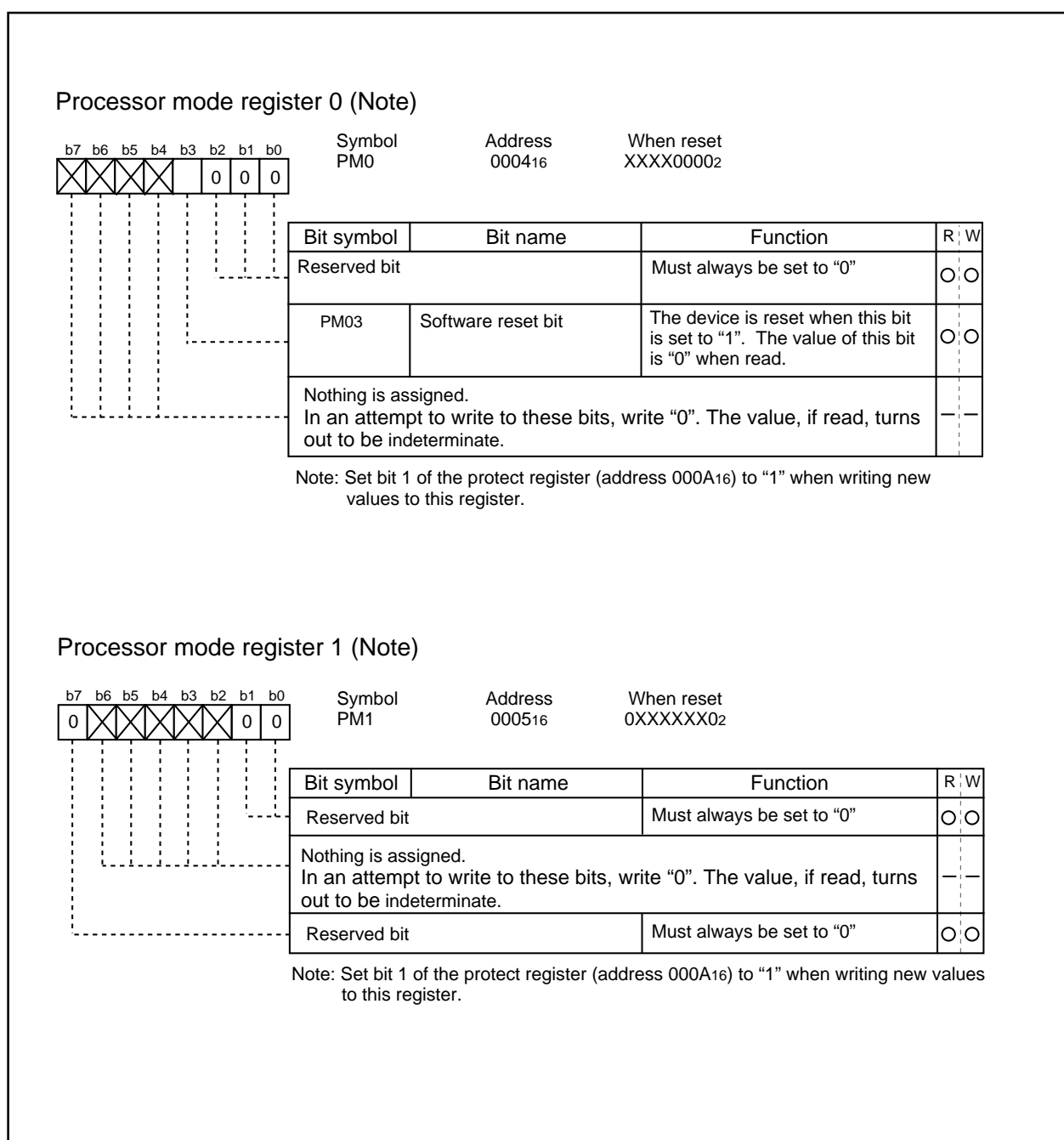


Figure 1.14. Processor mode register 0 and 1.

## Clock Generating Circuit

### Clock Generating Circuit

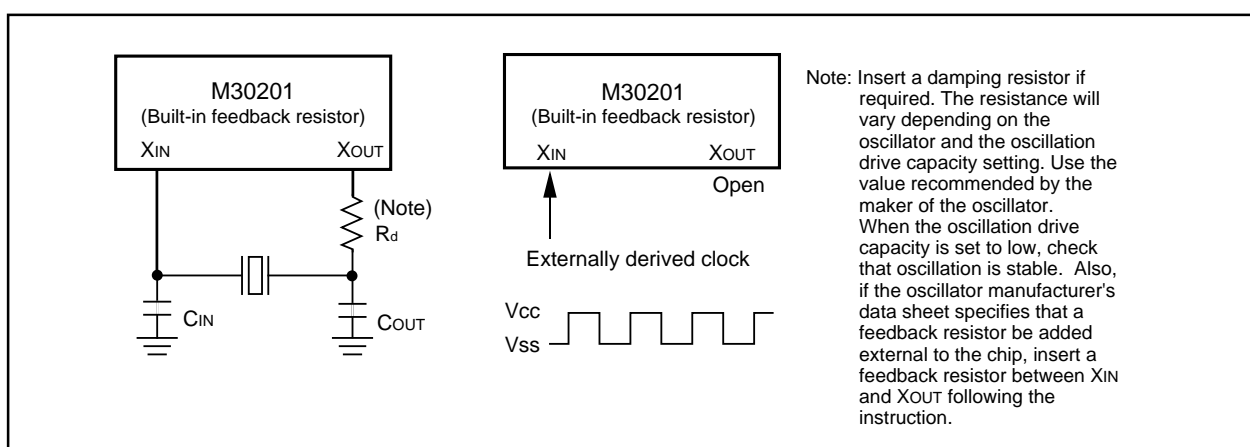
The clock generating circuit contains two oscillator circuits that supply the operating clock sources to the CPU and internal peripheral units.

**Table 1.2. Main clock and sub-clock generating circuits**

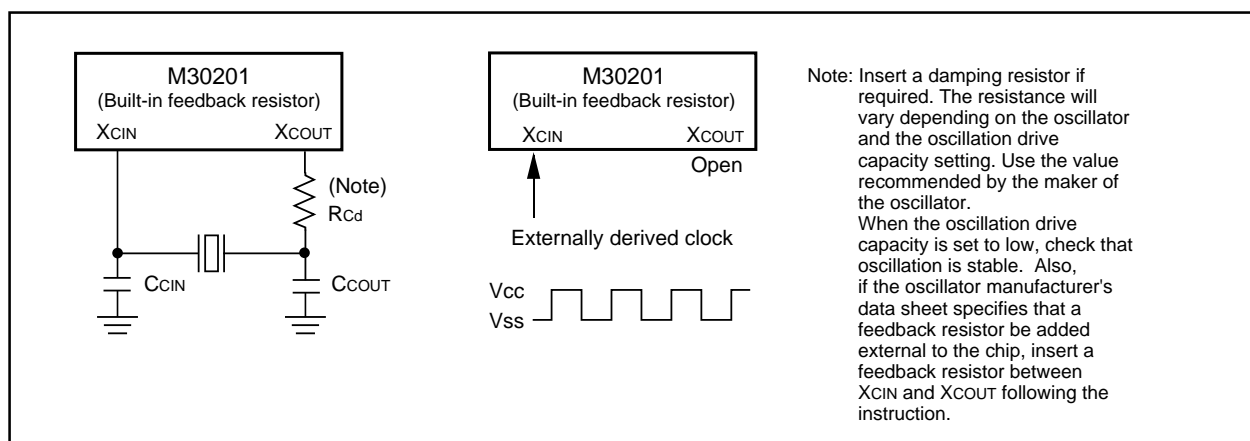
|   | Main clock generating circuit   | Sub clock generating circuit   |
|---|---|--|
| Use of clock                              | <ul style="list-style-type: none"> <li>• CPU's operating clock source</li> <li>• Internal peripheral units' operating clock source</li> </ul> | <ul style="list-style-type: none"> <li>• CPU's operating clock source</li> <li>• Timer A/B/X's count clock source</li> </ul> |
| Usable oscillator                         | Ceramic or crystal oscillator   | Crystal oscillator   |
| Pins to connect oscillator                | XIN, XOUT   | XCIN, XCOUT  |
| Oscillation stop/restart function         | Available   | Available  |
| Oscillator status immediately after reset | Oscillating   | Stopped  |
| Other                                     | Externally derived clock can be input   |  |

### Example of oscillator circuit

Figure 1.15 shows some examples of the main clock circuit, one using an oscillator connected to the circuit, and the other one using an externally derived clock for input. Figure 1.16 shows some examples of sub-clock circuits, one using an oscillator connected to the circuit, and the other one using an externally derived clock for input. Circuit constants in Figures 15 and 16 vary with each oscillator used. Use the values recommended by the manufacturer of your oscillator.



**Figure 1.15. Examples of main clock**



**Figure 1.16. Examples of sub-clock**

Figure 1.17 shows the block diagram of the clock generating circuit.



## Clock Generating Circuit

---

The following paragraphs describes the clocks generated by the clock generating circuit.

### (1) Main clock

The main clock is generated by the main clock oscillation circuit. After a reset, the clock is divided by 8 to BCLK. The clock can be stopped using the main clock stop bit (bit 5 at address 0006<sub>16</sub>). Stopping the clock, after switching the operating clock source of CPU to the sub-clock, reduces the power dissipation. After the oscillation of the main clock oscillation circuit has stabilized, the drive capacity of the main clock oscillation circuit can be reduced using the XIN-XOUT drive capacity select bit (bit 5 at address 0007<sub>16</sub>). Reducing the drive capacity of the main clock oscillation circuit reduces the power dissipation. This bit changes to "1" when shifting from high-speed/medium-speed mode to stop mode and at a reset. When shifting from low-speed/low power dissipation mode to stop mode, the value before stop mode is retained.

### (2) Sub-clock

The sub-clock is generated by the sub-clock oscillation circuit. No sub-clock is generated after a reset. After oscillation is started using the port Xc select bit (bit 4 at address 0006<sub>16</sub>), the sub-clock can be selected as BCLK by using the system clock select bit (bit 7 at address 0006<sub>16</sub>). However, be sure that the sub-clock oscillation has fully stabilized before switching.

After the oscillation of the sub-clock oscillation circuit has stabilized, the drive capacity of the sub-clock oscillation circuit can be reduced using the XCIN-XCOUT drive capacity select bit (bit 3 at address 0006<sub>16</sub>). Reducing the drive capacity of the sub-clock oscillation circuit reduces the power dissipation. This bit changes to "1" when shifting to stop mode and at a reset.

### (3) BCLK

The BCLK is the clock that drives the CPU, and is fc or the clock is derived by dividing the main clock by 1, 2, 4, 8, or 16. The BCLK is derived by dividing the main clock by 8 after a reset.

The main clock division select bit 0 (bit 6 at address 0006<sub>16</sub>) changes to "1" when shifting from high-speed/medium-speed to stop mode and at reset. When shifting from low-speed/low power dissipation mode to stop mode, the value before stop mode is retained.

### (4) Peripheral function clock (f<sub>1</sub>, f<sub>8</sub>, f<sub>32</sub>, f<sub>AD</sub>)

The clock for the peripheral devices is derived from the main clock or by dividing it by 8 or 32. The peripheral function clock is stopped by stopping the main clock or by setting the WAIT peripheral function clock stop bit (bit 2 at 0006<sub>16</sub>) to "1" and then executing a WAIT instruction.

### (5) fc32

This clock is derived by dividing the sub-clock by 32. It is used for the timer A, timer B and timer X counts.

### (6) fc

This clock has the same frequency as the sub-clock. It is used for BCLK and for the watchdog timer.

## Clock Generating Circuit

Figure 1.18 shows the system clock control registers 0 and 1.

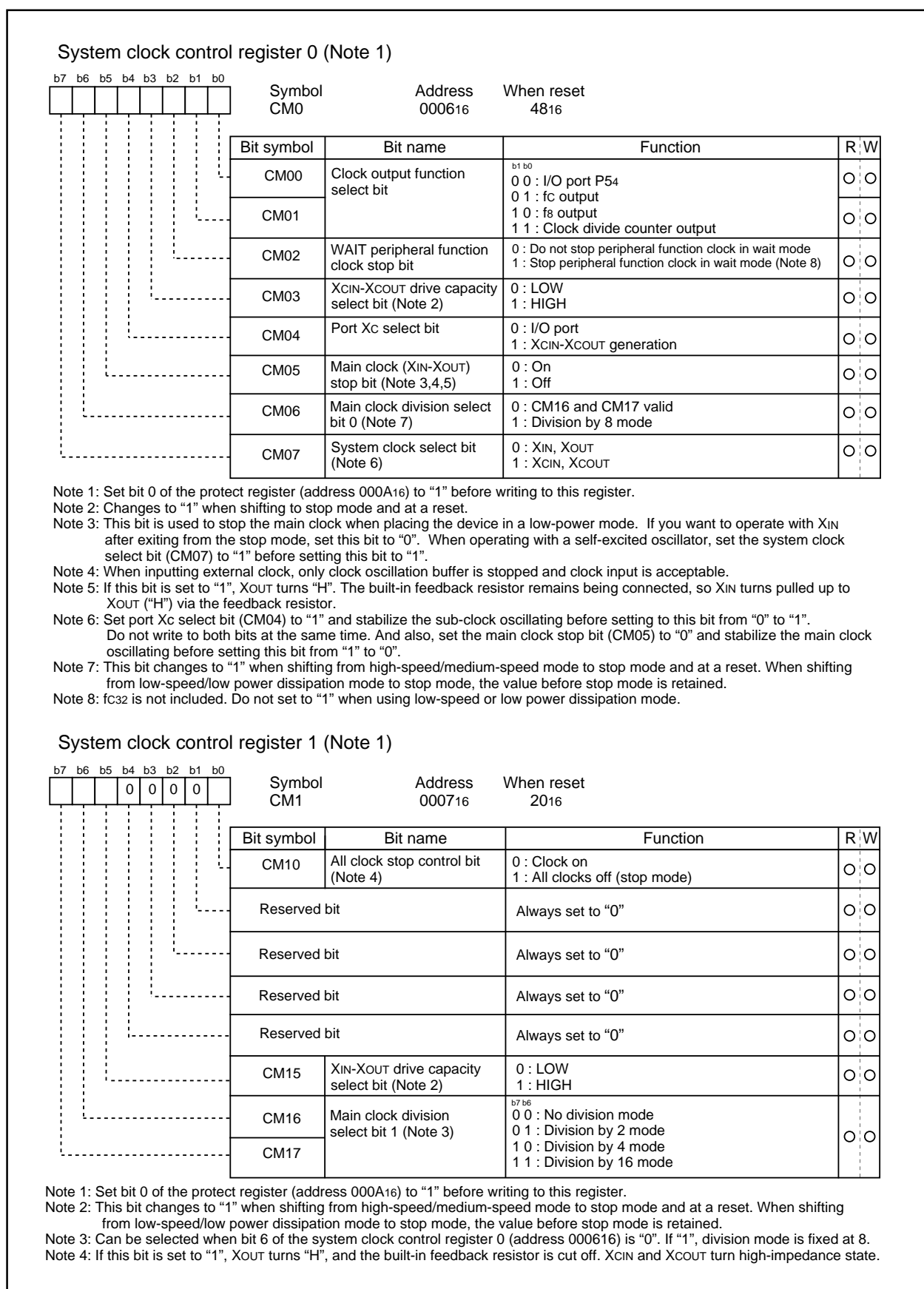


Figure 1.18. Clock control registers 0 and 1

## Clock Generating Circuit

### Clock Output

The clock output function select bit allows you to choose the clock from f8, fc, or a divide-by-n clock that is output from the P54/CKOUT pin. The clock divide counter is an 8-bit counter whose count source is f32, and its divide ratio can be set in the range of 0016 to FF16. Figure 1.19 shows a block diagram of clock output.

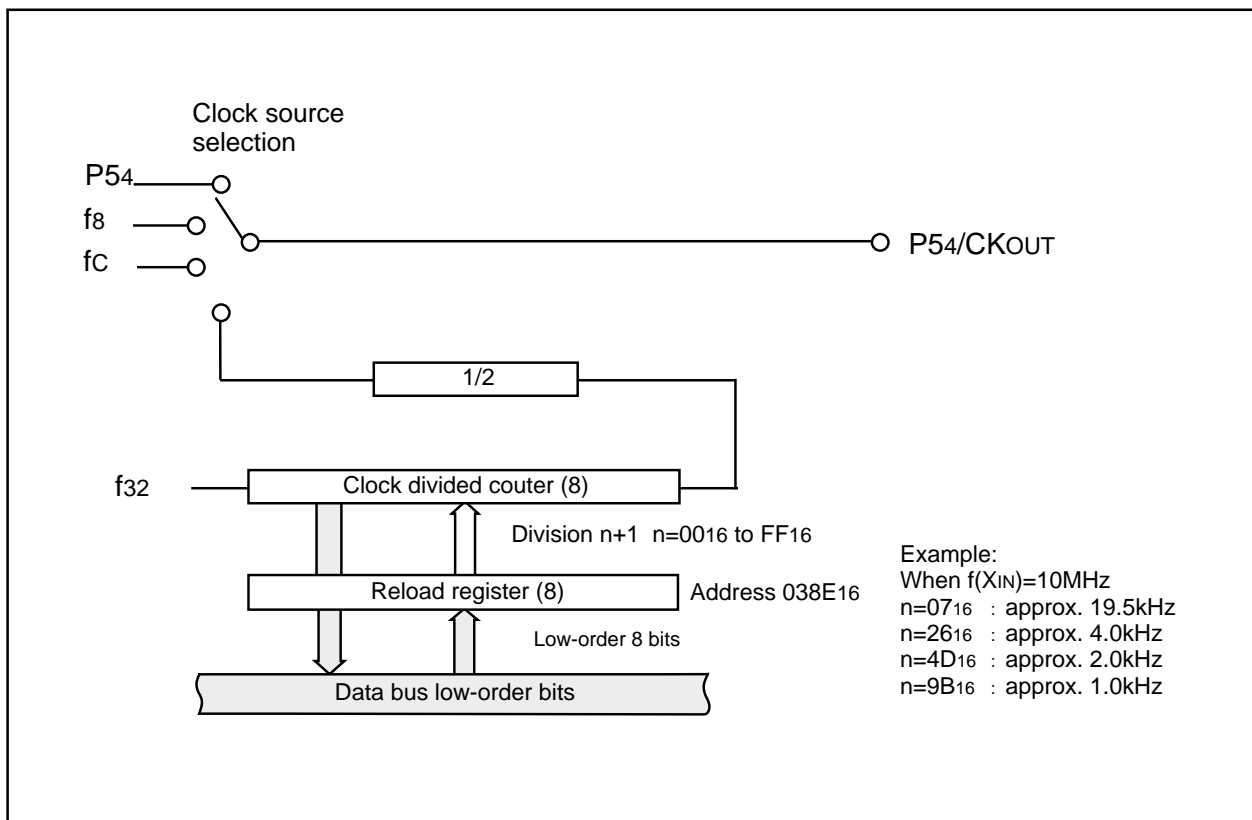


Figure 1.19. Block diagram of clock output

## Stop Mode, Wait Mode

### Stop Mode

Writing "1" to the all-clock stop control bit (bit 0 at address 0007<sub>16</sub>) stops all oscillation and the microcomputer enters stop mode. In stop mode, the content of the internal RAM is retained provided that VCC remains above 2V.

Because the oscillation of BCLK, f<sub>1</sub> to f<sub>32</sub>, f<sub>c</sub>, f<sub>c32</sub>, and f<sub>AD</sub> stops in stop mode, peripheral functions such as the A-D converter and watchdog timer do not function. However, timer A, timer B and timer X operate provided that the event counter mode is set to an external pulse, and UART0 functions provided an external clock is selected. Table 1.3 shows the status of the ports in stop mode.

Stop mode is cancelled by a hardware reset or an interrupt. If an interrupt is to be used to cancel stop mode, that interrupt must first have been enabled. If returning by an interrupt, that interrupt routine is executed.

When shifting from high-speed/medium-speed mode to stop mode and at a reset, the main clock division select bit 0 (bit 6 at address 0006<sub>16</sub>) is set to "1". When shifting from low-speed/low power dissipation mode to stop mode, the value before stop mode is retained.

**Table 1.3. Port status during stop mode**

| Pin    |   | States                          |
|--------|---|---------------------------------|
| Port   |   | Retains status before stop mode |
| CLKOUT | When f <sub>c</sub> selected                                | "H"                             |
|        | When f <sub>8</sub> , clock divided counter output selected | Retains status before stop mode |

### Wait Mode

When a WAIT instruction is executed, BCLK stops and the microcomputer enters the wait mode. In this mode, oscillation continues but BCLK and watchdog timer stop. Writing "1" to the WAIT peripheral function clock stop bit and executing a WAIT instruction stops the clock being supplied to the internal peripheral functions, allowing power dissipation to be reduced. However, peripheral function clock f<sub>c32</sub> does not stop so that the peripherals using f<sub>c32</sub> do not contribute to the power saving. When the MCU running in low-speed or low power dissipation mode, do not enter WAIT mode with this bit set to "1". Table 1.4 shows the status of the ports in wait mode.

Wait mode is cancelled by a hardware reset or interrupt. If an interrupt is used to cancel wait mode, the microcomputer restarts from the interrupt routine using as BCLK, the clock that had been selected when the WAIT instruction was executed.

**Table 1.4. Port status during wait mode**

| Pin    |   | States   |
|--------|---|--|
| Port   |   | Retains status before wait mode  |
| CLKOUT | When f <sub>c</sub> selected                                | Does not stop  |
|        | When f <sub>8</sub> , clock divided counter output selected | Does not stop when the WAIT peripheral function clock stop bit is "0".<br>When the WAIT peripheral function clock stop bit is "1", the status immediately prior to entering wait mode is maintained. |

## Status Transition of BCLK

### Status Transition of BCLK

Power dissipation can be reduced and low-voltage operation achieved by changing the count source for BCLK. Table 1.5 shows the operating modes corresponding to the settings of system clock control registers 0 and 1.

When reset, the device starts in division by 8 mode. The main clock division select bit 0(bit 6 at address 000616) changes to "1" when shifting from high-speed/medium-speed to stop mode and at a reset. When shifting from low-speed/low power dissipation mode to stop mode, the value before stop mode is retained. The following shows the operational modes of BCLK.

#### (1) Division by 2 mode

The main clock is divided by 2 to obtain the BCLK.

#### (2) Division by 4 mode

The main clock is divided by 4 to obtain the BCLK.

#### (3) Division by 8 mode

The main clock is divided by 8 to obtain the BCLK. When reset, the device starts operating from this mode. Before the user can go from this mode to no division mode, division by 2 mode, or division by 4 mode, the main clock must be oscillating stably. When going to low-speed or lower power consumption mode, make sure the sub-clock is oscillating stably.

#### (4) Division by 16 mode

The main clock is divided by 16 to obtain the BCLK.

#### (5) No-division mode

The main clock is divided by 1 to obtain the BCLK.

#### (6) Low-speed mode

fc is used as BCLK. Note that oscillation of both the main and sub-clocks must have stabilized before transferring from this mode to another or vice versa. At least 2 to 3 seconds are required after the sub-clock starts. Therefore, the program must be written to wait until this clock has stabilized immediately after powering up and after stop mode is cancelled.

#### (7) Low power dissipation mode

fc is the BCLK and the main clock is stopped.

Note : Before the count source for BCLK can be changed from XIN to XCIN or vice versa, the clock to which the count source is going to be switched must be oscillating stably. Allow a wait time in software for the oscillation to stabilize before switching over the clock.

**Table 1.5. Operating modes dictated by settings of system clock control registers 0 and 1**

| CM17    | CM16    | CM07 | CM06    | CM05 | CM04    | Operating mode of BCLK     |
|---------|---------|------|---------|------|---------|----------------------------|
| 0       | 1       | 0    | 0       | 0    | Invalid | Division by 2 mode         |
| 1       | 0       | 0    | 0       | 0    | Invalid | Division by 4 mode         |
| Invalid | Invalid | 0    | 1       | 0    | Invalid | Division by 8 mode         |
| 1       | 1       | 0    | 0       | 0    | Invalid | Division by 16 mode        |
| 0       | 0       | 0    | 0       | 0    | Invalid | No-division mode           |
| Invalid | Invalid | 1    | Invalid | 0    | 1       | Low-speed mode             |
| Invalid | Invalid | 1    | Invalid | 1    | 1       | Low power dissipation mode |



## Power Saving

---

### Power Saving

There are three power save modes.

#### (1) Normal operating mode

- **High-speed mode**

In this mode, one main clock cycle forms BCLK. The CPU operates on the BCLK. The peripheral functions operate on the clocks specified for each respective function.

- **Medium-speed mode**

In this mode, the main clock is divided into 2, 4, 8, or 16 to form BCLK. The CPU operates on the BCLK. The peripheral functions operated on the clocks specified for each respective function.

- **Low-speed mode**

In this mode, fc forms BCLK. The CPU operates on the fc clock. fc is the clock supplied by the subclock. The peripheral functions operate on the clocks specified for each respective function.

- **Low power-dissipation mode**

This mode is selected when the main clock is stopped from low-speed mode. The CPU operates on the fc clock. fc is the clock supplied by the subclock. Only the peripheral functions for which the subclock was selected as the count source continue to run.

#### (2) Wait mode

CPU operation is halted in this mode. The oscillator continues to run.

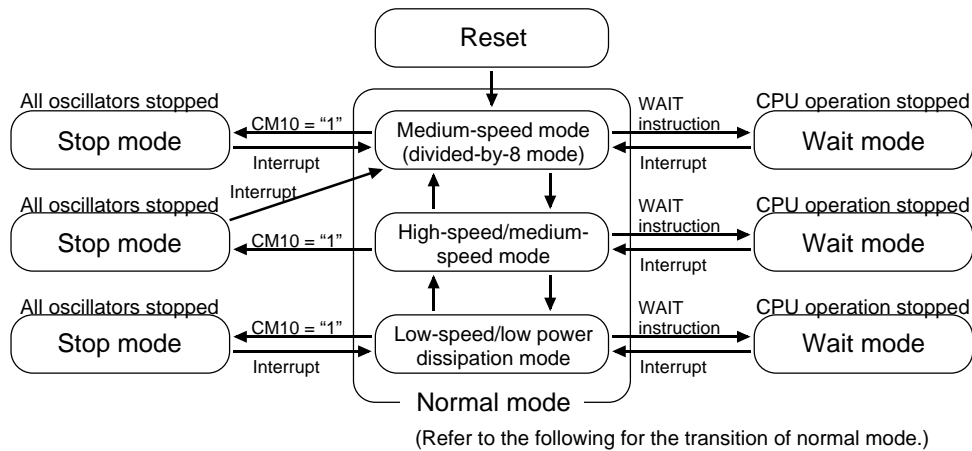
#### (3) Stop mode

All oscillators stop in this mode. The CPU and internal peripheral functions all stop. Of all 3 power saving modes, power savings are greatest in this mode.

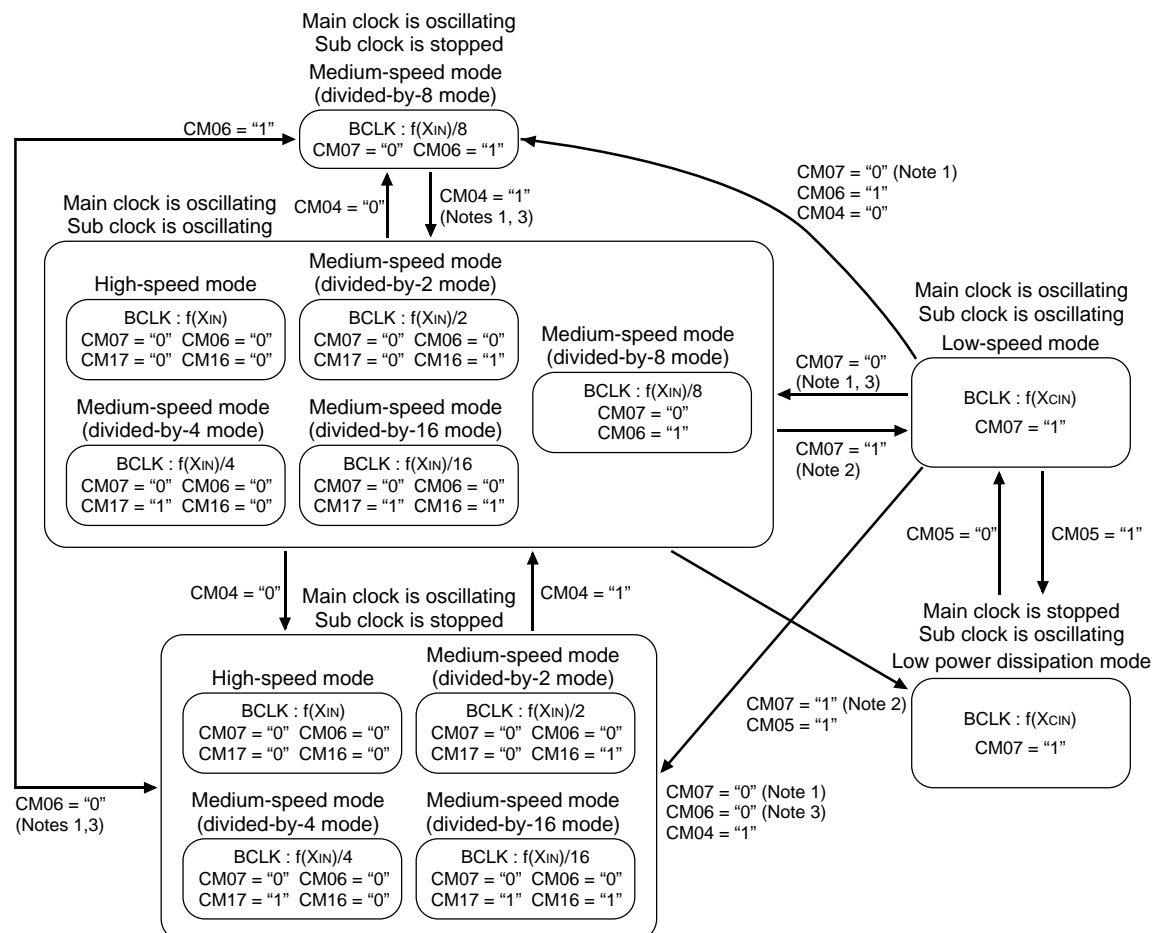
Figure 1.20 shows the transition between each of the three modes, (1), (2), and (3).

## Power Saving

## Transition of stop mode, wait mode



## Transition of normal mode



Note 1: Switch clock after oscillation of main clock is sufficiently stable.

Note 2: Switch clock after oscillation of sub clock is sufficiently stable.

Note 3: Change CM06 after changing CM17 and CM16.

Note 4: Transit in accordance with arrow.

Figure 1.20. Clock transition

## Protection

### Protection

The protection function is provided so that the values in important registers cannot be changed in the event that the program runs out of control. Figure 1.21 shows the protect register. The values in the processor mode register 0 (address 0004<sub>16</sub>), processor mode register 1 (address 0005<sub>16</sub>), system clock control register 0 (address 0006<sub>16</sub>), system clock control register 1 (address 0007<sub>16</sub>) and port P4 direction register (address 03EA<sub>16</sub>) can only be changed when the respective bit in the protect register is set to "1". Therefore, important outputs can be allocated to port P4.

If, after "1" (write-enabled) has been written to the port P4 direction register write-enable bit (bit 2 at address 000A<sub>16</sub>), a value is written to any address, the bit automatically reverts to "0" (write-inhibited). However, the system clock control registers 0 and 1 write-enable bit (bit 0 at 000A<sub>16</sub>) and processor mode register 0 and 1 write-enable bit (bit 1 at 000A<sub>16</sub>) do not automatically return to "0" after a value has been written to an address. The program must therefore be written to return these bits to "0".

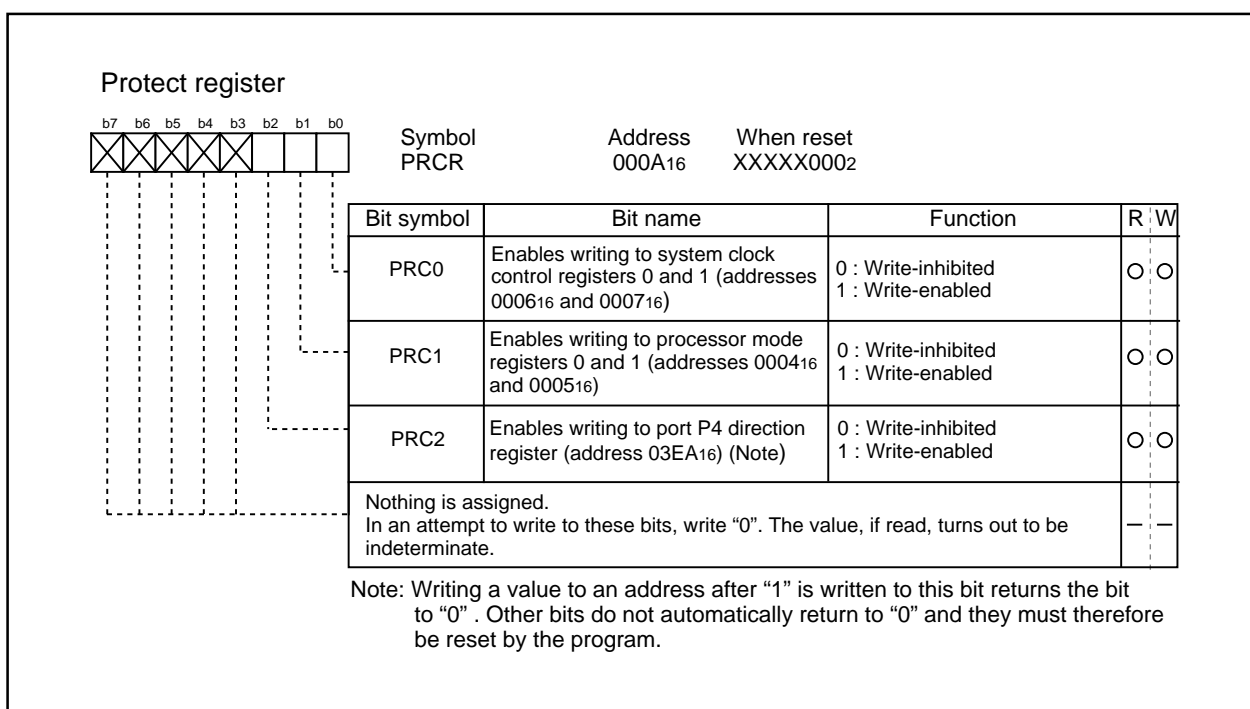


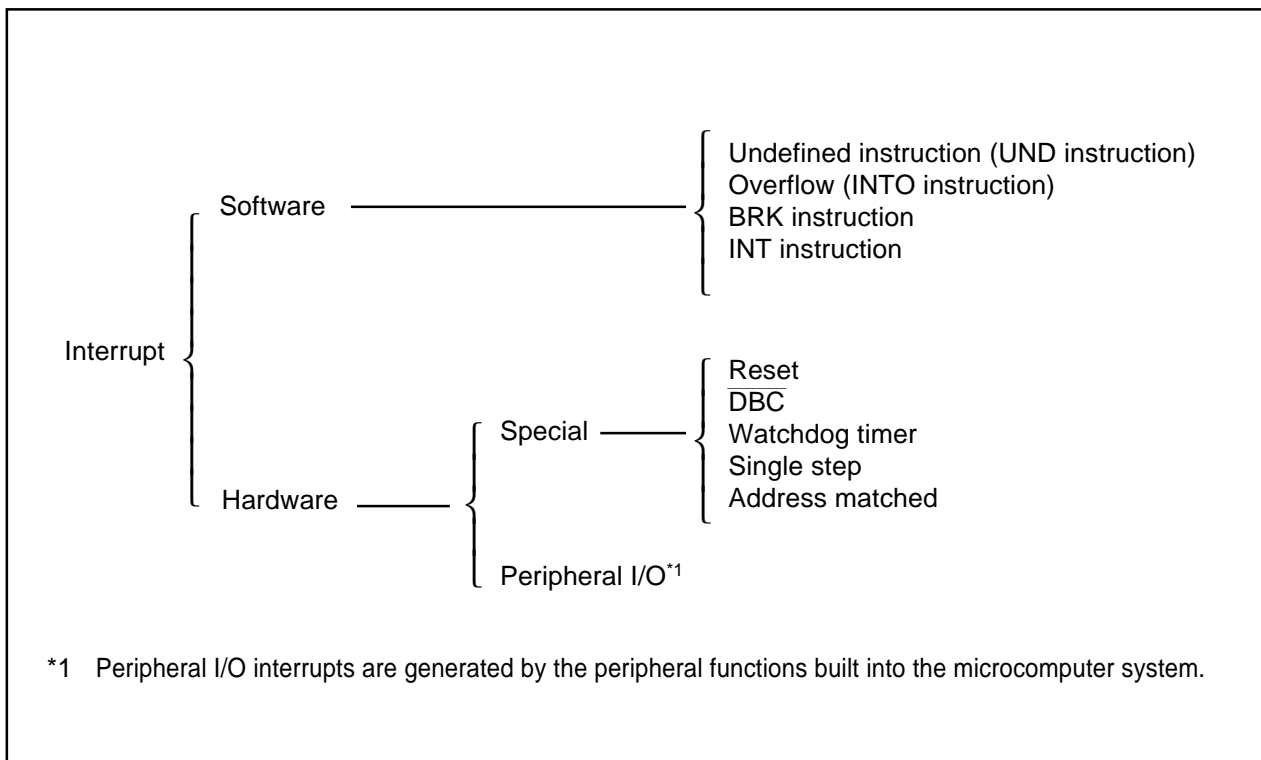
Figure 1.21. Protect register

## Interrupts

### Overview of Interrupt

#### Type of Interrupts

Figure 1.22 lists the types of interrupts.



**Figure 1.22. Classification of interrupts**

- Maskable interrupt : An interrupt which can be enabled (disabled) by the interrupt enable flag (I flag) or whose interrupt priority can be changed by priority level.
- Non-maskable interrupt : An interrupt which cannot be enabled (disabled) by the interrupt enable flag (I flag) or whose interrupt priority cannot be changed by priority level.

## Interrupts

---

### Software Interrupts

A software interrupt occurs when executing certain instructions. Software interrupts are non-maskable interrupts.

- **Undefined instruction interrupt**

An undefined instruction interrupt occurs when executing the UND instruction.

- **Overflow interrupt**

An overflow interrupt occurs when executing the INTO instruction with the overflow flag (O flag) set to "1".

The following are instructions whose O flag changes by arithmetic:

ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, SUB

- **BRK interrupt**

A BRK interrupt occurs when executing the BRK instruction.

- **INT interrupt**

An INT interrupt occurs when assigning one of software interrupt numbers 0 through 63 and executing the INT instruction. Software interrupt numbers 0 through 31 are assigned to peripheral I/O interrupts, so executing the INT instruction allows executing the same interrupt routine that a peripheral I/O interrupt does.

The stack pointer (SP) used for the INT interrupt is dependent on which software interrupt number is involved.

So far as software interrupt numbers 0 through 31 are concerned, the microcomputer saves the stack pointer assignment flag (U flag) when it accepts an interrupt request. It changes the U flag to "0" and selects the interrupt stack pointer (ISP), and then executes an interrupt sequence. When returning from the interrupt routine, the U flag is returned to the state it was before the acceptance of interrupt request. So far as software numbers 32 through 63 are concerned, the stack pointer does not make a shift.

## Interrupts

---

### Hardware Interrupts

Hardware interrupts are classified into two types — special interrupts and peripheral I/O interrupts.

#### (1) Special interrupts

Special interrupts are non-maskable interrupts.

- **Reset**

Reset occurs if an “L” is input to the RESET pin.

- **DBC interrupt**

This interrupt is exclusively for the debugger, do not use it in other circumstances.

- **Watchdog timer interrupt**

Generated by the watchdog timer.

- **Single-step interrupt**

This interrupt is exclusively for the debugger, do not use it in other circumstances. With the debug flag (D flag) set to “1”, a single-step interrupt occurs after one instruction is executed.

- **Address match interrupt**

An address match interrupt occurs immediately before the instruction held in the address indicated by the address match interrupt register is executed with the address match interrupt enable bit set to “1”. If an address other than the first address of the instruction in the address match interrupt register is set, no address match interrupt occurs.

#### (2) Peripheral I/O interrupts

A peripheral I/O interrupt is generated by one of built-in peripheral functions. The interrupt vector table is the same as the one for software interrupt numbers 0 through 31 the INT instruction uses. Peripheral I/O interrupts are maskable interrupts.

- **Key-input interrupt**

A key-input interrupt occurs if an “L” is input to the  $\overline{\text{KI}}$  pin.

- **A-D conversion interrupt**

This is an interrupt that the A-D converter generates.

- **UART0 and UART1 transmission interrupt**

These are interrupts that the serial I/O transmission generates.

- **UART0 and UART1 reception interrupt**

These are interrupts that the serial I/O reception generates.

- **Timer A0 interrupt**

This is an interrupts that timer A0 generates.

- **Timer B0 and timer B2 interrupt**

These are interrupts that timer B generates.

- **Timer X0 to timer X2 interrupt**

These are interrupts that timer X generates.

- **$\overline{\text{INT0}}$  and  $\overline{\text{INT1}}$  interrupt**

An  $\overline{\text{INT}}$  interrupt occurs if either a rising edge or a falling edge is input to the  $\overline{\text{INT}}$  pin.

## Interrupts

### Interrupts and Interrupt Vector Tables

If an interrupt request is accepted, a program branches to the interrupt routine set in the interrupt vector table. Set the first address of the interrupt routine in each vector table. Figure 1.23 shows format for specifying interrupt vector addresses.

Two types of interrupt vector tables are available — fixed vector table in which addresses are fixed and variable vector table in which addresses can be varied by the setting.

|                    | MSB         | LSB          |
|--------------------|-------------|--------------|
| Vector address + 0 | Low address |              |
| Vector address + 1 | Mid address |              |
| Vector address + 2 | 0 0 0 0     | High address |
| Vector address + 3 | 0 0 0 0     | 0 0 0 0      |

Figure 1.23. Format for specifying interrupt vector addresses

#### • Fixed vector tables

The fixed vector table is a table in which addresses are fixed. The vector tables are located in an area extending from FFFDC<sub>16</sub> to FFFFF<sub>16</sub>. One vector table comprises four bytes. Set the first address of interrupt routine in each vector table. Table 1.6 shows the interrupts assigned to the fixed vector tables and addresses of vector tables.

Table 1.6. Interrupt and fixed vector address

| Interrupt source      | Vector table addresses<br>Address (L) to address (H) | Remarks  |
|-----------------------|--|--|
| Undefined instruction | FFFD <sub>C16</sub> to FFFD <sub>F16</sub>           | Interrupt on UND instruction   |
| Overflow              | FFFE <sub>016</sub> to FFFE <sub>316</sub>           | Interrupt on INTO instruction  |
| BRK instruction       | FFFE <sub>416</sub> to FFFE <sub>716</sub>           | If the vector is filled with FF <sub>16</sub> , program execution starts from the address shown by the vector in the variable vector table |
| Address match         | FFFE <sub>816</sub> to FFFE <sub>B16</sub>           | There is an address-matching interrupt enable bit  |
| Single step (Note)    | FFFE <sub>C16</sub> to FFFE <sub>F16</sub>           | Do not use   |
| Watchdog timer        | FFFF <sub>016</sub> to FFFF <sub>316</sub>           |  |
| DBC (Note)            | FFFF <sub>416</sub> to FFFF <sub>716</sub>           | Do not use   |
| -                     | FFFF <sub>816</sub> to FFFF <sub>B16</sub>           | -  |
| Reset                 | FFFF <sub>C16</sub> to FFFF <sub>F16</sub>           |  |

Note: Interrupts used for debugging purposes only.

## Interrupts

### • Variable vector tables

The addresses in the variable vector table can be modified, according to the user's settings. Indicate the first address using the interrupt table register (INTB). The 256-byte area subsequent to the address the INTB indicates becomes the area for the variable vector tables. One vector table comprises four bytes. Set the first address of the interrupt routine in each vector table. Table 1.7 shows the interrupts assigned to the variable vector tables and addresses of vector tables.

**Table 1.7. Interrupt causes (variable interrupt vector addresses)**

| Software interrupt number  | Vector table address<br>Address (L) to address (H) | Interrupt source         | Remarks                    |
|--|--|--------------------------|----------------------------|
| Software interrupt number 0  | +0 to +3 (Note)                                    | BRK instruction          | Cannot be masked by I flag |
| —  |  | —                        |                            |
| Software interrupt number 11                                       | +44 to +47 (Note)                                  | —                        |                            |
| Software interrupt number 12                                       | +48 to +51 (Note)                                  | —                        |                            |
| Software interrupt number 13                                       | +52 to +55 (Note)                                  | Key input interrupt      |                            |
| Software interrupt number 14                                       | +56 to +59 (Note)                                  | A-D                      |                            |
| —  |  | —                        |                            |
| Software interrupt number 17                                       | +68 to +71 (Note)                                  | UART0 transmit           |                            |
| Software interrupt number 18                                       | +72 to +75 (Note)                                  | UART0 receive            |                            |
| Software interrupt number 19                                       | +76 to +79 (Note)                                  | UART1 transmit           |                            |
| Software interrupt number 20                                       | +80 to +83 (Note)                                  | UART1 receive            |                            |
| Software interrupt number 21                                       | +84 to +87 (Note)                                  | Timer A0                 |                            |
| Software interrupt number 22                                       | +88 to +91 (Note)                                  | Timer X0                 |                            |
| Software interrupt number 23                                       | +92 to +95 (Note)                                  | Timer X1                 |                            |
| Software interrupt number 24                                       | +96 to +99 (Note)                                  | Timer X2                 |                            |
| Software interrupt number 25                                       | +100 to +103 (Note)                                | —                        |                            |
| Software interrupt number 26                                       | +104 to +107 (Note)                                | Timer B0                 |                            |
| Software interrupt number 27                                       | +108 to +111 (Note)                                | Timer B1                 |                            |
| Software interrupt number 28                                       | +112 to +115 (Note)                                | —                        |                            |
| Software interrupt number 29                                       | +116 to +119 (Note)                                | $\overline{\text{INT0}}$ |                            |
| Software interrupt number 30                                       | +120 to +123 (Note)                                | $\overline{\text{INT1}}$ |                            |
| Software interrupt number 31                                       | +124 to +127 (Note)                                | —                        |                            |
| Software interrupt number 32<br>to<br>Software interrupt number 63 | +128 to +131 (Note)<br>to<br>+252 to +255 (Note)   | Software interrupt       | Cannot be masked by I flag |

Note : Address relative to address in interrupt table register (INTB).



## Interrupts

---

### Interrupt Control

Descriptions are given here regarding how to enable or disable maskable interrupts and how to set the priority to be accepted. What is described here does not apply to non-maskable interrupts.

Enable or disable a maskable interrupt using the interrupt enable flag (I flag), interrupt priority level select bit, and processor interrupt priority level (IPL). Whether an interrupt request is present or absent is indicated by the interrupt request bit. The interrupt request bit and the interrupt priority level selection bit are located in the interrupt control register of each interrupt. Also, the interrupt enable flag (I flag) and the IPL are located in the flag register (FLG).

Figure 1.24 shows the interrupt control registers.

## Interrupts

## Interrupt control register (Note 2)

| Symbol          | Address                                  | When reset |
|-----------------|--|------------|
| KUPIC           | 004D <sub>16</sub>                       | XXXXX0002  |
| ADIC            | 004E <sub>16</sub>                       | XXXXX0002  |
| SiTIC(i=0, 1)   | 0051 <sub>16</sub> , 0053 <sub>16</sub>  | XXXXX0002  |
| SiRIC(i=0, 1)   | 0052 <sub>16</sub> , 0054 <sub>16</sub>  | XXXXX0002  |
| TAiIC(i=0)      | 0055 <sub>16</sub>                       | XXXXX0002  |
| TXiIC(i=0 to 2) | 0056 <sub>16</sub> to 0058 <sub>16</sub> | XXXXX0002  |
| TBiIC(i=0, 1)   | 005A <sub>16</sub> , 005B <sub>16</sub>  | XXXXX0002  |

| Bit symbol  | Bit name                            | Function  | R | W             |
|---|-------------------------------------|---|---|---------------|
| ILVL0   | Interrupt priority level select bit | b2 b1 b0<br>0 0 0 : Level 0 (interrupt disabled)<br>0 0 1 : Level 1<br>0 1 0 : Level 2<br>0 1 1 : Level 3<br>1 0 0 : Level 4<br>1 0 1 : Level 5<br>1 1 0 : Level 6<br>1 1 1 : Level 7 | ○ | ○             |
| ILVL1   |                                     |   | ○ | ○             |
| ILVL2   |                                     |   | ○ | ○             |
| IR  | Interrupt request bit               | 0 : Interrupt not requested<br>1 : Interrupt requested  | ○ | ○<br>(Note 1) |
| Nothing is assigned.<br>In an attempt to write to these bits, write "0". The value, if read, turns out to be indeterminate. |                                     |   | — | —             |

Note 1: This bit can only be accessed for reset (= 0), but cannot be accessed for set (= 1).

Note 2: To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. For details, see the precautions for interrupts.

| Symbol         | Address                                 | When reset |
|----------------|---|------------|
| INTiIC(i=0, 1) | 005D <sub>16</sub> , 005E <sub>16</sub> | XX00X0002  |

| Bit symbol  | Bit name                            | Function  | R | W             |
|---|-------------------------------------|---|---|---------------|
| ILVL0   | Interrupt priority level select bit | b2 b1 b0<br>0 0 0 : Level 0 (interrupt disabled)<br>0 0 1 : Level 1<br>0 1 0 : Level 2<br>0 1 1 : Level 3<br>1 0 0 : Level 4<br>1 0 1 : Level 5<br>1 1 0 : Level 6<br>1 1 1 : Level 7 | ○ | ○             |
| ILVL1   |                                     |   | ○ | ○             |
| ILVL2   |                                     |   | ○ | ○             |
| IR  | Interrupt request bit               | 0: Interrupt not requested<br>1: Interrupt requested  | ○ | ○<br>(Note 1) |
| POL   | Polarity select bit                 | 0 : Selects falling edge<br>1 : Selects rising edge   | ○ | ○             |
| Reserved bit  |                                     |   | ○ | ○             |
| Nothing is assigned.<br>In an attempt to write to these bits, write "0". The value, if read, turns out to be indeterminate. |                                     |   | — | —             |

Note 1: This bit can only be accessed for reset (= 0), but cannot be accessed for set (= 1).

Note 2: To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. For details, see the precautions for interrupts.

Figure 1.24. Interrupt control register

## Interrupts

### Interrupt Enable Flag

The interrupt enable flag (I flag) controls the enabling and disabling of maskable interrupts. Setting this flag to "1" enables all maskable interrupts; setting it to "0" disables all maskable interrupts. This flag is set to "0" after reset.

### Interrupt Request Bit

The interrupt request bit is set to "1" by hardware when an interrupt is requested. After the interrupt is accepted and jumps to the corresponding interrupt vector, the request bit is set to "0" by hardware. The interrupt request bit can also be set to "0" by software. (Do not set this bit to "1").

### Interrupt Priority Level Select Bit and Processor Interrupt Priority Level (IPL)

Set the interrupt priority level using the interrupt priority level select bit, which is one of the component bits of the interrupt control register. When an interrupt request occurs, the interrupt priority level is compared with the IPL. The interrupt is enabled only when the priority level of the interrupt is higher than the IPL. Therefore, setting the interrupt priority level to "0" disables the interrupt.

Table 1.8 shows the settings of interrupt priority levels and Table 1.9 shows the interrupt levels enabled, according to the contents of the IPL.

The following are conditions under which an interrupt is accepted:

- interrupt enable flag (I flag) = 1
- interrupt request bit = 1
- interrupt priority level > IPL

The interrupt enable flag (I flag), the interrupt request bit, the interrupt priority select bit, and the IPL are independent, and they are not affected by one another.

**Table 1.8. Settings of interrupt priority levels**

| Interrupt priority level select bit | Interrupt priority level        | Priority order  |
|-------------------------------------|---------------------------------|---|
| b2 b1 b0<br>0 0 0                   | Level 0<br>(interrupt disabled) | ———   |
| 0 0 1                               | Level 1                         | <div style="text-align: center;"> Low<br/> ↓<br/> High </div> |
| 0 1 0                               | Level 2                         |   |
| 0 1 1                               | Level 3                         |   |
| 1 0 0                               | Level 4                         |   |
| 1 0 1                               | Level 5                         |   |
| 1 1 0                               | Level 6                         |   |
| 1 1 1                               | Level 7                         |   |

**Table 1.9. Interrupt levels enabled according to the contents of the IPL**

| IPL   | Enabled interrupt priority levels        |
|---|--|
| IPL <sub>2</sub> IPL <sub>1</sub> IPL <sub>0</sub><br>0 0 0 | Interrupt levels 1 and above are enabled |
| 0 0 1   | Interrupt levels 2 and above are enabled |
| 0 1 0   | Interrupt levels 3 and above are enabled |
| 0 1 1   | Interrupt levels 4 and above are enabled |
| 1 0 0   | Interrupt levels 5 and above are enabled |
| 1 0 1   | Interrupt levels 6 and above are enabled |
| 1 1 0   | Interrupt levels 7 and above are enabled |
| 1 1 1   | All maskable interrupts are disabled     |

## Interrupts

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### Changing the Interrupt Control Register

#### < Program examples >

The program examples are described as follow:

Example 1:

```
INT_SWITCH1:
    FCLR    I                ; Disable interrupts.
    AND.B   #00h, 0055h     ; Clear TA0IC int. priority level and int. request bit.
    NOP                                ; Four NOP instructions are required when using HOLD function.
    NOP
    FSET    I                ; Enable interrupts.
```

Example 2:

```
INT_SWITCH2:
    FCLR    I                ; Disable interrupts.
    AND.B   #00h, 0055h     ; Clear TA0IC int. priority level and int. request bit.
    MOV.W   MEM, R0         ; Dummy read.
    FSET    I                ; Enable interrupts.
```

Example 3:

```
INT_SWITCH3:
    PUSHC   FLG             ; Push Flag register onto stack
    FCLR    I                ; Disable interrupts.
    AND.B   #00h, 0055h     ; Clear TA0IC int. priority level and int. request bit.
    POPC    FLG             ; Enable interrupts.
```

The reason why two NOP instructions or dummy read are inserted before FSET I in Examples 1 and 2 is to prevent the interrupt enable flag I from being set before the interrupt control register is rewritten due to effects of the instruction queue.

If changing the interrupt control register using an instruction other than the instructions listed here, and if an interrupt occurs associated with this register during execution of the instruction, there can be instances in which the interrupt request bit is not set. To avoid this problem, use one of the instructions given below to change the register.

Following instructions: AND, OR, BCLR or BSET

## Interrupts

### Interrupt Sequence

An interrupt sequence — what are performed over a period from the instant an interrupt is accepted to the instant the interrupt routine is executed — is described here.

If an interrupt occurs during execution of an instruction, the processor determines its priority when the execution of the instruction is completed, and transfers control to the interrupt sequence from the next cycle. If an interrupt occurs during execution of either the SMOVB, SMOVF, SSTR or RMPA instruction, the processor temporarily suspends the instruction being executed, and transfers control to the interrupt sequence.

In the interrupt sequence, the processor carries out the following in sequence given:

- (1) CPU gets the interrupt information (the interrupt number and interrupt request level) by reading address 0000016. After this, the corresponding interrupt request bit becomes "0".
- (2) Saves the content of the flag register (FLG) as it was immediately before the start of interrupt sequence in the temporary register (Note) within the CPU.
- (3) Sets the interrupt enable flag (I flag), the debug flag (D flag), and the stack pointer select flag (U flag) to "0" (the U flag, however, does not change if the INT instruction, in software interrupt numbers 32 through 63, is executed).
- (4) Saves the content of the temporary register (Note) within the CPU in the stack area.
- (5) Saves the content of the program counter (PC) in the stack area.
- (6) Sets the interrupt priority level of the accepted instruction in the IPL.

After the interrupt sequence is completed, the processor resumes executing instructions from the first address of the interrupt routine.

Note: This register cannot be utilized by the user.

### Interrupt Response Time

'Interrupt response time' is the period between the instant an interrupt occurs and the instant the first instruction within the interrupt routine has been executed. This time comprises the period from the occurrence of an interrupt to the completion of the instruction under execution at that moment (a) and the time required for executing the interrupt sequence (b). Figure 1.25 shows the interrupt response time.

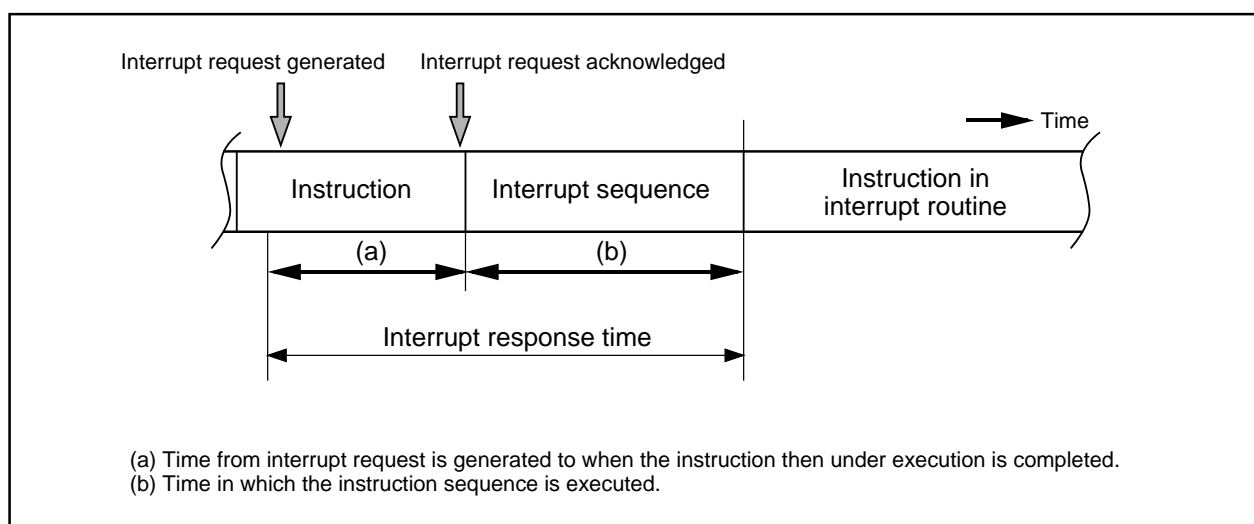


Figure 1.25. Interrupt response time

## Interrupts

Time (a) is dependent on the instruction under execution. Thirty cycles is the maximum required for the DIVX instruction (without wait).

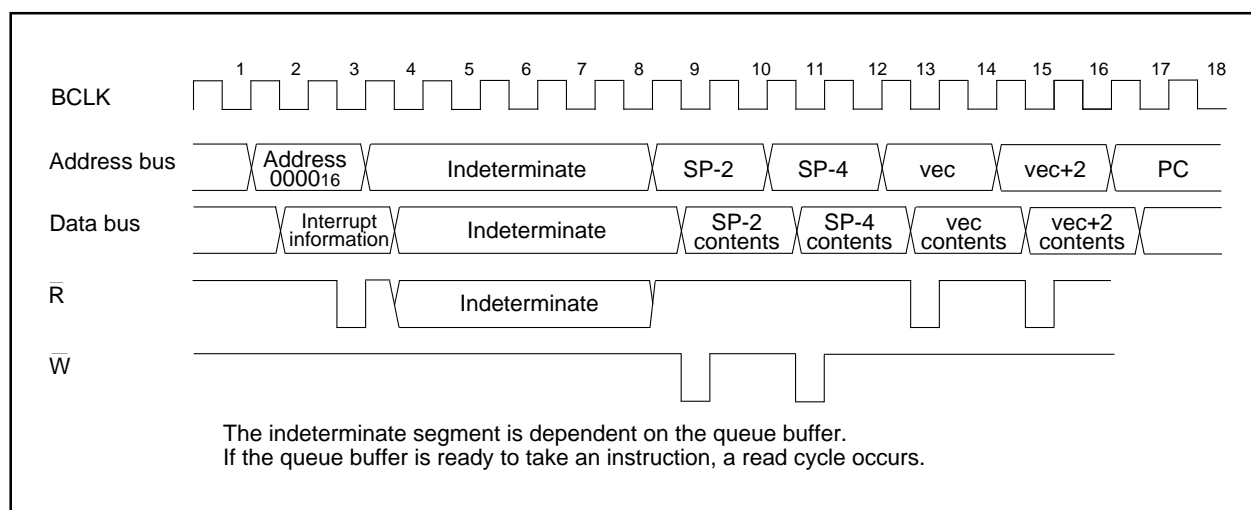
Time (b) is as shown in Table 1.10.

**Table 1.10. Time required for executing the interrupt sequence**

| Interrupt vector address | Stack pointer (SP) value | 16-bit bus, without wait | 8-bit bus, without wait |
|--------------------------|--------------------------|--------------------------|-------------------------|
| Even                     | Even                     | 18 cycles (Note 1)       | 20 cycles (Note 1)      |
| Even                     | Odd                      | 19 cycles (Note 1)       | 20 cycles (Note 1)      |
| Odd (Note 2)             | Even                     | 19 cycles (Note 1)       | 20 cycles (Note 1)      |
| Odd (Note 2)             | Odd                      | 20 cycles (Note 1)       | 20 cycles (Note 1)      |

Note 1: Add 2 cycles in the case of a DBC interrupt; add 1 cycle in the case either of an address match interrupt or of a single-step interrupt.

Note 2: Locate an interrupt vector address in an even address, if possible.



**Figure 1.26. Time required for executing the interrupt sequence**

### Variation of IPL when Interrupt Request is Accepted

If an interrupt request is accepted, the interrupt priority level of the accepted interrupt is set in the IPL.

If an interrupt request, that does not have an interrupt priority level, is accepted, one of the values shown in Table 1.11 is set in the IPL.

**Table 1.11. Relationship between interrupts without interrupt priority levels and IPL**

| Interrupt sources without priority levels | Value set in the IPL |
|---|----------------------|
| Watchdog timer                            | 7                    |
| Reset                                     | 0                    |
| Other                                     | Not changed          |

## Interrupts

### Saving Registers

In the interrupt sequence, only the contents of the flag register (FLG) and that of the program counter (PC) are saved in the stack area.

First, the processor saves the 4 high-order bits of the program counter, and 4 high-order bits and 8 low-order bits of the FLG register, 16 bits in total, in the stack area, then saves 16 low-order bits of the program counter. Figure 1.27 shows the state of the stack as it was before the acceptance of the interrupt request, and the state the stack after the acceptance of the interrupt request.

Save other necessary registers at the beginning of the interrupt routine using software. Using the PUSHM instruction alone can save all the registers except the stack pointer (SP).

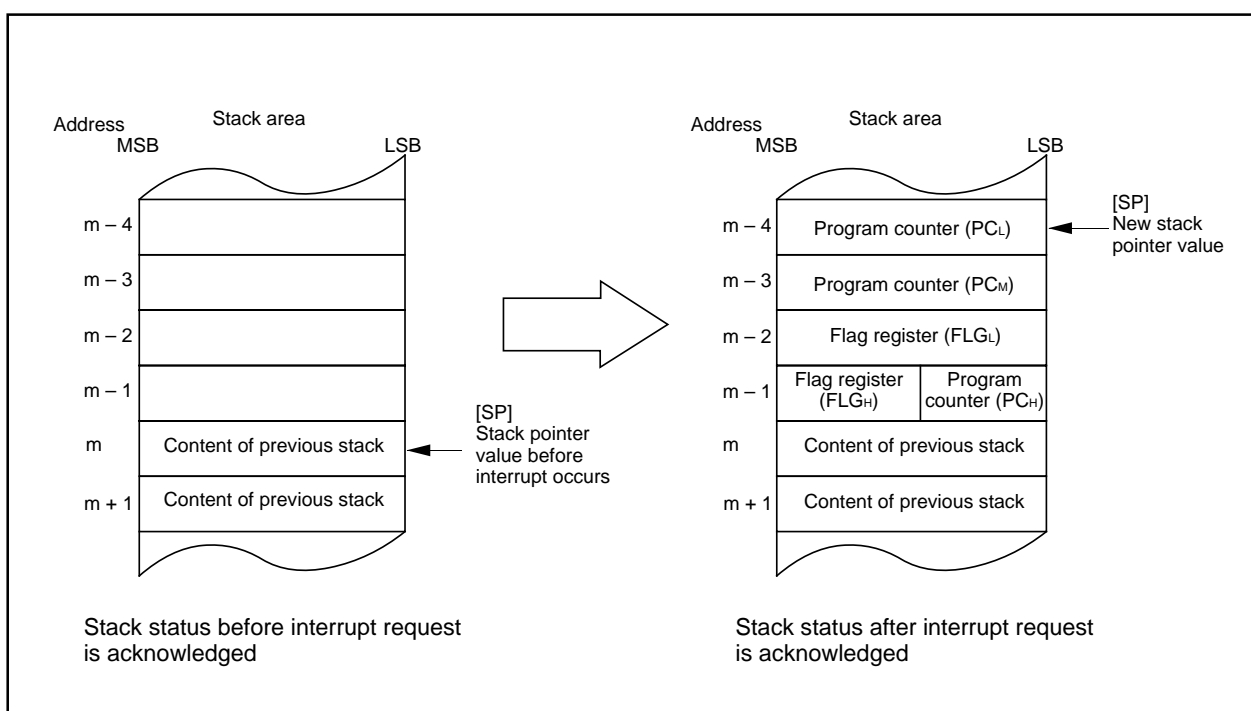


Figure 1.27. State of stack before and after acceptance of interrupt request

## Interrupts

The operation of saving registers carried out in the interrupt sequence is dependent on whether the content of the stack pointer (Note), at the time of acceptance of an interrupt request, is even or odd. If the content of the stack pointer (Note) is even, the content of the flag register (FLG) and the content of the program counter (PC) are saved, 16 bits at a time. If odd, their contents are saved in two steps, 8 bits at a time. Figure 1.28 shows the operation of the saving registers.

Note: When any INT instruction in software numbers 32 to 63 has been executed, this is the stack pointer indicated by the U flag. Otherwise, it is the interrupt stack pointer (ISP).

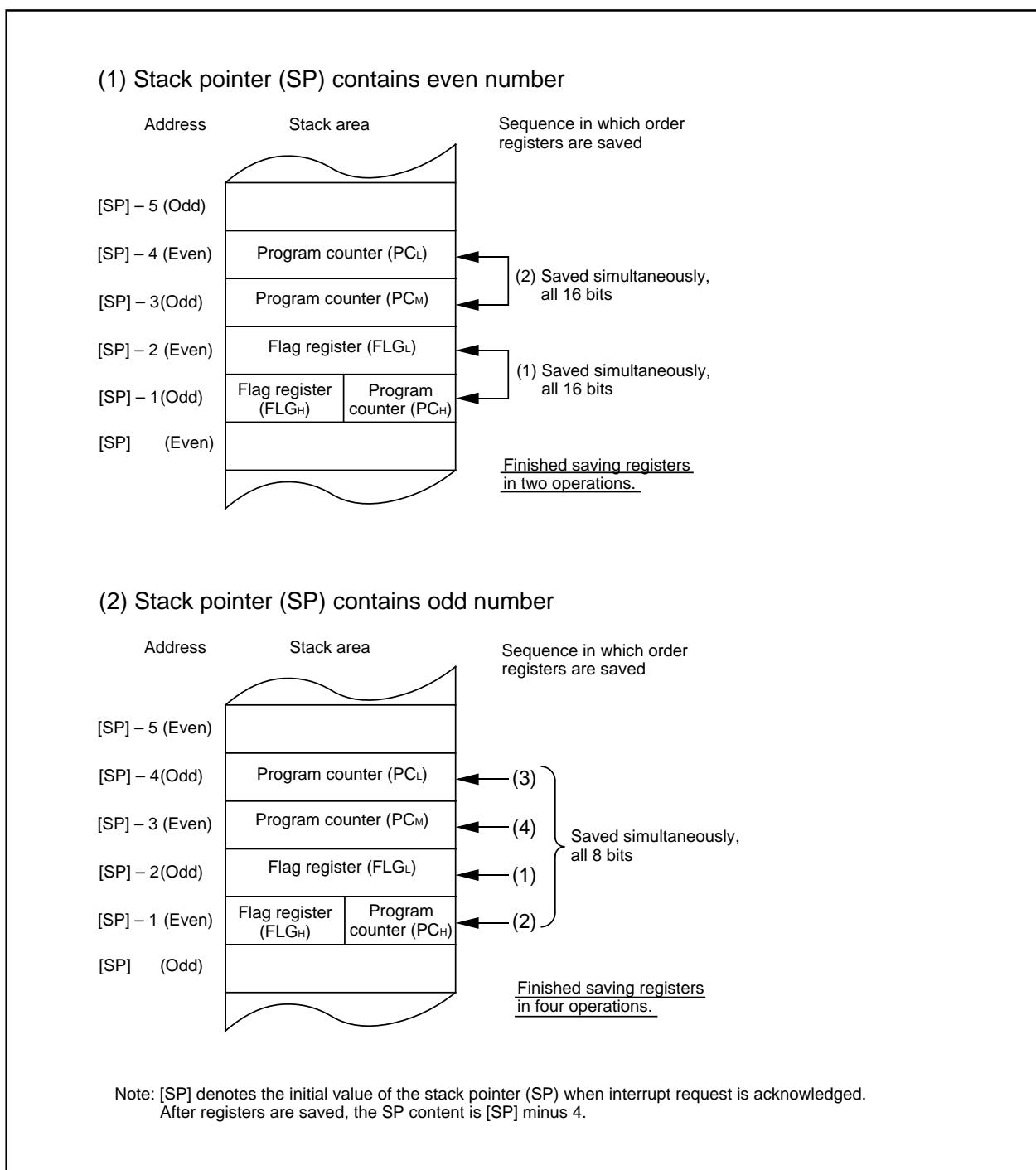


Figure 1.28. Operation of saving registers



## Interrupts

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### Returning from an Interrupt Routine

Executing the REIT instruction at the end of an interrupt routine returns the contents of the flag register (FLG) as it was immediately before the start of interrupt sequence and the contents of the program counter (PC), both of which have been saved in the stack area. Then control returns to the program that was being executed before the acceptance of the interrupt request, so that the suspended process resumes.

Return the other registers saved by software within the interrupt routine using the POPM or similar instruction before executing the REIT instruction.

### Interrupt Priority

If there are two or more interrupt requests occurring at a point in time within a single sampling (checking whether interrupt requests are made), the interrupt assigned a higher priority is accepted.

Assign an arbitrary priority to maskable interrupts (peripheral I/O interrupts) using the interrupt priority level select bit. If the same interrupt priority level is assigned, however, the interrupt assigned a higher hardware priority is accepted.

Priorities of the special interrupts, such as Reset (dealt with as an interrupt assigned the highest priority), watchdog timer interrupt, etc. are regulated by hardware.

Figure 1.29 shows the priorities of hardware interrupts.

Software interrupts are not affected by the interrupt priority. If an instruction is executed, control branches invariably to the interrupt routine.

### Interrupt Priority Level Judge Circuit

This circuit selects the interrupt with the highest priority level when two or more interrupts are generated simultaneously.

Figure 1.30 shows the interrupt resolution circuit.

## Interrupts

Reset >  $\overline{\text{DBC}}$  > Watchdog timer > Peripheral I/O > Single step > Address match

Figure 1.29. Hardware interrupts priorities

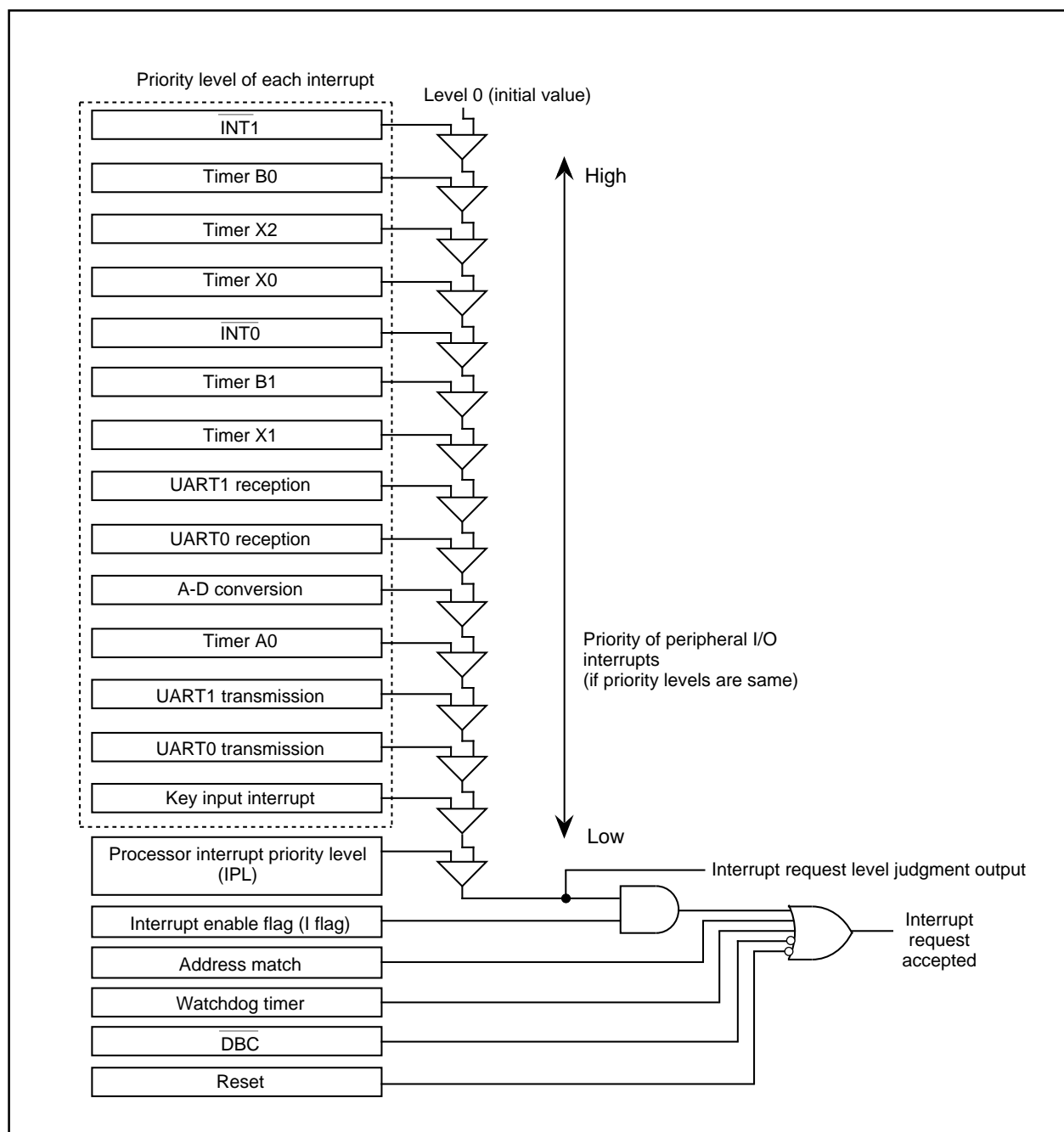


Figure 1.30. Interrupt resolution circuit

## Key Input Interrupt

### Key Input Interrupt

If the direction register of any of P00 to P07 is set for input and a falling edge is input to that port, a key input interrupt is generated. A key input interrupt can also be used as a key-on wakeup function for cancelling the wait mode or stop mode. Figure 1.31 shows the block diagram of the key input interrupt. Note that if an “L” level is input to any pin that has not been disabled for input, inputs to the other pins are not detected as an interrupt.

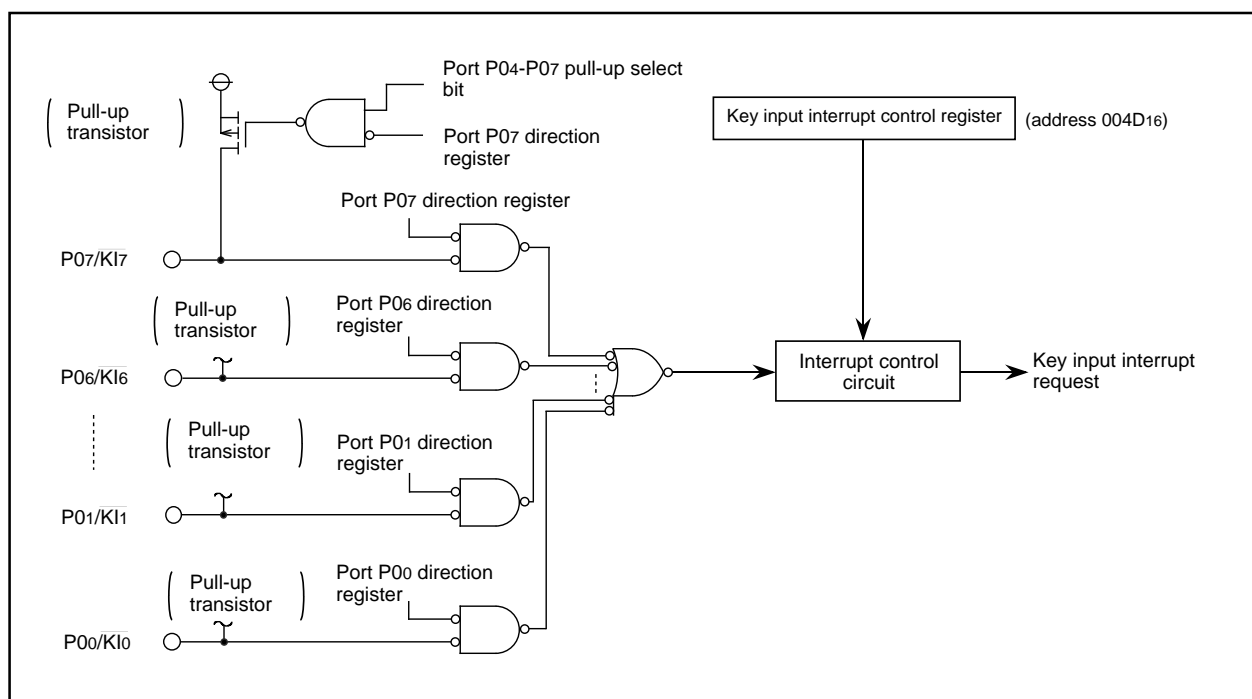


Figure 1.31. Block diagram of key input interrupt

## Address Match Interrupt

## Address Match Interrupt

An address match interrupt is generated when the address match interrupt address register contents match the program counter value. Two address match interrupts can be set, each of which can be enabled and disabled by an address match interrupt enable bit. Address match interrupts are not affected by the interrupt enable flag (I flag) and processor interrupt priority level (IPL). For an address match interrupt, the value of the program counter (PC) that is saved to the stack area varies depending on the instruction being executed.

Figure 1.32 shows the address match interrupt-related registers.

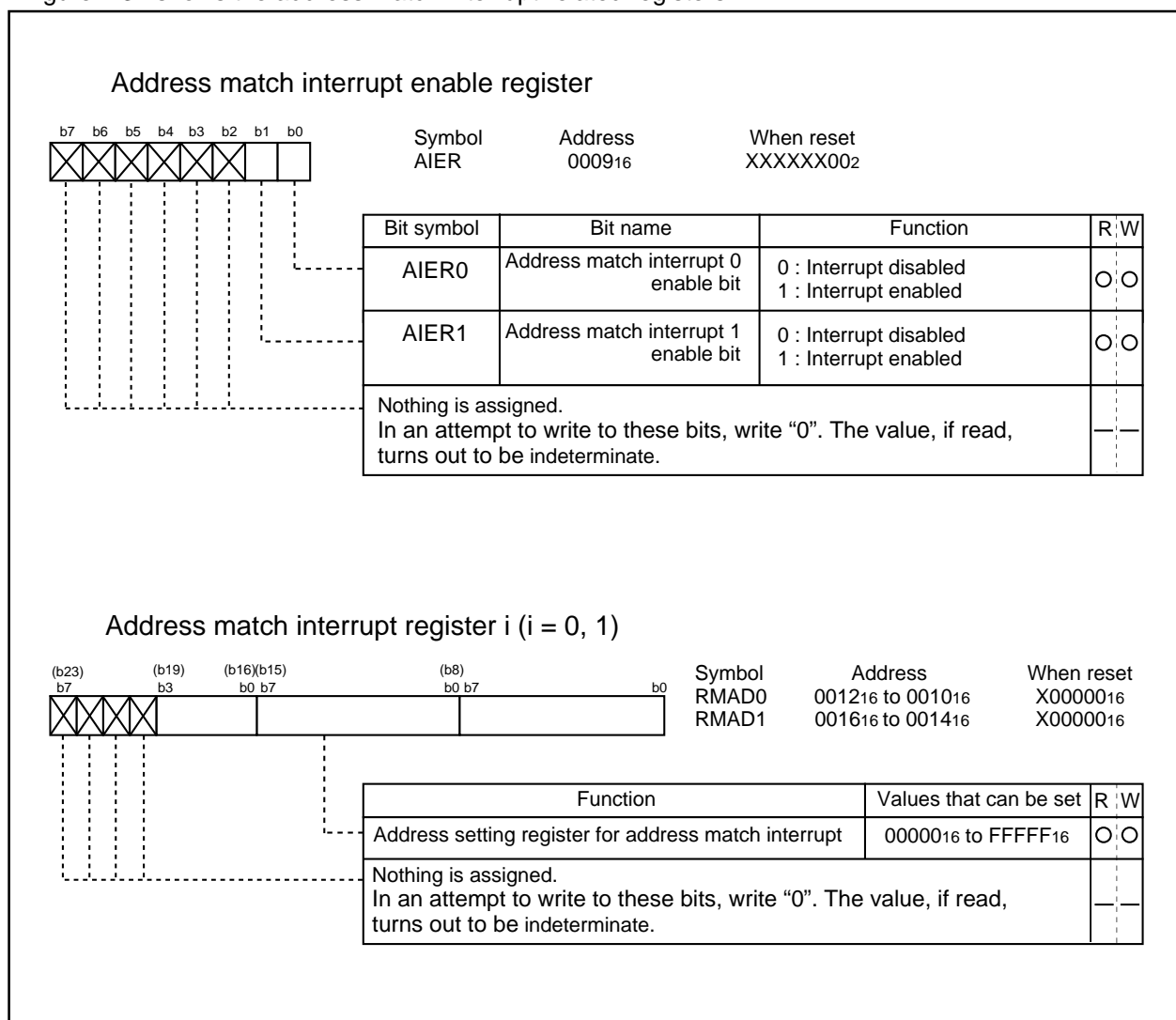


Figure 1.32. Address match interrupt-related registers

## Interrupts

### Precautions for Interrupts

#### (1) Reading address 00000<sub>16</sub>

- When maskable interrupt is occurred, CPU read the interrupt information (the interrupt number and interrupt request level) in the interrupt sequence.

The interrupt request bit of the certain interrupt written in address 00000<sub>16</sub> will then be set to "0".

Reading address 00000<sub>16</sub> by software sets enabled highest priority interrupt source request bit to "0".

Though the interrupt is generated, the interrupt routine may not be executed.

Do not read address 00000<sub>16</sub> by software.

#### (2) Setting the stack pointer

- The value of the stack pointer immediately after reset is initialized to 0000<sub>16</sub>. Accepting an interrupt before setting a value in the stack pointer may become a factor of runaway. Be sure to set a value in the stack pointer before accepting an interrupt. Concerning the first instruction immediately after reset, generating any interrupts is prohibited.

#### (3) External interrupt

- Either an "L" level or an "H" level of at least 250 ns width is necessary for the signal input to pins  $\overline{\text{INT0}}$  and  $\overline{\text{INT1}}$  regardless of the CPU operation clock.
- When changing a polarity of pins  $\overline{\text{INT0}}$  and  $\overline{\text{INT1}}$ , the interrupt request bit may become "1". Clear the interrupt request bit after changing the polarity. Figure 1.33 shows the switching condition of  $\overline{\text{INT}}$  interrupt request.

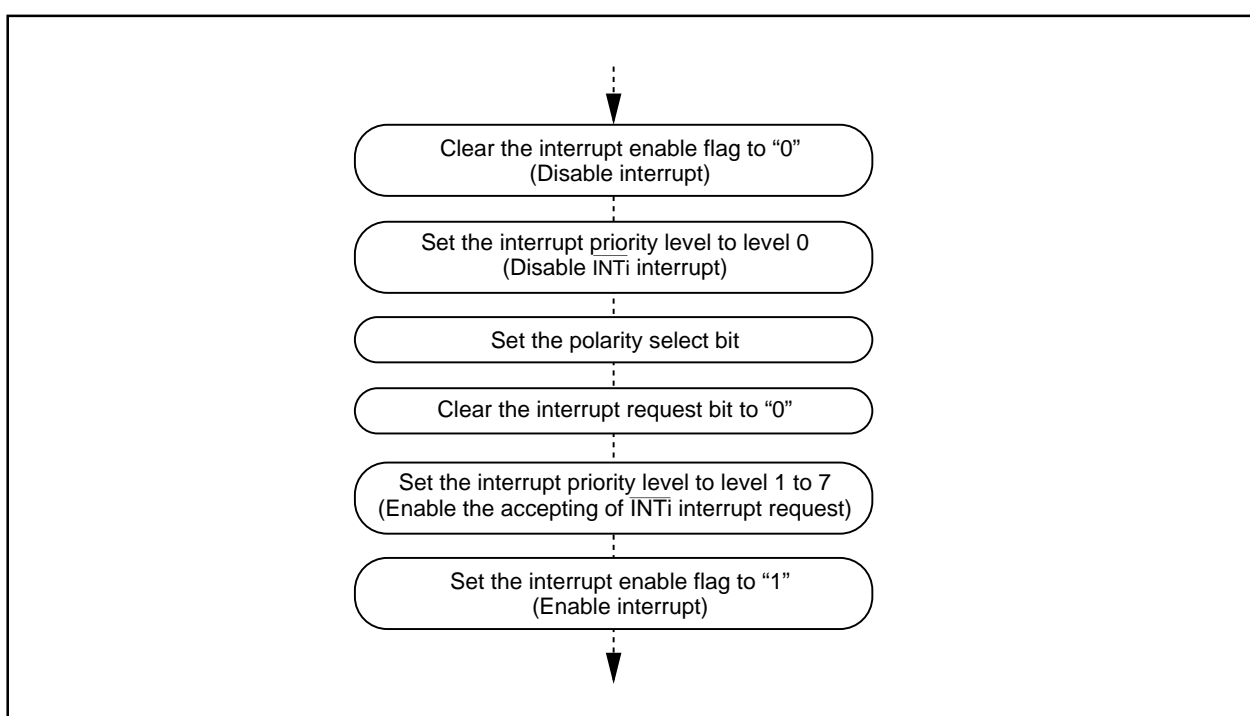


Figure 1.33. Switching condition of  $\overline{\text{INT}}$  interrupt request

#### (4) Changing interrupt control register

See "Changing Interrupt Control Register".

## Watchdog Timer

### Watchdog Timer

The watchdog timer has the function of detecting when the program is out of control. The watchdog timer is a 15-bit counter which down-counts the clock derived by dividing the BCLK using the prescaler. A watchdog timer interrupt is generated when an underflow occurs in the watchdog timer. When XIN is selected for the BCLK, bit 7 of the watchdog timer control register (address 000F<sub>16</sub>) selects the prescaler division ratio (by 16 or by 128). When XCIN is selected as the BCLK, the prescaler is set for division by 2 regardless of bit 7 of the watchdog timer control register (address 000F<sub>16</sub>).

When XIN is selected in BCLK

$$\text{Watchdog timer cycle} = \frac{\text{Prescaler division ratio (16 or 128)} \times \text{watchdog timer count (32768)}}{\text{BCLK}}$$

When XCIN is selected in BCLK

$$\text{Watchdog timer cycle} = \frac{\text{Prescaler division ratio (2)} \times \text{watchdog timer count (32768)}}{\text{BCLK}}$$

For example, when BCLK is 10MHz and the prescaler division ratio is set to 16, the watchdog timer cycle is approximately 52.4 ms.

The watchdog timer is initialized by writing to the watchdog timer start register (address 000E<sub>16</sub>) and when a watchdog timer interrupt request is generated. The prescaler is initialized only when the microcomputer is reset. After a reset is cancelled, the watchdog timer and prescaler are both stopped. The count is started by writing to the watchdog timer start register (address 000E<sub>16</sub>). In stop mode and wait mode the watchdog timer and prescaler are stopped. Counting is resumed from the held value when the modes are released. Figure 1.34 shows the block diagram of the watchdog timer. Figure 1.35 shows the watchdog timer-related registers.

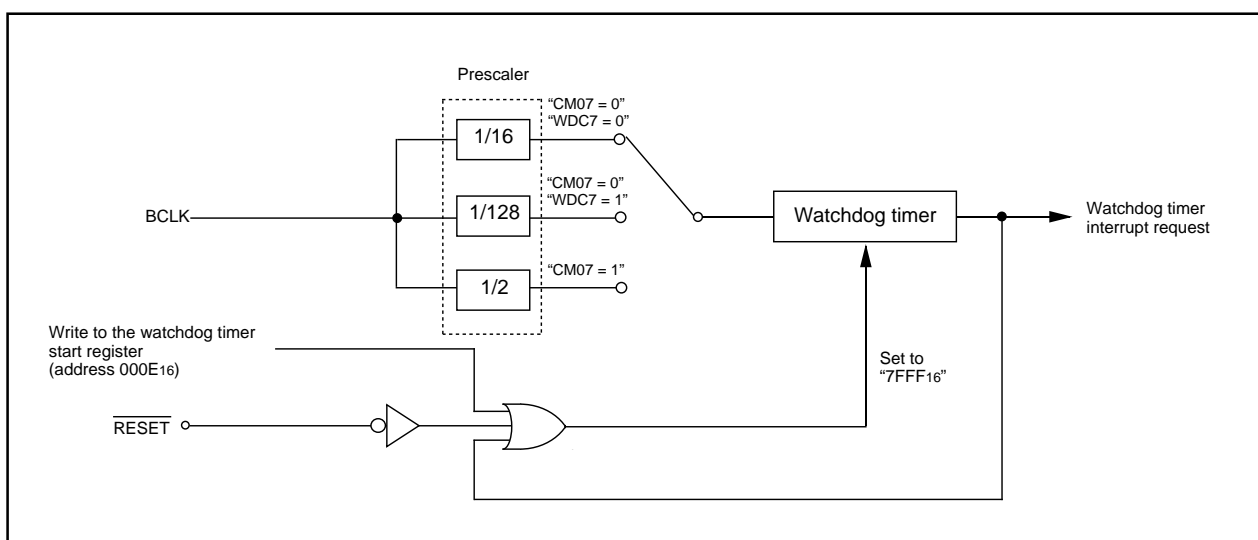


Figure 1.34. Block diagram of watchdog timer

## Watchdog Timer

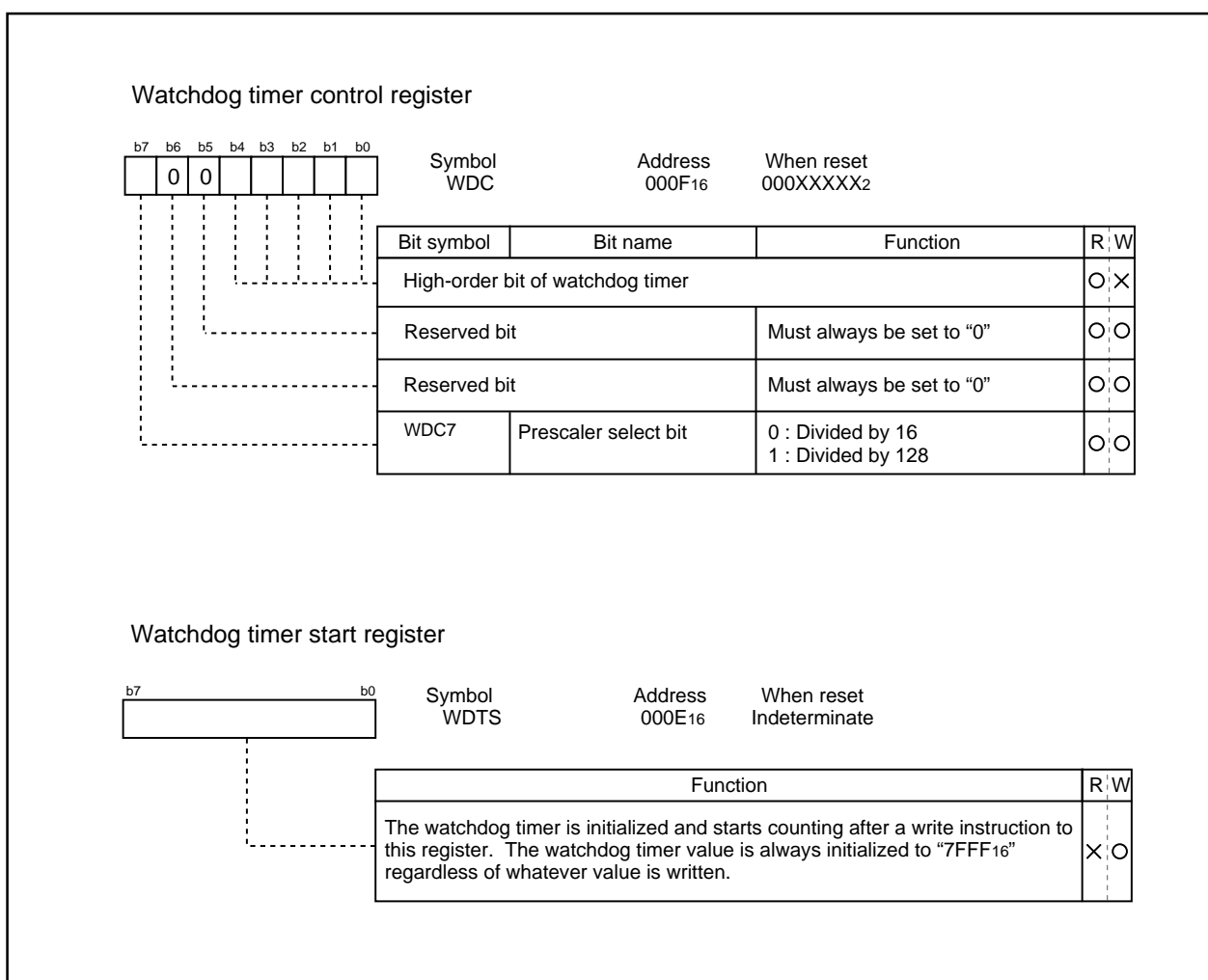


Figure 1.35. Watchdog timer control and start registers

## Timer

## Timer

There are six 16-bit timers. These timers can be classified by function into timer A (one), timers B (two) and timers X (three). All these timers function independently. Figure 1.36 show the block diagram of timers.

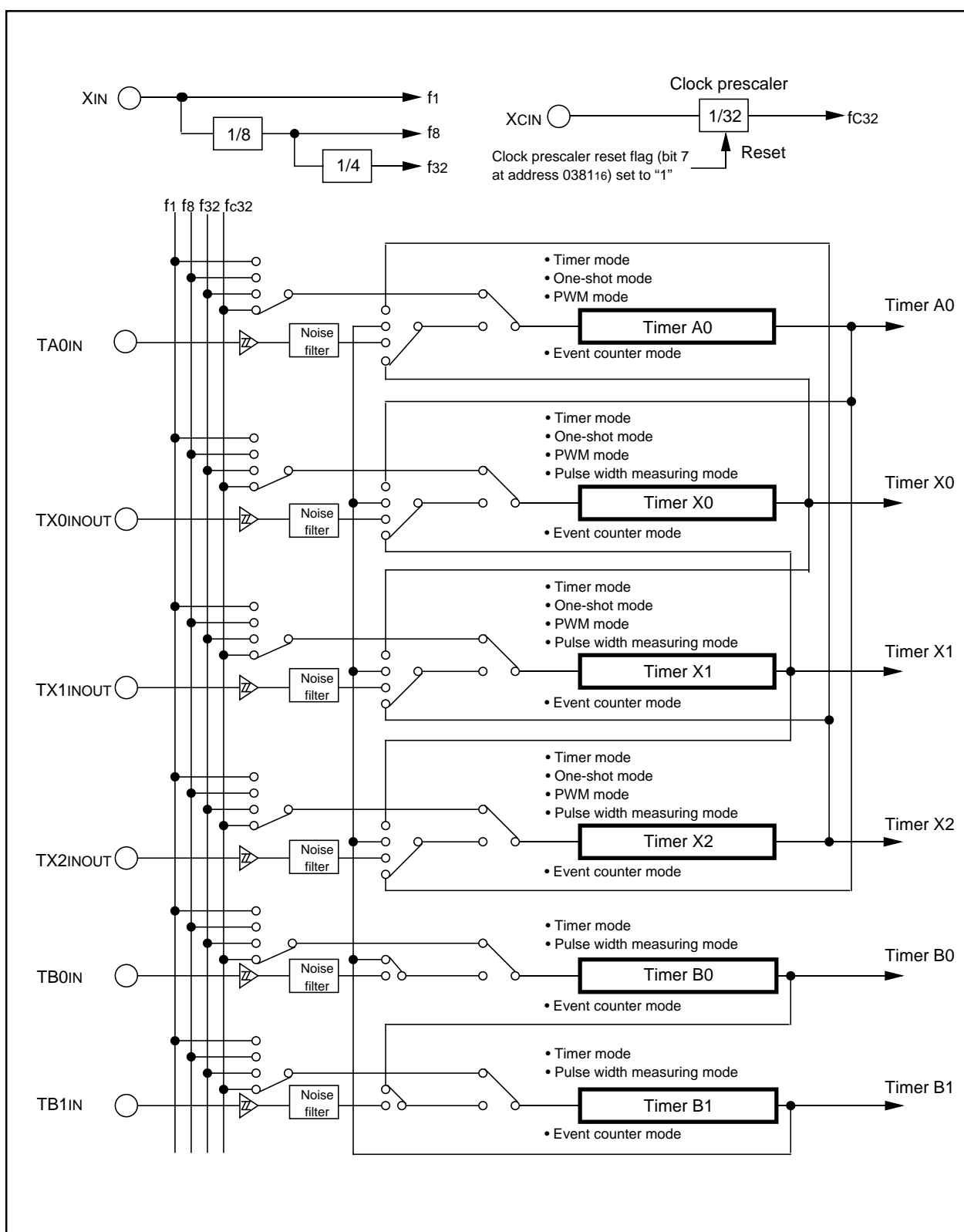


Figure 1.36. Timer block diagram





## Timer A

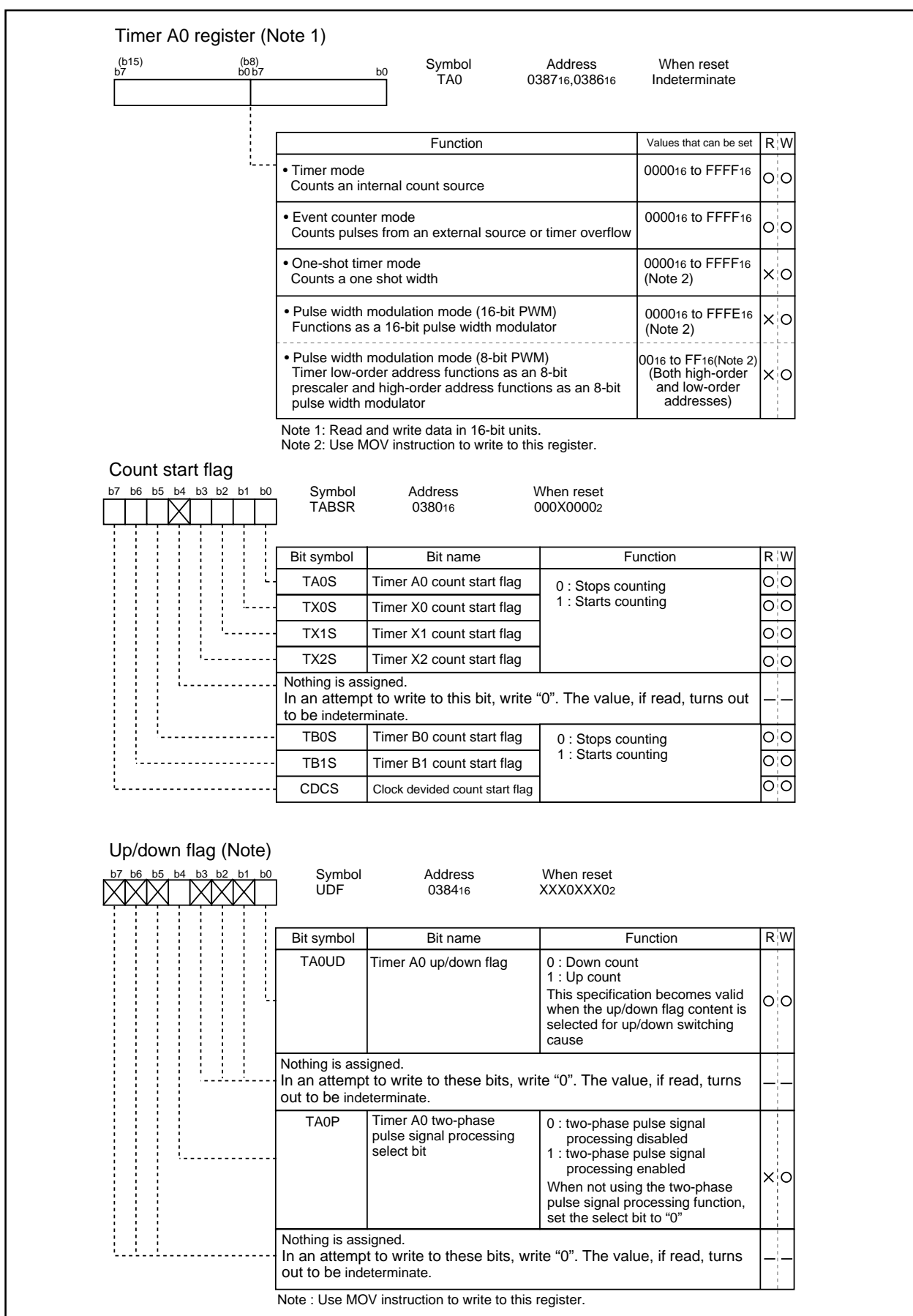


Figure 1.39. Timer A-related registers (2)

## Timer A

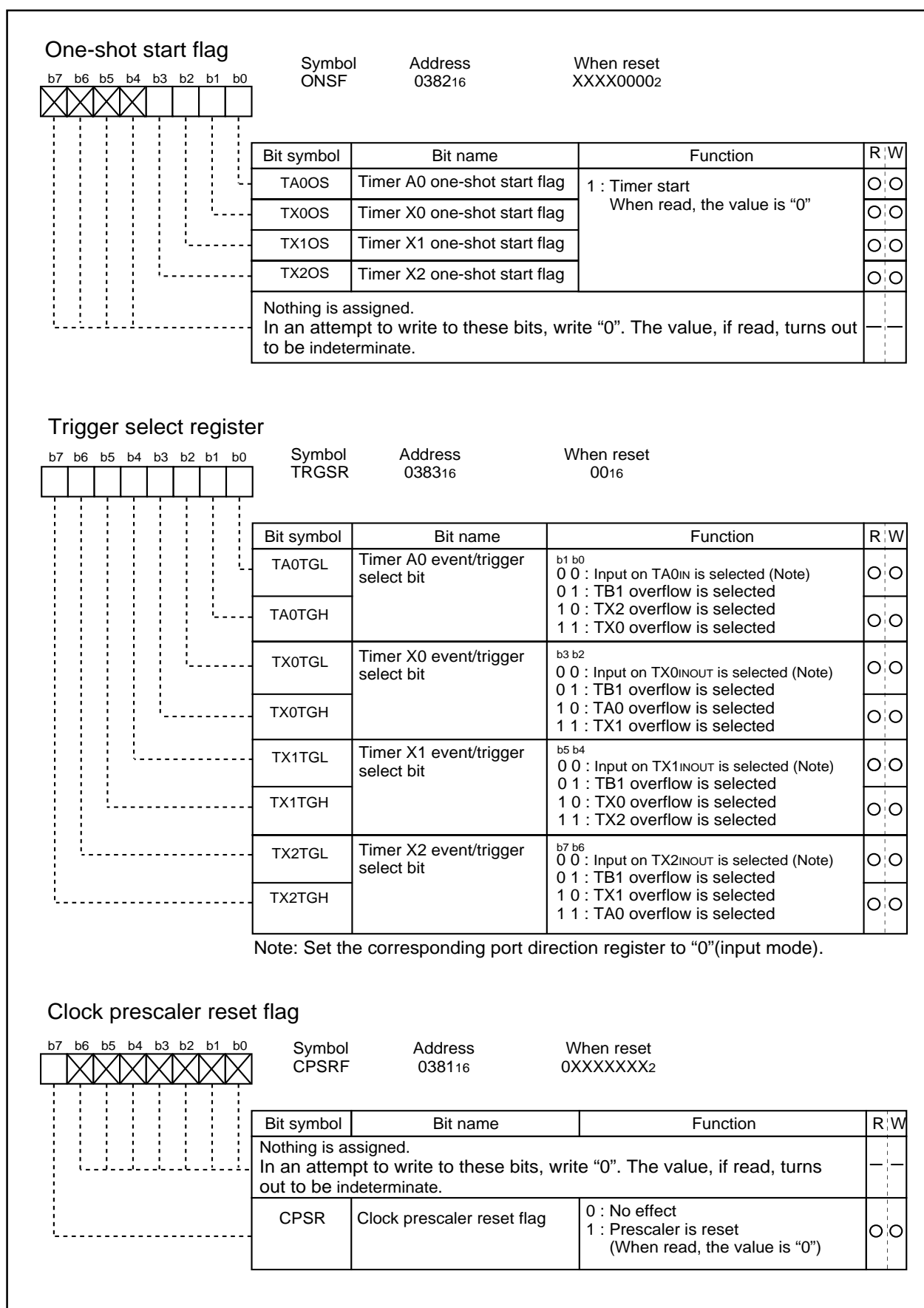


Figure 1.40. Timer A-related registers (3)

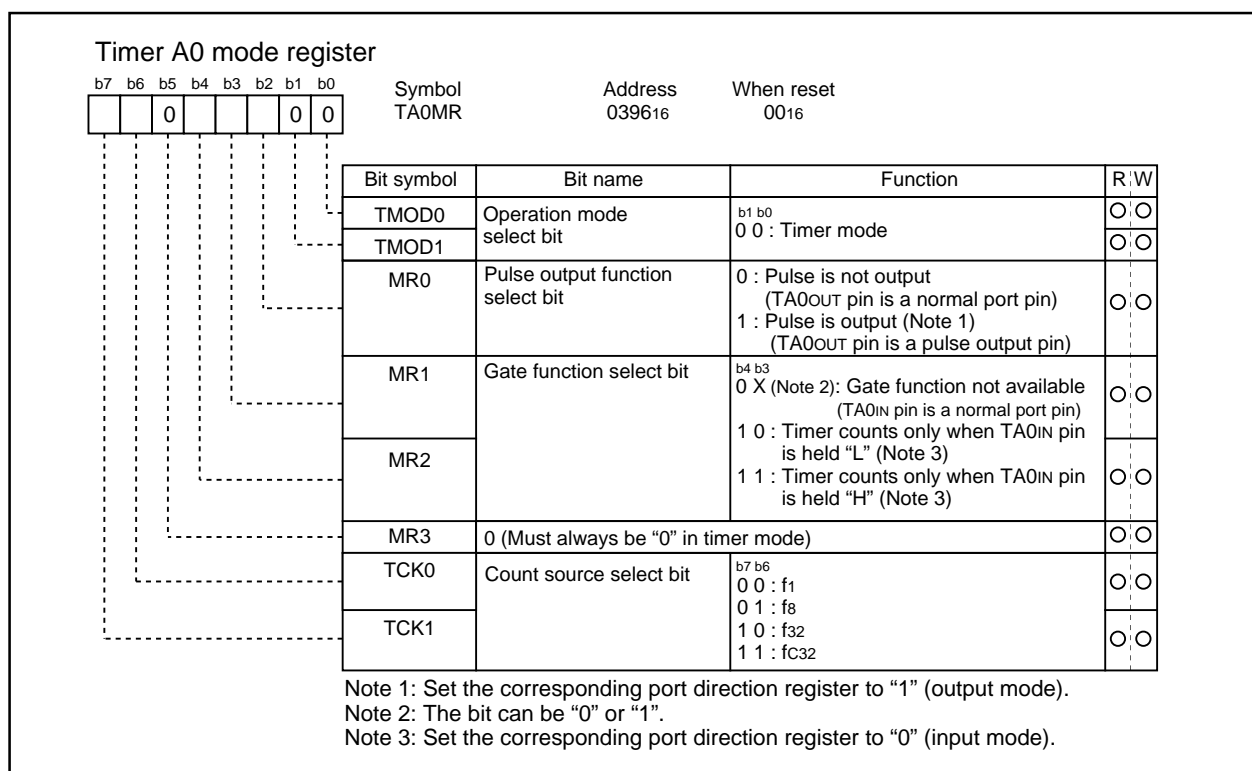
## Timer A

**(1) Timer mode**

In this mode, the timer counts an internally generated count source. (See Table 1.12.) Figure 1.41 shows the timer A0 mode register in timer mode.

**Table 1.12. Specifications of timer mode**

| Item                                | Specification   |
|-------------------------------------|---|
| Count source                        | f1, f8, f32, fc32   |
| Count operation                     | <ul style="list-style-type: none"> <li>• Down count</li> <li>• When the timer underflows, it reloads the reload register contents before continuing counting</li> </ul>   |
| Divide ratio                        | 1/(n+1)    n : Set value  |
| Count start condition               | Count start flag is set (= 1)   |
| Count stop condition                | Count start flag is reset (= 0)   |
| Interrupt request generation timing | When the timer underflows   |
| TA0IN pin function                  | Programmable I/O port or gate input   |
| TA0OUT pin function                 | Programmable I/O port or pulse output   |
| Read from timer                     | Count value can be read out by reading timer A0 register  |
| Write to timer                      | <ul style="list-style-type: none"> <li>• When counting stopped<br/>When a value is written to timer A0 register, it is written to both reload register and counter</li> <li>• When counting in progress<br/>When a value is written to timer A0 register, it is written to only reload register (Transferred to counter at next reload time)</li> </ul> |
| Select function                     | <ul style="list-style-type: none"> <li>• Gate function<br/>Counting can be started and stopped by the TA0IN pin's input signal</li> <li>• Pulse output function<br/>Each time the timer underflows, the TA0OUT pin's polarity is reversed</li> </ul>  |

**Figure 1.41. Timer A0 mode register in timer mode**

## Timer A

**(2) Event counter mode**

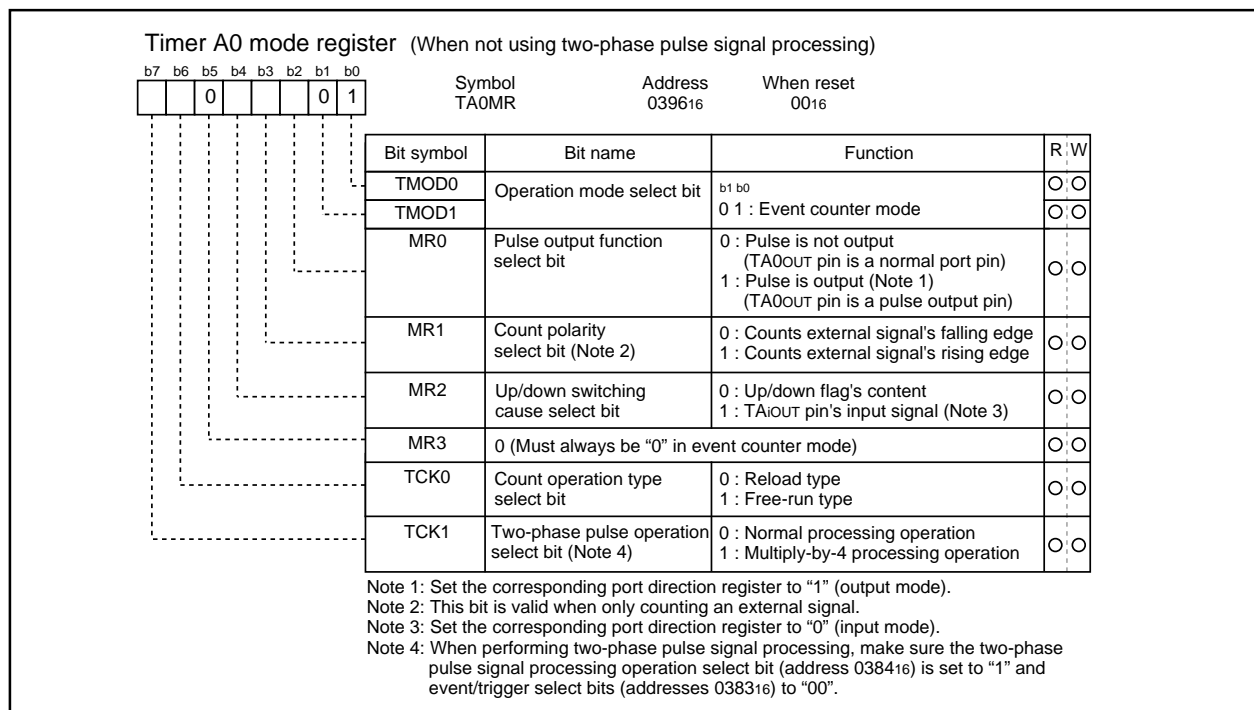
In this mode, the timer counts an external signal or an internal timer's overflow. Timer A0 can count a single-phase and a two-phase external signal. Table 1.13 lists timer specifications when counting a single-phase external signal. Figure 1.42 shows the timer A0 mode register in event counter mode.

Table 1.14 lists timer specifications when counting a two-phase external signal. Figure 1.43 shows the timer A0 mode register in event counter mode.

**Table 1.13. Timer specifications in event counter mode (when not processing two-phase pulse signal)**

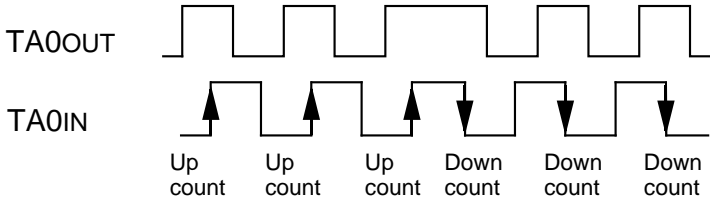
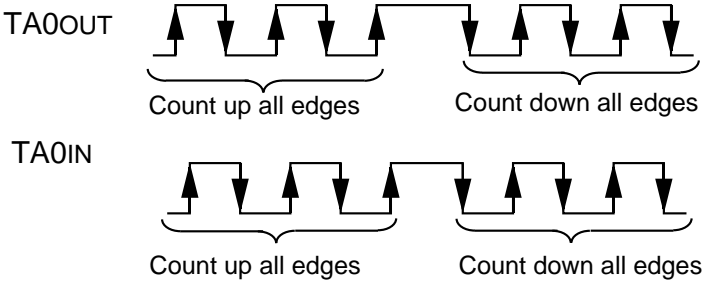
| Item                                | Specification   |
|-------------------------------------|---|
| Count source                        | <ul style="list-style-type: none"> <li>External signals input to TA0IN pin (effective edge can be selected by software)</li> <li>TB1 overflow, TX0 overflow, TX2 overflow</li> </ul>  |
| Count operation                     | <ul style="list-style-type: none"> <li>Up count or down count can be selected by external signal or software</li> <li>When the timer overflows or underflows, it reloads the reload register contents before continuing counting (Note)</li> </ul>  |
| Divide ratio                        | $1/(FFFF_{16} - n + 1)$ for up count<br>$1/(n + 1)$ for down count      n : Set value   |
| Count start condition               | Count start flag is set (= 1)   |
| Count stop condition                | Count start flag is reset (= 0)   |
| Interrupt request generation timing | The timer overflows or underflows   |
| TA0IN pin function                  | Programmable I/O port or count source input   |
| TA0OUT pin function                 | Programmable I/O port, pulse output, or up/down count select input  |
| Read from timer                     | Count value can be read out by reading timer A0 register  |
| Write to timer                      | <ul style="list-style-type: none"> <li>When counting stopped<br/>When a value is written to timer A0 register, it is written to both reload register and counter</li> <li>When counting in progress<br/>When a value is written to timer A0 register, it is written to only reload register (Transferred to counter at next reload time)</li> </ul> |
| Select function                     | <ul style="list-style-type: none"> <li>Free-run count function<br/>Even when the timer overflows or underflows, the reload register content is not reloaded to it</li> <li>Pulse output function<br/>Each time the timer overflows or underflows, the TA0OUT pin's polarity is reversed</li> </ul>  |

Note: This does not apply when the free-run function is selected.

**Figure 1.42. Timer A0 mode register in event counter mode**

## Timer A

**Table 1.14. Timer specifications in event counter mode (when processing two-phase pulse signal)**

| Item                                | Specification  |
|-------------------------------------|--|
| Count source                        | <ul style="list-style-type: none"> <li>Two-phase pulse signals input to TA0IN or TA0OUT pin</li> </ul>   |
| Count operation                     | <ul style="list-style-type: none"> <li>Up count or down count can be selected by two-phase pulse signal</li> <li>When the timer overflows or underflows, the reload register content is reloaded and the timer starts over again (Note)</li> </ul>   |
| Divide ratio                        | <ul style="list-style-type: none"> <li><math>1 / (FFFF_{16} - n + 1)</math> for up count</li> <li><math>1 / (n + 1)</math> for down count</li> </ul> <p style="text-align: right;">n : Set value</p>   |
| Count start condition               | Count start flag is set (= 1)  |
| Count stop condition                | Count start flag is reset (= 0)  |
| Interrupt request generation timing | Timer overflows or underflows  |
| TA0IN pin function                  | Two-phase pulse input  |
| TA0OUT pin function                 | Two-phase pulse input  |
| Read from timer                     | Count value can be read out by reading timer A0 register   |
| Write to timer                      | <ul style="list-style-type: none"> <li>When counting stopped<br/>When a value is written to timer A0 register, it is written to both reload register and counter</li> <li>When counting in progress<br/>When a value is written to timer A0 register, it is written to only reload register. (Transferred to counter at next reload time.)</li> </ul>  |
| Select function                     | <ul style="list-style-type: none"> <li>Normal processing operation<br/>The timer counts up rising edges or counts down falling edges on the TA0IN pin when input signal on the TA0OUT pin is "H"</li> </ul> <div style="text-align: center;">  </div> <ul style="list-style-type: none"> <li>Multiply-by-4 processing operation<br/>If the phase relationship is such that the TA0IN pin goes "H" when the input signal on the TA0OUT pin is "H", the timer counts up rising and falling edges on the TA0OUT and TA0IN pins. If the phase relationship is such that the TA0IN pin goes "L" when the input signal on the TA0OUT pin is "H", the timer counts down rising and falling edges on the TA0OUT and TA0IN pins.</li> </ul> <div style="text-align: center;">  </div> |

Note: This does not apply when the free-run function is selected.

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|    |    | 0  | 1  | 0  | 0  | 0  | 1  |

Address  
039616

When reset  
0016

|       | Bit name  | Function  | R | W |
|-------|---|---|---|---|
| TMOD0 | Operation mode select bit   | b1 b0<br>0 1 : Event counter mode   | O | C |
| TMOD1 |   |   | O | C |
| MR0   | 0 (Must always be “0” when using two-phase pulse signal processing) |   | O | C |
| MR1   | 0 (Must always be “0” when using two-phase pulse signal processing) |   | O | C |
| MR2   | 1 (Must always be “1” when using two-phase pulse signal processing) |   | O | C |
| MR3   | 0 (Must always be “0” when using two-phase pulse signal processing) |   | O | C |
| TCK0  | Count operation type select bit                                     | 0 : Reload type<br>1 : Free-run type                                      | O | C |
| TCK1  | Two-phase pulse processing operation select bit (Note)              | 0 : Normal processing operation<br>1 : Multiply-by-4 processing operation | O | C |

Figure 1.43. Timer A0 mode register in event counter mode

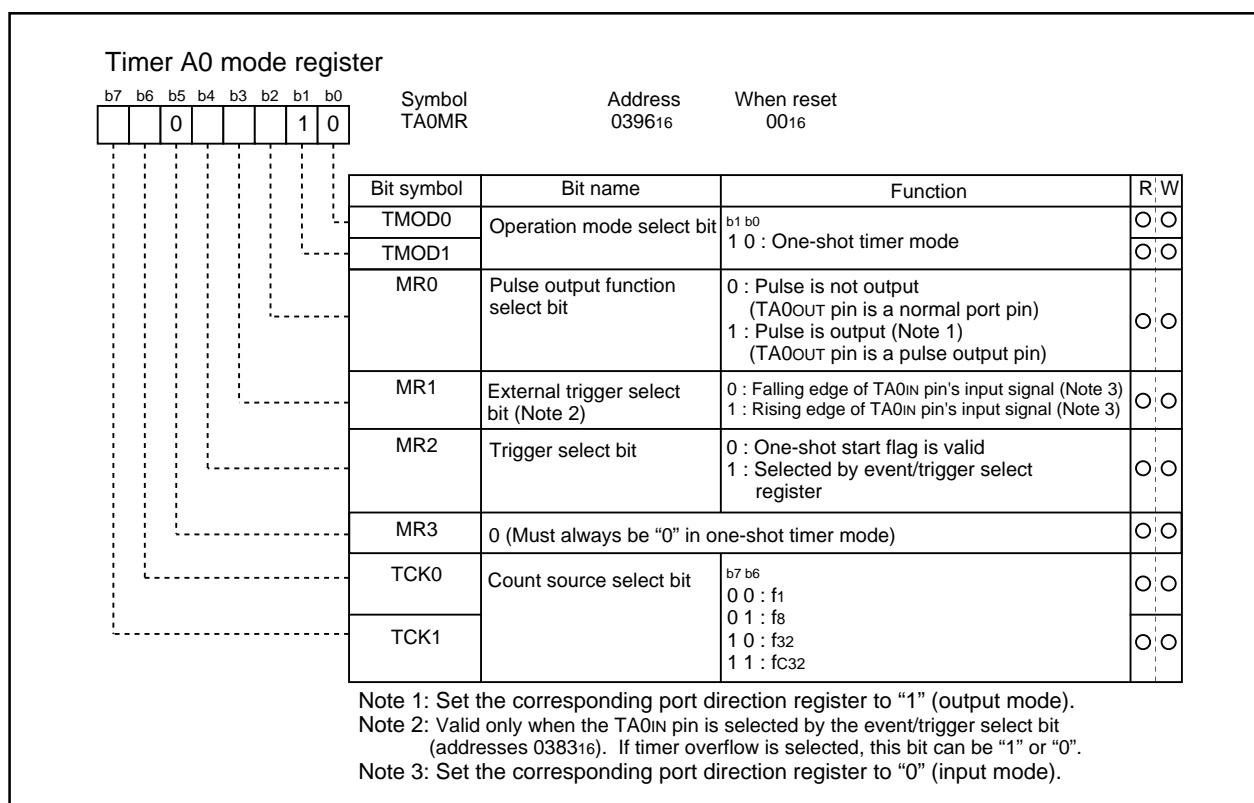
## Timer A

**(3) One-shot timer mode**

In this mode, the timer operates only once. (See Table 1.15.) When a trigger occurs, the timer starts up and continues operating for a given period. Figure 1.44 shows the timer A0 mode register in one-shot timer mode.

**Table 1.15. Timer specifications in one-shot timer mode**

| Item                                | Specification   |
|-------------------------------------|---|
| Count source                        | f1, f8, f32, fc32   |
| Count operation                     | <ul style="list-style-type: none"> <li>The timer counts down</li> <li>When the count reaches 0000<sub>16</sub>, the timer stops counting after reloading a new count</li> <li>If a trigger occurs when counting, the timer reloads a new count and restarts counting</li> </ul>   |
| Divide ratio                        | 1/n    n : Set value  |
| Count start condition               | <ul style="list-style-type: none"> <li>An external trigger is input</li> <li>The timer overflows</li> <li>The one-shot start flag is set (= 1)</li> </ul>   |
| Count stop condition                | <ul style="list-style-type: none"> <li>A new count is reloaded after the count has reached 0000<sub>16</sub></li> <li>The count start flag is reset (= 0)</li> </ul>  |
| Interrupt request generation timing | The count reaches 0000 <sub>16</sub>  |
| TA0IN pin function                  | Programmable I/O port or trigger input  |
| TA0OUT pin function                 | Programmable I/O port or pulse output   |
| Read from timer                     | When timer A0 register is read, it indicates an indeterminate value   |
| Write to timer                      | <ul style="list-style-type: none"> <li>When counting stopped<br/>When a value is written to timer A0 register, it is written to both reload register and counter</li> <li>When counting in progress<br/>When a value is written to timer A0 register, it is written to only reload register (Transferred to counter at next reload time)</li> </ul> |

**Figure 1.44. Timer A0 mode register in one-shot timer mode**



## Timer A

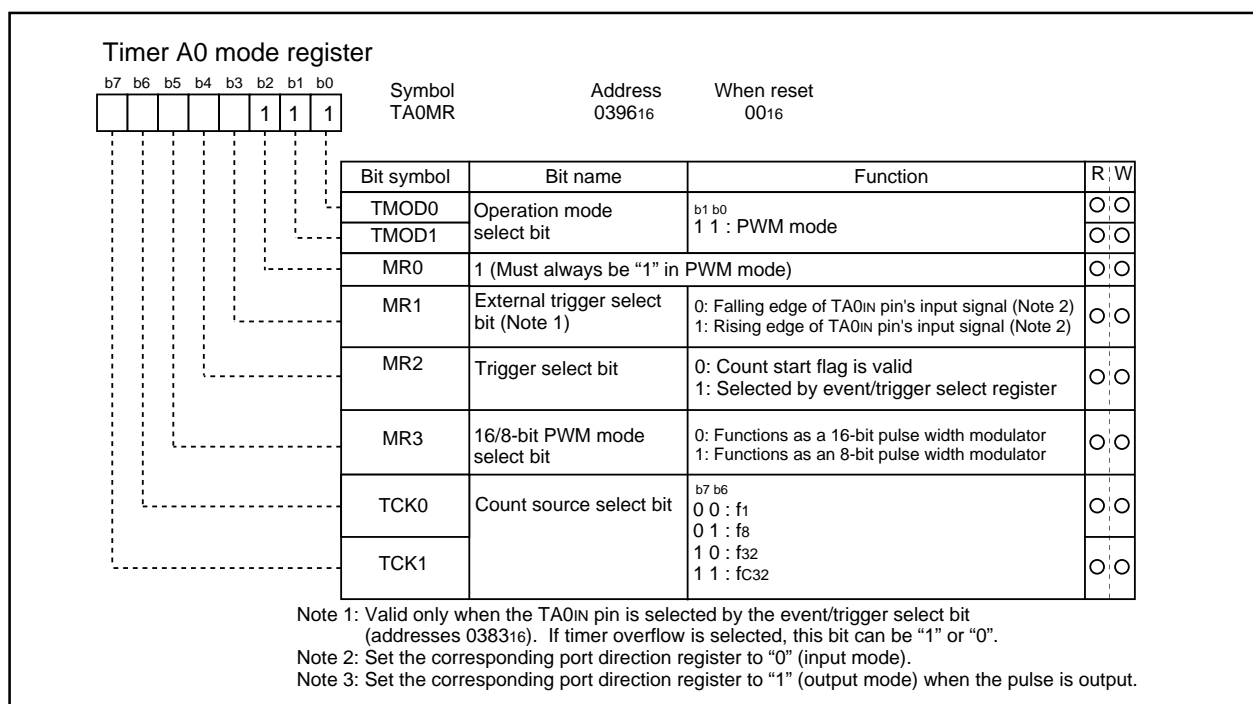
**(4) Pulse width modulation (PWM) mode**

In this mode, the timer outputs pulses of a given width in succession. (See Table 1.16.) In this mode, the counter functions as either a 16-bit pulse width modulator or an 8-bit pulse width modulator. Figure 1.45 shows the timer A0 mode register in pulse width modulation mode. Figure 1.46 shows the example of how a 16-bit pulse width modulator operates. Figure 1.47 shows the example of how an 8-bit pulse width modulator operates.

**Table 1.16. Timer specifications in pulse width modulation mode**

| Item                                |             | Specification   |
|-------------------------------------|-------------|---|
| Count source                        |             | f <sub>1</sub> , f <sub>8</sub> , f <sub>32</sub> , f <sub>c32</sub>  |
| Count operation                     |             | <ul style="list-style-type: none"> <li>The timer counts down (operating as an 8-bit or a 16-bit pulse width modulator)</li> <li>The timer reloads a new count at a rising edge of PWM pulse and continues counting</li> <li>The timer is not affected by a trigger that occurs when counting</li> </ul>                                       |
| 16-bit PWM                          |             | <ul style="list-style-type: none"> <li>High level width <math>n / f_i</math> <math>n</math>: Set value</li> <li>Cycle time <math>(2^{16}-1) / f_i</math> fixed</li> </ul>   |
| 8-bit PWM                           |             | <ul style="list-style-type: none"> <li>High level width <math>n \times (m+1) / f_i</math> <math>n</math>: values set to timer A0 register's high-order address</li> <li>Cycle time <math>(2^8-1) \times (m+1) / f_i</math> <math>m</math>: values set to timer A0 register's low-order address</li> </ul>                                     |
| Count start condition               |             | <ul style="list-style-type: none"> <li>External trigger is input</li> <li>The timer overflows</li> <li>The count start flag is set (= 1)</li> </ul>   |
| Count stop condition                |             | The count start flag is reset (= 0)   |
| Interrupt request generation timing | 8 bits PWM  | <ul style="list-style-type: none"> <li>Set value of "H" level width is except FF<sub>16</sub>, 00<sub>16</sub>: PWM pulse goes "L"</li> <li>Set value of "H" level width is FF<sub>16</sub>, 00<sub>16</sub>: Timing that count value goes to 01<sub>16</sub></li> </ul>  |
|                                     | 16 bits PWM | <ul style="list-style-type: none"> <li>Set value of "H" level width is except FFFF<sub>16</sub>, 0000<sub>16</sub>: PWM pulse goes "L"</li> <li>Set value of "H" level width is FFFF<sub>16</sub>, 0000<sub>16</sub>: Timing that count value goes to 0001<sub>16</sub></li> </ul>  |
| TA0IN pin function                  |             | Programmable I/O port or trigger input  |
| TA0OUT pin function                 |             | Pulse output  |
| Read from timer                     |             | When timer A0 register is read, it indicates an indeterminate value   |
| Write to timer                      |             | <ul style="list-style-type: none"> <li>When counting stopped: When a value is written to timer A0 register, it is written to both reload register and counter</li> <li>When counting in progress: When a value is written to timer A0 register, it is written to only reload register (Transferred to counter at next reload time)</li> </ul> |

Note: When set value of "H" level width is 00<sub>16</sub> or 0000<sub>16</sub>, pulse outputs "L" level and inversion value, FF<sub>16</sub> or FFFF<sub>16</sub> is set to timer.

**Figure 1.45. Timer A0 mode register in pulse width modulation mode**

## Timer A

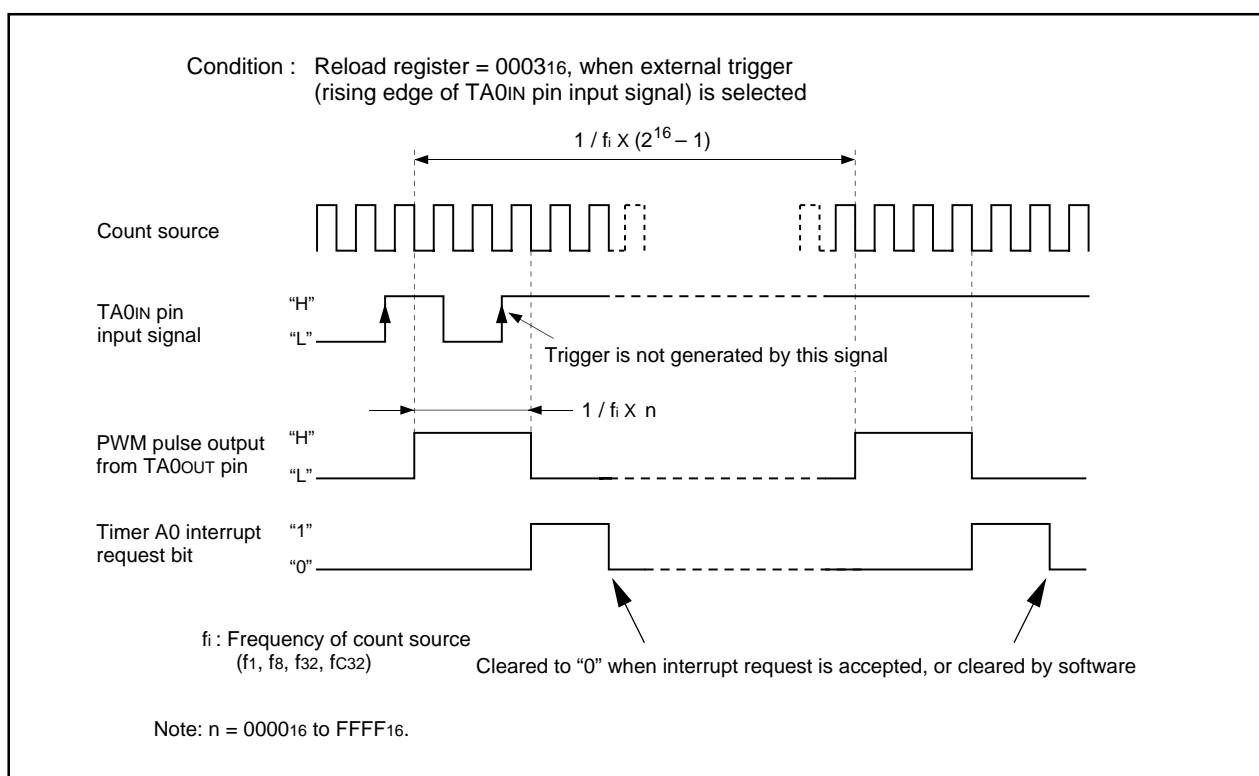


Figure 1.46. Example of how a 16-bit pulse width modulator operates

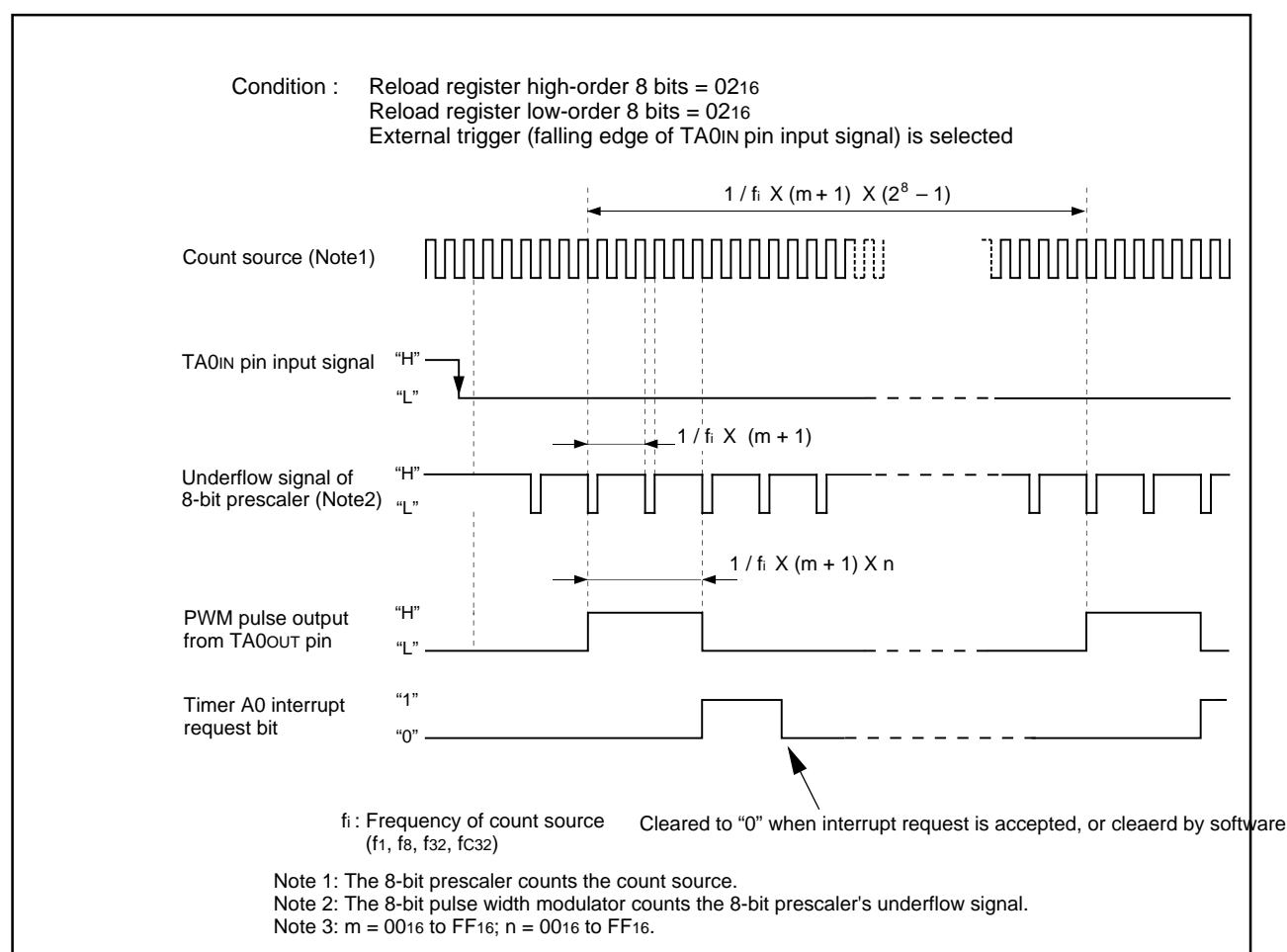


Figure 1.47. Example of how an 8-bit pulse width modulator operates

## Timer B

## Timer B

Figure 1.48 shows the block diagram of timer B. Figures 1.49 and 1.50 show the timer B-related registers. Use the timer Bi mode register (i = 0, 1) bits 0 and 1 to choose the desired mode.

Timer B has three operation modes listed as follows:

- Timer mode : The timer counts an internal count source.
- Event counter mode : The timer counts pulses from an external source or a timer overflow.
- Pulse period/pulse width measuring mode : The timer measures an external signal's pulse period or pulse width.

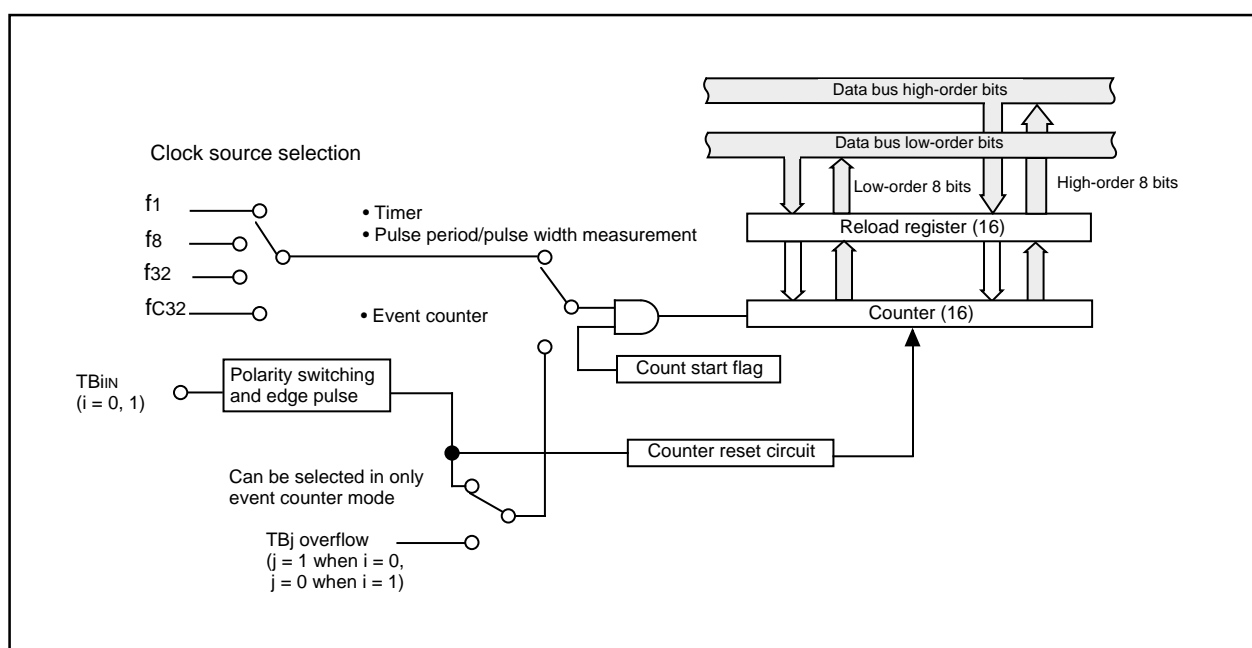


Figure 1.48. Block diagram of timer B

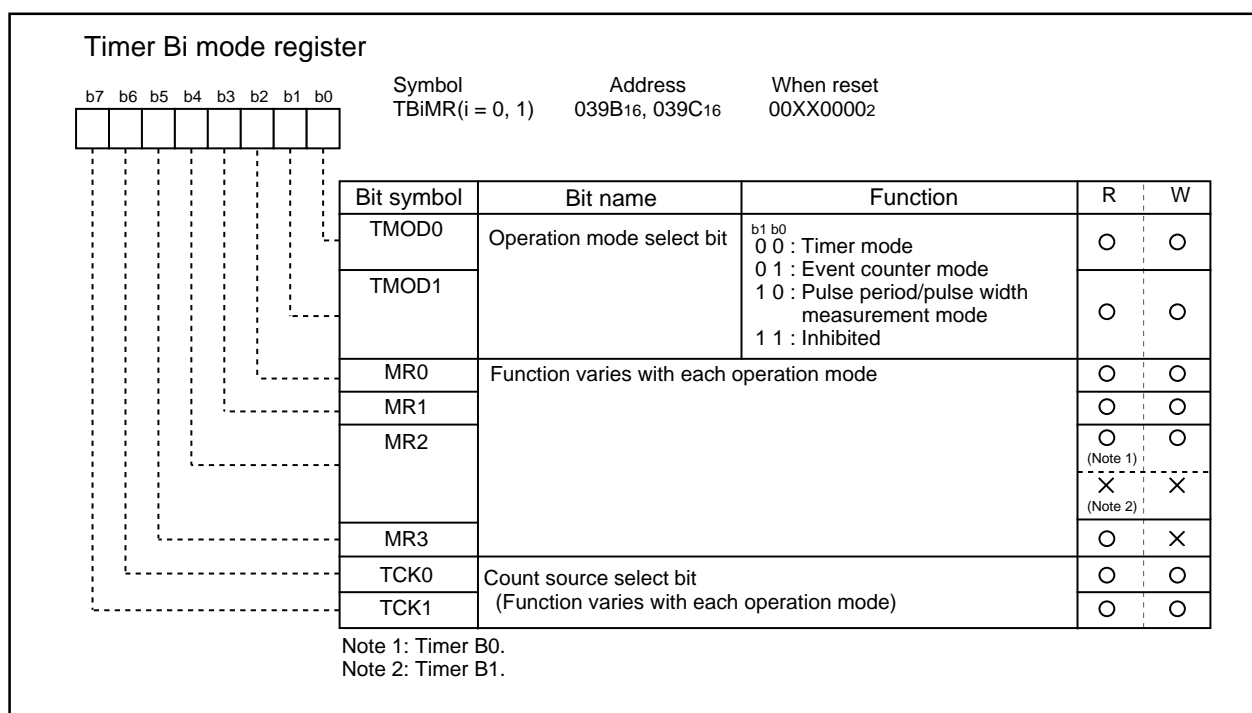


Figure 1.49. Timer B-related registers (1)

## Timer B

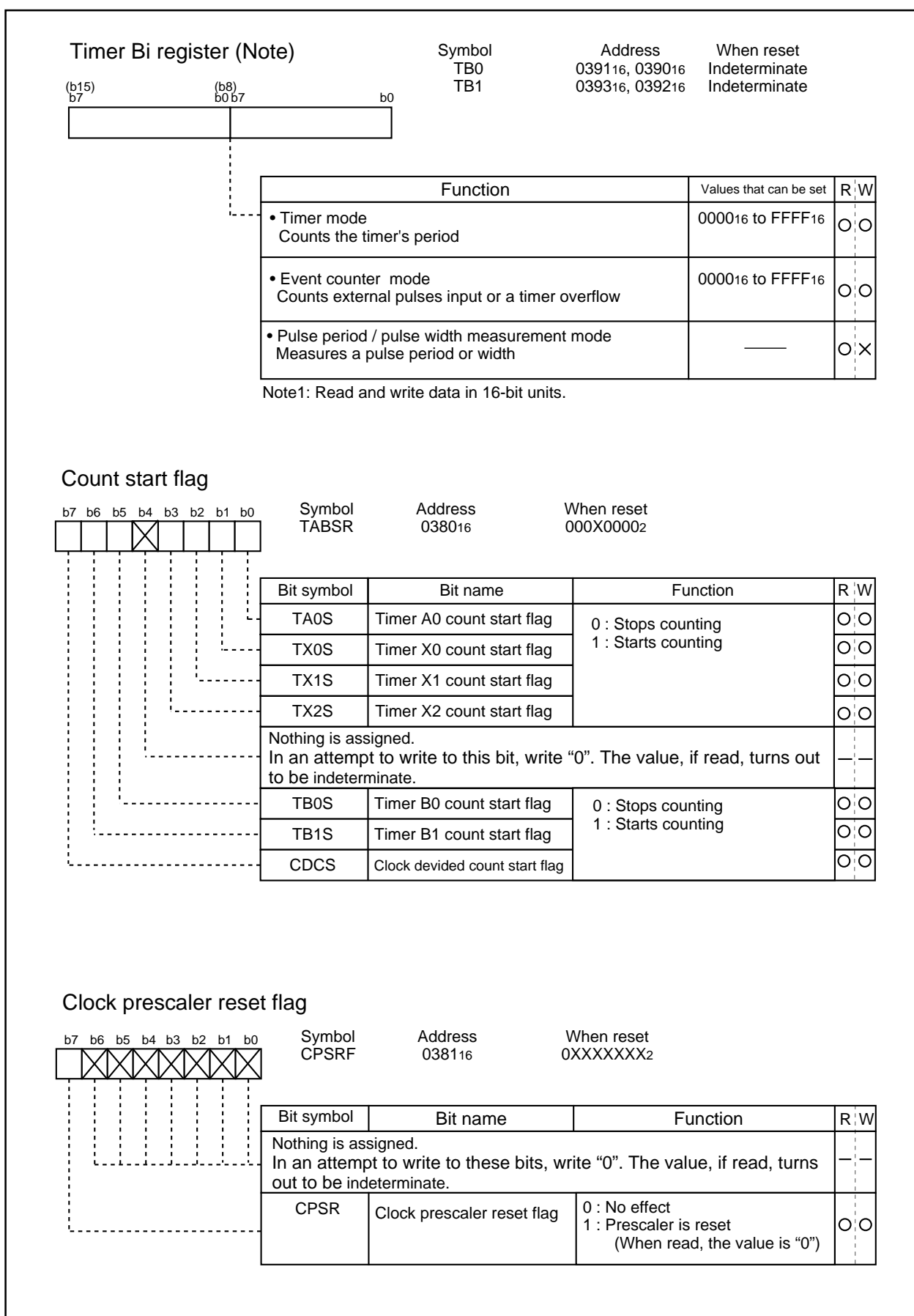


Figure 1.50. Timer B-related registers (2)

## Timer B

## (1) Timer mode

In this mode, the timer counts an internally generated count source. (See Table 1.17.) Figure 1.51 shows the timer Bi mode register in timer mode.

Table 1.17. Timer specifications in timer mode

| Item                                | Specification   |
|-------------------------------------|---|
| Count source                        | f1, f8, f32, fC32   |
| Count operation                     | <ul style="list-style-type: none"> <li>Counts down</li> <li>When the timer underflows, it reloads the reload register contents before continuing counting</li> </ul>  |
| Divide ratio                        | $1/(n+1)$ n : Set value   |
| Count start condition               | Count start flag is set (= 1)   |
| Count stop condition                | Count start flag is reset (= 0)   |
| Interrupt request generation timing | The timer underflows  |
| TBiIN pin function                  | Programmable I/O port   |
| Read from timer                     | Count value is read out by reading timer Bi register  |
| Write to timer                      | <ul style="list-style-type: none"> <li>When counting stopped<br/>When a value is written to timer Bi register, it is written to both reload register and counter</li> <li>When counting in progress<br/>When a value is written to timer Bi register, it is written to only reload register (Transferred to counter at next reload time)</li> </ul> |

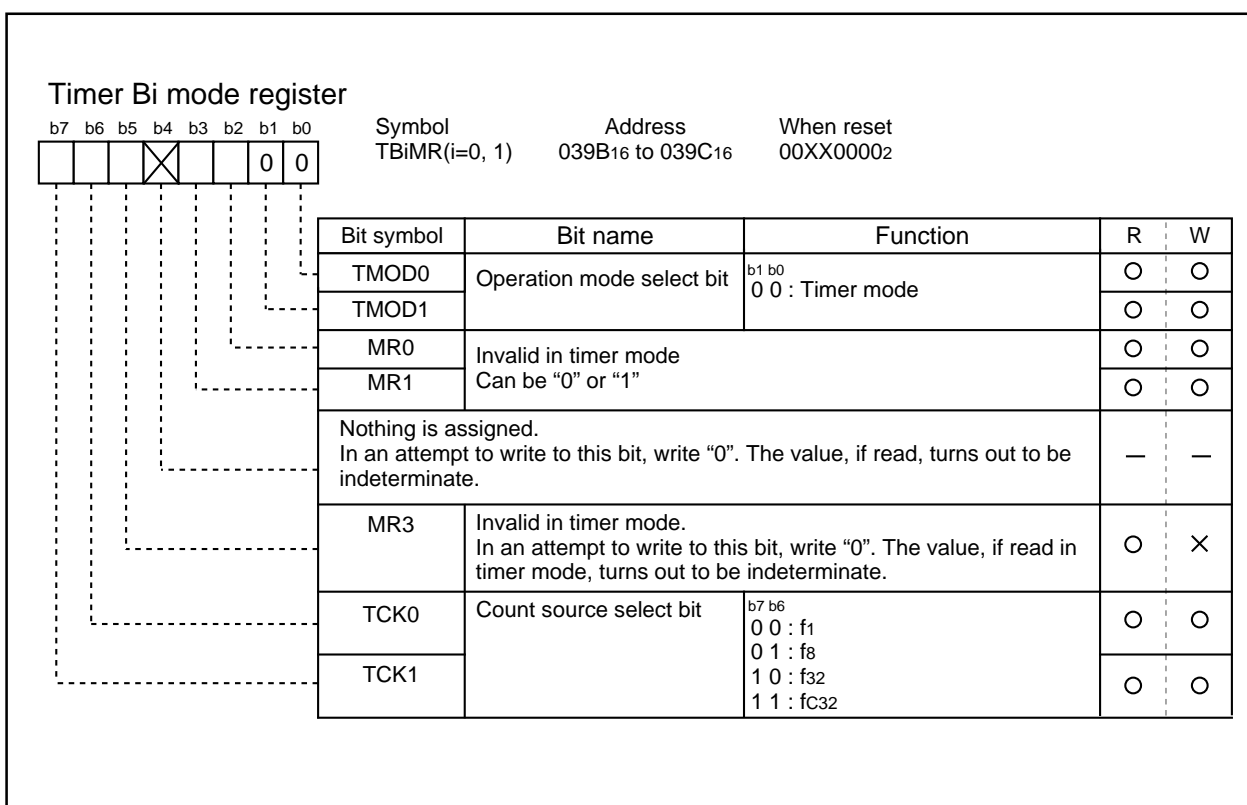


Figure 1.51. Timer Bi mode register in timer mode



## Timer B

**(3) Pulse period/pulse width measurement mode**

In this mode, the timer measures the pulse period or pulse width of an external signal. (See Table 1.19.)

Figure 1.53 shows the timer Bi mode register in pulse period/pulse width measurement mode. Figure

1.54 shows the operation timing when measuring a pulse period. Figure 1.55 shows the operation timing

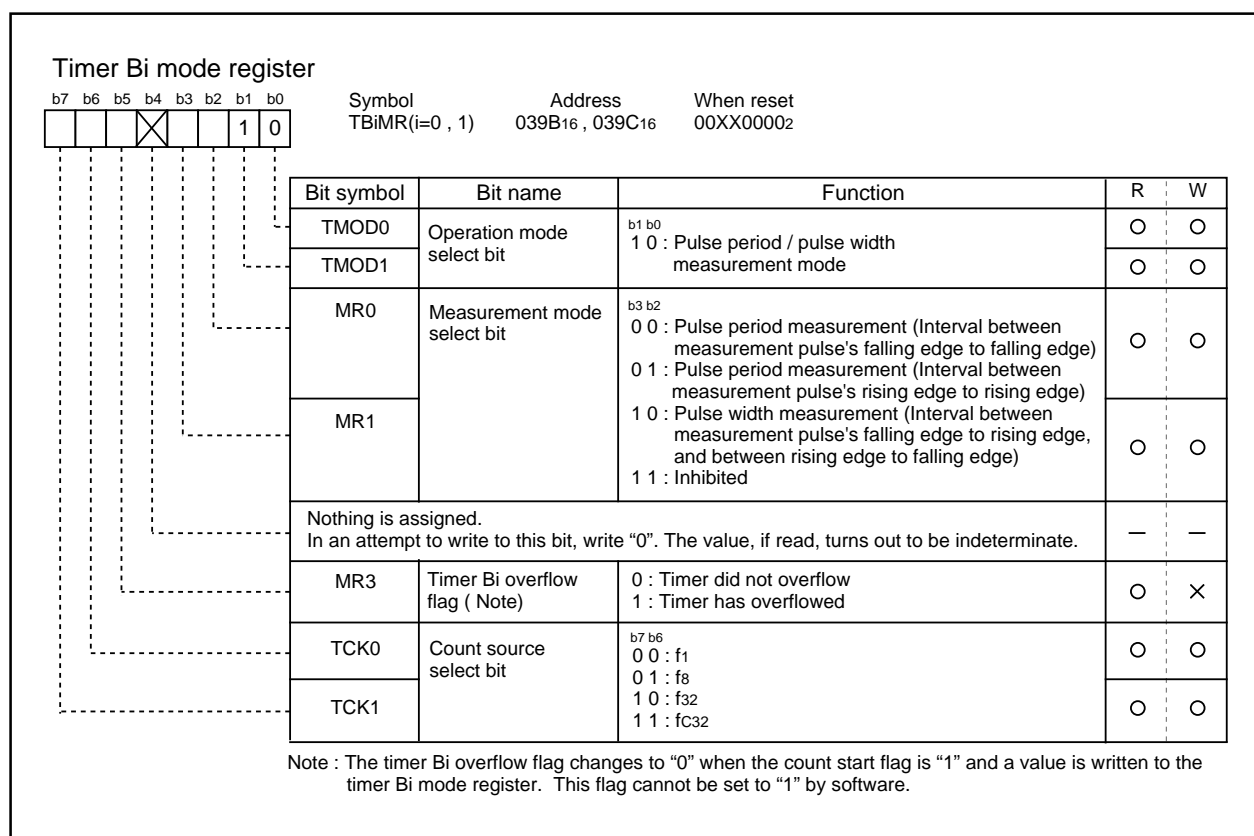
when measuring a pulse width.

**Table 1.19. Timer specifications in pulse period/pulse width measurement mode**

| Item                                | Specification   |
|-------------------------------------|---|
| Count source                        | f1, f8, f32, fc32   |
| Count operation                     | <ul style="list-style-type: none"> <li>• Up count</li> <li>• Counter value "000016" is transferred to reload register at measurement pulse's effective edge and the timer continues counting</li> </ul>   |
| Count start condition               | Count start flag is set (= 1)   |
| Count stop condition                | Count start flag is reset (= 0)   |
| Interrupt request generation timing | <ul style="list-style-type: none"> <li>• When measurement pulse's effective edge is input (Note 1)</li> <li>• When an overflow occurs. (Simultaneously, the timer Bi overflow flag changes to "1". The timer Bi overflow flag changes to "0" when the count start flag is "1" and a value is written to the timer Bi mode register.)</li> </ul> |
| TBiIN pin function                  | Measurement pulse input   |
| Read from timer                     | When timer Bi register is read, it indicates the reload register's content (measurement result) (Note 2)  |
| Write to timer                      | Cannot be written to  |

Note 1: An interrupt request is not generated when the first effective edge is input after the timer has started counting.

Note 2: The value read out from the timer Bi register is indeterminate until the second effective edge is input after the timer.



**Figure 1.53. Timer Bi mode register in pulse period/pulse width measurement mode**

## Timer B

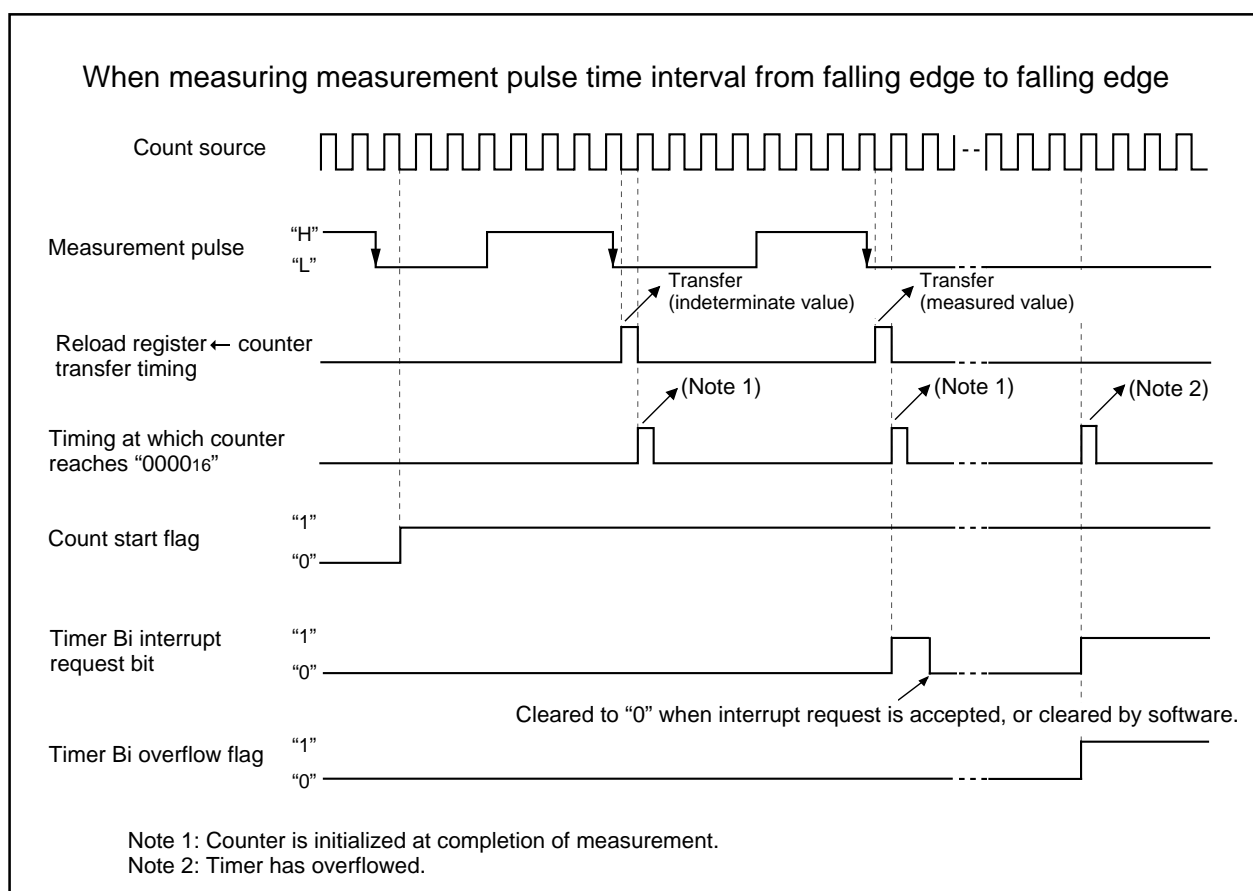


Figure 1.54. Operation timing when measuring a pulse period

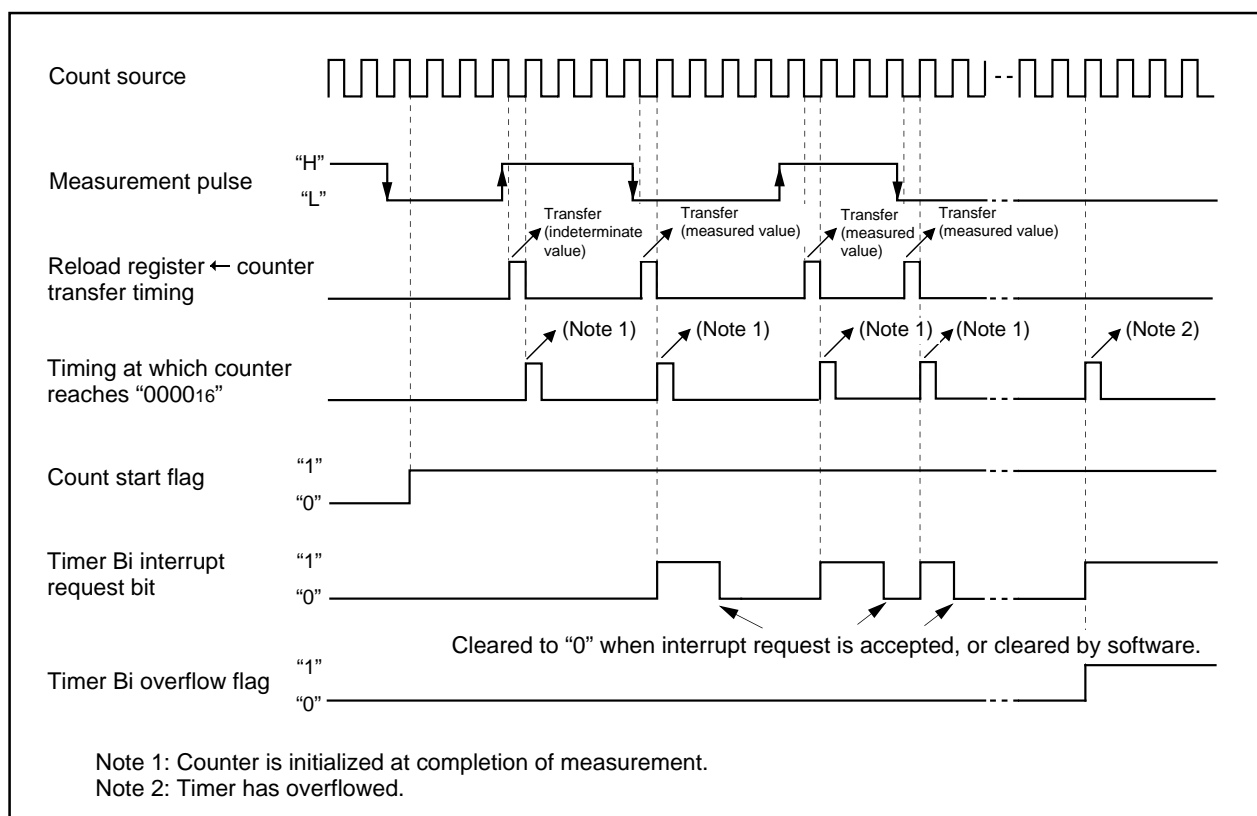


Figure 1.55. Operation timing when measuring a pulse width





## Timer X

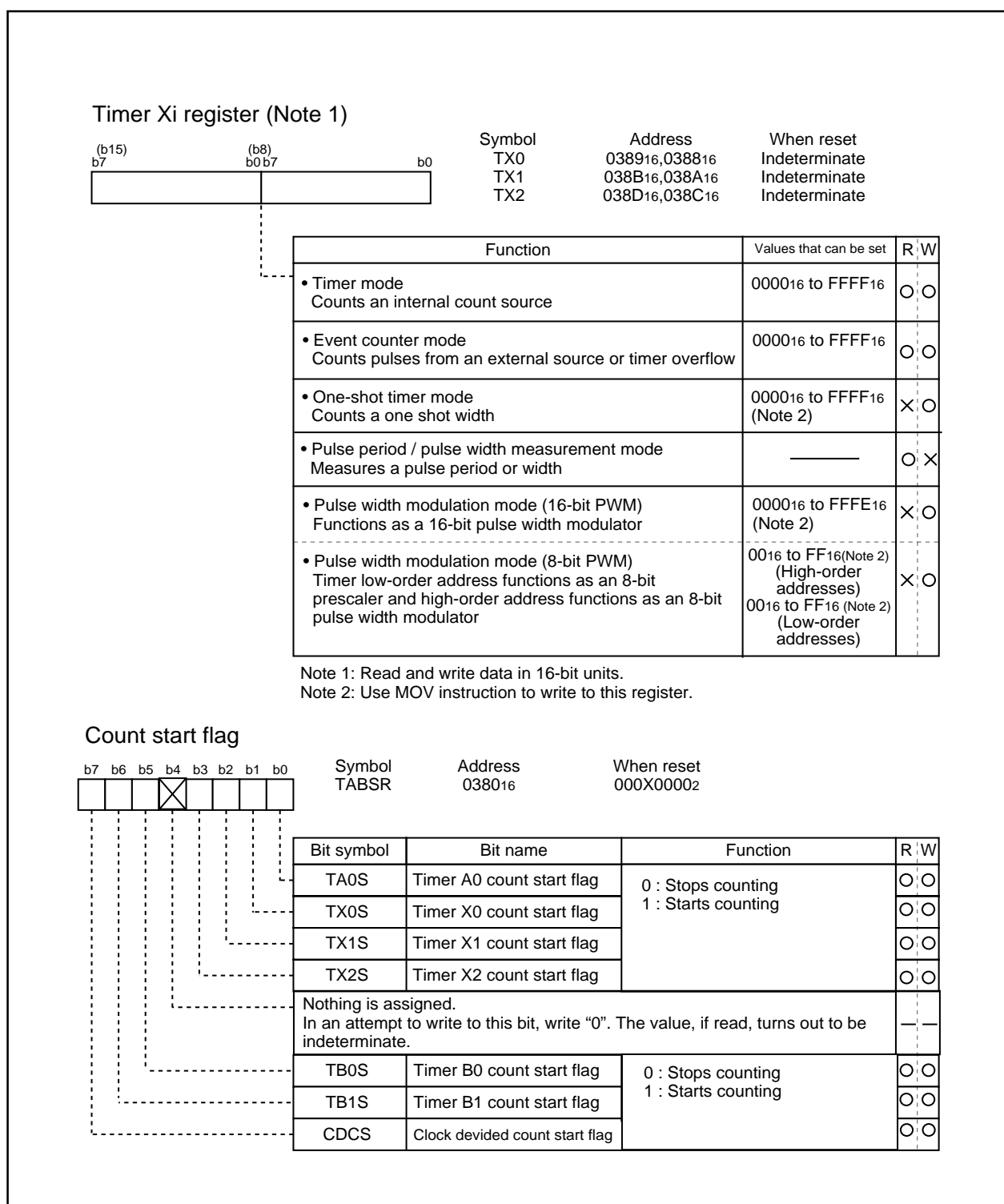


Figure 1.58. Timer X-related registers (2)

## Timer X

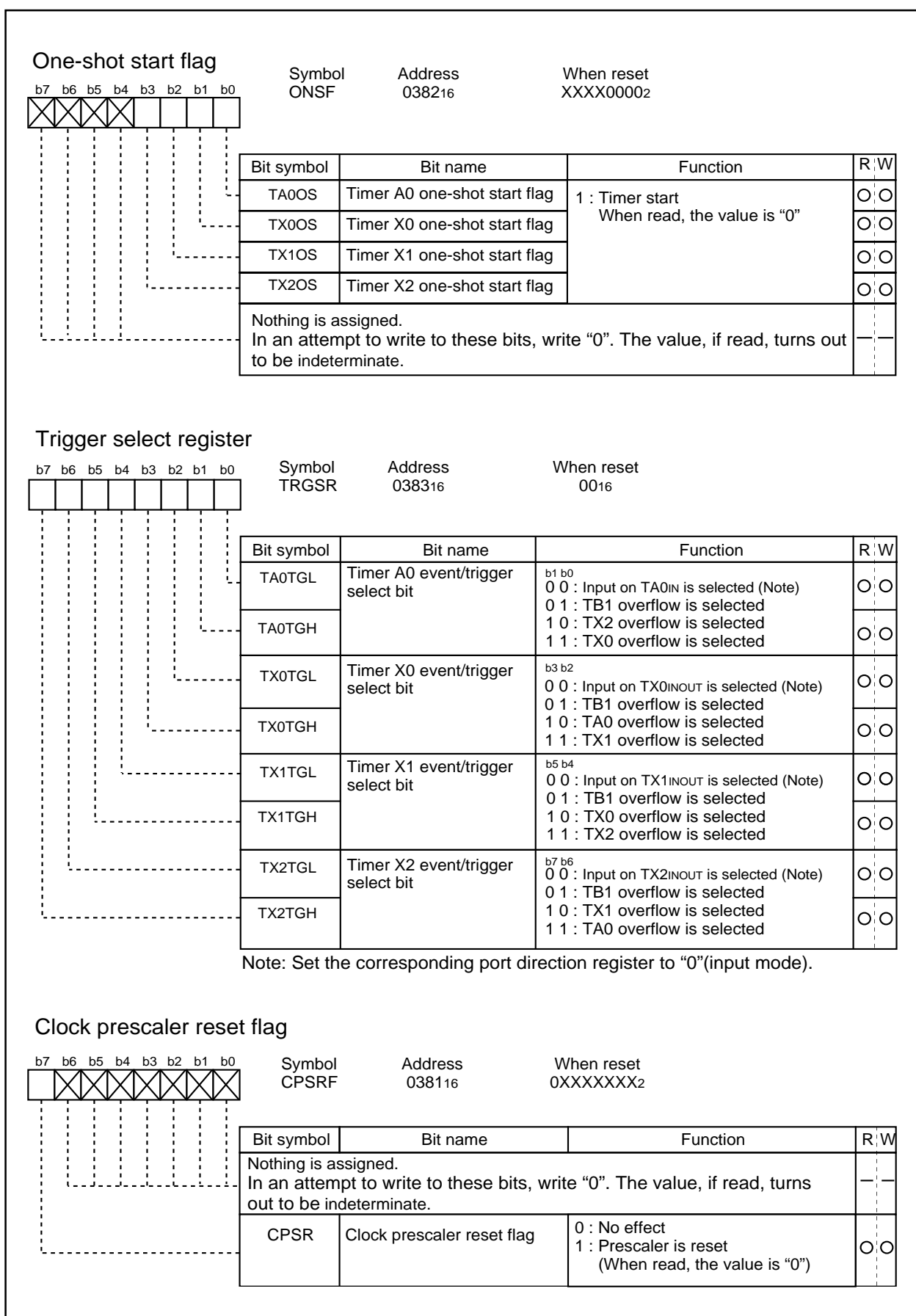


Figure 1.59. Timer X-related registers (3)

## Timer X

**(1) Timer mode**

In this mode, the timer counts an internally generated count source. (See Table 1.20.) Figure 1.60 shows the timer Xi mode register in timer mode.

**Table 1.20. Specifications of timer mode**

| Item                                | Specification   |
|-------------------------------------|---|
| Count source                        | f <sub>1</sub> , f <sub>8</sub> , f <sub>32</sub> , f <sub>C32</sub>  |
| Count operation                     | <ul style="list-style-type: none"> <li>• Down count</li> <li>• When the timer underflows, it reloads the reload register contents before continuing counting</li> </ul>   |
| Divide ratio                        | 1/(n+1)    n : Set value  |
| Count start condition               | Count start flag is set (= 1)   |
| Count stop condition                | Count start flag is reset (= 0)   |
| Interrupt request generation timing | When the timer underflows   |
| TXiINOUT pin function               | Programmable I/O port, gate input or pulse output   |
| Read from timer                     | Count value can be read out by reading timer Xi register  |
| Write to timer                      | <ul style="list-style-type: none"> <li>• When counting stopped<br/>When a value is written to timer Xi register, it is written to both reload register and counter</li> <li>• When counting in progress<br/>When a value is written to timer Xi register, it is written to only reload register (Transferred to counter at next reload time)</li> </ul> |
| Select function                     | <ul style="list-style-type: none"> <li>• Gate function<br/>Counting can be started and stopped by the TXiINOUT pin's input signal</li> <li>• Pulse output function<br/>Each time the timer underflows, the TXiINOUT pin's polarity is reversed</li> </ul>   |

**Timer Xi mode register**

|  |  |  |  |  |  |  |  |                   |   |   |     |
|--|--|--|--|--|--|--|--|-------------------|---|---|-----|
| <div><div><div>b7</div><div>b6</div><div>b5</div><div>b4</div><div>b3</div><div>b2</div><div>b1</div><div>b0</div></div><div><div></div><div></div><div>0</div><div></div><div></div><div></div><div>0</div><div>0</div></div></div> |  |  |  |  |  |  |  | Symbol            | Address                                       | When reset  |     |
|  |  |  |  |  |  |  |  | TXiMR(i = 0 to 2) | 0397 <sub>16</sub> to 0399 <sub>16</sub>      | 00 <sub>16</sub>  |     |
|  |  |  |  |  |  |  |  | Bit symbol        | Bit name                                      | Function  | R/W |
|  |  |  |  |  |  |  |  | TMOD0             | Operation mode select bit                     | b1 b0<br>0 0 : Timer mode   | ○ ○ |
|  |  |  |  |  |  |  |  | TMOD1             |   |   | ○ ○ |
|  |  |  |  |  |  |  |  | MR0               | Pulse output function select bit              | 0 : Pulse is not output<br>(TXiINOUT pin is a normal port pin)<br>1 : Pulse is output (Note 1)<br>(TXiINOUT pin is a pulse output pin)  | ○ ○ |
|  |  |  |  |  |  |  |  | MR1               | Gate function select bit                      | b4 b3<br>0 X (Note 2): Gate function not available<br>(TXiINOUT pin is a normal port pin)<br>1 0 : Timer counts only when TXiINOUT pin is held "L" (Note 3)<br>1 1 : Timer counts only when TXiINOUT pin is held "H" (Note 3) | ○ ○ |
|  |  |  |  |  |  |  |  | MR2               |   |   | ○ ○ |
|  |  |  |  |  |  |  |  | MR3               | 0 (Must always be fixed to "0" in timer mode) |   | ○ ○ |
|  |  |  |  |  |  |  |  | TCK0              | Count source select bit                       | b7 b6<br>0 0 : f <sub>1</sub><br>0 1 : f <sub>8</sub><br>1 0 : f <sub>32</sub><br>1 1 : f <sub>C32</sub>  | ○ ○ |
|  |  |  |  |  |  |  |  | TCK1              |   |   | ○ ○ |

Note 1: Set the corresponding port direction register to "1" (output mode). Gate function cannot be selected when pulse output function is selected.

Note 2: The bit can be "0" or "1".

Note 3: Set the corresponding port direction register to "0" (input mode). Pulse output function cannot be selected when gate function is selected.

**Figure 1.60. Timer Xi mode register in timer mode**

## Timer X

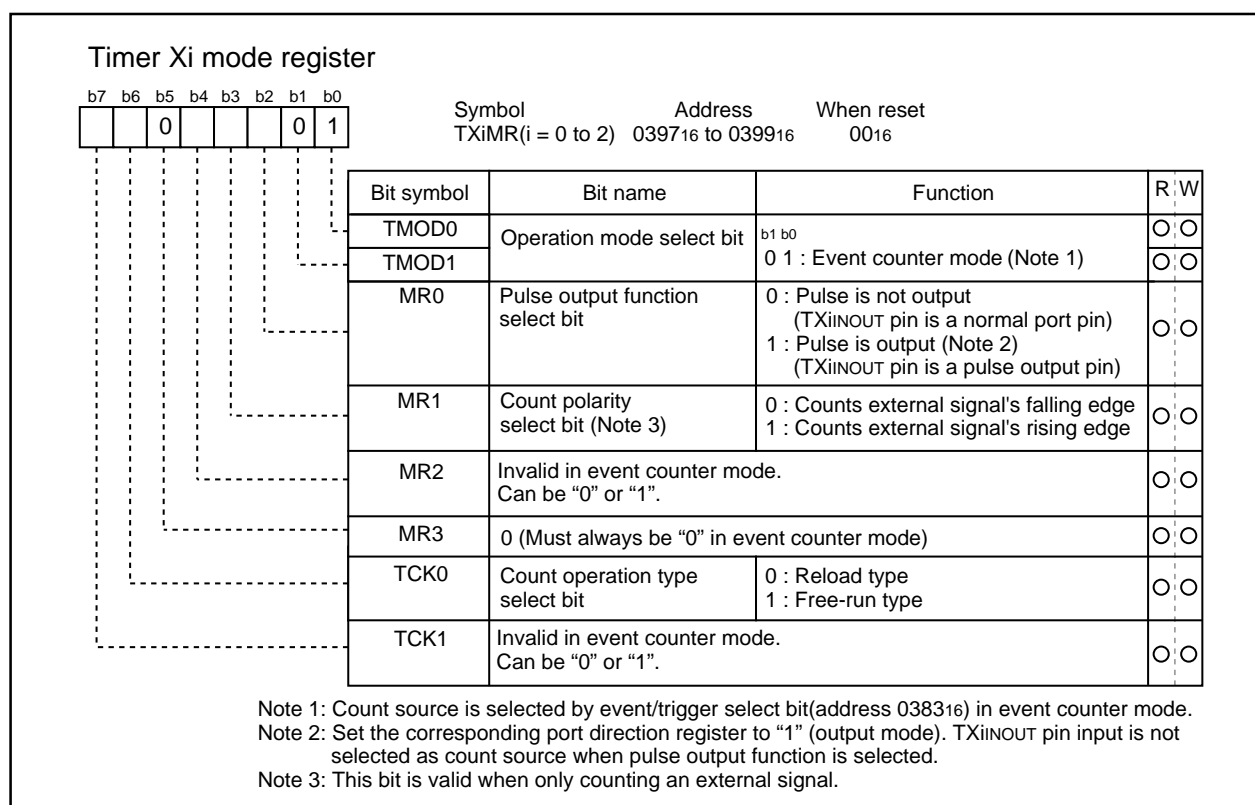
**(2) Event counter mode**

In this mode, the timer counts an external signal or an internal timer's overflow. (See Table 1.21.) Figure 1.61 shows the timer Xi mode register in event counter mode.

**Table 1.21. Timer specifications in event counter mode (when not processing two-phase pulse signal)**

| Item                                | Specification   |
|-------------------------------------|---|
| Count source                        | <ul style="list-style-type: none"> <li>External signals input to TXiINOUT pin (effective edge can be selected by software)</li> <li>TB1 overflow, TA0 overflow, TXi overflow</li> </ul>   |
| Count operation                     | <ul style="list-style-type: none"> <li>Down count</li> <li>When the timer underflows, it reloads the reload register contents before continuing counting (Note)</li> </ul>  |
| Divide ratio                        | $1/(n + 1)$ $n$ : Set value   |
| Count start condition               | Count start flag is set (= 1)   |
| Count stop condition                | Count start flag is reset (= 0)   |
| Interrupt request generation timing | The timer underflows  |
| TXiINOUT pin function               | Programmable I/O port, count source input or pulse output   |
| Read from timer                     | Count value can be read out by reading timer Xi register  |
| Write to timer                      | <ul style="list-style-type: none"> <li>When counting stopped<br/>When a value is written to timer Xi register, it is written to both reload register and counter</li> <li>When counting in progress<br/>When a value is written to timer Xi register, it is written to only reload register (Transferred to counter at next reload time)</li> </ul> |
| Select function                     | <ul style="list-style-type: none"> <li>Free-run count function<br/>Even when the timer underflows, the reload register content is not reloaded to it</li> <li>Pulse output function<br/>Each time the timer underflows, the TXiINOUT pin's polarity is reversed</li> </ul>  |

Note: This does not apply when the free-run function is selected.

**Figure 1.61. Timer Xi mode register in event counter mode**

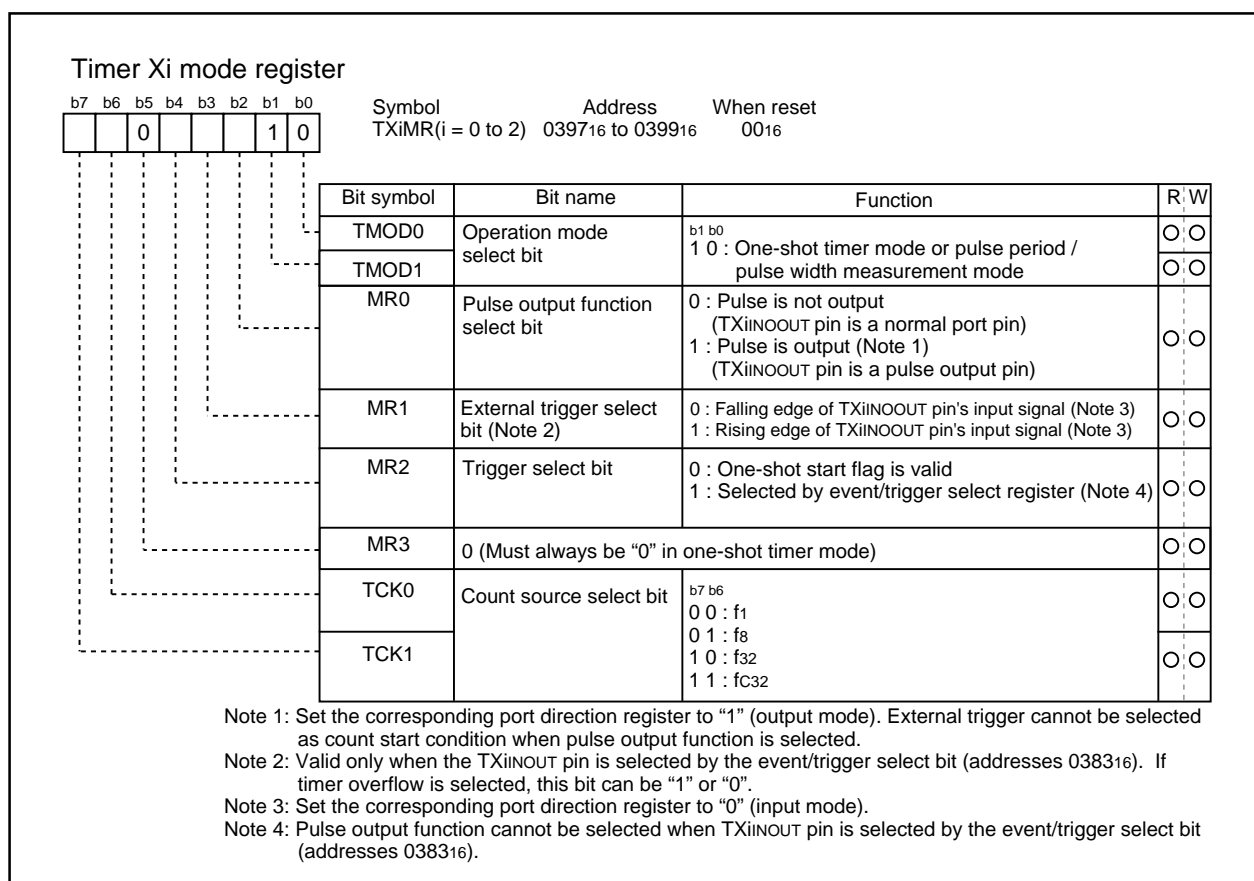
## Timer X

**(3) One-shot timer mode**

In this mode, the timer operates only once. (See Table 1.22.) When a trigger occurs, the timer starts up and continues operating for a given period. Figure 1.62 shows the timer Xi mode register in one-shot timer mode.

**Table 1.22. Timer specifications in one-shot timer mode**

| Item                                | Specification   |
|-------------------------------------|---|
| Count source                        | f <sub>1</sub> , f <sub>8</sub> , f <sub>32</sub> , f <sub>C32</sub>  |
| Count operation                     | <ul style="list-style-type: none"> <li>The timer counts down</li> <li>When the count reaches 0000<sub>16</sub>, the timer stops counting after reloading a new count</li> <li>If a trigger occurs when counting, the timer reloads a new count and restarts counting</li> </ul>   |
| Divide ratio                        | 1/n    n : Set value  |
| Count start condition               | <ul style="list-style-type: none"> <li>An external trigger is input</li> <li>The timer overflows</li> <li>The one-shot start flag is set (= 1)</li> </ul>   |
| Count stop condition                | <ul style="list-style-type: none"> <li>A new count is reloaded after the count has reached 0000<sub>16</sub></li> <li>The count start flag is reset (= 0)</li> </ul>  |
| Interrupt request generation timing | The count reaches 0000 <sub>16</sub>  |
| TXiNOOUT pin function               | Programmable I/O port, trigger input or pulse output  |
| Read from timer                     | When timer Xi register is read, it indicates an indeterminate value   |
| Write to timer                      | <ul style="list-style-type: none"> <li>When counting stopped<br/>When a value is written to timer Xi register, it is written to both reload register and counter</li> <li>When counting in progress<br/>When a value is written to timer Xi register, it is written to only reload register (Transferred to counter at next reload time)</li> </ul> |

**Figure 1.62. Timer Xi mode register in one-shot timer mode**

## Timer X

**(4) Pulse period/pulse width measurement mode**

In this mode, the timer measures the pulse period or pulse width of an external signal. (See Table 1.23.)

Figure 1.63 shows the timer Xi mode register in pulse period/pulse width measurement mode. Figure

1.64 shows the operation timing when measuring a pulse period. Figure 1.65 shows the operation timing

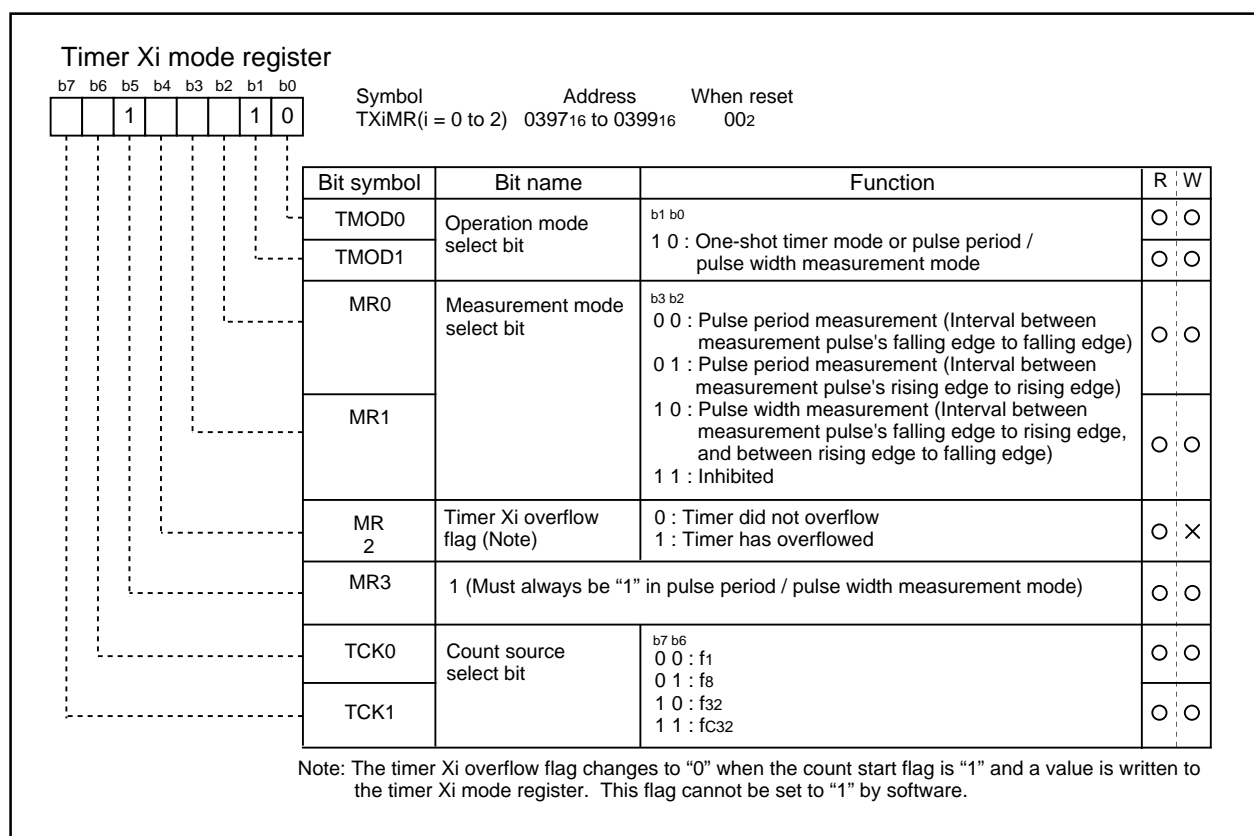
when measuring a pulse width.

**Table 1.23. Timer specifications in pulse period/pulse width measurement mode**

| Item                                | Specification   |
|-------------------------------------|---|
| Count source                        | f1, f8, f32, fc32   |
| Count operation                     | <ul style="list-style-type: none"> <li>• Up count</li> <li>• Counter value "000016" is transferred to reload register at measurement pulse's effective edge and the timer continues counting</li> </ul>   |
| Count start condition               | Count start flag is set (= 1)   |
| Count stop condition                | Count start flag is reset (= 0)   |
| Interrupt request generation timing | <ul style="list-style-type: none"> <li>• When measurement pulse's effective edge is input (Note 1)</li> <li>• When an overflow occurs. (Simultaneously, the timer Xi overflow flag changes to "1". The timer Xi overflow flag changes to "0" when the count start flag is "1" and a value is written to the timer Xi mode register.)</li> </ul> |
| TXiINOUT pin function               | Measurement pulse input   |
| Read from timer                     | When timer Xi register is read, it indicates the reload register's content (measurement result) (Note 2)  |
| Write to timer                      | Cannot be written to  |

Note 1: An interrupt request is not generated when the first effective edge is input after the timer has started counting.

Note 2: The value read out from the timer Xi register is indeterminate until the second effective edge is input after the timer.



**Figure 1.63. Timer Xi mode register in pulse period/pulse width measurement mode**

## Timer X

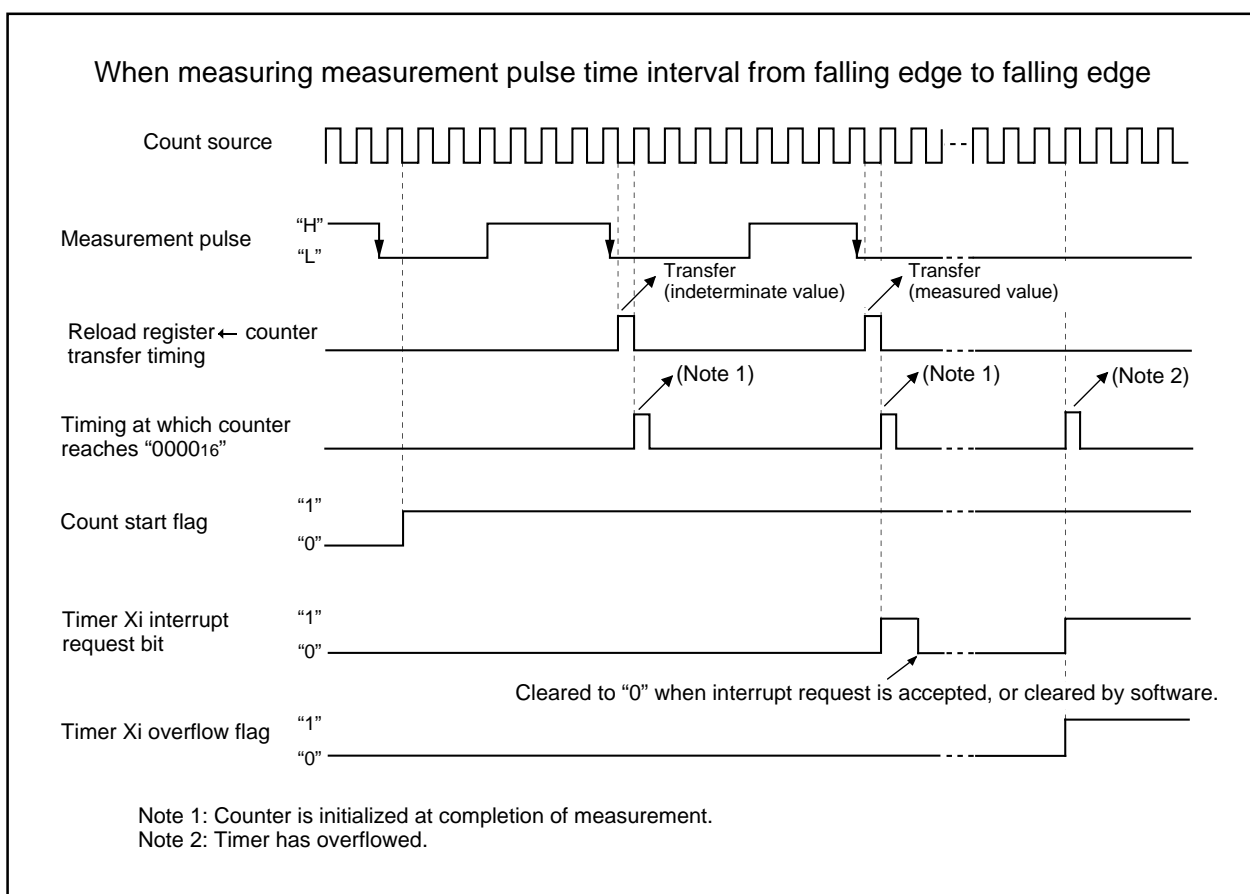


Figure 1.64. Operation timing when measuring a pulse period

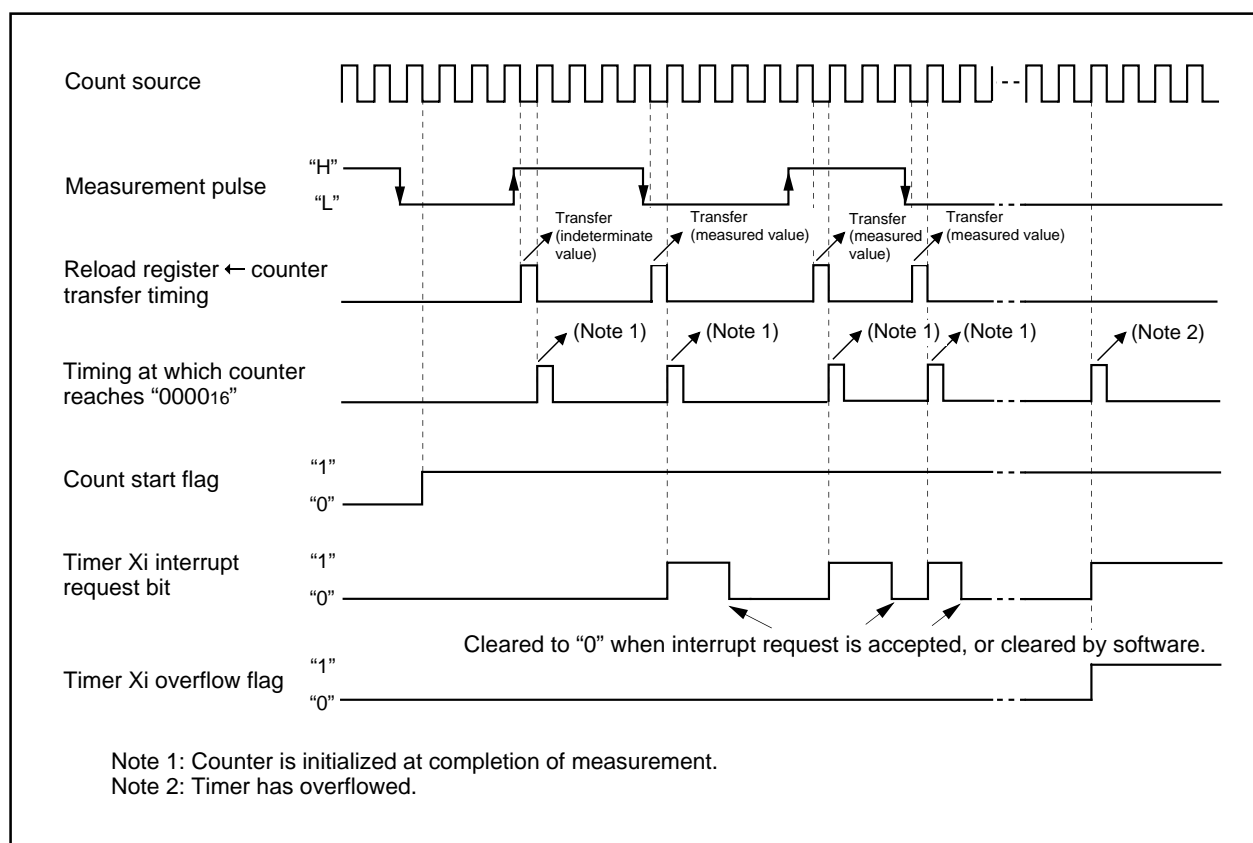


Figure 1.65. Operation timing when measuring a pulse width



## Timer X

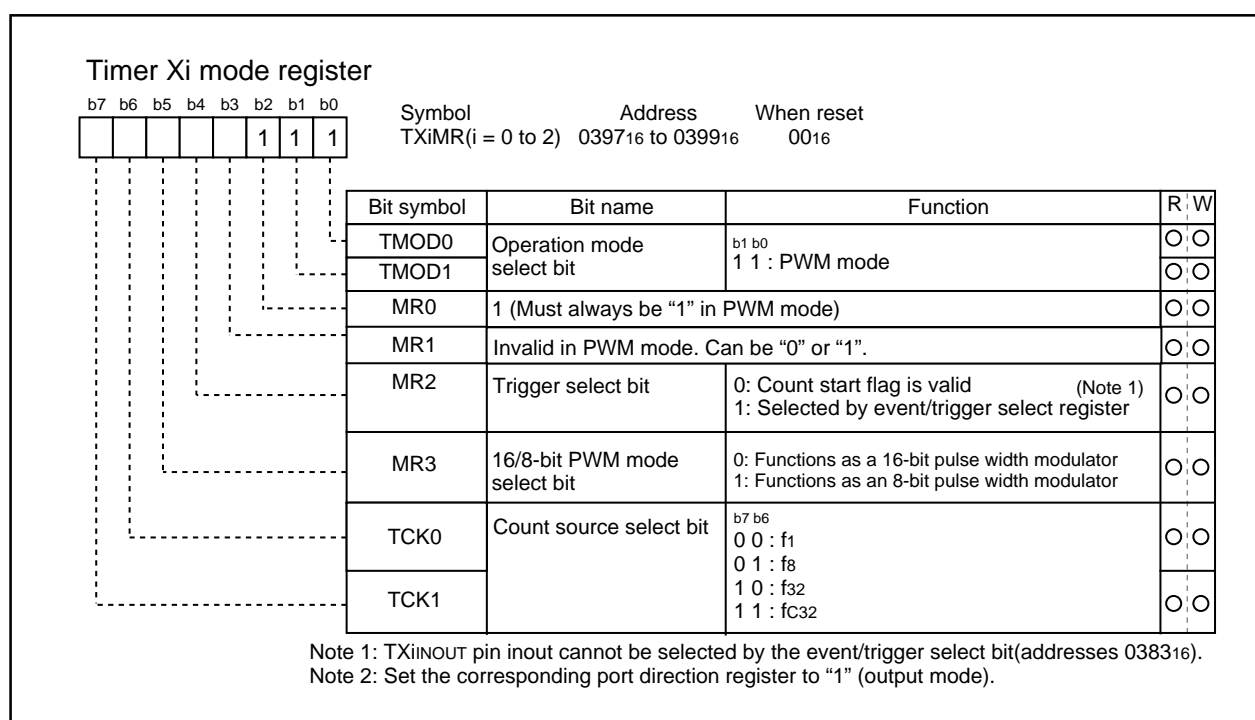
**(5) Pulse width modulation (PWM) mode**

In this mode, the timer outputs pulses of a given width in succession. (See Table 1.24.) In this mode, the counter functions as either a 16-bit pulse width modulator or an 8-bit pulse width modulator. Figure 1.66 shows the timer Xi mode register in pulse width modulation mode. Figure 1.67 shows the example of how a 16-bit pulse width modulator operates. Figure 1.68 shows the example of how an 8-bit pulse width modulator operates.

**Table 1.24. Timer specifications in pulse width modulation mode**

| Item                                |             | Specification   |
|-------------------------------------|-------------|---|
| Count source                        |             | f1, f8, f32, fc32   |
| Count operation                     |             | <ul style="list-style-type: none"> <li>Down counts (operating as an 8-bit or a 16-bit pulse width modulator)</li> <li>The timer reloads a new count at a rising edge of PWM pulse and continues counting</li> <li>The timer is not affected by a trigger that occurs when counting</li> </ul>   |
| 16-bit PWM                          |             | <ul style="list-style-type: none"> <li>"H" level width <math>n / f_i</math> <span style="float: right;">n : Set value</span></li> <li>Cycle time <math>(2^{16}-1) / f_i</math> fixed</li> </ul>   |
| 8-bit PWM                           |             | <ul style="list-style-type: none"> <li>"H" level width <math>n \times (m+1) / f_i</math> n: values set to timer Xi register's high-order address</li> <li>Cycle time <math>(2^8-1) \times (m+1) / f_i</math> m : values set to timer Xi register's low-order address</li> </ul>   |
| Count start condition               |             | <ul style="list-style-type: none"> <li>The timer overflows</li> <li>The count start flag is set (= 1)</li> </ul>  |
| Count stop condition                |             | <ul style="list-style-type: none"> <li>The count start flag is reset (= 0)</li> </ul>   |
| Interrupt request generation timing | 8 bits PWM  | <ul style="list-style-type: none"> <li>Set value of "H" level width is except FF<sub>16</sub>, 00<sub>16</sub> : PWM pulse goes "L"</li> <li>Set value of "H" level width is FF<sub>16</sub>, 00<sub>16</sub> : Timing that count value goes to 01<sub>16</sub></li> </ul>  |
|                                     | 16 bits PWM | <ul style="list-style-type: none"> <li>Set value of "H" level width is except FFFF<sub>16</sub>, 0000<sub>16</sub> : PWM pulse goes "L"</li> <li>Set value of "H" level width is FFFF<sub>16</sub>, 0000<sub>16</sub> : Timing that count value goes to 0001<sub>16</sub></li> </ul>  |
| TXiINOUT pin function               |             | Pulse output  |
| Read from timer                     |             | When timer Xi register is read, it indicates an indeterminate value   |
| Write to timer                      |             | <ul style="list-style-type: none"> <li>When counting stopped<br/>When a value is written to timer Xi register, it is written to both reload register and counter</li> <li>When counting in progress<br/>When a value is written to timer Xi register, it is written to only reload register (Transferred to counter at next reload time)</li> </ul> |

Note: When set value of "H" level width is 00<sub>16</sub> or 0000<sub>16</sub>, pulse outputs "L" level and inversion value, FF<sub>16</sub> or FFFF<sub>16</sub> is set to timer.

**Figure 1.66. Timer Xi mode register in pulse width modulation mode**

## Timer X

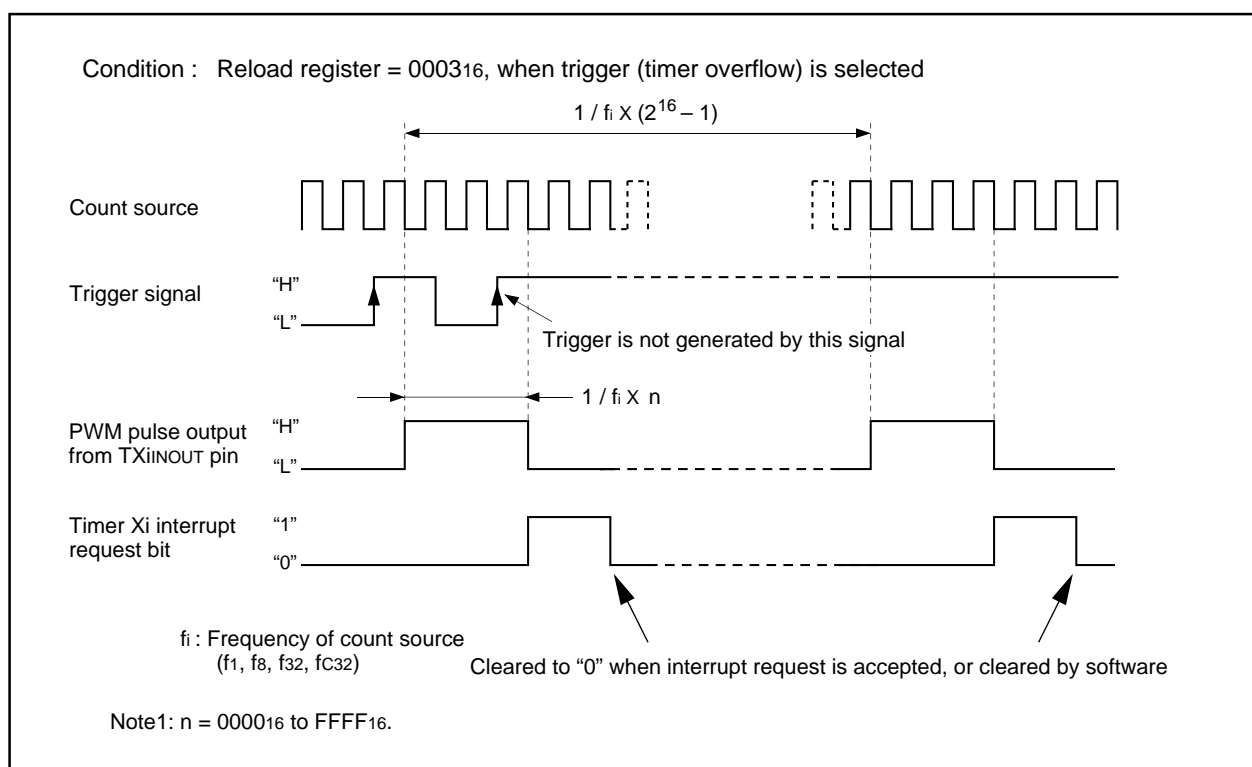


Figure 1.67. Example of how a 16-bit pulse width modulator operates

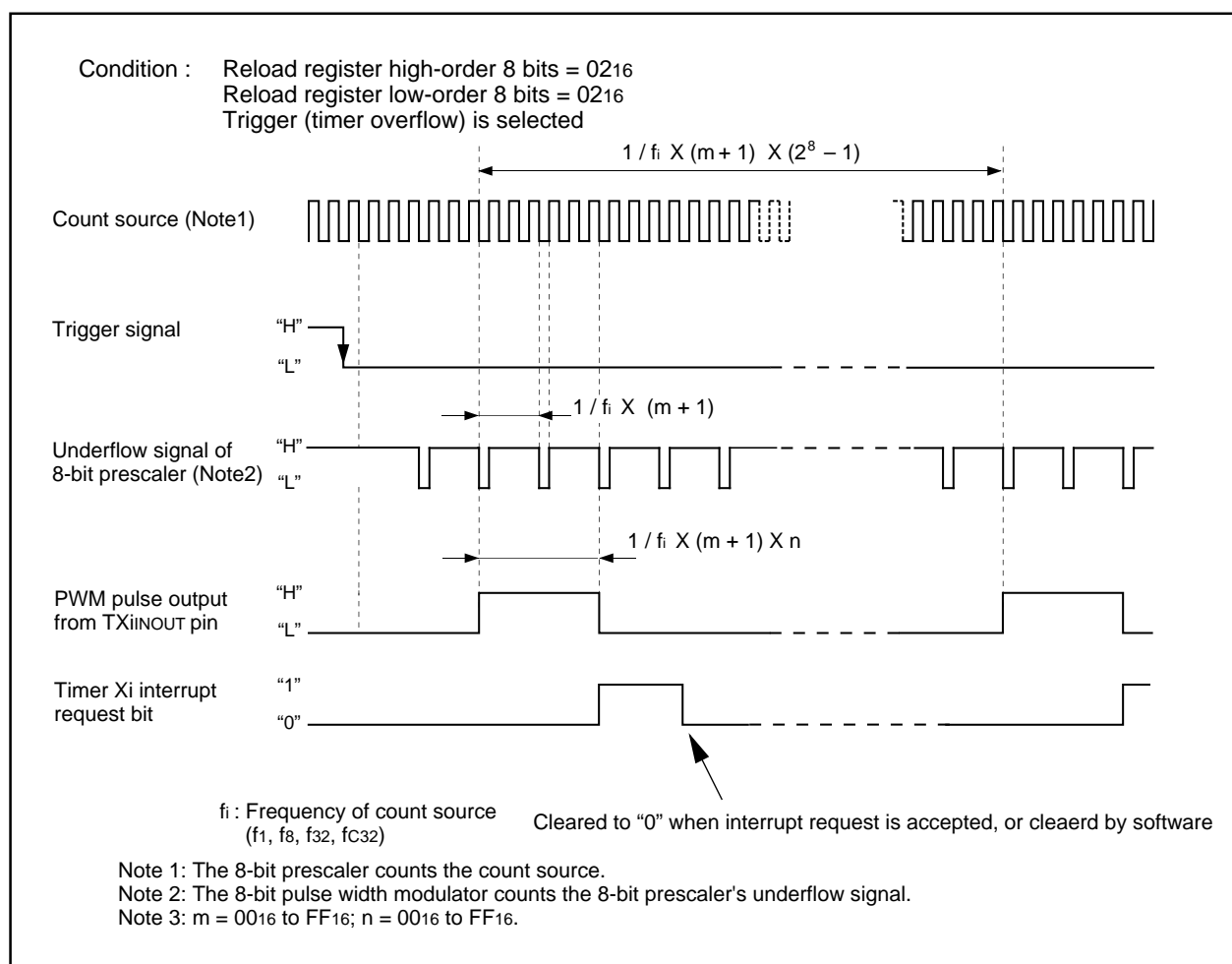


Figure 1.68. Example of how an 8-bit pulse width modulator operates

## Serial I/O

## Serial I/O

Serial I/O is configured as two channels: UART0 and UART1.

UART0 and UART1 each have an exclusive timer to generate a transfer clock, so they operate independently of each other.

Figure 1.69 shows the block diagram of UART0 and UART1. Figure 1.70 shows the block diagram of the transmit/receive unit.

UART0 has two operation modes: a clock synchronous serial I/O mode and a clock asynchronous serial I/O mode (UART mode). The contents of the serial I/O mode select bits (bits 0 to 2 at addresses 03A0<sub>16</sub> and 03A8<sub>16</sub>) determine whether UART0 is used as a clock synchronous serial I/O or as a UART.

UART1 is used as a UART only.

Figures 1.71 through 1.73 show the registers related to UARTi.

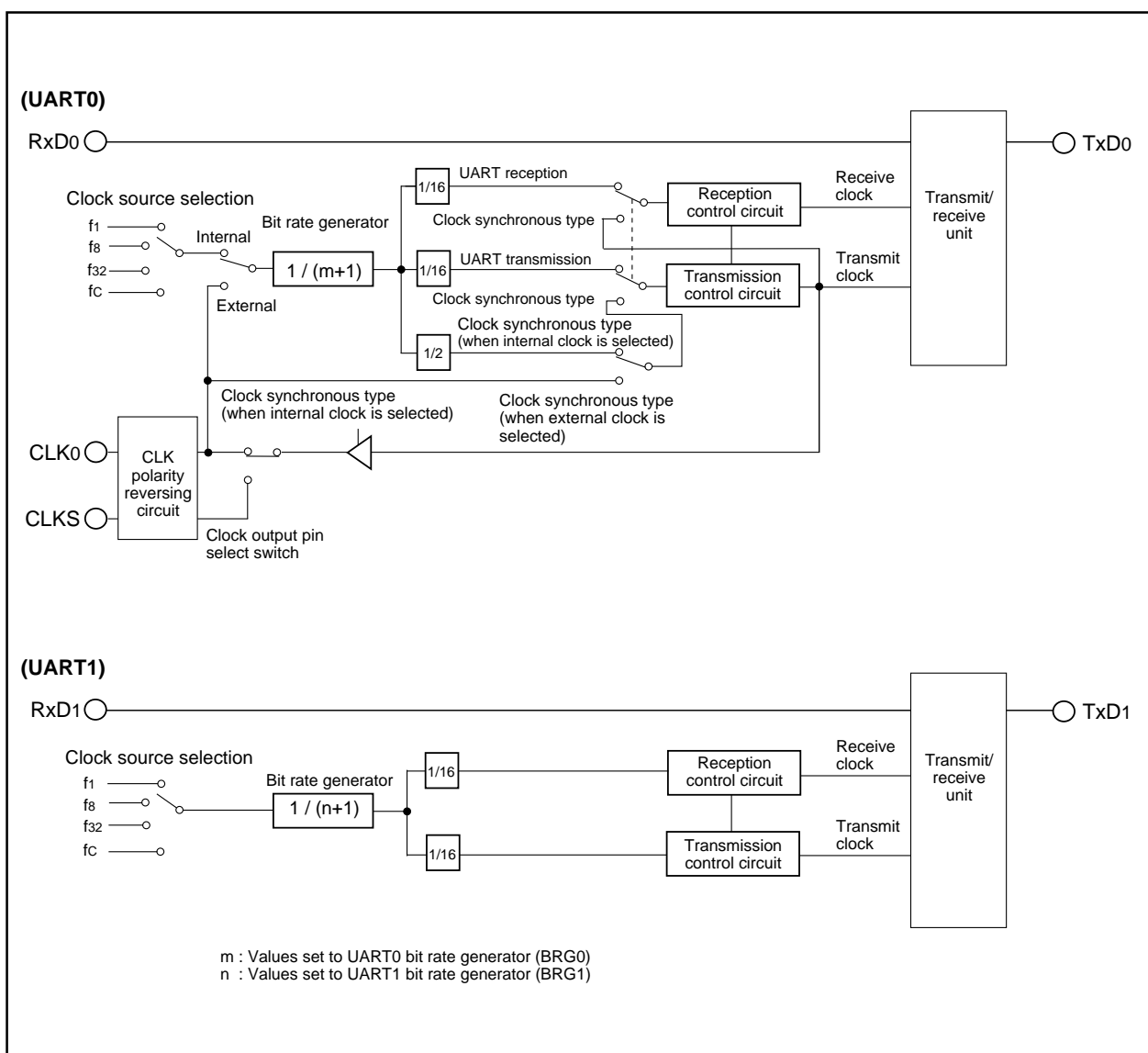


Figure 1.69. Block diagram of UARTi (i = 0, 1)

## Serial I/O

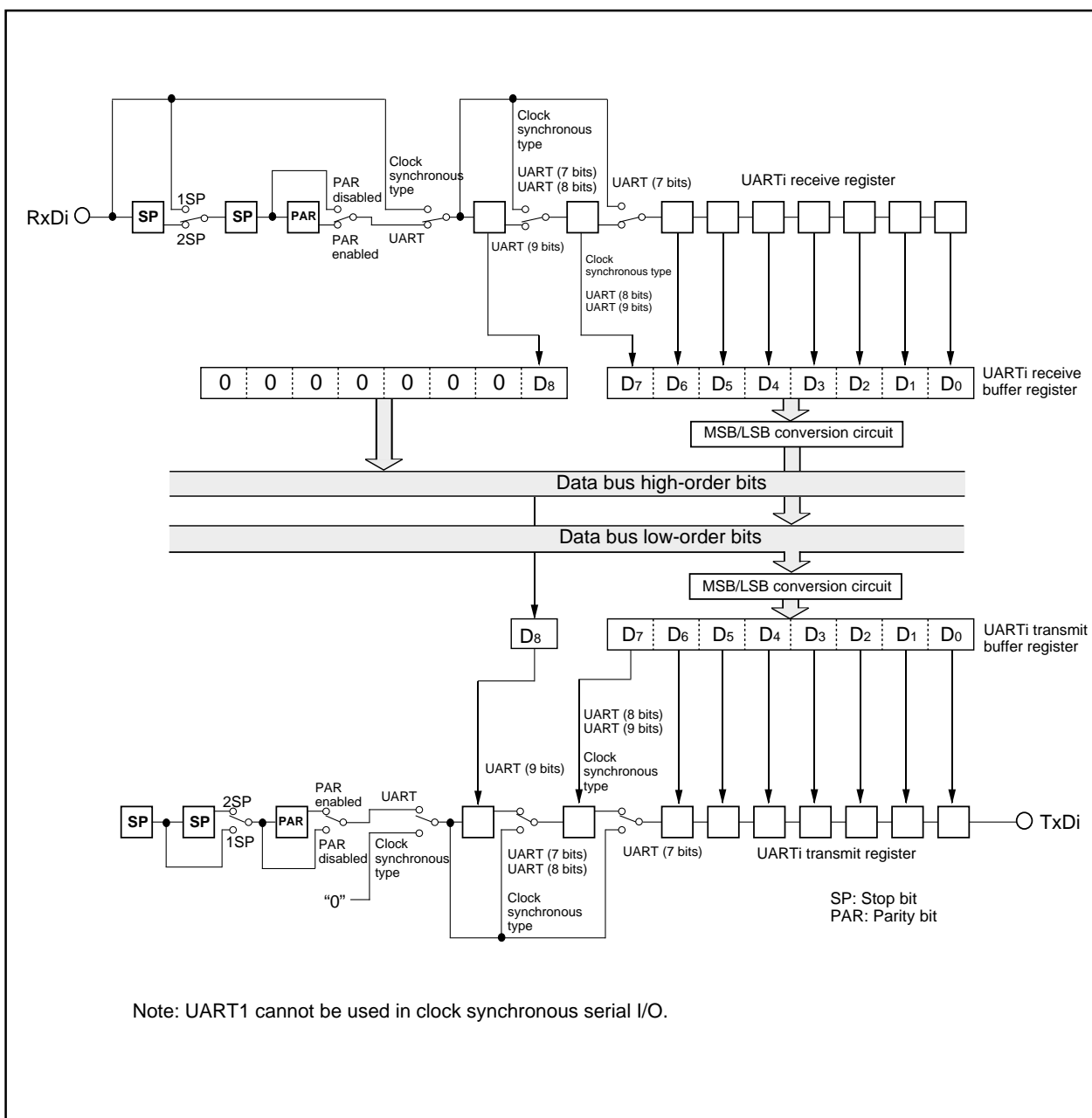


Figure 1.70. Block diagram of transmit/receive unit

## Serial I/O

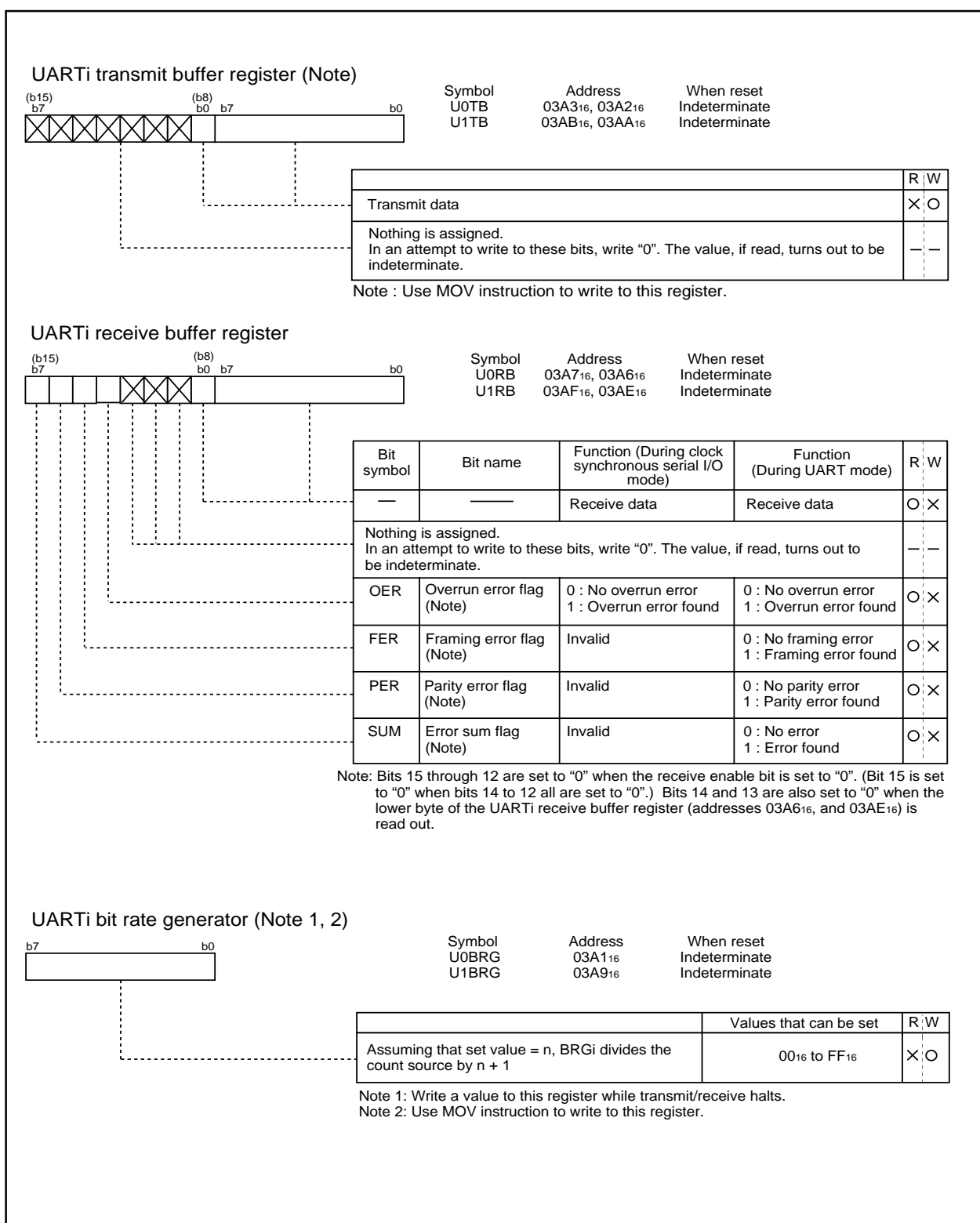
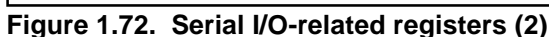
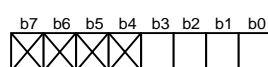


Figure 1.71. Serial I/O-related registers (1)



## Serial I/O

## UARTi transmit/receive control register 1



Symbol  
UiC1(i=0,1)

Address  
03A5<sub>16</sub>, 03AD<sub>16</sub>

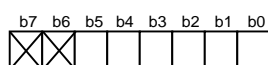
When reset  
02<sub>16</sub>

| Bit symbol  | Bit name                    | Function (Note 1)<br>(During clock synchronous serial I/O mode)                                 | Function<br>(During UART mode)  | R | W |
|---|-----------------------------|---|---|---|---|
| TE  | Transmit enable bit         | 0 : Transmission disabled<br>1 : Transmission enabled   | 0 : Transmission disabled<br>1 : Transmission enabled   | ○ | ○ |
| TI  | Transmit buffer empty flag  | 0 : Data present in transmit buffer register<br>1 : No data present in transmit buffer register | 0 : Data present in transmit buffer register<br>1 : No data present in transmit buffer register | ○ | × |
| RE  | Receive enable bit (Note 2) | 0 : Reception disabled<br>1 : Reception enabled   | 0 : Reception disabled<br>1 : Reception enabled   | ○ | ○ |
| RI  | Receive complete flag       | 0 : No data present in receive buffer register<br>1 : Data present in receive buffer register   | 0 : No data present in receive buffer register<br>1 : Data present in receive buffer register   | ○ | × |
| Nothing is assigned.<br>In an attempt to write to these bits, write "0". The value, if read, turns out to be indeterminate. |                             |   |   | — | — |

Note 1: UART1 cannot be used in clock synchronous serial I/O.

Note 2: If you are using clock asynchronous serial I/O mode, you can enable 'receive enable bit' when RxD port input is "H". If RxD port input is "L" and you have enabled 'receive enable bit', then receive operation starts immediately.

## UART transmit/receive control register 2



Symbol  
UCON

Address  
03B0<sub>16</sub>

When reset  
XX000000<sub>2</sub>

| Bit symbol  | Bit name                                  | Function<br>(During clock synchronous serial I/O mode)  | Function<br>(During UART mode)   | R | W |
|---|---|---|--|---|---|
| U0IRS   | UART0 transmit interrupt cause select bit | 0 : Transmit buffer empty (TI = 1)<br>1 : Transmission completed (TXEPT = 1)                                | 0 : Transmit buffer empty (TI = 1)<br>1 : Transmission completed (TXEPT = 1) | ○ | ○ |
| U1IRS   | UART1 transmit interrupt cause select bit | Set this bit to "0".  | 0 : Transmit buffer empty (TI = 1)<br>1 : Transmission completed (TXEPT = 1) | ○ | ○ |
| U0RRM   | UART0 continuous receive mode enable bit  | 0 : Continuous receive mode disabled<br>1 : Continuous receive mode enable                                  | Must always be "0"   | ○ | ○ |
| Set this bit to "0".  |   |   |  | ○ | ○ |
| CLKMD0  | CLK/CLKS select bit 0                     | Valid when bit 5 = "1"<br>0 : Clock output to CLK1<br>1 : Clock output to CLKS1                             | Must always be "0"   | ○ | ○ |
| CLKMD1  | CLK/CLKS select bit 1 (Note 2)            | 0 : Normal mode (CLK output is CLK0 only)<br>1 : Transfer clock output from multiple pins function selected | Must always be "0"   | ○ | ○ |
| Nothing is assigned.<br>In an attempt to write to these bits, write "0". The value, if read, turns out to be indeterminate. |   |   |  | — | — |

Note 1: UART1 cannot be used in clock synchronous serial I/O.

Note 2: When using multiple pins to output the transfer clock, the following requirements must be met:

- UART0 internal/external clock select bit (bit 3 at address 03A0<sub>16</sub>) = "0".

Figure 1.73. Serial I/O-related registers (3)

## Clock synchronous serial I/O mode

**(1) Clock synchronous serial I/O mode**

The clock synchronous serial I/O mode uses a transfer clock to transmit and receive data. (See Table 1.25.) Figure 1.65 shows the UART0 transmit/receive mode register.

**Table 1.25. Specifications of clock synchronous serial I/O mode**

| Item                                | Specification   |
|-------------------------------------|---|
| Transfer data format                | <ul style="list-style-type: none"> <li>• Transfer data length: 8 bits</li> </ul>  |
| Transfer clock                      | <ul style="list-style-type: none"> <li>• When internal clock is selected (bit 3 at address 03A0<sub>16</sub> = "0") : <math>f_i / 2(n+1)</math> (Note 1)<br/> <math>f_i = f_1, f_8, f_{32}, f_c</math></li> <li>• When external clock is selected (bit 3 at address 03A0<sub>16</sub> = "1") : Input from CLK0 pin</li> </ul>   |
| Transmission start condition        | <ul style="list-style-type: none"> <li>• To start transmission, the following requirements must be met: <ul style="list-style-type: none"> <li>– Transmit enable bit (bit 0 at address 03A5<sub>16</sub>) = "1"</li> <li>– Transmit buffer empty flag (bit 1 at addresses 03A5<sub>16</sub>) = "0"</li> </ul> </li> <li>• Furthermore, if external clock is selected, the following requirements must also be met: <ul style="list-style-type: none"> <li>– CLK0 polarity select bit (bit 6 at address 03A4<sub>16</sub>) = "0": CLK0 input level = "H"</li> <li>– CLK0 polarity select bit (bit 6 at address 03A4<sub>16</sub>) = "1": CLK0 input level = "L"</li> </ul> </li> </ul>   |
| Reception start condition           | <ul style="list-style-type: none"> <li>• To start reception, the following requirements must be met: <ul style="list-style-type: none"> <li>– Receive enable bit (bit 2 at address 03A5<sub>16</sub>) = "1"</li> <li>– Transmit enable bit (bit 0 at address 03A5<sub>16</sub>) = "1"</li> <li>– Transmit buffer empty flag (bit 1 at address 03A5<sub>16</sub>) = "0"</li> </ul> </li> <li>• Furthermore, if external clock is selected, the following requirements must also be met: <ul style="list-style-type: none"> <li>– CLK0 polarity select bit (bit 6 at address 03A4<sub>16</sub>) = "0": CLK0 input level = "H"</li> <li>– CLK0 polarity select bit (bit 6 at address 03A4<sub>16</sub>) = "1": CLK0 input level = "L"</li> </ul> </li> </ul> |
| Interrupt request generation timing | <ul style="list-style-type: none"> <li>• When transmitting <ul style="list-style-type: none"> <li>– Transmit interrupt cause select bit (bit 0 at address 03B0<sub>16</sub>) = "0": Interrupts requested when data transfer from UART0 transfer buffer register to UART0 transmit register is completed</li> <li>– Transmit interrupt cause select bit (bit 0 at address 03B0<sub>16</sub>) = "1": Interrupts requested when data transmission from UART0 transfer register is completed</li> </ul> </li> <li>• When receiving <ul style="list-style-type: none"> <li>– Interrupts requested when data transfer from UART0 receive register to UART0 receive buffer register is completed</li> </ul> </li> </ul>  |
| Error detection                     | <ul style="list-style-type: none"> <li>• Overrun error (Note 2)<br/> This error occurs when the next data is ready before contents of UART0 receive buffer register are read out</li> </ul>   |
| Select function                     | <ul style="list-style-type: none"> <li>• CLK polarity selection<br/> Whether transmit data is output/input at the rising edge or falling edge of the transfer clock can be selected</li> <li>• LSB first/MSB first selection<br/> Whether transmission/reception begins with bit 0 or bit 7 can be selected</li> <li>• Continuous receive mode selection<br/> Reception is enabled simultaneously by a read from the receive buffer register</li> <li>• Transfer clock output from multiple pins selection<br/> UART0 transfer clock can be chosen by software to be output from one of the two pins set</li> </ul>   |

Note 1: "n" denotes the value 00<sub>16</sub> to FF<sub>16</sub> that is set to the UART bit rate generator.

Note 2: If an overrun error occurs, the UART0 receive buffer will have the next data written in. Note also that the UART0 receive interrupt request bit does not change.



## Clock synchronous serial I/O mode

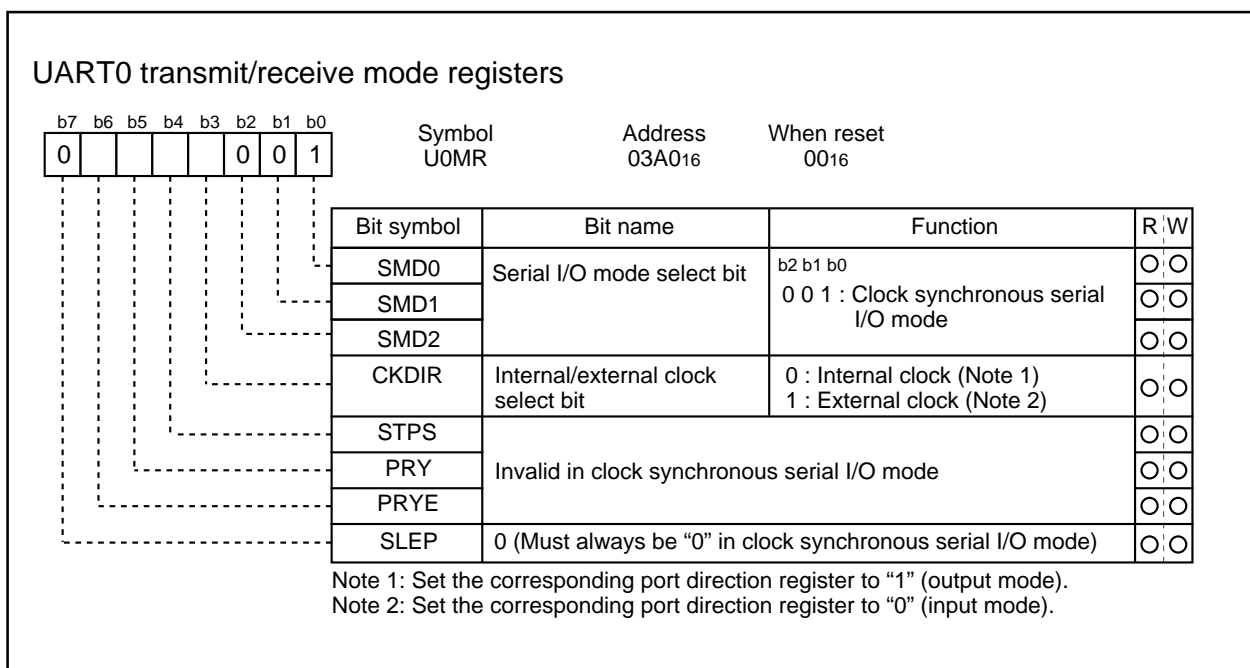


Figure 1.74. UART0 transmit/receive mode register in clock synchronous serial I/O mode

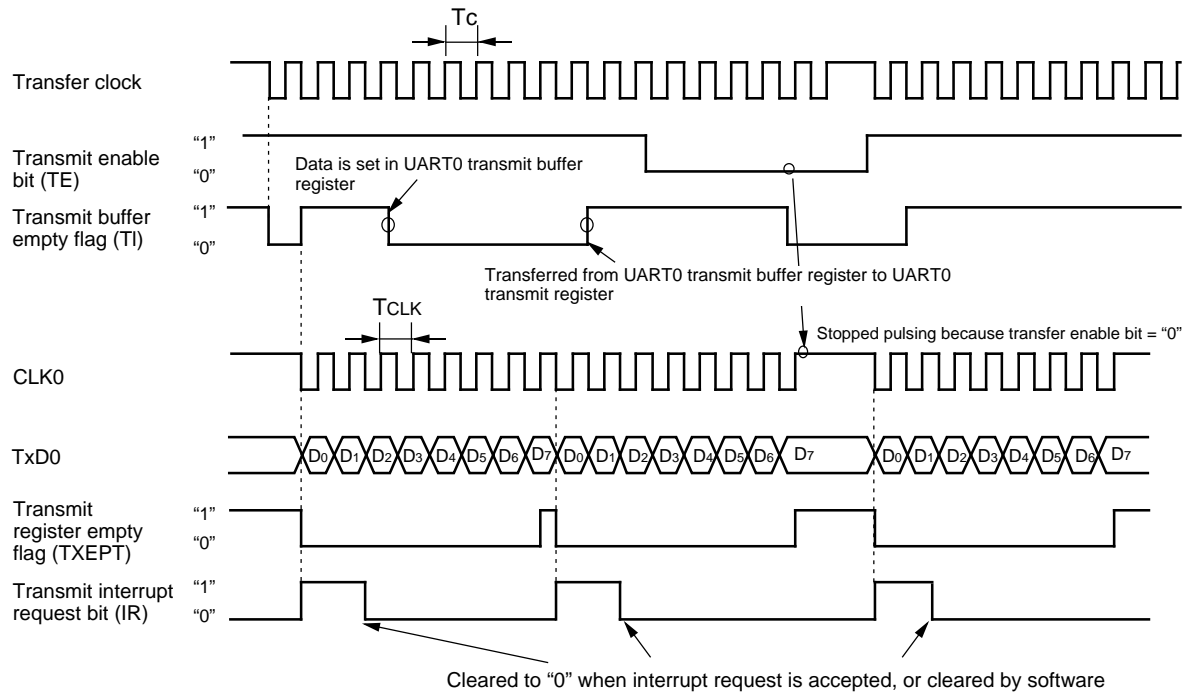
Table 1.26 lists the functions of the input/output pins during clock synchronous serial I/O mode. Note that for a period from when the UART0 operation mode is selected to when transfer starts, the TxD0 pin outputs a "H". (If the N-channel open-drain is selected, this pin is in floating state.)

Table 1.26. Input/output pin functions in clock synchronous serial I/O mode

| Pin name   | Function              | Method of selection   |
|------------|-----------------------|---|
| TxD0 (P50) | Serial data output    | Port P50 direction register (bit 0 at address 03EB <sub>16</sub> ) = "1"<br>(Outputs dummy data when performing reception only)                             |
| RxD0 (P51) | Serial data input     | Port P51 direction register (bit 1 at address 03EB <sub>16</sub> ) = "0"<br>(Can be used as an input port when performing transmission only)                |
| CLK0 (P52) | Transfer clock output | Internal/external clock select bit (bit 3 at address 03A0 <sub>16</sub> ) = "0"   |
|            | Transfer clock input  | Internal/external clock select bit (bit 3 at address 03A0 <sub>16</sub> ) = "1"<br>Port P52 direction register (bit 2 at address 03EB <sub>16</sub> ) = "0" |

## Clock synchronous serial I/O mode

## • Example of transmit timing (when internal clock is selected)



Shown in ( ) are bit symbols.

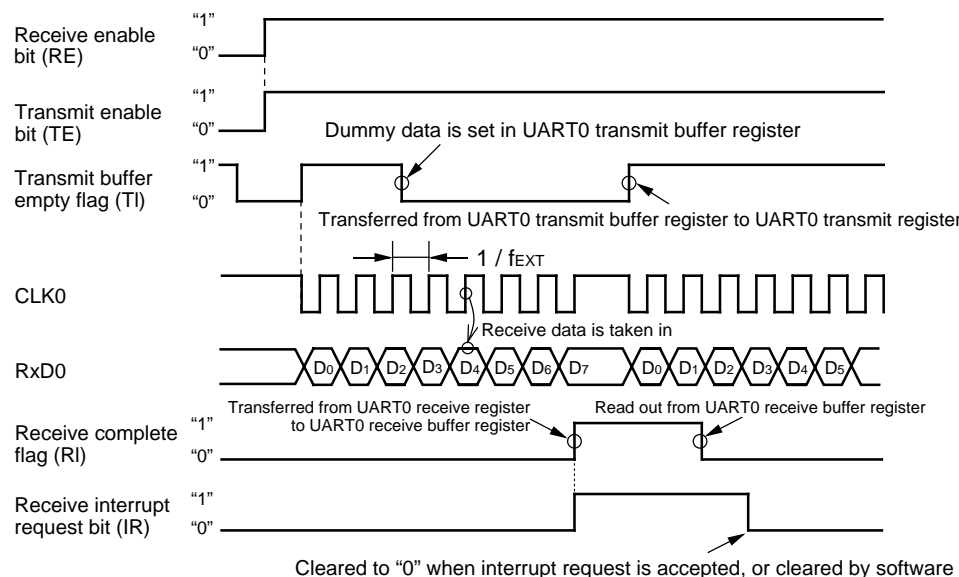
The above timing applies to the following settings:

- Internal clock is selected.
- CLK polarity select bit = "0".
- Transmit interrupt cause select bit = "0".

$$T_c = T_{CLK} = 2(n + 1) / f_i$$

$f_i$ : frequency of BRG0 count source ( $f_1, f_8, f_{32}, f_c$ )  
 $n$ : value set to BRG0

## • Example of receive timing (when external clock is selected)



Shown in ( ) are bit symbols.

The above timing applies to the following settings:

- External clock is selected.
- CLK polarity select bit = "0".

$f_{EXT}$ : frequency of external clock

Meet the following conditions are met when the CLK input before data reception = "H"

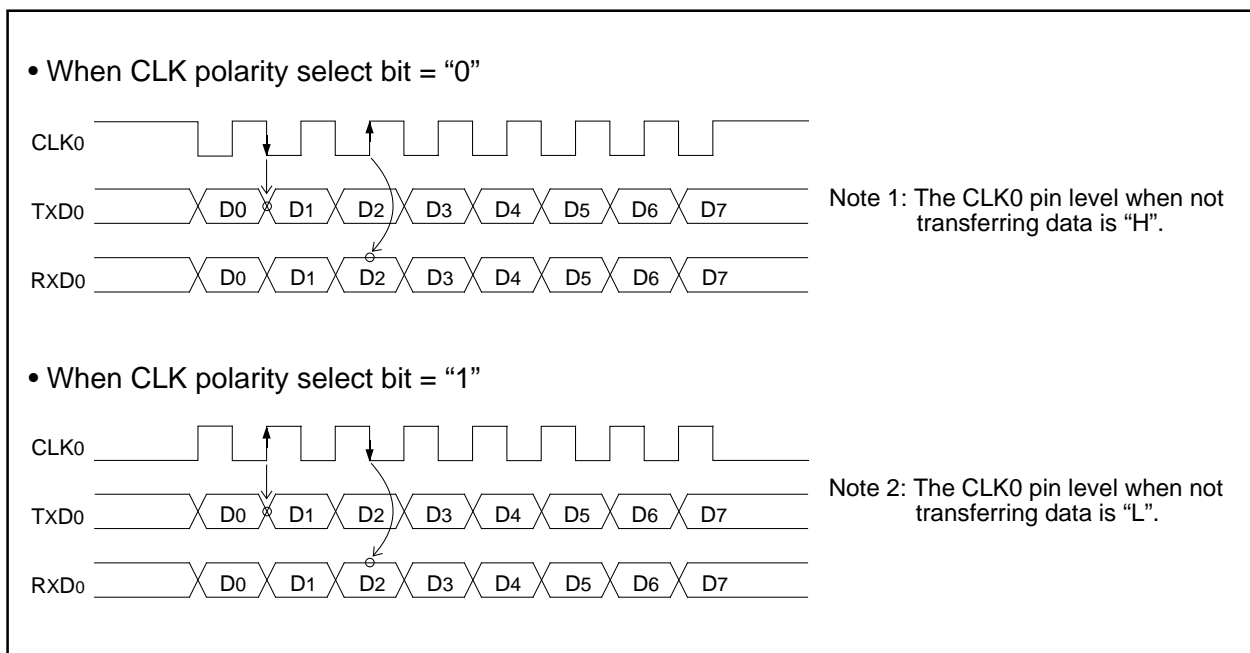
- Transmit enable bit → "1"
- Receive enable bit → "1"
- Dummy data write to UART0 transmit buffer register

Figure 1.75. Typical transmit/receive timings in clock synchronous serial I/O mode

## Clock synchronous serial I/O mode

**(a) Polarity select function**

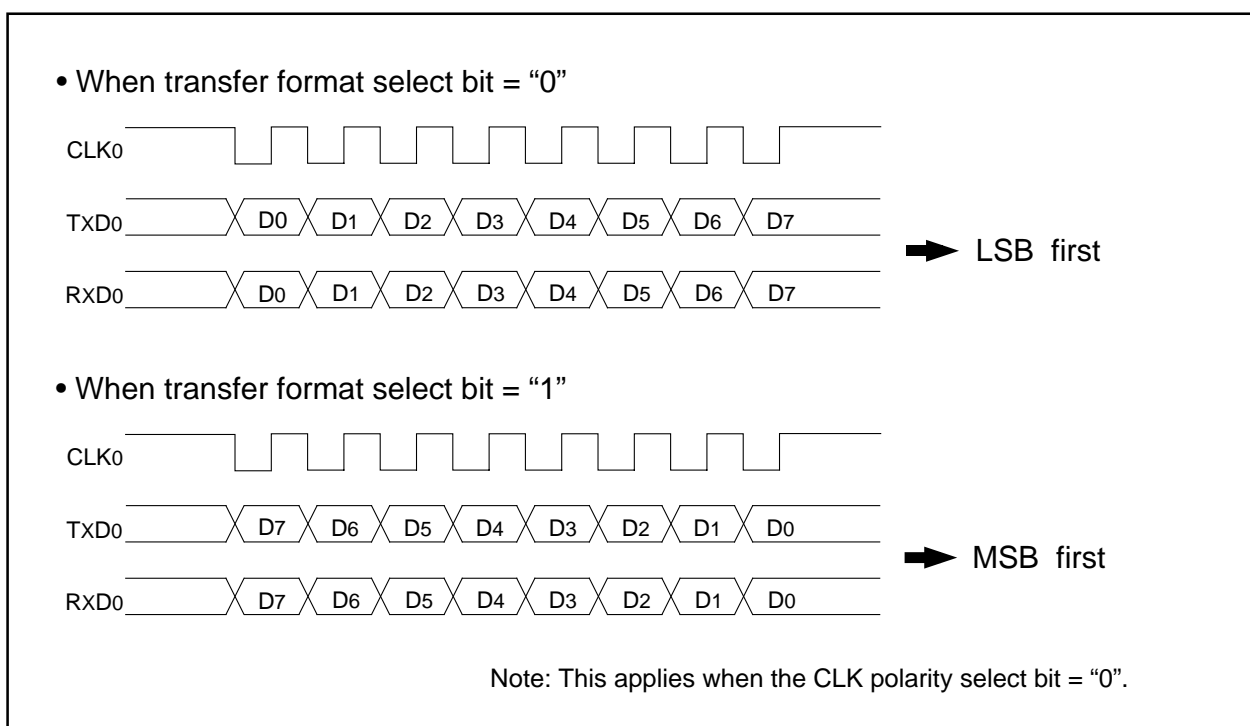
As shown in Figure 1.76, the CLK polarity select bit (bit 6 at addresses 03A4<sub>16</sub>) allows selection of the polarity of the transfer clock.



**Figure 1.76. Polarity of transfer clock**

**(b) LSB first/MSB first select function**

As shown in Figure 1.77, when the transfer format select bit (bit 7 at addresses 03A4<sub>16</sub>) = "0", the transfer format is "LSB first"; when the bit = "1", the transfer format is "MSB first".

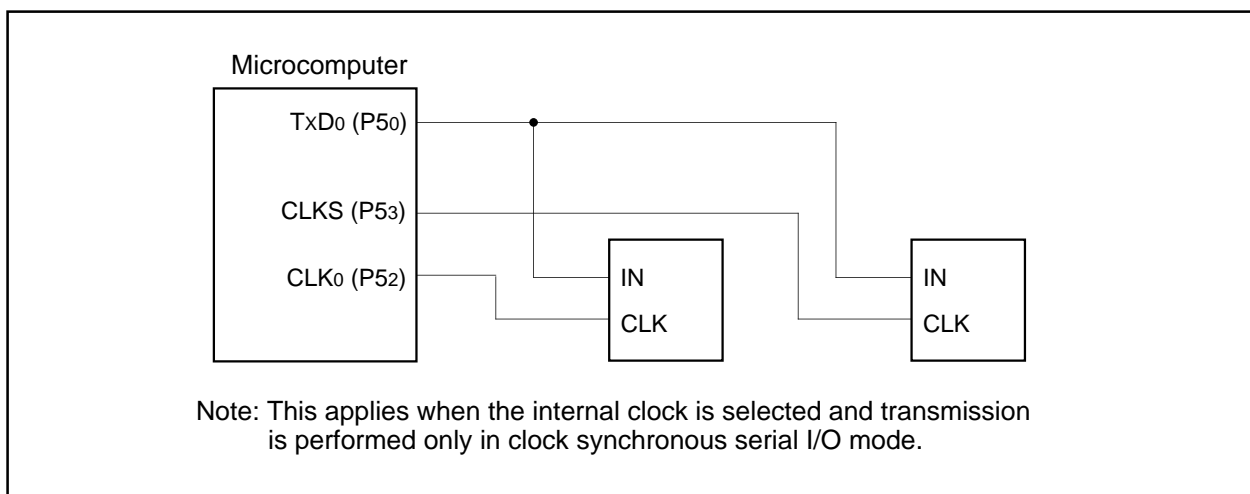


**Figure 1.77. Transfer format**

## Clock synchronous serial I/O mode

**(c) Transfer clock output from multiple pins function**

This function allows the setting two transfer clock output pins and choosing one of the two to output a clock by using the CLK and CLKS select bit (bits 4 and 5 at address 03B016). (See Figure 1.78.) The multiple pins function is valid only when the internal clock is selected for UART0.



**Figure 1.78. The transfer clock output from the multiple pins function usage**

**(d) Continuous receive mode**

If the continuous receive mode enable bit (bits 2 and 3 at address 03B016) is set to "1", the unit is placed in continuous receive mode. In this mode, when the receive buffer register is read out, the unit simultaneously goes to a receive enable state without having to set dummy data to the transmit buffer register back again.

## Clock asynchronous serial I/O (UART) mode

**(2) Clock asynchronous serial I/O (UART) mode**

The UART mode allows transmitting and receiving data after setting the desired transfer rate and transfer data format. (See Table 1.27.) Figure 1.79 shows the UARTi transmit/receive mode register.

**Table 1.27. Specifications of UART Mode**

| Item                                | Specification   |
|-------------------------------------|---|
| Transfer data format                | <ul style="list-style-type: none"> <li>• Character bit (transfer data): 7 bits, 8 bits, or 9 bits as selected</li> <li>• Start bit: 1 bit</li> <li>• Parity bit: Odd, even, or nothing as selected</li> <li>• Stop bit: 1 bit or 2 bits as selected</li> </ul>  |
| Transfer clock                      | <ul style="list-style-type: none"> <li>• When internal clock is selected (bit 3 at addresses 03A0<sub>16</sub>, 03A8<sub>16</sub> = "0") : <math>f_{i/16(n+1)}</math> (Note 1) <math>f_i = f_1, f_8, f_{32}, f_c</math></li> <li>• When external clock is selected (bit 3 at addresses 03A0<sub>16</sub> = "1") : <math>f_{EXT/16(n+1)}</math> (Note 1) (Note 2)</li> </ul>   |
| Transmission start condition        | <ul style="list-style-type: none"> <li>• To start transmission, the following requirements must be met: <ul style="list-style-type: none"> <li>- Transmit enable bit (bit 0 at addresses 03A5<sub>16</sub>, 03AD<sub>16</sub>) = "1"</li> <li>- Transmit buffer empty flag (bit 1 at addresses 03A5<sub>16</sub>, 03AD<sub>16</sub>) = "0"</li> </ul> </li> </ul>   |
| Reception start condition           | <ul style="list-style-type: none"> <li>• To start reception, the following requirements must be met: <ul style="list-style-type: none"> <li>- Receive enable bit (bit 2 at addresses 03A5<sub>16</sub>, 03AD<sub>16</sub>) = "1"</li> <li>- Start bit detection</li> </ul> </li> </ul>  |
| Interrupt request generation timing | <ul style="list-style-type: none"> <li>• When transmitting <ul style="list-style-type: none"> <li>- Transmit interrupt cause select bits (bits 0,1 at address 03B0<sub>16</sub>) = "0": Interrupts requested when data transfer from UARTi transfer buffer register to UARTi transmit register is completed</li> <li>- Transmit interrupt cause select bits (bits 0, 1 at address 03B0<sub>16</sub>) = "1": Interrupts requested when data transmission from UARTi transfer register is completed</li> </ul> </li> <li>• When receiving <ul style="list-style-type: none"> <li>- Interrupts requested when data transfer from UARTi receive register to UARTi receive buffer register is completed</li> </ul> </li> </ul> |
| Error detection                     | <ul style="list-style-type: none"> <li>• Overrun error (Note 3)<br/>This error occurs when the next data is ready before contents of UARTi receive buffer register are read out</li> <li>• Framing error<br/>This error occurs when the number of stop bits set is not detected</li> <li>• Parity error<br/>This error occurs when if parity is enabled, the number of 1's in parity and character bits does not match the number of 1's set</li> <li>• Error sum flag<br/>This flag is set (= 1) when any of the overrun, framing, and parity errors is encountered</li> </ul>   |
| Select function                     | <ul style="list-style-type: none"> <li>• Sleep mode selection<br/>This mode is used to transfer data to and from one of multiple slave micro-computers</li> </ul>   |

Note 1: 'n' denotes the value 00<sub>16</sub> to FF<sub>16</sub> that is set to the UART bit rate generator.

Note 2: f<sub>EXT</sub> is input from the CLK0 pin. Since UART1 does not have this pin, cannot select external clock.

Note 3: If an overrun error occurs, the UARTi receive buffer will have the next data written in. Note also that the UARTi receive interrupt request bit does not change.

## Clock asynchronous serial I/O (UART) mode

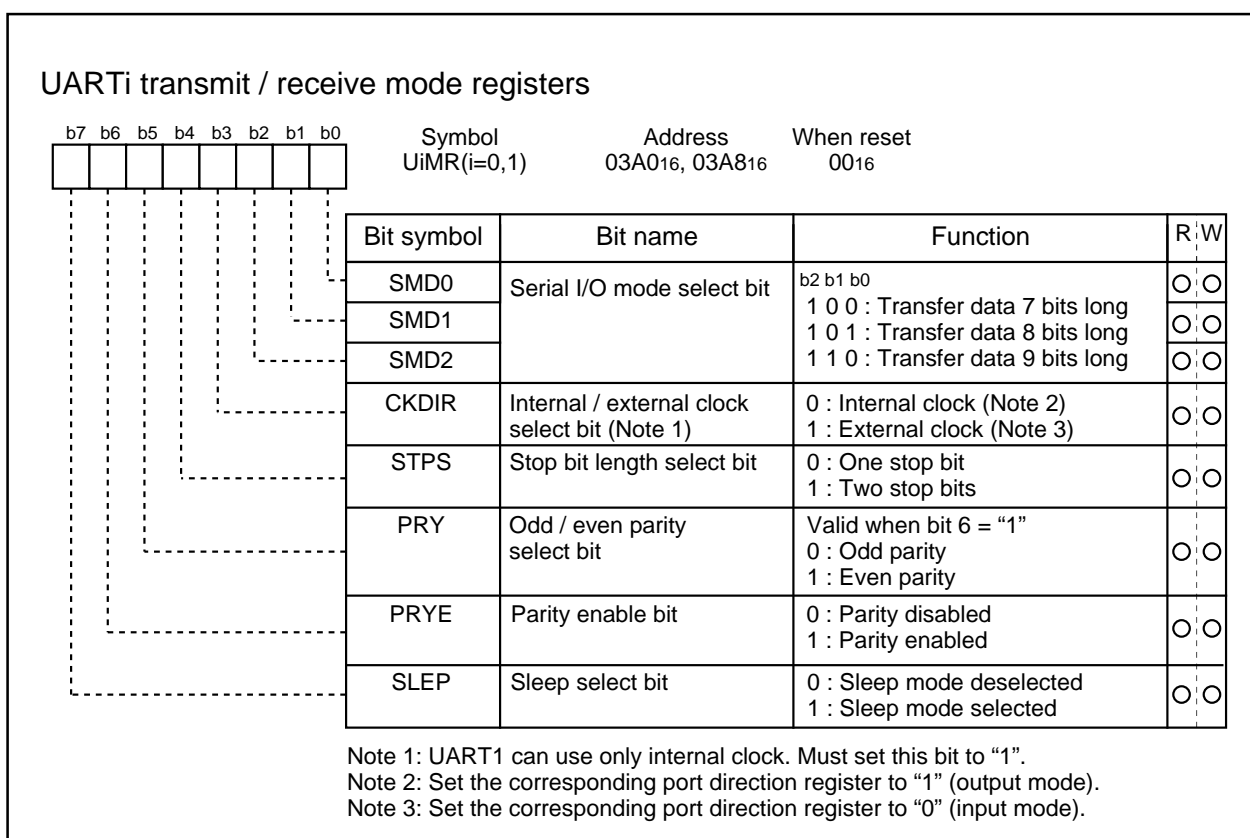


Figure 1.79. UARTi transmit/receive mode register in UART mode

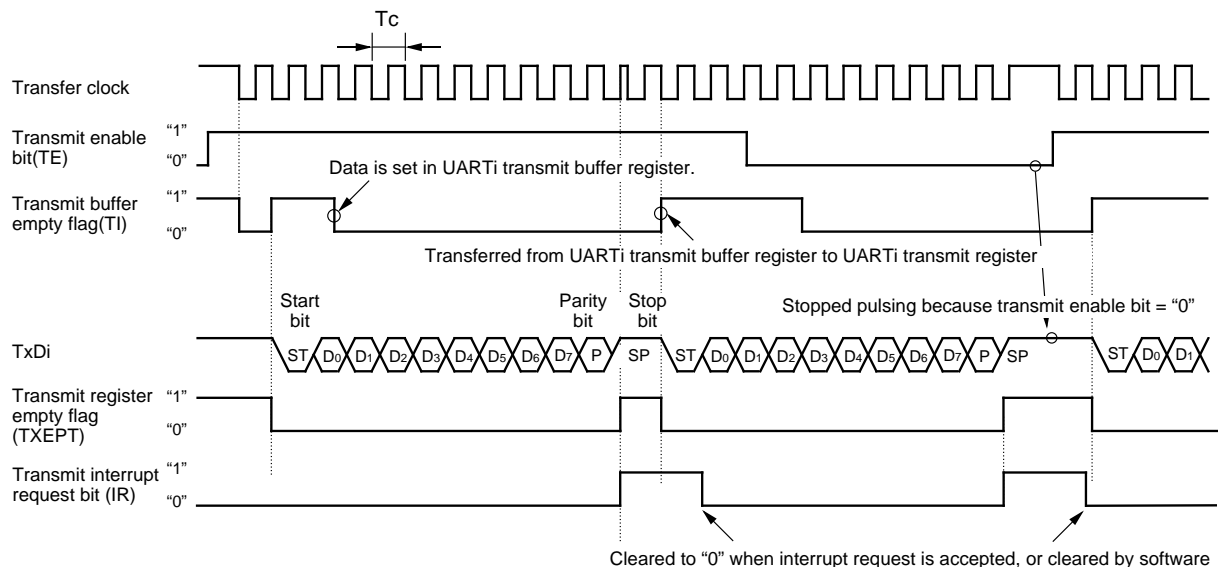
Table 1.28 lists the functions of the input/output pins during UART mode. Note that for a period from when the UARTi operation mode is selected to when transfer starts, the TxDi pin outputs a "H". (If the N-channel open-drain is selected, this pin is in floating state.)

Table 1.28. Input/output pin functions in UART mode

| Pin name           | Function              | Method of selection  |
|--------------------|-----------------------|--|
| TxDi<br>(P50, P40) | Serial data output    | Port P51 and P42 direction register (bit 0 at address 03EB16, bit 0 at address 03EA16) = "1"<br>(Can be used as an input port when performing reception only)    |
| RxDi<br>(P51, P42) | Serial data input     | Port P51 and P42 direction register (bit 1 at address 03EB16, bit 2 at address 03EA16) = "0"<br>(Can be used as an input port when performing transmission only) |
| CLK0<br>(P52)      | Programmable I/O port | Internal/external clock select bit (bit 3 at address 03A016) = "0"   |
|                    | Transfer clock input  | Internal/external clock select bit (bit 3 at address 03A016) = "1"   |

## Clock asynchronous serial I/O (UART) mode

- Example of transmit timing when transfer data is 8 bits long (parity enabled, one stop bit)



Shown in ( ) are bit symbols.

The above timing applies to the following settings :

- Parity is enabled.
- One stop bit.
- Transmit interrupt cause select bit = "1".

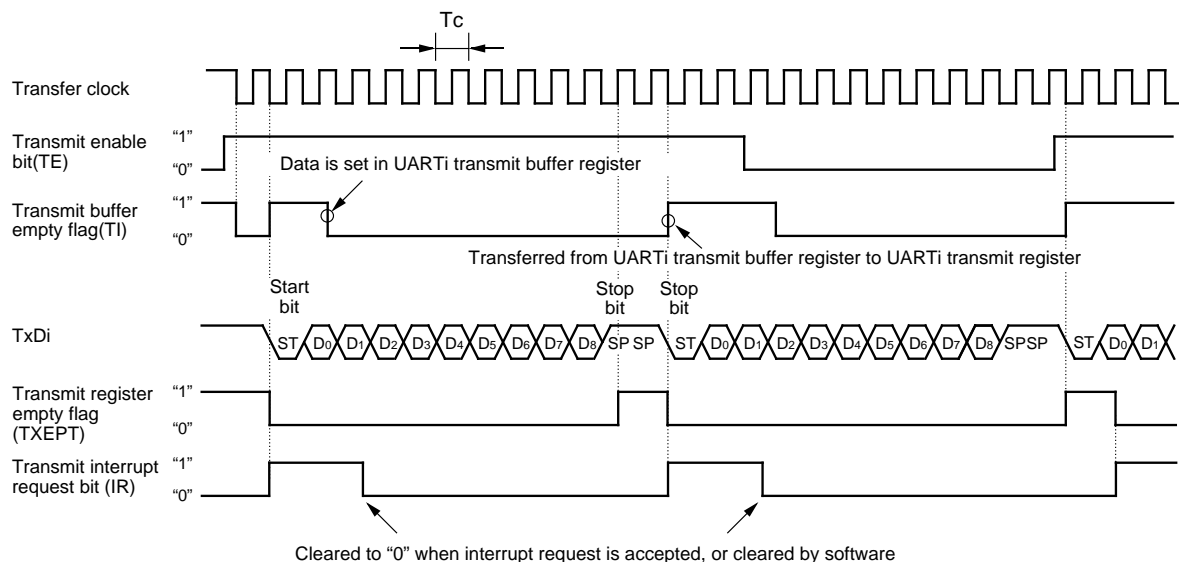
$$T_c = 16(n+1) / f_i \text{ or } 16(n+1) / f_{EXT}$$

$f_i$  : frequency of BRGi count source ( $f_1, f_8, f_{32}, f_c$ )

$f_{EXT}$  : frequency of BRGi count source (external clock)

$n$  : value set to BRGi

- Example of transmit timing when transfer data is 9 bits long (parity disabled, two stop bits)



Shown in ( ) are bit symbols.

The above timing applies to the following settings :

- Parity is disabled.
- Two stop bits.
- Transmit interrupt cause select bit = "0".

$$T_c = 16(n+1) / f_i \text{ or } 16(n+1) / f_{EXT}$$

$f_i$  : frequency of BRGi count source ( $f_1, f_8, f_{32}$ )

$f_{EXT}$  : frequency of BRGi count source (external clock)

$n$  : value set to BRGi

Figure 1.80. Typical transmit timings in UART mode

## Clock asynchronous serial I/O (UART) mode

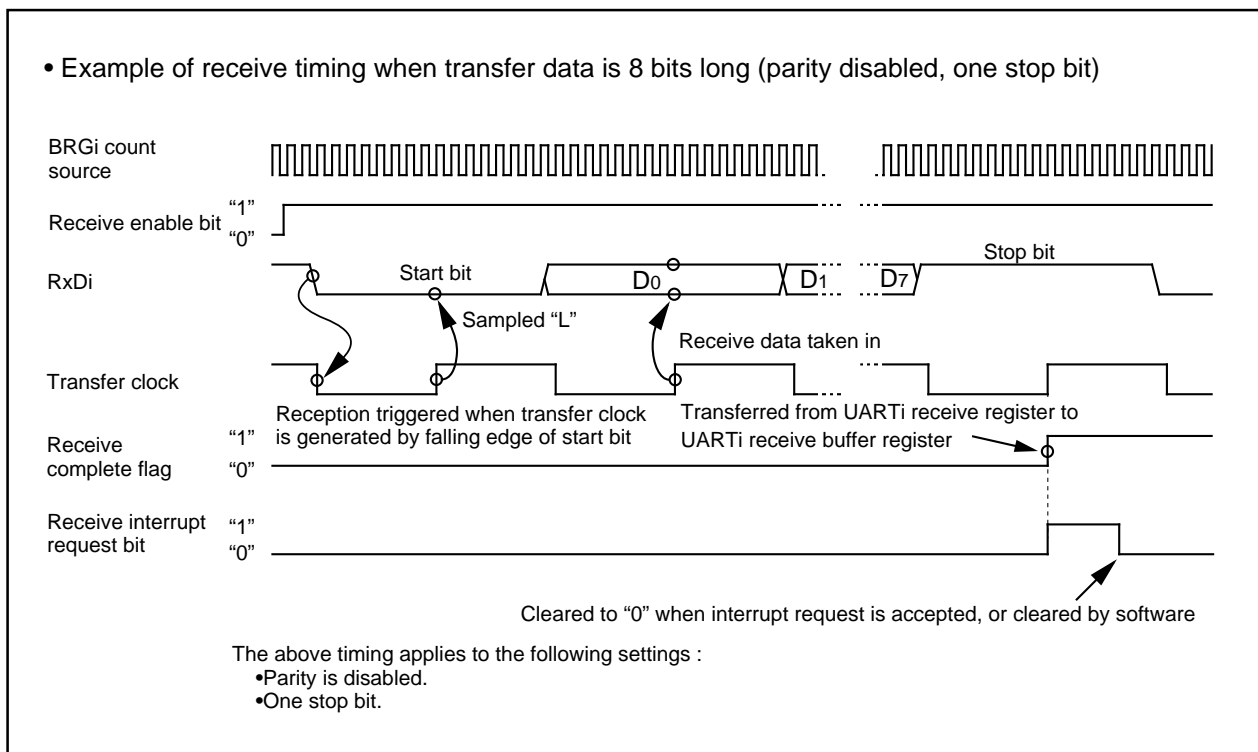


Figure 1.81. Typical receive timing in UART mode

## (a) Sleep mode

This mode is used to transfer data between specific microcomputers among multiple microcomputers connected using UARTi. The sleep mode is selected when the sleep select bit (bit 7 at addresses 03A016, 03A816) is set to "1" during reception. In this mode, the unit performs receive operation when the MSB of the received data = "1" and does not perform receive operation when the MSB = "0".



## A-D Converter

### A-D Converter

The A-D converter consists of one 10-bit successive approximation A-D converter circuit with a capacitive coupling amplifier. Pins P60 to P67, and P50 to P54 also function as the analog signal input pins. The direction registers of these pins for A-D conversion must therefore be set to input. The Vref connect bit (bit 5 at address 03D716) can be used to isolate the resistance ladder of the A-D converter from the reference voltage input pin (VREF) when the A-D converter is not used. Doing so stops any current flowing into the resistance ladder from VREF, reducing the power dissipation. When using the A-D converter, start A-D conversion only after setting bit 5 of 03D716 to connect VREF.

The result of A-D conversion is stored in the A-D registers of the selected pins. When set to 10-bit precision, the low 8 bits are stored in the even addresses and the high 2 bits in the odd addresses. When set to 8-bit precision, the low 8 bits are stored in the even addresses.

Table 1.29 shows the performance of the A-D converter. Figure 1.82 shows the block diagram of the A-D converter, and Figures 1.83 and 1.84 show the A-D converter-related registers.

**Table 1.29. Performance of A-D converter**

| Item                                 | Performance  |
|--------------------------------------|--|
| Method of A-D conversion             | Successive approximation (capacitive coupling amplifier)   |
| Analog input voltage (Note 1)        | 0V to AVCC (VCC)   |
| Operating clock $\phi_{AD}$ (Note 2) | VCC = 5V $f_{AD}$ , divide-by-2 of $f_{AD}$ , divide-by-4 of $f_{AD}$ , $f_{AD}=f(XIN)$<br>VCC = 3V    divide-by-2 of $f_{AD}$ , divide-by-4 of $f_{AD}$ , $f_{AD}=f(XIN)$   |
| Resolution                           | 8-bit or 10-bit (selectable)   |
| Absolute precision                   | VCC = 5V    • Without sample and hold function<br>$\pm 3\text{LSB}$<br>• With sample and hold function (8-bit resolution)<br>$\pm 2\text{LSB}$<br>• With sample and hold function (10-bit resolution)<br>$\pm 3\text{LSB}$<br>VCC = 3V    • Without sample and hold function (8-bit resolution)<br>$\pm 2\text{LSB}$ |
| Operating modes                      | One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0, and repeat sweep mode 1  |
| Analog input pins                    | 8 pins (AN0 to AN7) + 5 pins (AN50 to AN54)  |
| A-D conversion start condition       | • Software trigger<br>A-D conversion starts when the A-D conversion start flag changes to "1"  |
| Conversion speed per pin             | • Without sample and hold function<br>8-bit resolution: 49 $\phi_{AD}$ cycles, 10-bit resolution: 59 $\phi_{AD}$ cycles<br>• With sample and hold function<br>8-bit resolution: 28 $\phi_{AD}$ cycles, 10-bit resolution: 33 $\phi_{AD}$ cycles  |

Note 1: Does not depend on use of sample and hold function.

Note 2: Without sample and hold function, set the  $\phi_{AD}$  frequency to 250kHz min.

With the sample and hold function, set the  $\phi_{AD}$  frequency to 1MHz min.

## A-D Converter

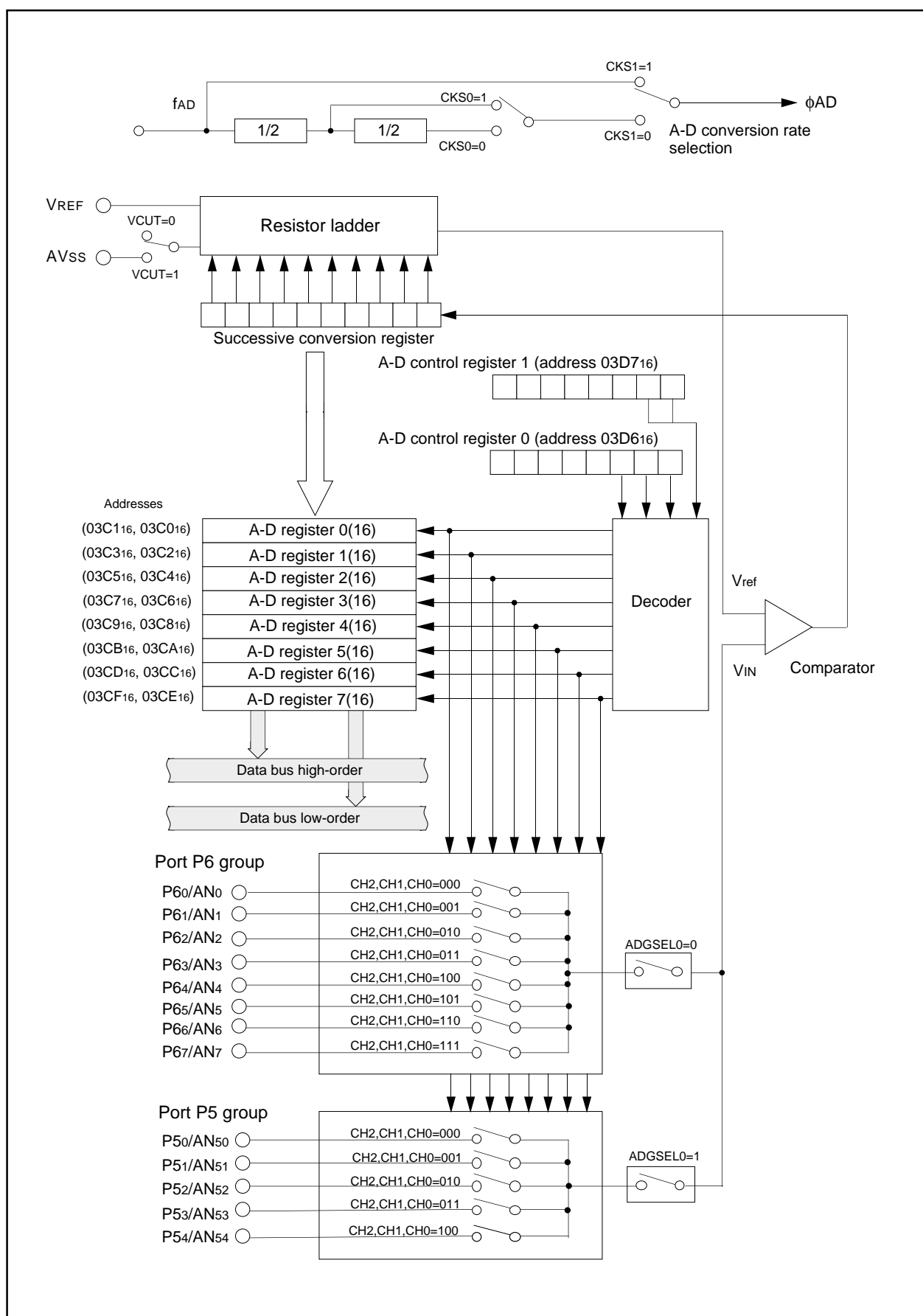


Figure 1.82. Block diagram of A-D converter

## A-D Converter

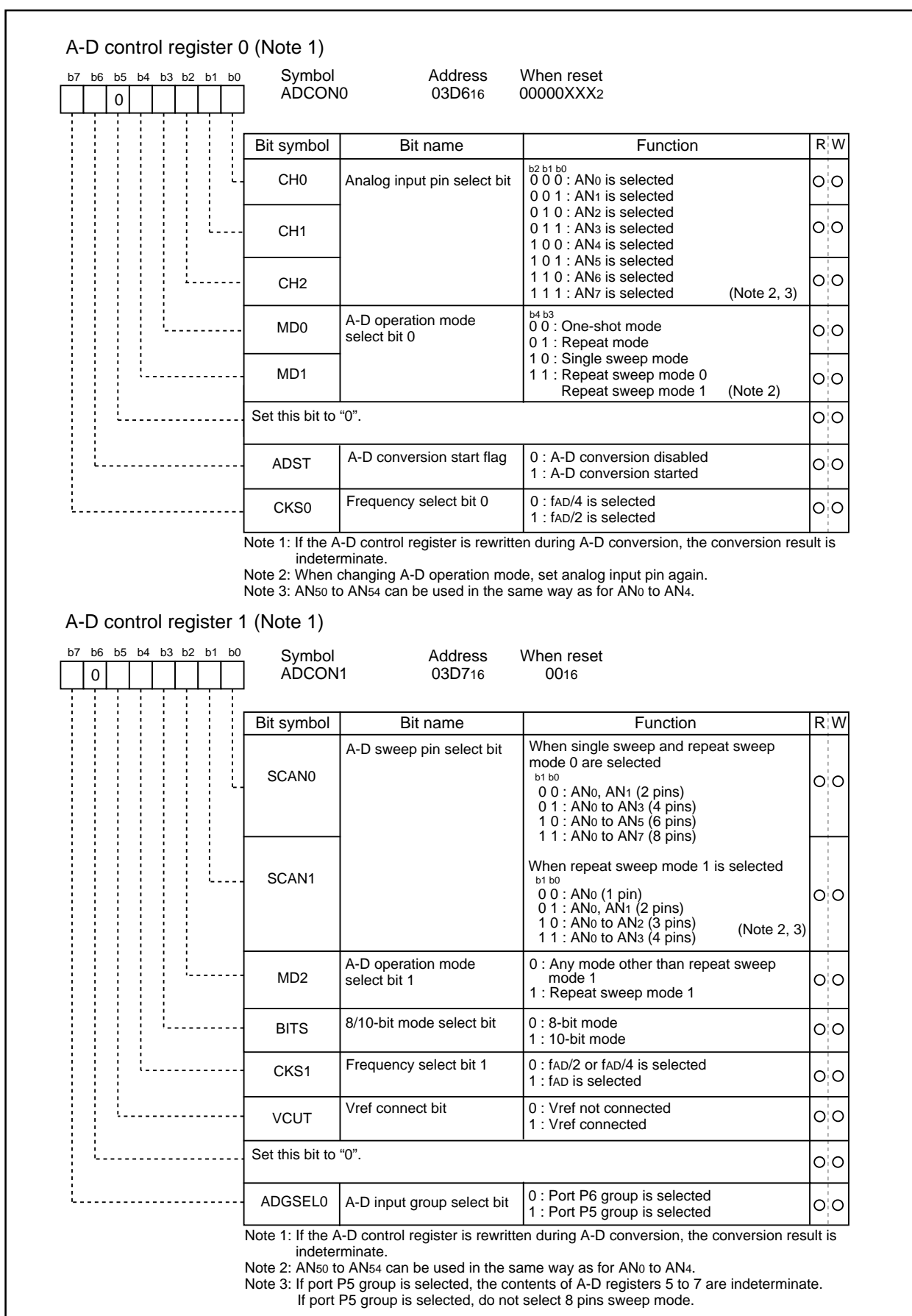


Figure 1.83. A-D converter-related registers (1)

## A-D Converter

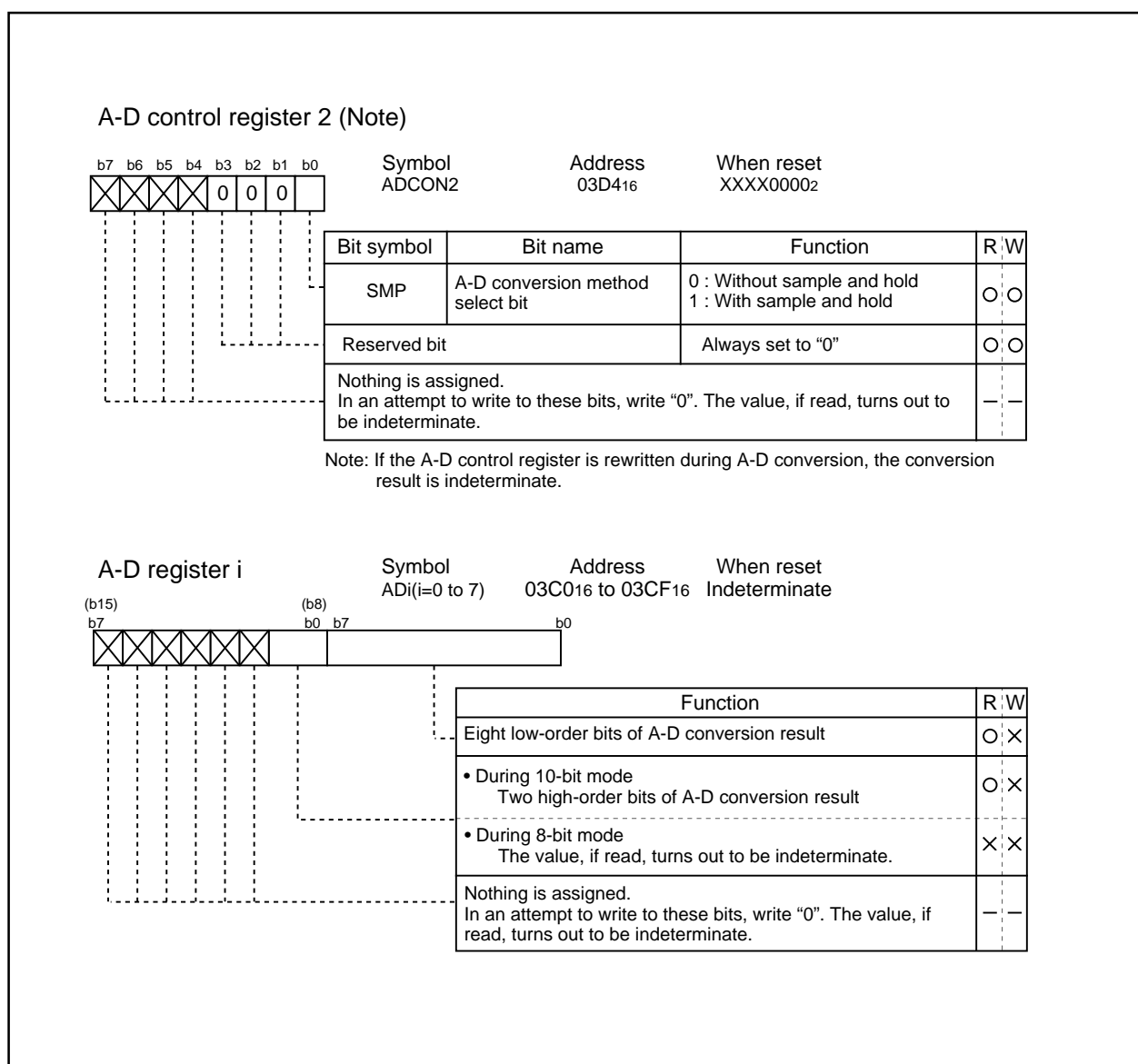


Figure 1.84. A-D converter-related registers (2)

## A-D Converter

## (1) One-shot mode

In one-shot mode, the pin selected using the analog input pin select bit is used for one-shot A-D conversion. (See Table 1.30.) Figure 1.85 shows the A-D control register in one-shot mode.

Table 1.30. One-shot mode specifications

| Item                                | Specification  |
|-------------------------------------|--|
| Function                            | The pin selected by the analog input pin select bit is used for one A-D conversion   |
| Start condition                     | Writing "1" to A-D conversion start flag   |
| Stop condition                      | <ul style="list-style-type: none"> <li>End of A-D conversion (A-D conversion start flag changes to "0")</li> <li>Writing "0" to A-D conversion start flag</li> </ul> |
| Interrupt request generation timing | End of A-D conversion  |
| Input pin                           | One of AN <sub>0</sub> to AN <sub>7</sub> , as selected (Note)   |
| Reading of result of A-D converter  | Read A-D register corresponding to selected pin  |

Note : AN<sub>50</sub> to AN<sub>54</sub> can be used in the same way as for AN<sub>0</sub> to AN<sub>4</sub>.

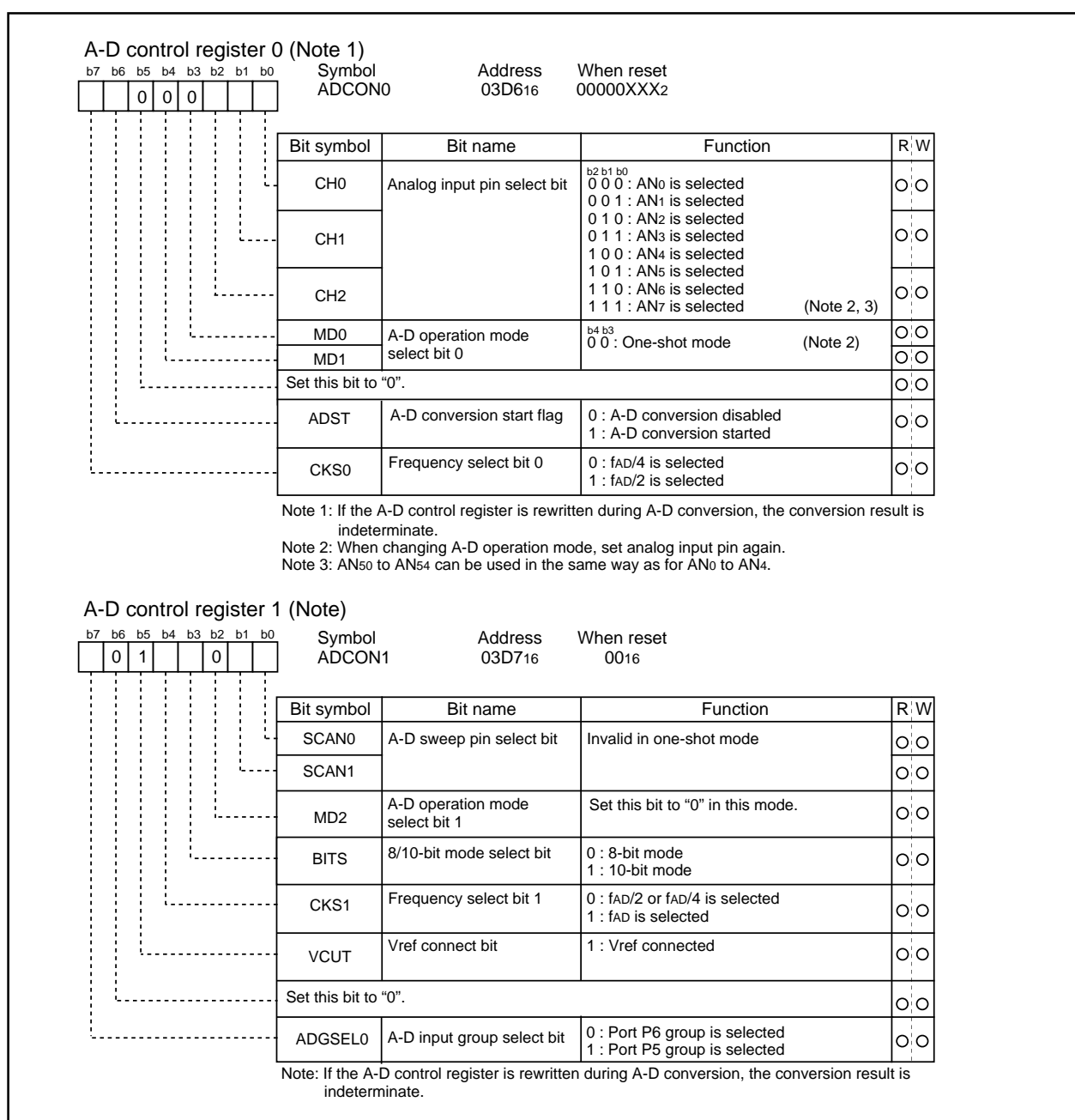


Figure 1.85. A-D conversion register in one-shot mode

## A-D Converter

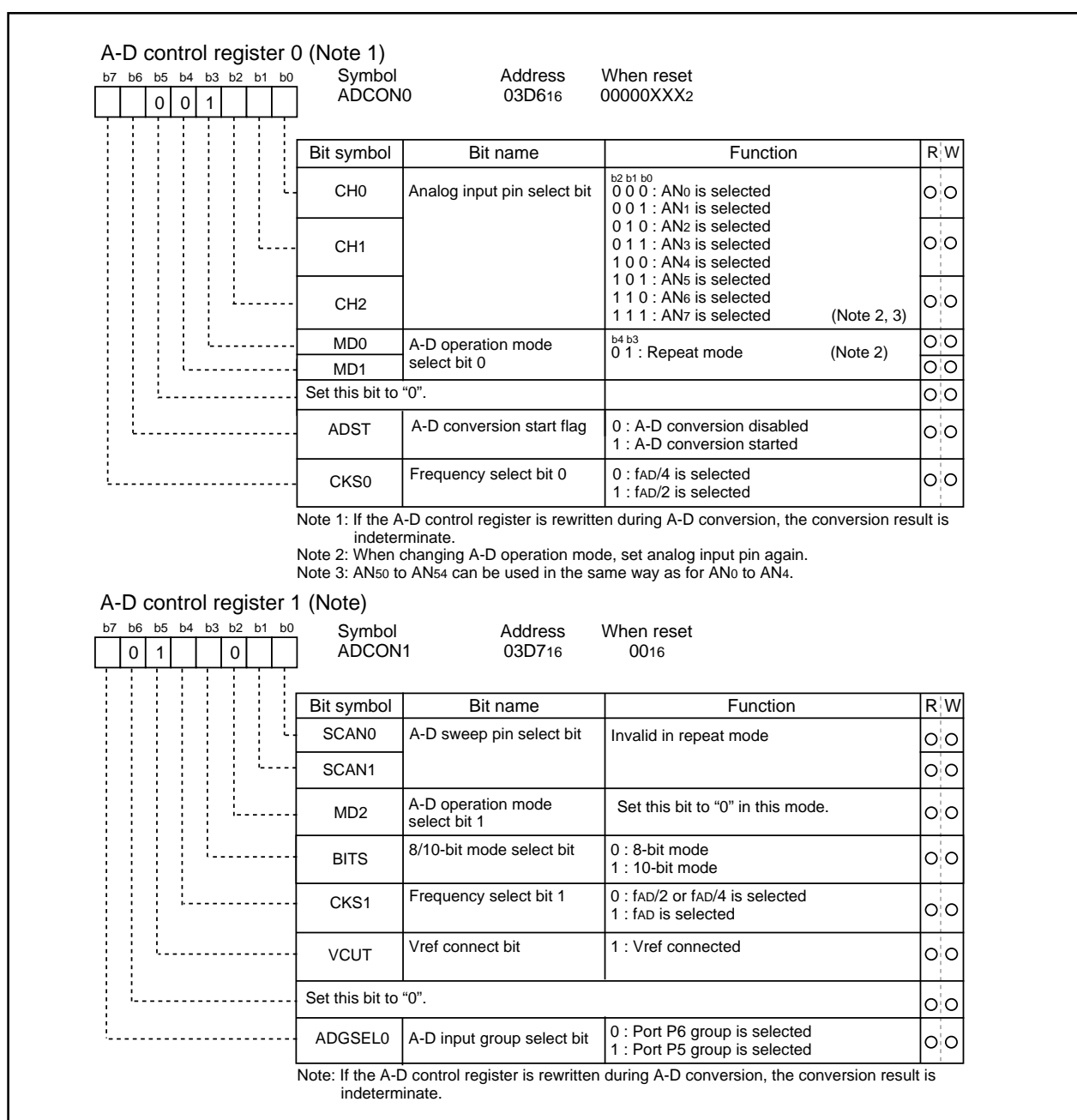
**(2) Repeat mode**

In repeat mode, the pin selected using the analog input pin select bit is used for repeated A-D conversion. (See Table 1.31.) Figure 1.86 shows the A-D control register in repeat mode.

**Table 1.31. Repeat mode specifications**

| Item                                | Specification   |
|-------------------------------------|---|
| Function                            | The pin selected by the analog input pin select bit is used for repeated A-D conversion |
| Start condition                     | Writing "1" to A-D conversion start flag  |
| Stop condition                      | Writing "0" to A-D conversion start flag  |
| Interrupt request generation timing | None generated  |
| Input pin                           | One of AN0 to AN7, as selected (Note)   |
| Reading of result of A-D converter  | Read A-D register corresponding to selected pin (at any time)                           |

Note : AN50 to AN54 can be used in the same way as for AN0 to AN4.

**Figure 1.86. A-D conversion register in repeat mode**

## A-D Converter

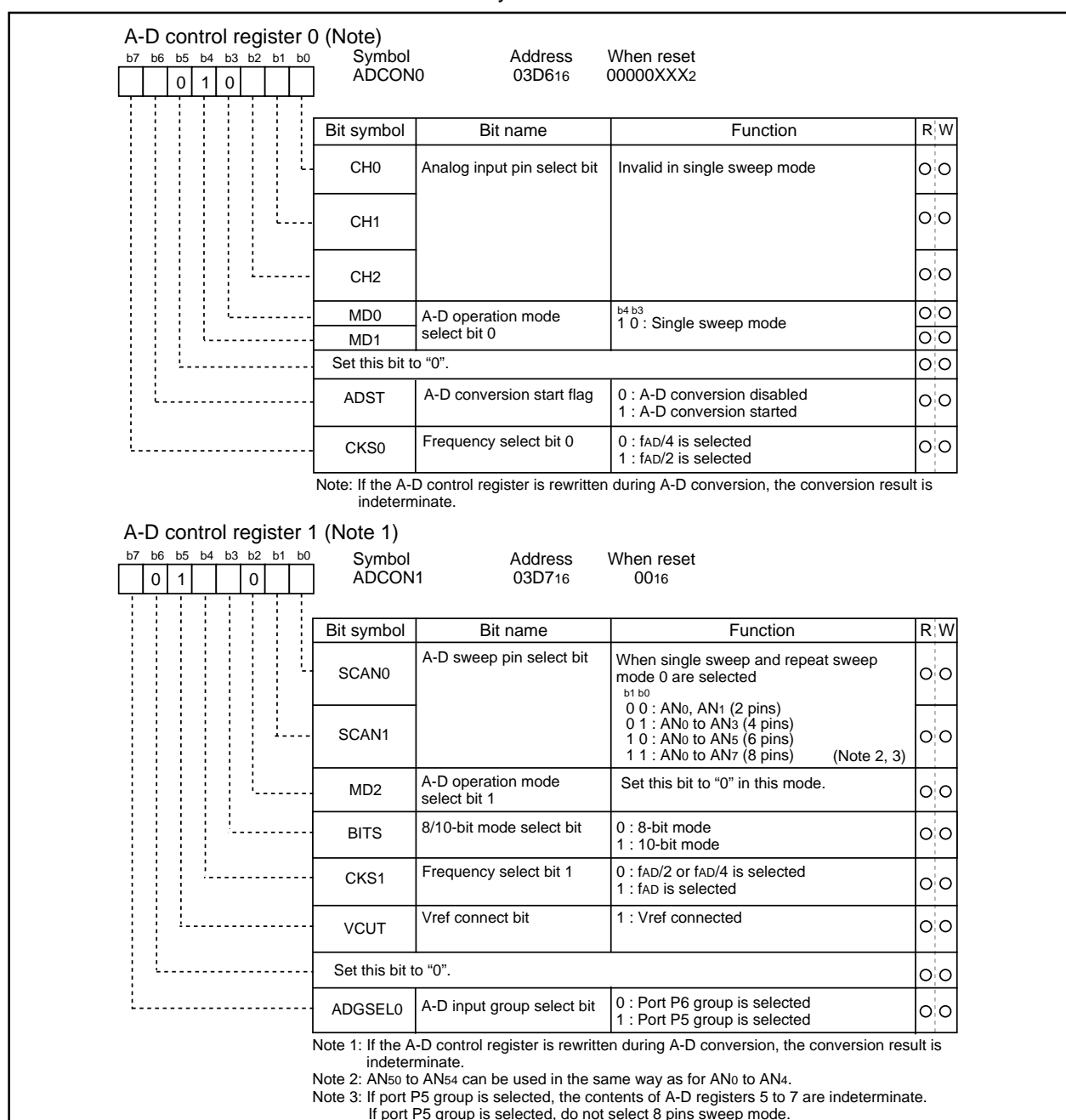
**(3) Single sweep mode**

In single sweep mode, the pins selected using the A-D sweep pin select bit are used for one-by-one A-D conversion. (See Table 1.32.) Figure 1.87 shows the A-D control register in single sweep mode.

**Table 1.32. Single sweep mode specifications**

| Item                                | Specification  |
|-------------------------------------|--|
| Function                            | The pins selected by the A-D sweep pin select bit are used for one-by-one A-D conversion   |
| Start condition                     | Writing "1" to A-D converter start flag  |
| Stop condition                      | <ul style="list-style-type: none"> <li>End of A-D conversion (A-D conversion start flag changes to "0".)</li> <li>Writing "0" to A-D conversion start flag</li> </ul>                        |
| Interrupt request generation timing | End of A-D conversion  |
| Input pin                           | AN <sub>0</sub> and AN <sub>1</sub> (2 pins), AN <sub>0</sub> to AN <sub>3</sub> (4 pins), AN <sub>0</sub> to AN <sub>5</sub> (6 pins), or AN <sub>0</sub> to AN <sub>7</sub> (8 pins)(Note) |
| Reading of result of A-D converter  | Read A-D register corresponding to selected pin  |

Note : AN<sub>50</sub> to AN<sub>54</sub> can be used in the same way as for AN<sub>0</sub> to AN<sub>4</sub>.

**Figure 1.87. A-D conversion register in single sweep mode**

## A-D Converter

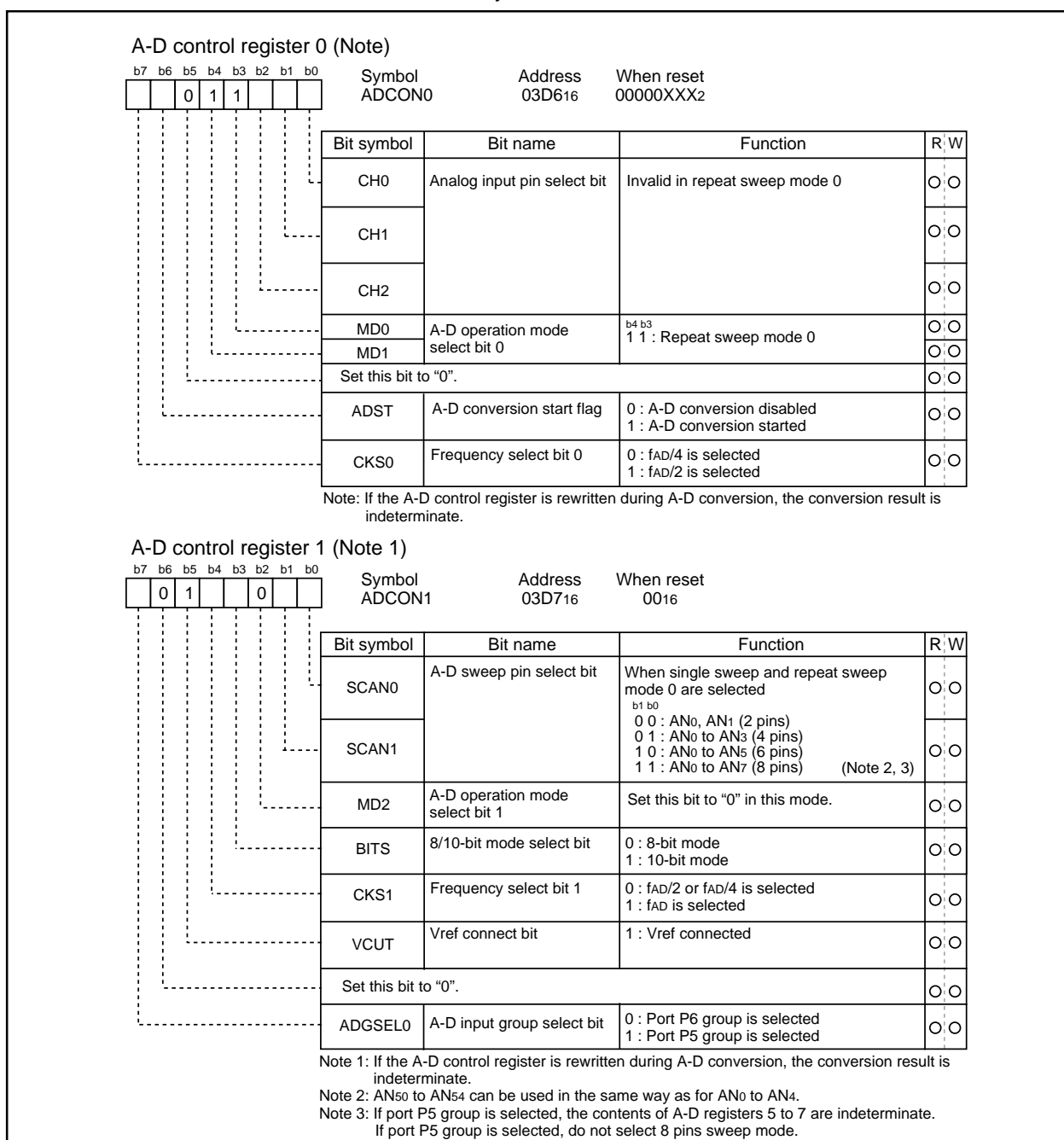
**(4) Repeat sweep mode 0**

In repeat sweep mode 0, the pins selected using the A-D sweep pin select bit are used for repeat sweep A-D conversion. (See Table 1.33.) Figure 1.88 shows the A-D control register in repeat sweep mode 0.

**Table 1.33. Repeat sweep mode 0 specifications**

| Item                                | Specification  |
|-------------------------------------|--|
| Function                            | The pins selected by the A-D sweep pin select bit are used for repeat sweep A-D conversion   |
| Start condition                     | Writing "1" to A-D conversion start flag   |
| Stop condition                      | Writing "0" to A-D conversion start flag   |
| Interrupt request generation timing | None generated   |
| Input pin                           | AN0 and AN1 (2 pins), AN0 to AN3 (4 pins), AN0 to AN5 (6 pins), or AN0 to AN7 (8 pins)(Note) |
| Reading of result of A-D converter  | Read A-D register corresponding to selected pin (at any time)                                |

Note : AN50 to AN54 can be used in the same way as for AN0 to AN4.

**Figure 1.88. A-D conversion register in repeat sweep mode 0**



## A-D Converter

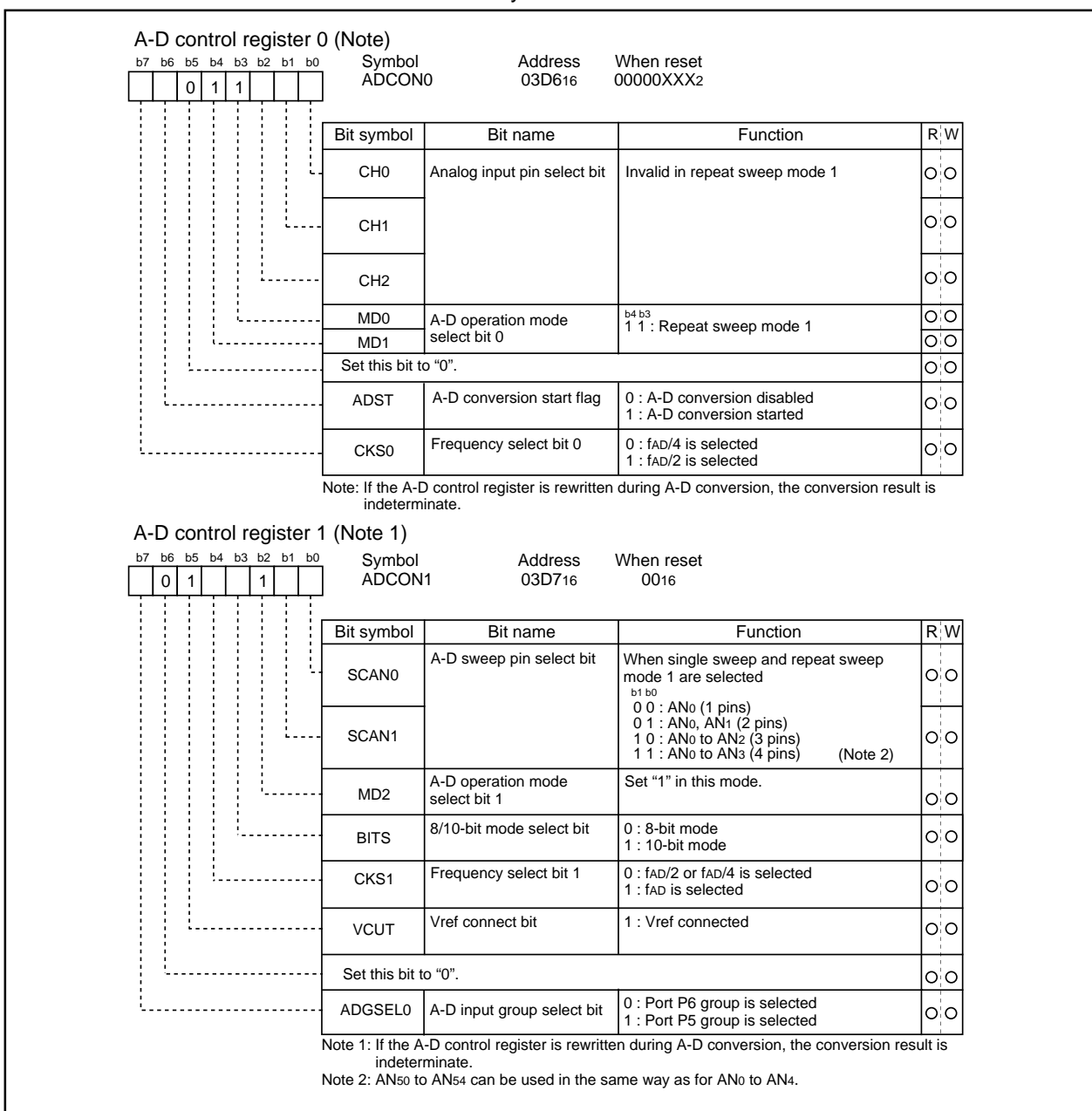
**(5) Repeat sweep mode 1**

In repeat sweep mode 1, all pins are used for A-D conversion with emphasis on the pin or pins selected using the A-D sweep pin select bit. (See Table 1.34.) Figure 1.89 shows the A-D control register in repeat sweep mode 1.

**Table 1.34. Repeat sweep mode 1 specifications**

| Item                                | Specification  |
|-------------------------------------|--|
| Function                            | All pins perform repeat sweep A-D conversion, with emphasis on the pin or pins selected by the A-D sweep pin select bit<br>Example : AN <sub>0</sub> selected    AN <sub>0</sub> → AN <sub>1</sub> → AN <sub>0</sub> → AN <sub>2</sub> → AN <sub>0</sub> → AN <sub>3</sub> , etc |
| Start condition                     | Writing "1" to A-D conversion start flag   |
| Stop condition                      | Writing "0" to A-D conversion start flag   |
| Interrupt request generation timing | None generated   |
| Input pin                           | AN <sub>0</sub> (1 pin), AN <sub>0</sub> and AN <sub>1</sub> (2 pins), AN <sub>0</sub> to AN <sub>2</sub> (3 pins), AN <sub>0</sub> to AN <sub>3</sub> (4 pins) (Note)   |
| Reading of result of A-D converter  | Read A-D register corresponding to selected pin (at any time)  |

Note : AN<sub>50</sub> to AN<sub>54</sub> can be used in the same way as for AN<sub>0</sub> to AN<sub>4</sub>.

**Figure 1.89. A-D conversion register in repeat sweep mode 1**

## A-D Converter

---

- **Sample and hold**

Sample and hold is selected by setting bit 0 of the A-D control register 2 (address 03D416) to “1”. When sample and hold is selected, the rate of conversion of each pin increases. As a result, a 28  $\phi_{AD}$  cycle is achieved with 8-bit resolution and 33  $\phi_{AD}$  with 10-bit resolution. Sample and hold can be selected in all modes. However, in all modes, be sure to specify before starting A-D conversion whether sample and hold is to be used.

## Programmable I/O Ports

There are 43 programmable I/O ports: P0 to P7. Each port can be set independently for input or output using the direction register. A pull-up resistance for each block of 4 ports can be set. The port P1 allows the drive capacity of its N-channel output transistor to be set as necessary.

Figures 1.90 to 1.92 show the programmable I/O ports.

Each pin functions as a programmable I/O port and as the I/O for the built-in peripheral devices.

To use the pins as the inputs for the built-in peripheral devices, set the direction register of each pin to input mode. When the pins are used as the outputs for the built-in peripheral devices, they function as outputs regardless of the contents of the direction registers. See the descriptions of the respective functions for how to set up the built-in peripheral devices.

### (1) Direction registers

Figure 1.93 shows the direction registers.

These registers are used to choose the direction of the programmable I/O ports. Each bit in these registers corresponds one for one to each I/O pin.

### (2) Port registers

Figure 1.94 shows the port registers.

These registers are used to write and read data for input and output to and from an external device. A port register consists of a port latch to hold output data and a circuit to read the status of a pin. Each bit in port registers corresponds one for one to each I/O pin.

### (3) Pull-up control registers

Figure 1.95 shows the pull-up control registers.

The pull-up control register can be set to apply a pull-up resistance to each block of 4 ports. When ports are set to have a pull-up resistance, the pull-up resistance is connected only when the direction register is set for input.

### (4) Port P1 drive capacity control register

Figure 1.95 shows a structure of the port P1 drive capacity control register.

This register is used to control the drive capacity of the port P1's N-channel output transistor. Each bit in this register corresponds one for one to the port pins.

## Programmable I/O Port

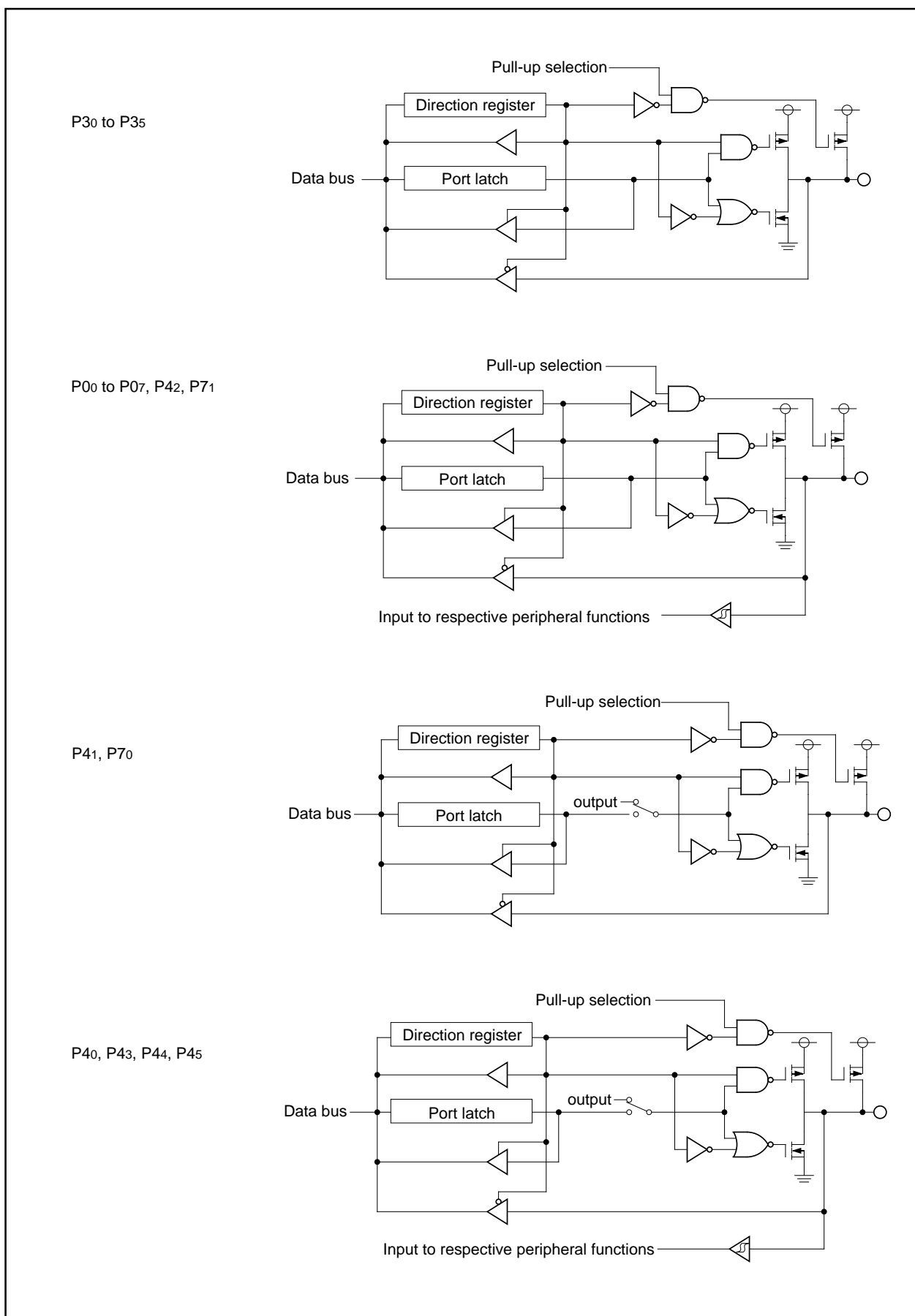


Figure 1.90. Programmable I/O ports (1)

## Programmable I/O Port

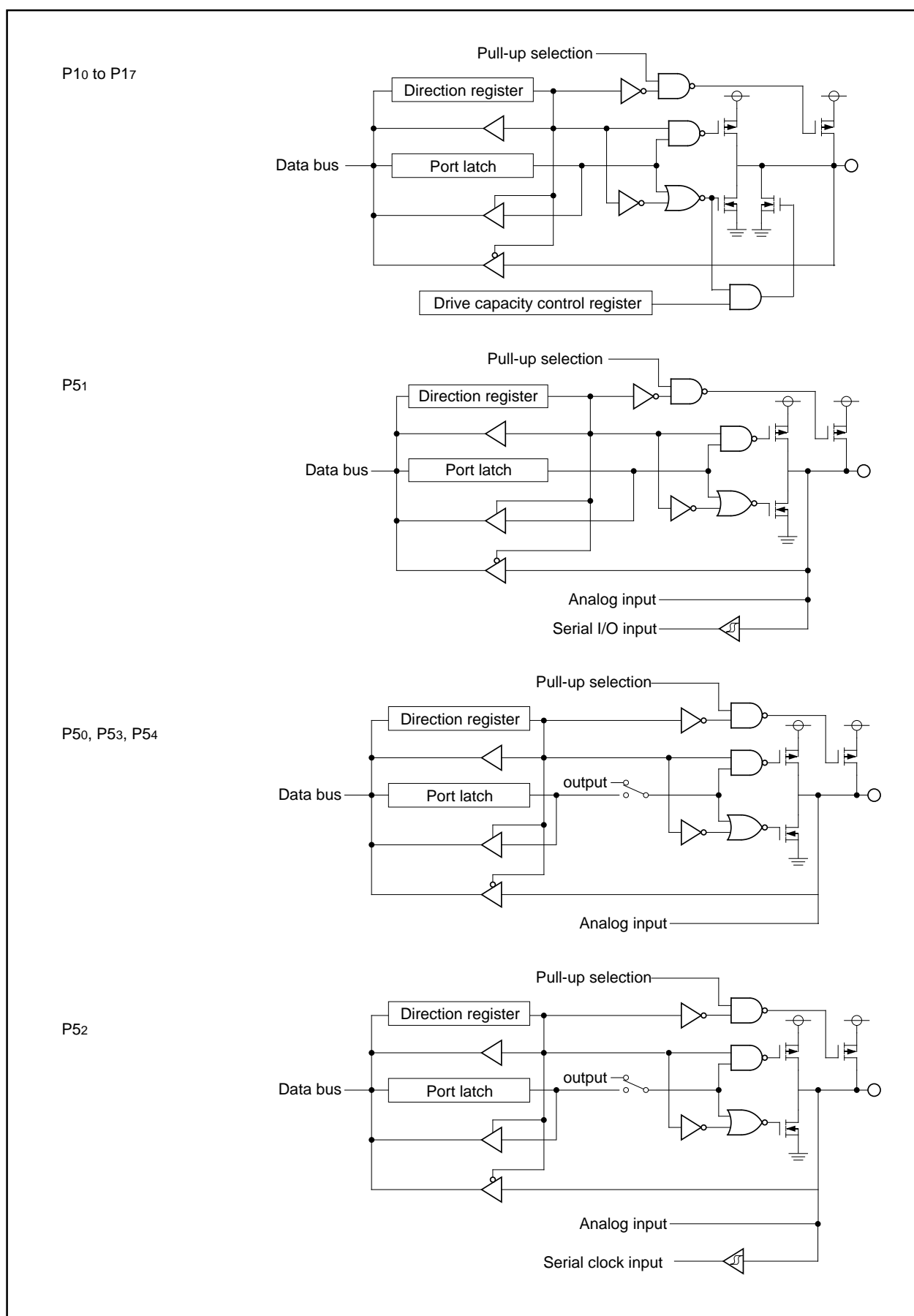


Figure 1.91. Programmable I/O ports (2)

## Programmable I/O Port

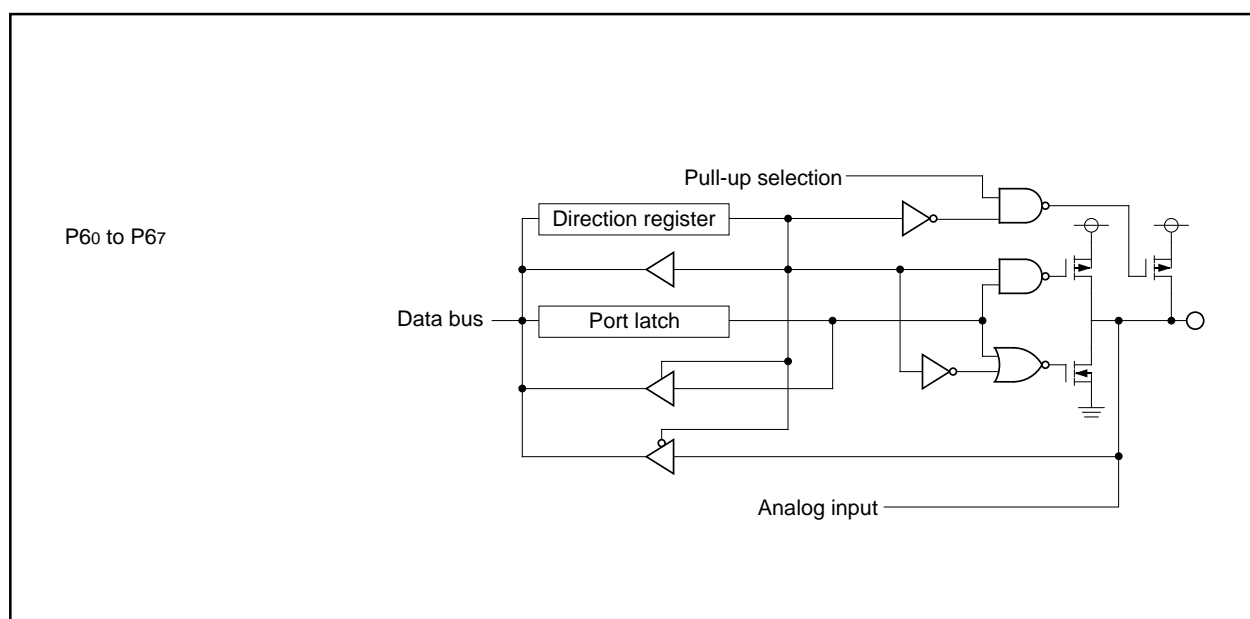


Figure 1.92. Programmable I/O ports (3)

## Programmable I/O Port

## Port Pi direction register (Note 1)

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Symbol           | Address   | When reset  |     |
|----|----|----|----|----|----|----|----|------------------|---|---|-----|
|    |    |    |    |    |    |    |    | PDi (i = 0 to 7) | 03E2 <sub>16</sub> , 03E3 <sub>16</sub> , 03E7 <sub>16</sub> , 03EA <sub>16</sub> ,<br>03EB <sub>16</sub> , 03EE <sub>16</sub> , 03EF <sub>16</sub> | 00 <sub>16</sub><br>00 <sub>16</sub>  |     |
|    |    |    |    |    |    |    |    | Bit symbol       | Bit name  | Function  | R/W |
|    |    |    |    |    |    |    |    | PDi_0            | Port Pi0 direction register   | 0 : Input mode<br>(Functions as an input port)<br>1 : Output mode<br>(Functions as an output port)<br>(i = 0 to 7 except 2) | ○/○ |
|    |    |    |    |    |    |    |    | PDi_1            | Port Pi1 direction register   |   | ○/○ |
|    |    |    |    |    |    |    |    | PDi_2            | Port Pi2 direction register   |   | ○/○ |
|    |    |    |    |    |    |    |    | PDi_3            | Port Pi3 direction register   |   | ○/○ |
|    |    |    |    |    |    |    |    | PDi_4            | Port Pi4 direction register   |   | ○/○ |
|    |    |    |    |    |    |    |    | PDi_5            | Port Pi5 direction register   |   | ○/○ |
|    |    |    |    |    |    |    |    | PDi_6            | Port Pi6 direction register   |   | ○/○ |
|    |    |    |    |    |    |    |    | PDi_7            | Port Pi7 direction register   |   | ○/○ |

Note 1: Set bit 2 of protect register (address 000A<sub>16</sub>) to "1" before rewriting to the port P4 direction register.

Note 2: Nothing is assigned in direction register of P3<sub>6</sub>, P3<sub>7</sub>, P4<sub>6</sub>, P4<sub>7</sub>, P5<sub>5</sub> to p5<sub>7</sub>, P7<sub>2</sub> to P7<sub>7</sub>. These bits can either be set nor reset. When read, its contents are indeterminate.

Figure 1.93. Direction register

## Programmable I/O Port

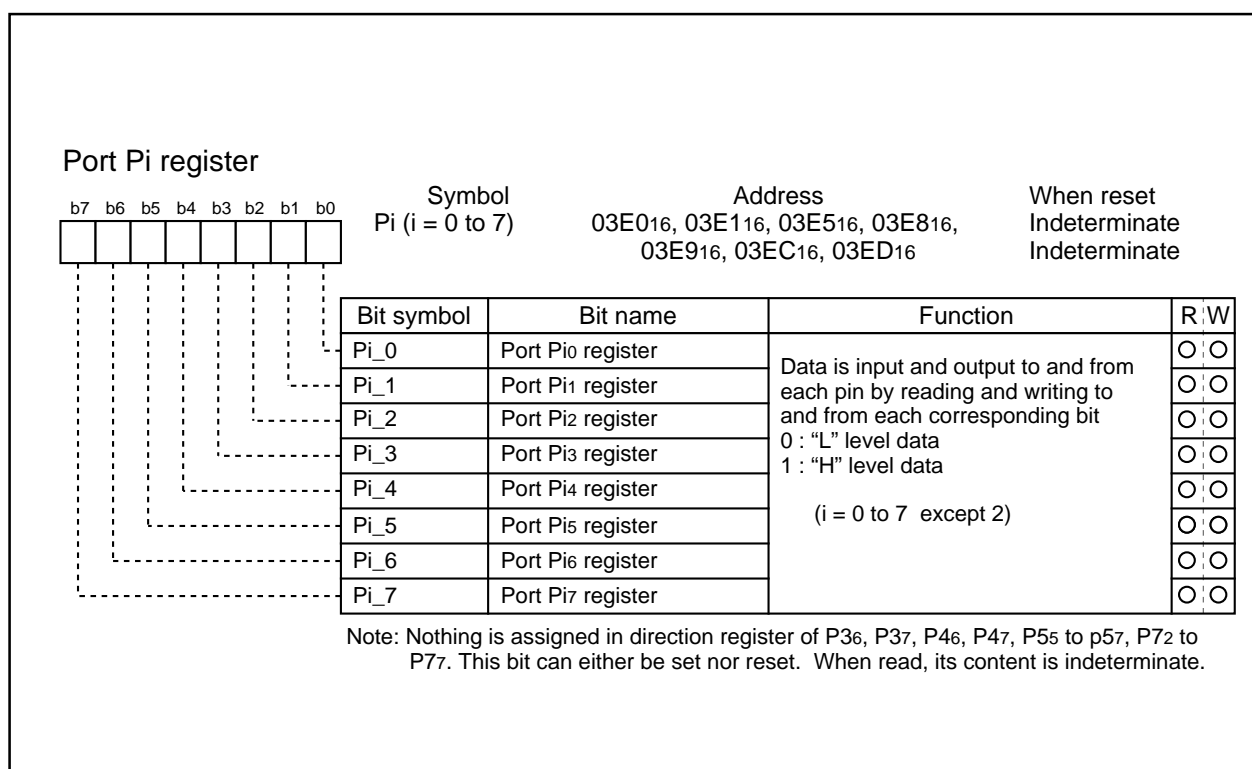
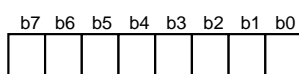


Figure 1.94. Port register



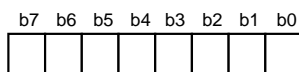
## Programmable I/O Port

## Pull-up control register 0

Symbol  
PUR0Address  
03FC<sub>16</sub>When reset  
00<sub>16</sub>

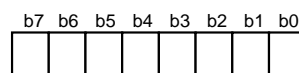
| Bit symbol | Bit name           | Function  | R | W |
|------------|--------------------|---|---|---|
| PU00       | P00 to P03 pull-up | The corresponding port is pulled high with a pull-up resistor<br>0 : Not pulled high<br>1 : Pulled high | ○ | ○ |
| PU01       | P04 to P07 pull-up |   | ○ | ○ |
| PU02       | P10 to P13 pull-up |   | ○ | ○ |
| PU03       | P14 to P17 pull-up |   | ○ | ○ |
| —          | —                  |   | ○ | ○ |
| —          | —                  |   | ○ | ○ |
| PU06       | P30 to P33 pull-up |   | ○ | ○ |
| PU07       | P34 to P35 pull-up |   | ○ | ○ |

## Pull-up control register 1

Symbol  
PUR1Address  
03FD<sub>16</sub>When reset  
00<sub>16</sub>

| Bit symbol | Bit name           | Function  | R | W |
|------------|--------------------|---|---|---|
| PU10       | P40 to P43 pull-up | The corresponding port is pulled high with a pull-up resistor<br>0 : Not pulled high<br>1 : Pulled high | ○ | ○ |
| PU11       | P44 to P47 pull-up |   | ○ | ○ |
| PU12       | P50 to P53 pull-up |   | ○ | ○ |
| PU13       | P54 pull-up        |   | ○ | ○ |
| PU14       | P60 to P63 pull-up |   | ○ | ○ |
| PU15       | P64 to P67 pull-up |   | ○ | ○ |
| PU16       | P70 to P71 pull-up |   | ○ | ○ |
| —          | —                  |   | ○ | ○ |

## Port P1 drive capacity control register

Symbol  
DRRAddress  
03FE<sub>16</sub>When reset  
00<sub>16</sub>

| Bit symbol | Bit name                | Function   | R | W |
|------------|-------------------------|--|---|---|
| DRR0       | Port P10 drive capacity | Set P1 N-channel output transistor drive capacity<br>0 : LOW<br>1 : HIGH | ○ | ○ |
| DRR1       | Port P11 drive capacity |  | ○ | ○ |
| DRR2       | Port P12 drive capacity |  | ○ | ○ |
| DRR3       | Port P13 drive capacity |  | ○ | ○ |
| DRR4       | Port P14 drive capacity |  | ○ | ○ |
| DRR5       | Port P15 drive capacity |  | ○ | ○ |
| DRR6       | Port P16 drive capacity |  | ○ | ○ |
| DRR7       | Port P17 drive capacity |  | ○ | ○ |

Figure 1.95. Pull-up control register

Programmable I/O Port

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**Example connection of unused pins****Table 1.36. Example connection of unused pins**

| Pin name               | Connection   |
|------------------------|--|
| Ports P0, P1, P3 to P7 | After setting for input mode, connect every pin to Vss (pull-down); or after setting for output mode, leave these pins open. |
| XOUT (Note)            | Open   |
| AVCC                   | Connect to VCC   |
| AVSS, VREF             | Connect to VSS   |

Note: With external clock input to XIN pin.

## Usage precaution

**Usage Precaution****Timer A (timer mode)**

- (1) Reading the timer A0 register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer A0 register with the reload timing gets "FFFF<sub>16</sub>". Reading the timer A0 register after setting a value in the timer A0 register with a count halted but before the counter starts counting gets a proper value.

**Timer A (event counter mode)**

- (1) Reading the timer A0 register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer A0 register with the reload timing gets "FFFF<sub>16</sub>" by under-flow or "0000<sub>16</sub>" by overflow. Reading the timer A0 register after setting a value in the timer A0 register with a count halted but before the counter starts counting gets a proper value.
- (2) When stop counting in free run type, set timer again.

**Timer A (one-shot timer mode)**

- (1) Setting the count start flag to "0" while a count is in progress causes as follows:
  - The counter stops counting and a content of reload register is reloaded.
  - The TA0OUT pin outputs "L" level.
  - The interrupt request generated and the timer A0 interrupt request bit goes to "1".
- (2) The timer A0 interrupt request bit goes to "1" if the timer's operation mode is set using any of the following procedures:
  - Selecting one-shot timer mode after reset.
  - Changing operation mode from timer mode to one-shot timer mode.
  - Changing operation mode from event counter mode to one-shot timer mode.

Therefore, to use timer A0 interrupt (interrupt request bit), set timer A0 interrupt request bit to "0" after the above listed changes have been made.

**Timer A (pulse width modulation mode)**

- (1) The timer A0 interrupt request bit becomes "1" if setting operation mode of the timer in compliance with any of the following procedures:
  - Selecting PWM mode after reset.
  - Changing operation mode from timer mode to PWM mode.
  - Changing operation mode from event counter mode to PWM mode.

Therefore, to use timer A0 interrupt (interrupt request bit), set timer A0 interrupt request bit to "0" after the above listed changes have been made.

- (2) Setting the count start flag to "0" while PWM pulses are being output causes the counter to stop counting. If the TA0OUT pin is outputting an "H" level in this instance, the output level goes to "L", and the timer A0 interrupt request bit goes to "1". If the TA0OUT pin is outputting an "L" level in this instance, the level does not change, and the timer A0 interrupt request bit does not becomes "1".

## Usage precaution

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### Timer B (timer mode, event counter mode)

- (1) Reading the timer Bi register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Bi register with the reload timing gets "FFFF<sub>16</sub>". Reading the timer Bi register after setting a value in the timer Bi register with a count halted but before the counter starts counting gets a proper value.

### Timer B (pulse period/pulse width measurement mode)

- (1) If changing the measurement mode select bit is set after a count is started, the timer Bi interrupt request bit goes to "1".
- (2) When the first effective edge is input after a count is started, an indeterminate value is transferred to the reload register. At this time, timer Bi interrupt request is not generated.

### Timer X (timer mode)

- (1) Reading the timer Xi register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Xi register with the reload timing gets "FFFF<sub>16</sub>". Reading the timer A0 register after setting a value in the timer Xi register with a count halted but before the counter starts counting gets a proper value.

### Timer X (event counter mode)

- (1) Reading the timer Xi register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Xi register with the reload timing gets "FFFF<sub>16</sub>" by underflow or "0000<sub>16</sub>" by overflow. Reading the timer Xi register after setting a value in the timer Xi register with a count halted but before the counter starts counting gets a proper value.
- (2) When stop counting in free run type, set timer again.

### Timer X (one-shot timer mode)

- (1) Setting the count start flag to "0" while a count is in progress causes as follows:
  - The counter stops counting and a content of reload register is reloaded.
  - The TXiINOUT pin outputs "L" level.
  - The interrupt request generated and the timer Xi interrupt request bit goes to "1".
- (2) The timer Xi interrupt request bit goes to "1" if the timer's operation mode is set using any of the following procedures:
  - Selecting one-shot timer mode after reset.
  - Changing operation mode from timer mode to one-shot timer mode.
  - Changing operation mode from event counter mode to one-shot timer mode.

Therefore, to use timer Xi interrupt (interrupt request bit), set timer Xi interrupt request bit to "0" after the above listed changes have been made.

## Usage precaution

**Timer X (pulse width modulation mode)**

- (1) The timer Xi interrupt request bit becomes "1" if setting operation mode of the timer in compliance with any of the following procedures:

- Selecting PWM mode after reset.
- Changing operation mode from timer mode to PWM mode.
- Changing operation mode from event counter mode to PWM mode.

Therefore, to use timer Xi interrupt (interrupt request bit), set timer Xi interrupt request bit to "0" after the above listed changes have been made.

- (2) Setting the count start flag to "0" while PWM pulses are being output causes the counter to stop counting. If the TXiINOUT pin is outputting an "H" level in this instance, the output level goes to "L", and the timer Xi interrupt request bit goes to "1". If the TXiINOUT pin is outputting an "L" level in this instance, the level does not change, and the timer Xi interrupt request bit does not become "1".

**Timer X (pulse period/pulse width measurement mode)**

- (1) If changing the measurement mode select bit is set after a count is started, the timer Xi interrupt request bit goes to "1".
- (2) When the first effective edge is input after a count is started, an indeterminate value is transferred to the reload register. At this time, timer Xi interrupt request is not generated.

**A-D Converter**

- (1) Write to each bit (except bit 6) of A-D control register 0, to each bit of A-D control register 1, and to bit 0 of A-D control register 2 when A-D conversion is stopped (before a trigger occurs).  
In particular, when the Vref connection bit is changed from "0" to "1", start A-D conversion after an elapse of 1  $\mu$ s or longer.
- (2) When changing A-D operation mode, select analog input pin again.
- (3) Using one-shot mode or single sweep mode  
Read the correspondence A-D register after confirming A-D conversion is finished. (It is known by A-D conversion interrupt request bit.)
- (4) Using repeat mode, repeat sweep mode 0 or repeat sweep mode 1  
Use the undivided main clock as the internal CPU clock.

**Stop Mode and Wait Mode**

- (1) When returning from stop mode by hardware reset,  $\overline{\text{RESET}}$  pin must be set to "L" level until main clock oscillation is stabilized.
- (2) When shifting to WAIT mode or STOP mode, the program stops after reading 8 bytes from the WAIT instruction and the instruction that sets all clock stop bits to "1" in the instruction queue. Therefore, insert a minimum of 8 NOPs after the WAIT instruction and the instruction that sets all clock stop bits to "1".
- (3) When the MCU running in low-speed or low power dissipation mode, do not enter WAIT mode with WAIT peripheral function clock stop bit set to "1".

## Usage precaution

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### Interrupts

(1) Reading address 00000<sub>16</sub>

- When maskable interrupt is occurred, CPU read the interrupt information (the interrupt number and interrupt request level) in the interrupt sequence.

The interrupt request bit of the certain interrupt written in address 00000<sub>16</sub> will then be set to "0".

Reading address 00000<sub>16</sub> by software sets enabled highest priority interrupt source request bit to "0".

Though the interrupt is generated, the interrupt routine may not be executed.

Do not read address 00000<sub>16</sub> by software.

(2) Setting the stack pointer

- The value of the stack pointer immediately after reset is initialized to 0000<sub>16</sub>. Accepting an interrupt before setting a value in the stack pointer may become a factor of runaway. Be sure to set a value in the stack pointer before accepting an interrupt.

Concerning the first instruction immediately after reset, generating any interrupt is prohibited.

(3) External interrupt

- When changing a polarity of pins  $\overline{\text{INT0}}$  and  $\overline{\text{INT1}}$ , the interrupt request bit may become "1". Clear the interrupt request bit after changing the polarity.

(4) Changing interrupt control register

See "Changing Interrupt Control Register".

## Electrical characteristics

### Electrical characteristics

**Table 1.36. Absolute maximum ratings**

| Symbol           | Parameter   | Condition              | Rated value                                | Unit |
|------------------|---|------------------------|--|------|
| V <sub>cc</sub>  | Supply voltage  |                        | - 0.3 to 6.5 (Note 1)                      | V    |
| AV <sub>cc</sub> | Analog supply voltage   |                        | - 0.3 to 6.5 (Note 1)                      | V    |
| V <sub>I</sub>   | Input voltage<br>RESET, CNV <sub>ss</sub> , P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>5</sub> ,<br>P4 <sub>0</sub> to P4 <sub>5</sub> , P5 <sub>0</sub> to P5 <sub>4</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> ,<br>P7 <sub>0</sub> , P7 <sub>1</sub> , VREF, XIN |                        | - 0.3 to V <sub>cc</sub> + 0.3<br>(Note 2) | V    |
| V <sub>O</sub>   | Output voltage<br>P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>5</sub> , P4 <sub>0</sub> to P4 <sub>5</sub> ,<br>P5 <sub>0</sub> to P5 <sub>4</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>0</sub> , P7 <sub>1</sub> , VREF, XIN                              |                        | - 0.3 to V <sub>cc</sub> + 0.3             | V    |
| P <sub>d</sub>   | Power dissipation   | T <sub>a</sub> = 25 °C | 1000 (Note 3)                              | mW   |
| T <sub>opr</sub> | Operating ambient temperature   |                        | - 20 to 85 (Note 4)                        | °C   |
| T <sub>stg</sub> | Storage temperature   |                        | - 40 to 150 (Note 5)                       | °C   |

Note 1: Flash memory version: -0.3 to 7 (V) .

Note 2: When writing to flash MCU, CNV<sub>ss</sub> is -0.3 to 13 (V) .

Note 3: Flat package (56P6S-A) is 300 mW.

Note 4: Extended operating temperature version: -40 to 85 °C. When flash memory version is program/erase mode: 25±5 °C.

Note 5: Extended operating temperature version: -65 to 150 °C.

## Electrical characteristics

**Table 1.37. Recommended operating conditions (Note 1)**

| Symbol                 | Parameter                              |   | Standard                      |                 |                              | Unit |
|------------------------|--|---|-------------------------------|-----------------|------------------------------|------|
|                        |  |   | Min                           | Typ.            | Max.                         |      |
| V <sub>CC</sub>        | Supply voltage                         | Mask ROM version  | 2.7                           | 5.0             | 5.5                          | V    |
|                        |  | Flash memory version  | 4.0                           | 5.0             | 5.5                          |      |
| A <sub>V</sub> CC      | Analog supply voltage                  |   |                               | V <sub>CC</sub> |                              | V    |
| V <sub>SS</sub>        | Supply voltage                         |   |                               | 0               |                              | V    |
| A <sub>V</sub> SS      | Analog supply voltage                  |   |                               | 0               |                              | V    |
| V <sub>IH</sub>        | HIGH input voltage                     | P00 to P07, P10 to P17, P30 to P35, P40 to P45,<br>P50 to P54, P60 to P67, P70, P71, X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , | 0.8V <sub>CC</sub>            |                 | V <sub>CC</sub>              | V    |
| V <sub>IL</sub>        | LOW input voltage                      | P00 to P07, P10 to P17, P30 to P35, P40 to P45,<br>P50 to P54, P60 to P67, P70, P71, X <sub>IN</sub> , RESET, CNV <sub>SS</sub>   | 0                             |                 | 0.2V <sub>CC</sub>           | V    |
| I <sub>OH</sub> (peak) | HIGH peak output current               | P00 to P07, P10 to P17, P30 to P35, P40 to P45,<br>P50 to P54, P60 to P67, P70, P71   |                               |                 | - 10.0                       | mA   |
| I <sub>OL</sub> (peak) | LOW peak output current                | P00 to P07, P30 to P35, P40 to P45,<br>P50 to P54, P60 to P67, P70, P71   |                               |                 | 10.0                         | mA   |
| I <sub>OL</sub> (peak) | LOW peak output current                | P10 to P17  |                               |                 | 30.0                         | mA   |
|                        |  | HIGHPOWER<br>LOWPOWER   |                               |                 | 10.0                         |      |
| I <sub>OH</sub> (avg)  | HIGH average output current            | P00 to P07, P10 to P17, P30 to P35, P40 to P45,<br>P50 to P54, P60 to P67, P70, P71   |                               |                 | - 5.0                        | mA   |
| I <sub>OL</sub> (avg)  | LOW average output current             | P00 to P07, P30 to P35, P40 to P45,<br>P50 to P54, P60 to P67, P70, P71   |                               |                 | 5.0                          | mA   |
| I <sub>OL</sub> (avg)  | LOW average output current             | P10 to P17  |                               |                 | 15.0                         | mA   |
|                        |  | HIGHPOWER<br>LOWPOWER   |                               |                 | 5.0                          |      |
| f (X <sub>IN</sub> )   | Main clock input oscillation frequency | Mask ROM version  | V <sub>CC</sub> =4.0V to 5.5V | 0               | 10                           | MHz  |
|                        |  |   | V <sub>CC</sub> =2.7V to 4.0V | 0               | 5 x V <sub>CC</sub> - 10.000 | MHz  |
|                        |  | Flash memory version  | V <sub>CC</sub> =4.0V to 5.5V | 0               | 10                           | MHz  |
| f (X <sub>CIN</sub> )  | Subclock oscillation frequency         |   |                               | 32.768          | 50                           | kHz  |

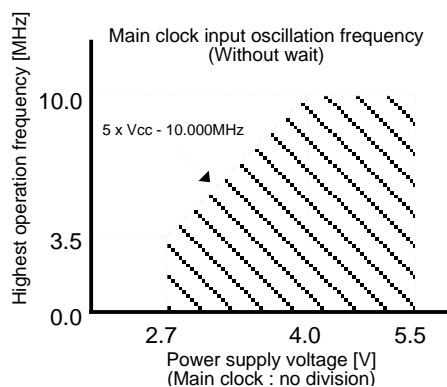
Note 1: Unless otherwise noted: V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 20 to 85°C (Extended operating temperature version:- 40 to 85°C). Flash version: V<sub>CC</sub> = 4.0V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 20 to 85°C (Extended operating temperature version:- 40 to 85°C.)

Note 2: The average output current is an average value measured over 100ms.

Note 3: Keep output current as follows:

The sum of port P3 and P4 I<sub>OL</sub> (peak) is under 40 mA. The sum of port P1 I<sub>OL</sub> (peak) is under 60 mA. The sum of port P1, P3 and P4 I<sub>OH</sub> (peak) is under 40 mA. The sum of port P0, P5, P6 and P7 I<sub>OL</sub> (peak) is under 80 mA. The sum of port P0, P5, P6 and P7 I<sub>OH</sub> (peak) is under 80 mA.

Note 4: Relationship between main clock oscillation frequency and supply voltage.





Electrical characteristics (V<sub>CC</sub> = 5V)

V<sub>CC</sub> = 5V

**Table 1.38. Electrical characteristics (Note1)**

| Symbol                           | Parameter             |  | Measuring condition  | Standard |      |       | Unit |
|----------------------------------|-----------------------|--|--|----------|------|-------|------|
|                                  |                       |  |  | Min.     | Typ. | Max.  |      |
| V <sub>OH</sub>                  | HIGH output voltage   | P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>5</sub> ,<br>P4 <sub>0</sub> to P4 <sub>5</sub> , P5 <sub>0</sub> to P5 <sub>4</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>0</sub> , P7 <sub>1</sub>                   | I <sub>OH</sub> = - 5 mA   | 3.0      |      |       | V    |
| V <sub>OH</sub>                  | HIGH output voltage   | P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>5</sub> ,<br>P4 <sub>0</sub> to P4 <sub>5</sub> , P5 <sub>0</sub> to P5 <sub>4</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>0</sub> , P7 <sub>1</sub>                   | I <sub>OH</sub> = - 200 μA   | 4.7      |      |       | V    |
| V <sub>OH</sub>                  | HIGH output voltage   | X <sub>OUT</sub>   | HIGHPOWER  | 3.0      |      |       | V    |
|                                  |                       |  | LOWPOWER   | 3.0      |      |       |      |
| V <sub>OH</sub>                  | HIGH output voltage   | X <sub>COU</sub> T   | HIGHPOWER  |          | 3.0  |       | V    |
|                                  |                       |  | LOWPOWER   |          | 1.6  |       |      |
| V <sub>OL</sub>                  | LOW output voltage    | P0 <sub>0</sub> to P0 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>5</sub> , P4 <sub>0</sub> to P4 <sub>5</sub><br>P5 <sub>0</sub> to P5 <sub>4</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>0</sub> , P7 <sub>1</sub>  | I <sub>OL</sub> = 5 mA   |          |      | 2.0   | V    |
| V <sub>OL</sub>                  | LOW output voltage    | P0 <sub>0</sub> to P0 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>5</sub> , P4 <sub>0</sub> to P4 <sub>5</sub><br>P5 <sub>0</sub> to P5 <sub>4</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>0</sub> , P7 <sub>1</sub>  | I <sub>OL</sub> = 200 μA   |          |      | 0.45  | V    |
| V <sub>OL</sub>                  | LOW output voltage    | P1 <sub>0</sub> to P1 <sub>7</sub>   | HIGHPOWER  |          |      | 2.0   | V    |
|                                  |                       |  | LOWPOWER   |          |      | 2.0   |      |
| V <sub>OL</sub>                  | LOW output voltage    | P1 <sub>0</sub> to P1 <sub>7</sub>   | HIGHPOWER  |          |      | 0.3   | V    |
|                                  |                       |  | LOWPOWER   |          |      | 0.45  |      |
| V <sub>OL</sub>                  | LOW output voltage    | X <sub>OUT</sub>   | HIGHPOWER  |          |      | 2.0   | V    |
|                                  |                       |  | LOWPOWER   |          |      | 2.0   |      |
| V <sub>OL</sub>                  | LOW output voltage    | X <sub>OUT</sub>   | HIGHPOWER  |          | 0    |       | V    |
|                                  |                       |  | LOWPOWER   |          | 0    |       |      |
| V <sub>T+</sub> -V <sub>T-</sub> | Hysteresis            | TA0IN, TX0INOUT, TX1INOUT, TX2INOUT<br>TB0IN, TB1IN INT0, INT1, CLK0, KI0 to KI7<br>RxD0, RxD1   |  | 0.2      |      | 0.8   | V    |
| V <sub>T+</sub> -V <sub>T-</sub> | Hysteresis            | RESET  |  | 0.2      |      | 1.8   | V    |
| I <sub>IH</sub>                  | HIGH input current    | P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>5</sub> ,<br>P4 <sub>0</sub> to P4 <sub>5</sub> , P5 <sub>0</sub> to P5 <sub>4</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> ,<br>P7 <sub>0</sub> , P7 <sub>1</sub> , RESET, CNVss | V <sub>I</sub> = 5V  |          |      | 5.0   | μA   |
| I <sub>IL</sub>                  | LOW input current     | P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>5</sub> ,<br>P4 <sub>0</sub> to P4 <sub>5</sub> , P5 <sub>0</sub> to P5 <sub>4</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> ,<br>P7 <sub>0</sub> , P7 <sub>1</sub> , RESET, CNVss | V <sub>I</sub> = 0V  |          |      | -5.0  | μA   |
| R <sub>PULLUP</sub>              | Pull-up resistor      | P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>5</sub> ,<br>P4 <sub>0</sub> to P4 <sub>5</sub> , P5 <sub>0</sub> to P5 <sub>4</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>0</sub> , P7 <sub>1</sub>                   | V <sub>I</sub> = 0V  | 30.0     | 50.0 | 167.0 | kΩ   |
| R <sub>XIN</sub>                 | Feedback resistor     | X <sub>IN</sub>  |  |          | 1.0  |       | MΩ   |
| R <sub>XCIN</sub>                | Feedback resistor     | X <sub>CIN</sub>   |  |          | 6.0  |       | MΩ   |
| V <sub>RAM</sub>                 | RAM retention voltage |  | When clock is stopped  | 2.0      |      |       | V    |
| I <sub>CC</sub>                  | Power supply current  | I/O pin has no load  | f(X <sub>IN</sub> )=10MHz<br>Square wave, no division                      |          | 19.0 | 38.0  | mA   |
|                                  |                       |  | f(X <sub>CIN</sub> )=32kHz<br>Square wave                                  |          | 90.0 |       | μA   |
|                                  |                       |  | f(X <sub>CIN</sub> )=32kHz<br>When a WAIT instruction is executed (Note 2) |          | 4.0  |       | μA   |
|                                  |                       |  | Ta=25℃ when clock is stopped   |          |      | 1.0   | μA   |
|                                  |                       |  | Ta=85℃ when clock is stopped   |          |      | 20.0  |      |

Note 1: Unless otherwise noted: V<sub>CC</sub> = 5V, V<sub>SS</sub> = 0V at Ta = -20 to 85°C, f(X<sub>IN</sub>) = 10MHz

(Extended operating temperature version; -40 to 85°C)

Note 2: With one timer operated using fc32.

Electrical characteristics ( $V_{CC} = 5V$ )

$V_{CC} = 5V$

**Table 1.39. A-D conversion characteristics (Note)**

| Symbol       | Parameter              |   | Measuring condition     | Standard |      |           | Unit    |
|--------------|------------------------|---|-------------------------|----------|------|-----------|---------|
|              |                        |   |                         | Min.     | Typ. | Max.      |         |
| —            | Resolution             |   | $V_{REF} = V_{CC}$      |          |      | 10        | Bits    |
| —            | Absolute accuracy      | Sample & hold function not available    | $V_{REF} = V_{CC} = 5V$ |          |      | $\pm 3$   | LSB     |
|              |                        | Sample & hold function available(10bit) | $V_{REF} = V_{CC} = 5V$ |          |      | $\pm 3$   | LSB     |
|              |                        | Sample & hold function available(8bit)  | $V_{REF} = V_{CC} = 5V$ |          |      | $\pm 2$   | LSB     |
| $R_{LADDER}$ | Ladder resistance      |   | $V_{REF} = V_{CC}$      | 10       |      | 40        | kohm    |
| $t_{CONV}$   | Conversion time(10bit) |   |                         | 3.3      |      |           | $\mu s$ |
| $t_{CONV}$   | Conversion time(8bit)  |   |                         | 2.8      |      |           | $\mu s$ |
| $t_{SAMP}$   | Sampling time          |   |                         | 0.3      |      |           | $\mu s$ |
| $V_{REF}$    | Reference voltage      |   |                         | 2        |      | $V_{CC}$  | V       |
| $V_{IA}$     | Analog input voltage   |   |                         | 0        |      | $V_{REF}$ | V       |

Note : Unless otherwise noted:  $V_{CC} = AV_{CC} = V_{REF} = 5V$ ,  $V_{SS} = AV_{SS} = 0V$  at  $T_a = -25^{\circ}C$ ,  $f(XIN) = 10MHz$

Electrical characteristics (V<sub>CC</sub> = 5V)

V<sub>CC</sub> = 5V

Timing requirements (referenced to V<sub>CC</sub> = 5V, V<sub>SS</sub> = 0V at T<sub>a</sub> = -20 to 85°C<sup>(\*)</sup> unless otherwise specified)

\* Extended operating temperature version; -40 to 85°C

Table 1.40. External clock input

| Symbol            | Parameter                             | Standard |      | Unit |
|-------------------|---------------------------------------|----------|------|------|
|                   |                                       | Min.     | Max. |      |
| t <sub>c</sub>    | External clock input cycle time       | 100      |      | ns   |
| t <sub>w(H)</sub> | External clock input HIGH pulse width | 40       |      | ns   |
| t <sub>w(L)</sub> | External clock input LOW pulse width  | 40       |      | ns   |
| t <sub>r</sub>    | External clock rise time              |          | 15   | ns   |
| t <sub>f</sub>    | External clock fall time              |          | 15   | ns   |

Table 1.41. Timer A input (counter input in event counter mode)

| Symbol              | Parameter                    | Standard |      | Unit |
|---------------------|------------------------------|----------|------|------|
|                     |                              | Min.     | Max. |      |
| t <sub>c(TA)</sub>  | TA0IN input cycle time       | 100      |      | ns   |
| t <sub>w(TAH)</sub> | TA0IN input HIGH pulse width | 40       |      | ns   |
| t <sub>w(TAL)</sub> | TA0IN input LOW pulse width  | 40       |      | ns   |

Table 1.42. Timer A input (gating input in timer mode)

| Symbol              | Parameter                    | Standard |      | Unit |
|---------------------|------------------------------|----------|------|------|
|                     |                              | Min.     | Max. |      |
| t <sub>c(TA)</sub>  | TA0IN input cycle time       | 400      |      | ns   |
| t <sub>w(TAH)</sub> | TA0IN input HIGH pulse width | 200      |      | ns   |
| t <sub>w(TAL)</sub> | TA0IN input LOW pulse width  | 200      |      | ns   |

Table 1.43. Timer A input (external trigger input in one-shot timer mode)

| Symbol              | Parameter                    | Standard |      | Unit |
|---------------------|------------------------------|----------|------|------|
|                     |                              | Min.     | Max. |      |
| t <sub>c(TA)</sub>  | TA0IN input cycle time       | 200      |      | ns   |
| t <sub>w(TAH)</sub> | TA0IN input HIGH pulse width | 100      |      | ns   |
| t <sub>w(TAL)</sub> | TA0IN input LOW pulse width  | 100      |      | ns   |

Table 1.44. Timer A input (external trigger input in pulse width modulation mode)

| Symbol              | Parameter                    | Standard |      | Unit |
|---------------------|------------------------------|----------|------|------|
|                     |                              | Min.     | Max. |      |
| t <sub>w(TAH)</sub> | TA0IN input HIGH pulse width | 100      |      | ns   |
| t <sub>w(TAL)</sub> | TA0IN input LOW pulse width  | 100      |      | ns   |

Table 1.45. Timer A input (up/down input in event counter mode)

| Symbol                  | Parameter                     | Standard |      | Unit |
|-------------------------|-------------------------------|----------|------|------|
|                         |                               | Min.     | Max. |      |
| t <sub>c(UP)</sub>      | TA0OUT input cycle time       | 2000     |      | ns   |
| t <sub>w(UPH)</sub>     | TA0OUT input HIGH pulse width | 1000     |      | ns   |
| t <sub>w(UPL)</sub>     | TA0OUT input LOW pulse width  | 1000     |      | ns   |
| t <sub>su(UP-TIN)</sub> | TA0OUT input setup time       | 400      |      | ns   |
| t <sub>h(TIN-UP)</sub>  | TA0OUT input hold time        | 400      |      | ns   |

Electrical characteristics ( $V_{CC} = 5V$ )

$V_{CC} = 5V$

Timing requirements (referenced to  $V_{CC} = 5V$ ,  $V_{SS} = 0V$  at  $T_a = -20$  to  $85^{\circ}C^{(*)}$  unless otherwise specified)

\* Extended operating temperature version;  $-40$  to  $85^{\circ}C$

**Table 1.46. Timer B input (counter input in event counter mode)**

| Symbol       | Parameter  | Standard |      | Unit |
|--------------|--|----------|------|------|
|              |  | Min.     | Max. |      |
| $t_{c(TB)}$  | TBiin input cycle time (counted on one edge)         | 100      |      | ns   |
| $t_{w(TBH)}$ | TBiin input HIGH pulse width (counted on one edge)   | 40       |      | ns   |
| $t_{w(TBL)}$ | TBiin input LOW pulse width (counted on one edge)    | 40       |      | ns   |
| $t_{c(TB)}$  | TBiin input cycle time (counted on both edges)       | 200      |      | ns   |
| $t_{w(TBH)}$ | TBiin input HIGH pulse width (counted on both edges) | 80       |      | ns   |
| $t_{w(TBL)}$ | TBiin input LOW pulse width (counted on both edges)  | 80       |      | ns   |

**Table 1.47. Timer B input (pulse period measurement mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{c(TB)}$  | TBiin input cycle time       | 400      |      | ns   |
| $t_{w(TBH)}$ | TBiin input HIGH pulse width | 200      |      | ns   |
| $t_{w(TBL)}$ | TBiin input LOW pulse width  | 200      |      | ns   |

**Table 1.48. Timer B input (pulse width measurement mode)**

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{c(TB)}$  | TBiin input cycle time       | 400      |      | ns   |
| $t_{w(TBH)}$ | TBiin input HIGH pulse width | 200      |      | ns   |
| $t_{w(TBL)}$ | TBiin input LOW pulse width  | 200      |      | ns   |

**Table 1.49. Timer X input (counter input in event counter mode)**

| Symbol       | Parameter                       | Standard |      | Unit |
|--------------|---------------------------------|----------|------|------|
|              |                                 | Min.     | Max. |      |
| $t_{c(TX)}$  | TXiINOUT input cycle time       | 100      |      | ns   |
| $t_{w(TXH)}$ | TXiINOUT input HIGH pulse width | 40       |      | ns   |
| $t_{w(TXL)}$ | TXiINOUT input LOW pulse width  | 40       |      | ns   |

**Table 1.50. Timer X input (gate input in timer mode)**

| Symbol       | Parameter                       | Standard |      | Unit |
|--------------|---------------------------------|----------|------|------|
|              |                                 | Min.     | Max. |      |
| $t_{c(TX)}$  | TXiINOUT input cycle time       | 400      |      | ns   |
| $t_{w(TXH)}$ | TXiINOUT input HIGH pulse width | 200      |      | ns   |
| $t_{w(TXL)}$ | TXiINOUT input LOW pulse width  | 200      |      | ns   |

**Table 1.51. Timer X input (external trigger input in one-shot timer mode)**

| Symbol       | Parameter                       | Standard |      | Unit |
|--------------|---------------------------------|----------|------|------|
|              |                                 | Min.     | Max. |      |
| $t_{c(TX)}$  | TXiINOUT input cycle time       | 200      |      | ns   |
| $t_{w(TXH)}$ | TXiINOUT input HIGH pulse width | 100      |      | ns   |
| $t_{w(TXL)}$ | TXiINOUT input LOW pulse width  | 100      |      | ns   |

## Electrical characteristics (V<sub>CC</sub> = 5V)

V<sub>CC</sub> = 5V

**Timing requirements (referenced to V<sub>CC</sub> = 5V, V<sub>SS</sub> = 0V at Ta = -20 to 85°C<sup>(\*)</sup> unless otherwise specified)**

**\* Extended operating temperature version; -40 to 85°C**

**Table 1.52. Timer X input (pulse period measurement mode)**

| Symbol               | Parameter                       | Standard |      | Unit |
|----------------------|---------------------------------|----------|------|------|
|                      |                                 | Min.     | Max. |      |
| t <sub>c</sub> (TX)  | TXiINOUT input cycle time       | 400      |      | ns   |
| t <sub>w</sub> (TXH) | TXiINOUT input HIGH pulse width | 200      |      | ns   |
| t <sub>w</sub> (TXL) | TXiINOUT input LOW pulse width  | 200      |      | ns   |

**Table 1.53. Timer X input (pulse width measurement mode)**

| Symbol               | Parameter                       | Standard |      | Unit |
|----------------------|---------------------------------|----------|------|------|
|                      |                                 | Min.     | Max. |      |
| t <sub>c</sub> (TX)  | TXiINOUT input cycle time       | 400      |      | ns   |
| t <sub>w</sub> (TXH) | TXiINOUT input HIGH pulse width | 200      |      | ns   |
| t <sub>w</sub> (TXL) | TXiINOUT input LOW pulse width  | 200      |      | ns   |

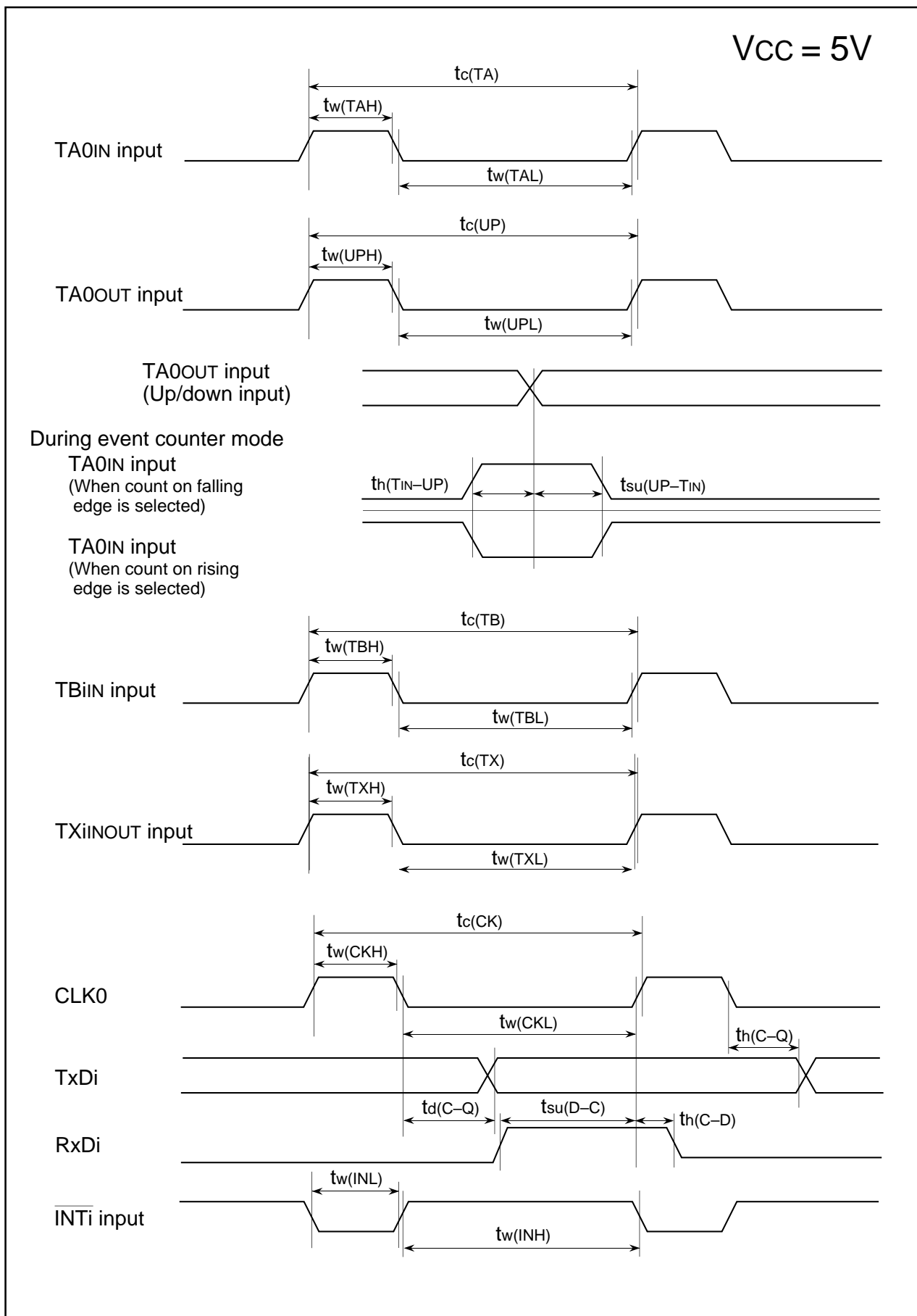
**Table 1.54. Serial I/O**

| Symbol                | Parameter                   | Standard |      | Unit |
|-----------------------|-----------------------------|----------|------|------|
|                       |                             | Min.     | Max. |      |
| t <sub>c</sub> (CK)   | CLK0 input cycle time       | 200      |      | ns   |
| t <sub>w</sub> (CKH)  | CLK0 input HIGH pulse width | 100      |      | ns   |
| t <sub>w</sub> (CKL)  | CLK0 input LOW pulse width  | 100      |      | ns   |
| t <sub>d</sub> (C-Q)  | TxDi output delay time      |          | 80   | ns   |
| t <sub>h</sub> (C-Q)  | TxDi hold time              | 0        |      | ns   |
| t <sub>su</sub> (D-C) | RxDi input setup time       | 30       |      | ns   |
| t <sub>h</sub> (C-D)  | RxDi input hold time        | 90       |      | ns   |

**Table 1.55. External interrupt INTi inputs**

| Symbol               | Parameter                   | Standard |      | Unit |
|----------------------|-----------------------------|----------|------|------|
|                      |                             | Min.     | Max. |      |
| t <sub>w</sub> (INH) | INTi input HIGH pulse width | 250      |      | ns   |
| t <sub>w</sub> (INL) | INTi input LOW pulse width  | 250      |      | ns   |

Electrical characteristics ( $V_{CC} = 5V$ )



Electrical characteristics (V<sub>CC</sub> = 3V)V<sub>CC</sub> = 3V

Table 1.56. Electrical characteristics (Note 1)

| Symbol                           | Parameter             |  | Measuring condition   | Standard |       |       | Unit |
|----------------------------------|-----------------------|--|---|----------|-------|-------|------|
|                                  |                       |  |   | Min.     | Typ.  | Max.  |      |
| V <sub>OH</sub>                  | HIGH output voltage   | P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>5</sub> , P4 <sub>0</sub> to P4 <sub>5</sub> , P5 <sub>0</sub> to P5 <sub>4</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>0</sub> , P7 <sub>1</sub>                | I <sub>OH</sub> = - 1mA   | 2.5      |       |       | V    |
| V <sub>OH</sub>                  | HIGH output voltage   | X <sub>OUT</sub>   | HIGHPOWER   | 2.5      |       |       | V    |
|                                  |                       |  | LOWPOWER  | 2.5      |       |       |      |
| V <sub>OH</sub>                  | HIGH output voltage   | X <sub>COUT</sub>  | HIGHPOWER   |          | 3.0   |       | V    |
|                                  |                       |  | LOWPOWER  |          | 1.6   |       |      |
| V <sub>OL</sub>                  | LOW output voltage    | P0 <sub>0</sub> to P0 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>5</sub> , P4 <sub>0</sub> to P4 <sub>5</sub> , P5 <sub>0</sub> to P5 <sub>4</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>0</sub> , P7 <sub>1</sub>   | I <sub>OL</sub> = 1 mA  |          |       | 0.5   | V    |
| V <sub>OL</sub>                  | LOW output voltage    | P1 <sub>0</sub> to P1 <sub>7</sub>   | HIGHPOWER   |          |       | 0.5   | V    |
|                                  |                       |  | LOWPOWER  |          |       | 0.5   |      |
| V <sub>OL</sub>                  | LOW output voltage    | X <sub>OUT</sub>   | HIGHPOWER   |          |       | 0.5   | V    |
|                                  |                       |  | LOWPOWER  |          |       | 0.5   |      |
| V <sub>OL</sub>                  | LOW output voltage    | X <sub>OUT</sub>   | HIGHPOWER   |          | 0     |       | V    |
|                                  |                       |  | LOWPOWER  |          | 0     |       |      |
| V <sub>T+</sub> -V <sub>T-</sub> | Hysteresis            | TA0IN, TX0INOUT, TX1INOUT, TX2INOUT<br>TB0IN, TB1IN INT0, INT1, CLK0, K10 to K17<br>RxD0, RxD1   |   | 0.2      |       | 0.8   | V    |
| V <sub>T+</sub> -V <sub>T-</sub> | Hysteresis            | RESET  |   | 0.2      |       | 1.8   | V    |
| I <sub>IH</sub>                  | HIGH input current    | P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>5</sub> , P4 <sub>0</sub> to P4 <sub>5</sub> , P5 <sub>0</sub> to P5 <sub>4</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>0</sub> , P7 <sub>1</sub> , RESET, CNVss | V <sub>I</sub> = 3V   |          |       | 4.0   | μA   |
| I <sub>IL</sub>                  | LOW input current     | P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>5</sub> , P4 <sub>0</sub> to P4 <sub>5</sub> , P5 <sub>0</sub> to P5 <sub>4</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>0</sub> , P7 <sub>1</sub> , RESET, CNVss | V <sub>I</sub> = 0V   |          |       | -4.0  | μA   |
| R <sub>PULLUP</sub>              | Pull-up resistor      | P0 <sub>0</sub> to P0 <sub>7</sub> , P1 <sub>0</sub> to P1 <sub>7</sub> , P3 <sub>0</sub> to P3 <sub>5</sub> , P4 <sub>0</sub> to P4 <sub>5</sub> , P5 <sub>0</sub> to P5 <sub>4</sub> , P6 <sub>0</sub> to P6 <sub>7</sub> , P7 <sub>0</sub> , P7 <sub>1</sub>                | V <sub>I</sub> = 0V   | 66.0     | 120.0 | 500.0 | kΩ   |
| R <sub>XIN</sub>                 | Feedback resistor     | X <sub>IN</sub>  |   |          | 3.0   |       | MΩ   |
| R <sub>XIN</sub>                 | Feedback resistor     | X <sub>IN</sub>  |   |          | 10.0  |       | MΩ   |
| V <sub>RAM</sub>                 | RAM retention voltage |  | When clock is stopped   | 2.0      |       |       | V    |
| I <sub>CC</sub>                  | Power supply current  | I/O pin has no load  | f(X <sub>IN</sub> )=3.5MHz<br>Square wave, no division  |          | 3.5   | 7.0   | mA   |
|                                  |                       |  | f(X <sub>CIN</sub> )=32kHz<br>Square wave   |          | 40.0  |       | μA   |
|                                  |                       |  | f(X <sub>CIN</sub> )=32kHz<br>When a WAIT instruction is executed<br>Oscillation capacity HIGH (Note 2) |          | 2.8   |       | μA   |
|                                  |                       |  | f(X <sub>CIN</sub> )=32kHz<br>When a WAIT instruction is executed<br>Oscillation capacity LOW (Note 2)  |          | 0.9   |       | μA   |
|                                  |                       |  | Ta=25°C when clock is stopped   |          |       | 1.0   | μA   |
|                                  |                       |  | Ta=85°C when clock is stopped   |          |       | 20.0  |      |

Note 1: Unless otherwise noted: V<sub>CC</sub> = 3V, V<sub>SS</sub> = 0V at Ta = -20 to 85°C, f(X<sub>IN</sub>) = 3.5MHz)

(Extended operating temperature version; -40 to 85°C)

Note 2: With one timer operated using fc32.

Electrical characteristics ( $V_{CC} = 3V$ ) $V_{CC} = 3V$ **Table 1.57. A-D conversion characteristics (Note)**

| Symbol       | Parameter             |   | Measuring condition                                    | Standard |      |           | Unit    |
|--------------|-----------------------|---|--|----------|------|-----------|---------|
|              |                       |   |  | Min.     | Typ. | Max.      |         |
| —            | Resolution            |   | $V_{REF} = V_{CC}$                                     |          |      | 10        | Bits    |
| —            | Absolute accuracy     | Sample & hold function not available (8bit) | $V_{REF} = V_{CC} = 3V$ ,<br>$\emptyset_{AD} = f_{AD}$ |          |      | $\pm 2$   | LSB     |
| $R_{LADDER}$ | Ladder resistance     |   | $V_{REF} = V_{CC}$                                     | 10       |      | 40        | kohm    |
| $t_{CONV}$   | Conversion time(8bit) |   |  | 14.0     |      |           | $\mu s$ |
| $V_{REF}$    | Reference voltage     |   |  | 2.7      |      | $V_{CC}$  | V       |
| $V_{IA}$     | Analog input voltage  |   |  | 0        |      | $V_{REF}$ | V       |

Note : Unless otherwise noted:  $V_{CC} = AV_{CC} = V_{REF} = 3V$ ,  $V_{SS} = AV_{SS} = 0V$  at  $T_a = 25^\circ C$ ,  $f(XIN) = 3.5MHz$ .



Electrical characteristics ( $V_{CC} = 3V$ ) $V_{CC} = 3V$ 

Timing requirements (referenced to  $V_{CC} = 3V$ ,  $V_{SS} = 0V$  at  $T_a = -20$  to  $85^{\circ}C^{(*)}$  unless otherwise specified)

\* Extended operating temperature version;  $-40$  to  $85^{\circ}C$

Table 1.58. External clock input

| Symbol     | Parameter                             | Standard |      | Unit |
|------------|---------------------------------------|----------|------|------|
|            |                                       | Min.     | Max. |      |
| $t_c$      | External clock input cycle time       | 286      |      | ns   |
| $t_{w(H)}$ | External clock input HIGH pulse width | 120      |      | ns   |
| $t_{w(L)}$ | External clock input LOW pulse width  | 120      |      | ns   |
| $t_r$      | External clock rise time              |          | 18   | ns   |
| $t_f$      | External clock fall time              |          | 18   | ns   |

Table 1.59. Timer A input (counter input in event counter mode)

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_c(TA)$    | TA0IN input cycle time       | 300      |      | ns   |
| $t_{w(TAH)}$ | TA0IN input HIGH pulse width | 120      |      | ns   |
| $t_{w(TAL)}$ | TA0IN input LOW pulse width  | 120      |      | ns   |

Table 1.60. Timer A input (gating input in timer mode)

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_c(TA)$    | TA0IN input cycle time       | 1200     |      | ns   |
| $t_{w(TAH)}$ | TA0IN input HIGH pulse width | 600      |      | ns   |
| $t_{w(TAL)}$ | TA0IN input LOW pulse width  | 600      |      | ns   |

Table 1.61. Timer A input (external trigger input in one-shot timer mode)

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_c(TA)$    | TA0IN input cycle time       | 600      |      | ns   |
| $t_{w(TAH)}$ | TA0IN input HIGH pulse width | 300      |      | ns   |
| $t_{w(TAL)}$ | TA0IN input LOW pulse width  | 300      |      | ns   |

Table 1.62. Timer A input (external trigger input in pulse width modulation mode)

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{w(TAH)}$ | TA0IN input HIGH pulse width | 300      |      | ns   |
| $t_{w(TAL)}$ | TA0IN input LOW pulse width  | 300      |      | ns   |

Table 1.63. Timer A input (up/down input in event counter mode)

| Symbol           | Parameter                     | Standard |      | Unit |
|------------------|-------------------------------|----------|------|------|
|                  |                               | Min.     | Max. |      |
| $t_c(UP)$        | TA0OUT input cycle time       | 6000     |      | ns   |
| $t_{w(UPH)}$     | TA0OUT input HIGH pulse width | 3000     |      | ns   |
| $t_{w(UPL)}$     | TA0OUT input LOW pulse width  | 3000     |      | ns   |
| $t_{su}(UP-TIN)$ | TA0OUT input setup time       | 1200     |      | ns   |
| $t_h(TIN-UP)$    | TA0OUT input hold time        | 1200     |      | ns   |

Electrical characteristics ( $V_{CC} = 3V$ ) $V_{CC} = 3V$ 

Timing requirements (referenced to  $V_{CC} = 3V$ ,  $V_{SS} = 0V$  at  $T_a = -20$  to  $85^{\circ}C^{(*)}$  unless otherwise specified)

\* Extended operating temperature version;  $-40$  to  $85^{\circ}C$

Table 1.64. Timer B input (counter input in event counter mode)

| Symbol       | Parameter  | Standard |      | Unit |
|--------------|--|----------|------|------|
|              |  | Min.     | Max. |      |
| $t_{c(TB)}$  | TBiIN input cycle time (counted on one edge)         | 300      |      | ns   |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width (counted on one edge)   | 120      |      | ns   |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width (counted on one edge)    | 120      |      | ns   |
| $t_{c(TB)}$  | TBiIN input cycle time (counted on both edges)       | 600      |      | ns   |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width (counted on both edges) | 320      |      | ns   |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width (counted on both edges)  | 320      |      | ns   |

Table 1.65. Timer B input (pulse period measurement mode)

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{c(TB)}$  | TBiIN input cycle time       | 1200     |      | ns   |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width | 600      |      | ns   |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width  | 600      |      | ns   |

Table 1.66. Timer B input (pulse width measurement mode)

| Symbol       | Parameter                    | Standard |      | Unit |
|--------------|------------------------------|----------|------|------|
|              |                              | Min.     | Max. |      |
| $t_{c(TB)}$  | TBiIN input cycle time       | 1200     |      | ns   |
| $t_{w(TBH)}$ | TBiIN input HIGH pulse width | 600      |      | ns   |
| $t_{w(TBL)}$ | TBiIN input LOW pulse width  | 600      |      | ns   |

Table 1.67. Timer X input (counter input in event counter mode)

| Symbol       | Parameter                       | Standard |      | Unit |
|--------------|---------------------------------|----------|------|------|
|              |                                 | Min.     | Max. |      |
| $t_{c(TX)}$  | TXiINOUT input cycle time       | 300      |      | ns   |
| $t_{w(TXH)}$ | TXiINOUT input HIGH pulse width | 120      |      | ns   |
| $t_{w(TXL)}$ | TXiINOUT input LOW pulse width  | 120      |      | ns   |

Table 1.68. Timer X input (gate input in timer mode)

| Symbol       | Parameter                       | Standard |      | Unit |
|--------------|---------------------------------|----------|------|------|
|              |                                 | Min.     | Max. |      |
| $t_{c(TX)}$  | TXiINOUT input cycle time       | 1200     |      | ns   |
| $t_{w(TXH)}$ | TXiINOUT input HIGH pulse width | 600      |      | ns   |
| $t_{w(TXL)}$ | TXiINOUT input LOW pulse width  | 600      |      | ns   |

Table 1.69. Timer X input (external trigger input in one-shot timer mode)

| Symbol       | Parameter                       | Standard |      | Unit |
|--------------|---------------------------------|----------|------|------|
|              |                                 | Min.     | Max. |      |
| $t_{c(TX)}$  | TXiINOUT input cycle time       | 600      |      | ns   |
| $t_{w(TXH)}$ | TXiINOUT input HIGH pulse width | 300      |      | ns   |
| $t_{w(TXL)}$ | TXiINOUT input LOW pulse width  | 300      |      | ns   |

Electrical characteristics ( $V_{CC} = 3V$ ) $V_{CC} = 3V$ 

Timing requirements (referenced to  $V_{CC} = 3V$ ,  $V_{SS} = 0V$  at  $T_a = -20$  to  $85^{\circ}C^{(*)}$  unless otherwise specified)

\* Extended operating temperature version;  $-40$  to  $85^{\circ}C$

Table 1.70. Timer X input (pulse period measurement mode)

| Symbol       | Parameter                      | Standard |      | Unit |
|--------------|--------------------------------|----------|------|------|
|              |                                | Min.     | Max. |      |
| $t_{c(TX)}$  | TXiNOUT input cycle time       | 1200     |      | ns   |
| $t_{w(TXH)}$ | TXiNOUT input HIGH pulse width | 600      |      | ns   |
| $t_{w(TXL)}$ | TXiNOUT input LOW pulse width  | 600      |      | ns   |

Table 1.71. Timer X input (pulse width measurement mode)

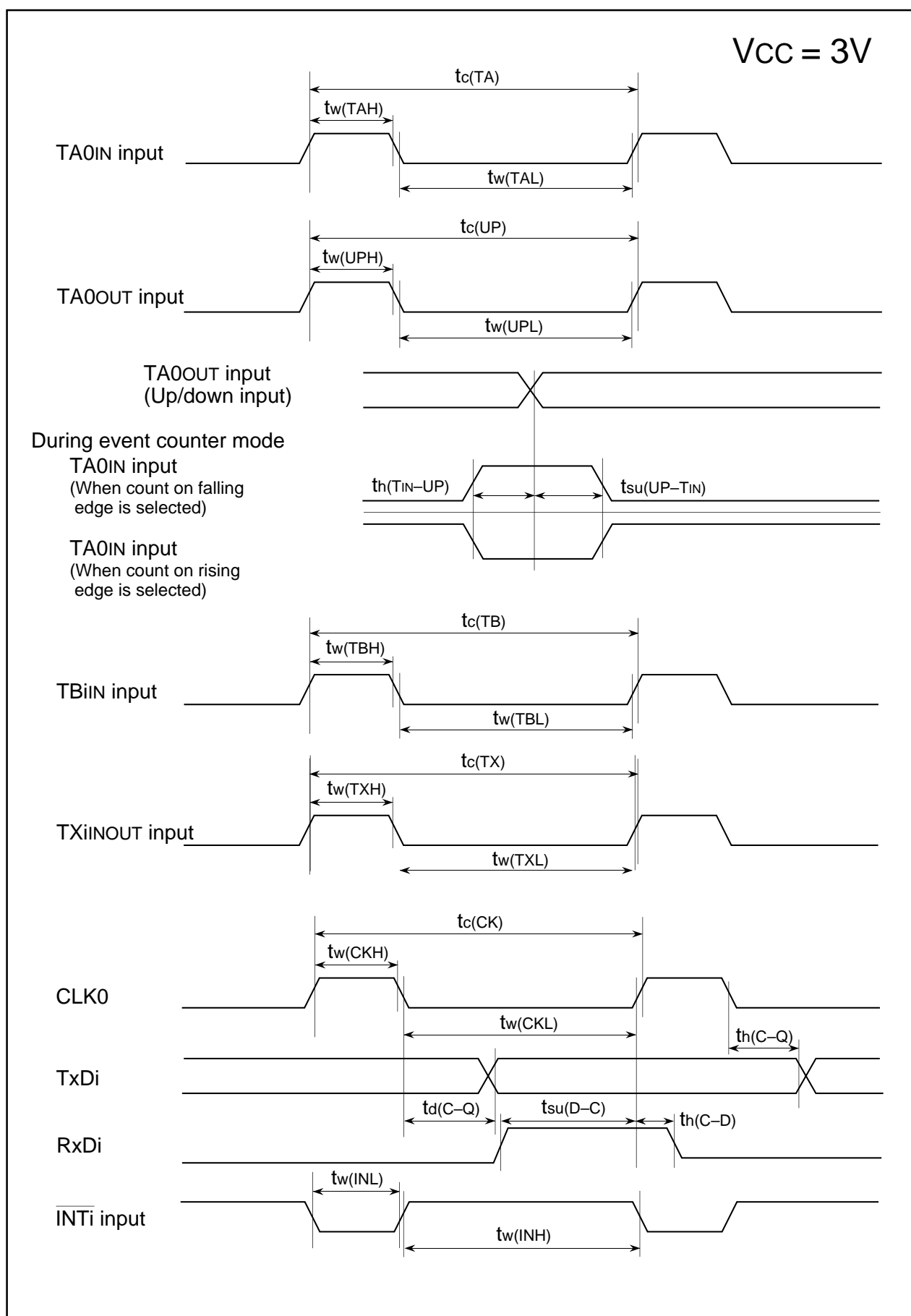
| Symbol       | Parameter                      | Standard |      | Unit |
|--------------|--------------------------------|----------|------|------|
|              |                                | Min.     | Max. |      |
| $t_{c(TX)}$  | TXiNOUT input cycle time       | 1200     |      | ns   |
| $t_{w(TXH)}$ | TXiNOUT input HIGH pulse width | 600      |      | ns   |
| $t_{w(TXL)}$ | TXiNOUT input LOW pulse width  | 600      |      | ns   |

Table 1.72. Serial I/O

| Symbol        | Parameter                   | Standard |      | Unit |
|---------------|-----------------------------|----------|------|------|
|               |                             | Min.     | Max. |      |
| $t_{c(CK)}$   | CLK0 input cycle time       | 300      |      | ns   |
| $t_{w(CKH)}$  | CLK0 input HIGH pulse width | 150      |      | ns   |
| $t_{w(CKL)}$  | CLK0 input LOW pulse width  | 150      |      | ns   |
| $t_{d(C-Q)}$  | TxDi output delay time      |          | 160  | ns   |
| $t_{h(C-Q)}$  | TxDi hold time              | 0        |      | ns   |
| $t_{su(D-C)}$ | RxDi input setup time       | 50       |      | ns   |
| $t_{h(C-D)}$  | RxDi input hold time        | 90       |      | ns   |

Table 1.73. External interrupt  $\overline{INTi}$  inputs

| Symbol       | Parameter                                | Standard |      | Unit |
|--------------|--|----------|------|------|
|              |  | Min.     | Max. |      |
| $t_{w(INH)}$ | $\overline{INTi}$ input HIGH pulse width | 380      |      | ns   |
| $t_{w(INL)}$ | $\overline{INTi}$ input LOW pulse width  | 380      |      | ns   |

Electrical characteristics ( $V_{CC} = 3V$ )

## Description (Flash memory version)

## Outline Performance

Table 1.74 shows the outline performance of the M30201 (flash memory version).

**Table 1.74. Outline Performance of the M30201 (flash memory version)**

| Item                         |               | Performance  |
|------------------------------|---------------|--|
| Power supply voltage         |               | 4.0V to 5.5 V ( $f(XIN)=10MHz$ )                               |
| Program/erase voltage        |               | $V_{PP}=12V \pm 5\%$ ( $f(XIN)=10MHz$ , $T_a=25\pm5^\circ C$ ) |
|                              |               | $V_{CC}=5V \pm 10\%$ ( $f(XIN)=10MHz$ , $T_a=25\pm5^\circ C$ ) |
| Flash memory operation mode  |               | Three modes (parallel I/O, standard serial I/O, CPU rewrite)   |
| Erase block division         | User ROM area | See Figure 1.96  |
|                              | Boot ROM area | One division (3.5 Kbytes) (Note)                               |
| Program method               |               | In units of byte   |
| Erase method                 |               | Collective erase   |
| Program/erase control method |               | Program/erase control by software command                      |
| Number of commands           |               | 6 commands   |
| Program/erase count          |               | 100 times  |
| ROM code protect             |               | Parallel I/O mode is supported.                                |

Note: The boot ROM area contains a standard serial I/O mode control program which is stored in it when shipped from the factory. This area can be erased and programmed in only parallel I/O mode.

## Description (Flash memory version)

## Flash Memory

The M30201 (flash memory version) contains the NOR type of flash memory that requires a high-voltage VPP power supply for program/erase operations, in addition to the VCC power supply for device operation. For this flash memory, three flash memory modes are available in which to read, program, and erase: parallel I/O and standard serial I/O modes in which the flash memory can be manipulated using a programmer and a CPU rewrite mode in which the flash memory can be manipulated by the Central Processing Unit (CPU). Each mode is detailed in the pages to follow.

In addition to the ordinary user ROM area to store a microcomputer operation control program, the flash memory has a boot ROM area that is used to store a program to control rewriting in CPU rewrite and standard serial I/O modes. This boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. However, the user can write a rewrite control program in this area that suits the user's application system. This boot ROM area can be rewritten in only parallel I/O mode.

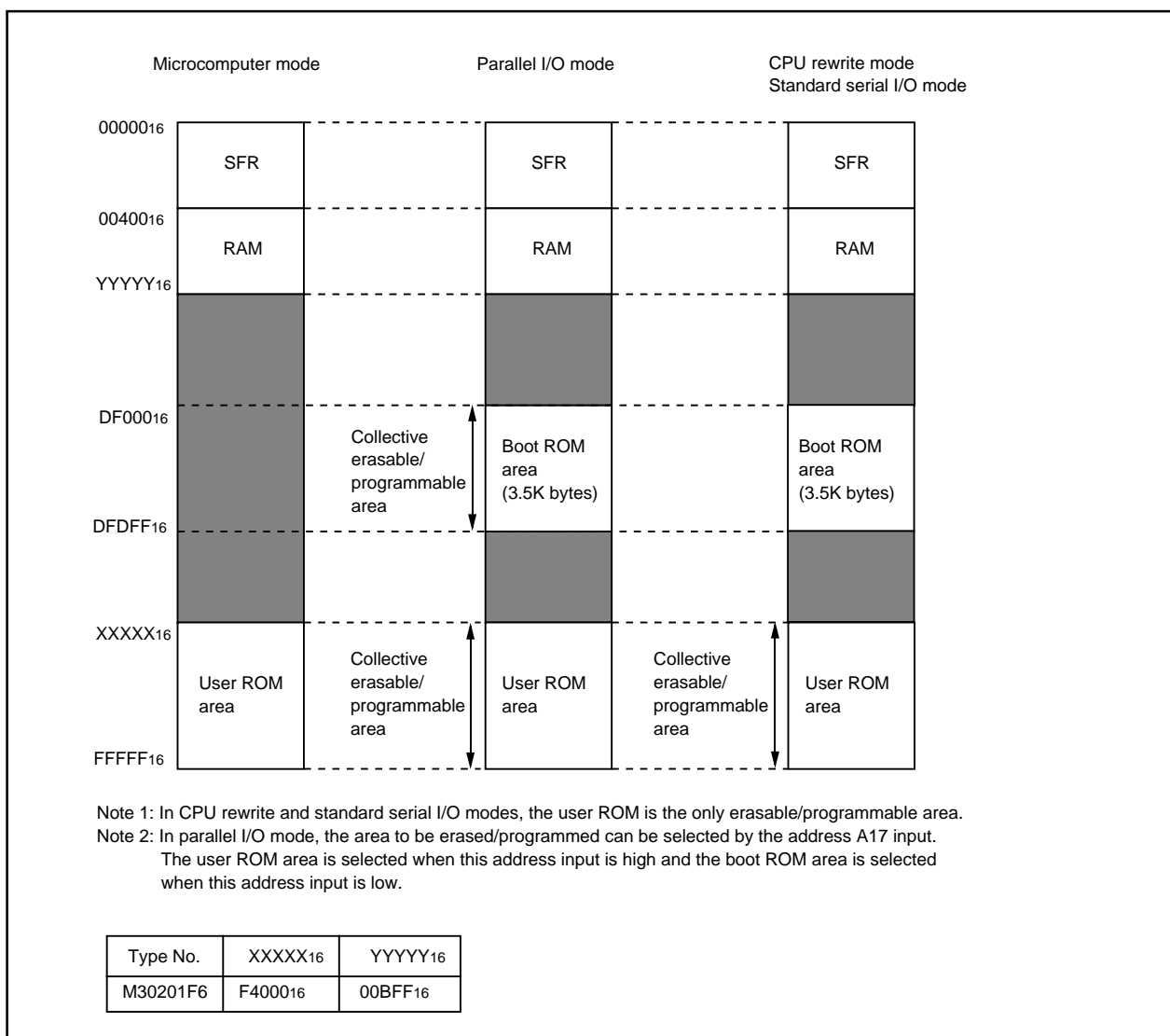


Figure 1.96. Block diagram of flash memory version

## CPU Rewrite Mode (Flash memory version)

## CPU Rewrite Mode

In CPU rewrite mode, the on-chip flash memory can be operated on (read, program, or erase) under control of the Central Processing Unit (CPU). In CPU rewrite mode, the flash memory can be operated on by reading or writing to the flash memory control register and flash command register. Figure 1.97, Figure 1.98 show the flash memory control register, and flash command register respectively.

Also, in CPU rewrite mode, the CNVss pin is used as the VPP power supply pin. Apply the power supply voltage, VPPH, from an external source to this pin.

In CPU rewrite mode, only the user ROM area shown in Figure 1.96 can be rewritten; the boot ROM area cannot be rewritten. Make sure the program and block commands are issued for only the user ROM area. The control program for CPU rewrite mode can be stored in either user ROM or boot ROM area. In the CPU rewrite mode, because the flash memory cannot be read from the CPU, the rewrite control program must be transferred to internal RAM before it can be executed.

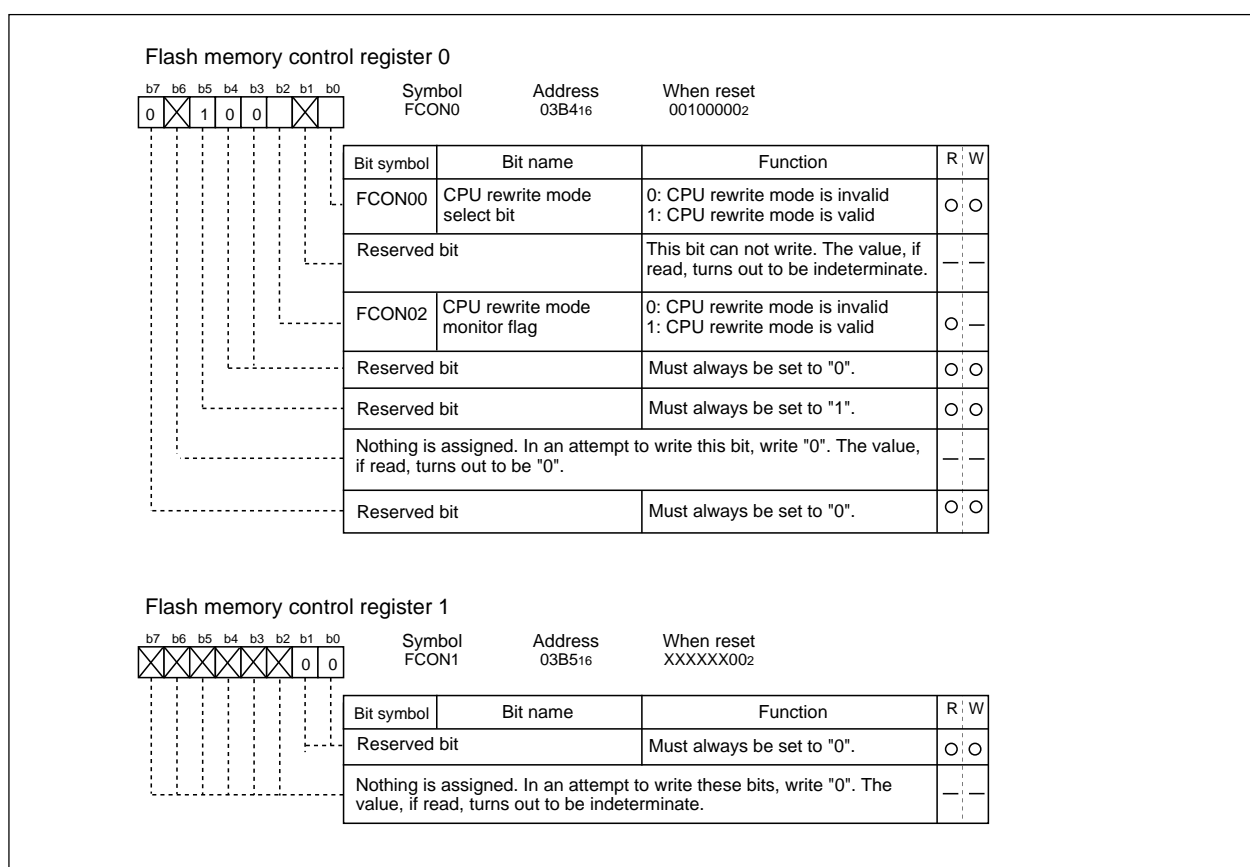


Figure 1.97. Flash memory control register

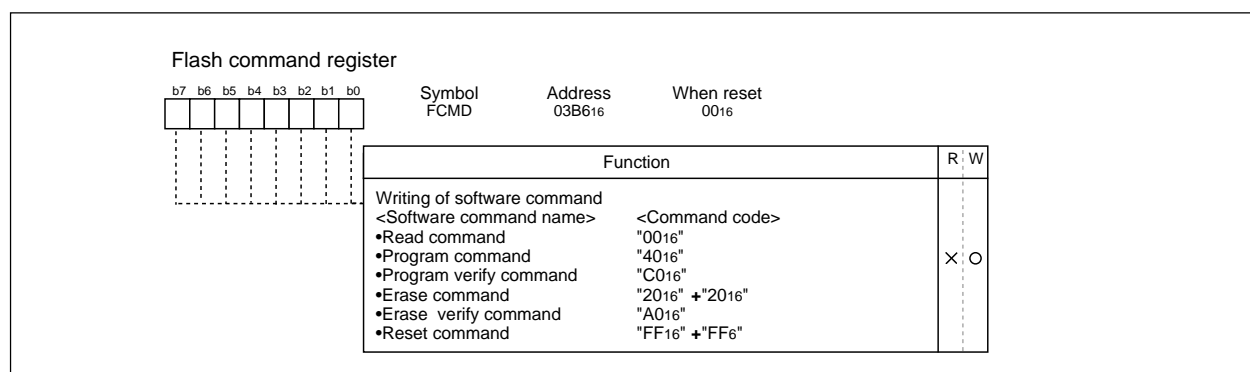


Figure 1.98. Flash command register

## CPU Rewrite Mode (Flash memory version)

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### Microcomputer Mode and Boot Mode

The control program for CPU rewrite mode must be written into the user ROM or boot ROM area in parallel I/O mode beforehand. (If the control program is written into the boot ROM area, the standard serial I/O mode becomes unusable.)

See Figure 1.96 for details about the boot ROM area.

Normal microcomputer mode is entered when the microcomputer is reset with pulling CNVSS pin low (Vss). In this case, the CPU starts operating using the control program in the user ROM area.

When the microcomputer is reset by pulling the P52 pin high (VCC), the CNVSS pin high (VPPH), the CPU starts operating using the control program in the boot ROM area. This mode is called the "boot" mode.

The control program in the boot ROM area can also be used to rewrite the user ROM area.

### CPU rewrite mode operation procedure

The internal flash memory can be operated on to program, read, verify, or erase it while being placed on-board by writing commands from the CPU to the flash memory control register (addresses 03B416, 03B516) and flash command register (address 03B616). Note that when in CPU rewrite mode, the boot ROM area cannot be accessed for program, read, verify, or erase operations. Before this can be accomplished, a CPU write control program must be written into the boot ROM area in parallel input/output mode. The following shows a CPU rewrite mode operation procedure.

#### <Start procedure (Note 1)>

- (1) Apply VPPH to the CNVSS/VPP pin and VCC to the port P52 pin for reset release. Or the user can jump from the user ROM area to the boot ROM area using the JMP instruction and execute the CPU write control program. In this case, set the CPU write mode select bit of the flash memory control register to "1" before applying VPPH to the CNVSS/VPP pin.
- (2) After transferring the CPU write control program from the boot ROM area to the internal RAM, jump to this control program in RAM. (The operations described below are controlled by this program.)
- (3) Set the CPU rewrite mode select bit to "1".
- (4) Read the CPU rewrite mode monitor flag to see that the CPU rewrite mode is enabled.
- (5) Execute operation on the flash memory by writing software commands to the flash command register.

Note 1: In addition to the above, various other operations need to be performed, such as for entering the data to be written to flash memory from an external source (e.g., serial I/O), initializing the ports, and writing to the watchdog timer.

#### <Clearing procedure>

- (1) Apply Vss to the CNVSS/VPP pin.
- (2) Set the CPU rewrite mode select bit to "0".



## CPU Rewrite Mode (Flash memory version)

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### Precautions on CPU Rewrite Mode

Described below are the precautions to be observed when rewriting the flash memory in CPU rewrite mode.

#### (1) Operation speed

During erase/program mode, set BCLK to 5 MHz or less by changing the divide ratio.

#### (2) Instructions inhibited against use

The instructions listed below cannot be used during CPU rewrite mode because they refer to the internal data of the flash memory:

UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction

#### (3) Interrupts inhibited against use

No interrupts can be used that look up the fixed vector table in the flash memory area. Maskable interrupts may be used by setting the interrupt vector table in a location outside the flash memory area.

## CPU Rewrite Mode (Flash memory version)

### Software Commands

Table 1.75 lists the software commands available with the M30201 (flash memory version).

When CPU rewrite mode is enabled, write software commands to the flash command register to specify the operation to erase or program.

The content of each software command is explained below.

**Table 1.75. List of Software Commands (CPU Rewrite Mode)**

| Command        | First bus cycle |                    |  | Second bus cycle |                    |  |
|----------------|-----------------|--------------------|--|------------------|--------------------|--|
|                | Mode            | Address            | Data (D <sub>0</sub> to D <sub>7</sub> ) | Mode             | Address            | Data (D <sub>0</sub> to D <sub>7</sub> ) |
| Read           | Write           | 03B6 <sub>16</sub> | 00 <sub>16</sub>                         |                  |                    |  |
| Program        | Write           | 03B6 <sub>16</sub> | 40 <sub>16</sub>                         | Write            | Program address    | Program data                             |
| Program verify | Write           | 03B6 <sub>16</sub> | C0 <sub>16</sub>                         | Read             | Verify address     | Verify data                              |
| Erase          | Write           | 03B6 <sub>16</sub> | 20 <sub>16</sub>                         | Write            | 03B6 <sub>16</sub> | 20 <sub>16</sub>                         |
| Erase verify   | Write           | 03B6 <sub>16</sub> | A0 <sub>16</sub>                         | Read             | Verify address     | Verify data                              |
| Reset          | Write           | 03B6 <sub>16</sub> | FF <sub>16</sub>                         | Write            | 03B6 <sub>16</sub> | FF <sub>16</sub>                         |

#### Read Command (00<sub>16</sub>)

The read mode is entered by writing the command code “00<sub>16</sub>” to the flash command register in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the content of the specified address is read out at the data bus (D<sub>0</sub>–D<sub>7</sub>), 8 bits at a time.

The read mode is retained intact until another command is written.

After reset and after the reset command is executed, the read mode is set.

#### Program Command (40<sub>16</sub>)

The program mode is entered by writing the command code “40<sub>16</sub>” to the flash command register in the first bus cycle. When the user execute an instruction to write byte data to the desired address (e.g., STE instruction) in the second bus cycle, the flash memory control circuit executes the program operation. The program operation requires approximately 20 μs. Wait for 20 μs or more before the user go to the next processing.

During program operation, the watchdog timer remains idle, with the value “7FFF<sub>16</sub>” set in it.

Note 1: The write operation is not completed immediately by writing a program command once. The user must always execute a program-verify command after each program command executed. And if verification fails, the user need to execute the program command repeatedly until the verification passes. See Figure 1.99 for an example of a programming flowchart.

## CPU Rewrite Mode (Flash memory version)

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### Program-verify command (C016)

The program-verify mode is entered by writing the command code "C016" to the flash command register in the first bus cycle. When the user execute an instruction (e.g., LDE instruction) to read byte data from the address to be verified (the previously programmed address) in the second bus cycle, the content that has actually been written to the address is read out from the memory.

The CPU compares this read data with the data that it previously wrote to the address using the program command. If the compared data do not match, the user need to execute the program and program-verify operations one more time.

### Erase command (2016 + 2016)

The flash memory control circuit executes an erase operation by writing command code "2016" to the flash command register in the first bus cycle and the same command code to the flash command register again in the second bus cycle. The erase operation requires approximately 20 ms. Wait for 20 ms or more before the user go to the next processing.

Before this erase command can be performed, all memory locations to be erased must have had data "0016" written to by using the program and program-verify commands. During erase operation, the watchdog timer remains idle, with the value "7FFF16 set in it.

Note 1: The erase operation is not completed immediately by writing an erase command once. The user must always execute an erase-verify command after each erase command executed. And if verification fails, the user need to execute the erase command repeatedly until the verification passes. See Figure 1.99 for an example of an erase flowchart.

### Erase-verify command (A016)

The erase-verify mode is entered by writing the command code "A016" to the flash command register in the first bus cycle. When the user execute an instruction to read byte data from the address to be verified (e.g., LDE instruction) in the second bus cycle, the content of the address is read out.

The CPU must sequentially erase-verify memory contents one address at a time, over the entire area erased. If any address is encountered whose content is not "FF16" (not erased), the CPU must stop erase-verify at that point and execute erase and erase-verify operations one more time.

Note 1: If any unerased memory location is encountered during erase-verify operation, be sure to execute erase and erase-verify operations one more time. In this case, however, the user does not need to write data "0016" to memory before erasing.

## CPU Rewrite Mode (Flash memory version)

**Reset command (FF<sub>16</sub> + FF<sub>16</sub>)**

The reset command is used to stop the program command or the erase command in the middle of operation. After writing command code "40<sub>16</sub>" or "20<sub>16</sub>" twice to the flash command register, write command code "FF<sub>16</sub>" to the flash command register in the first bus cycle and the same command code to the flash command register again in the second bus cycle. The program command or erase command is disabled, with the flash memory placed in read mode.

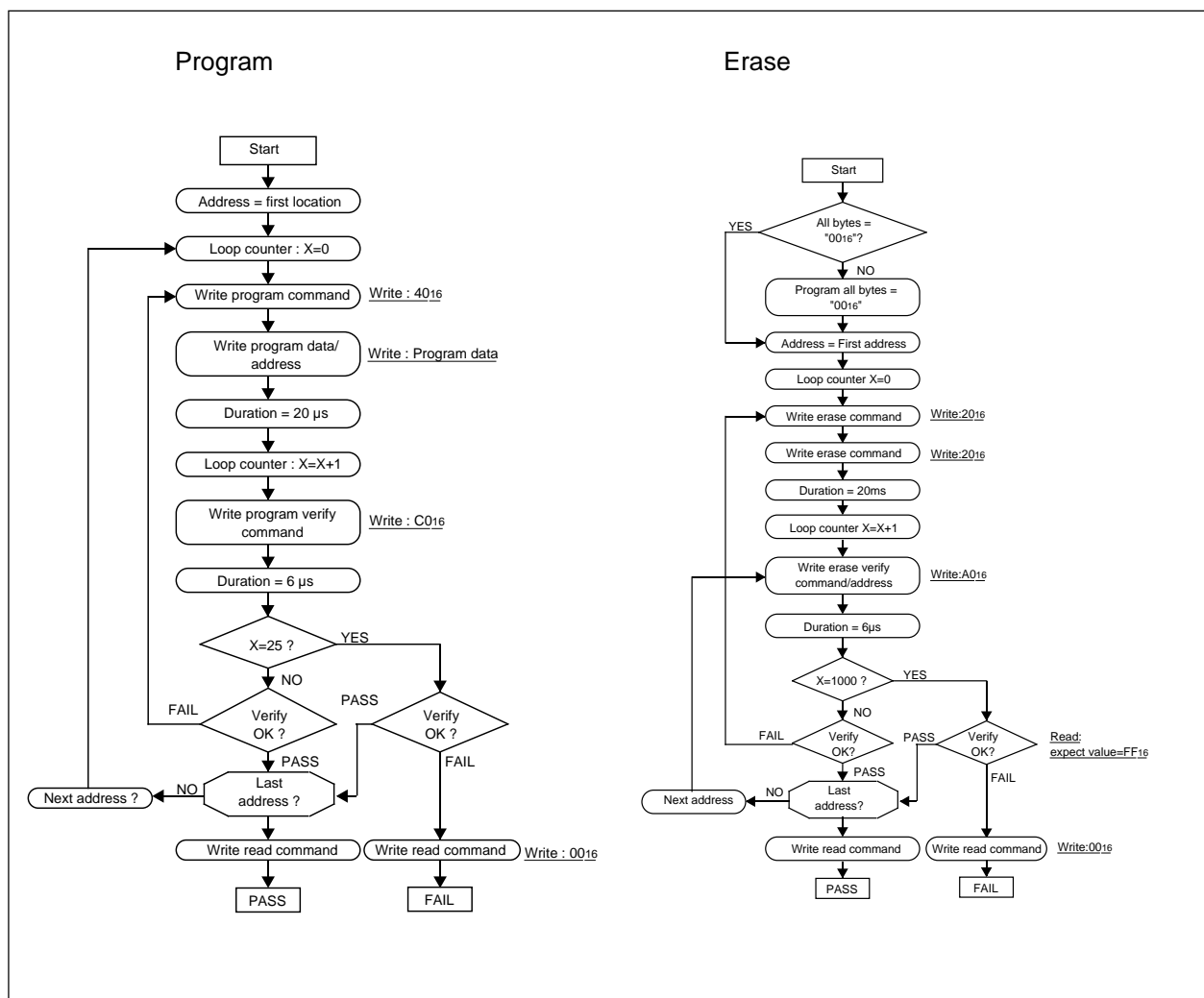


Figure 1.99. Program and erase execution flowchart in the CPU rewrite mode

## Appendix Parallel I/O Mode (Flash memory version)

### Description of Pin Function (Flash Memory Parallel I/O Mode)

| Pin name      | Signal name               | I/O | Function  |
|---------------|---------------------------|-----|---|
| Vcc, Vss      | Power supply input        |     | Apply 5 V $\pm$ 10 % to the Vcc pin and 0 V to the Vss pin.   |
| CNVss         | CNVss                     | I   | Apply 12 V $\pm$ 5 % to the CNVss pin.  |
| RESET         | Reset input               | I   | Connect this pin to Vss.  |
| XIN           | Clock input               | I   | Connect a ceramic or crystal resonator between the XIN and XOUT pins. When entering an externally derived clock, enter it from XIN and leave XOUT open. |
| XOUT          | Clock output              | O   |   |
| AVcc, AVss    | Analog power supply input |     | Connect AVss to Vss and AVcc to Vcc, respectively.  |
| VREF          | Reference voltage input   | I   | Connect this pin to Vss.  |
| P00 to P07    | Data I/O D0 to D7         | I/O | These are data D0–D7 input/output pins.   |
| P10 to P17    | Address input A8 to A15   | I   | These are address A8–A15 input pins.  |
| P30 to P33    | Address input A4 to A7    | I   | These are address A4–A7 input pins.   |
| P34 to P35    | Input port P3             | I   | Enter low signals to these pins.  |
| P40           | WE input                  | I   | This is a WE input pin.   |
| P41           | OE input                  | I   | This is a OE input pin.   |
| P43           | CE input                  | I   | This is a CE input pin.   |
| P42, P44, P45 | Input port P4             | I   | Enter high signals or low signals to these pins.  |
| P50           | Address input A17         | I   | This is address A17 input pin.  |
| P51           | VRFY input                | I   | Apply VIH (5 V) to this pin when VPP = VPPH (12 V), or VIL (0 V) when VPP = VPPL (5 V).   |
| P52           | Input port P5             | I   | Enter low signal to this pin.   |
| P53, P54      | Input port P5             | I   | Enter high signals or low signals to these pins.  |
| P60 to P63    | Address input A0 to A3    | I   | These are address A0–A3 input pins.   |
| P64 to P67    | Input port P6             | I   | Enter high signals or low signals to these pins.  |
| P70 to P71    | Input port P7             | I   | Enter high signals or low signals to these pins.  |

## Appendix Parallel I/O Mode (Flash memory version)

## Parallel I/O Mode

The parallel I/O mode is entered by making connections shown in Figures 1.101 and 1.102 and then turning the VPPH power supply on. In this mode, the M30201 (flash memory version) operates in a manner similar to the NOR flash memory M5M28F101 from Mitsubishi. Note, however, that there are some differences with regard to the functions not available with the microcomputer (function of read device identification code) and matters related to memory capacity.

Table 1.76 shows pin relationship between the M30201 and M5M28F101 in parallel I/O mode.

Table 1.76. Pin relationship in parallel I/O mode

|                    | M30201(flash memory version)               | M5M28F101      |
|--------------------|--|----------------|
| VCC                | VCC  | VCC            |
| VSS                | VSS  | VSS            |
| Address input      | P60 to P63, P30 to P33,<br>P10 to P17, P50 | A0 to A15, A17 |
| Data I/O           | P00 to P07                                 | D0 to D7       |
| OE input           | P41  | OE             |
| CE input           | P43  | CE             |
| WE input           | P40  | WE             |
| VERFY input (Note) | P51  | —              |

Note: The VRFY input only selects read-only or read/write mode, and does not have any pin associated with it on the M5M28F101.

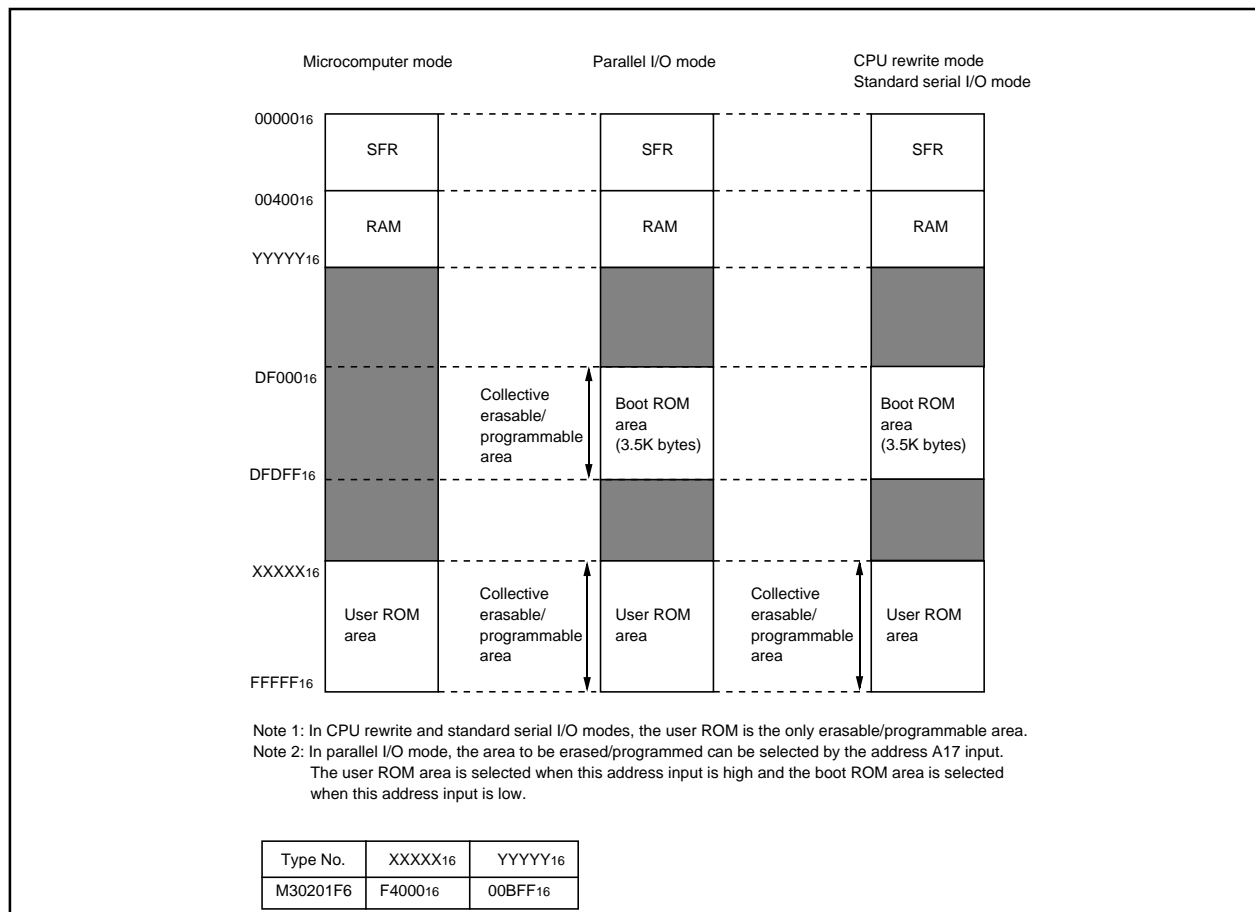


Figure 1.100. Block diagram of flash memory version

## Appendix Parallel I/O Mode (Flash memory version)

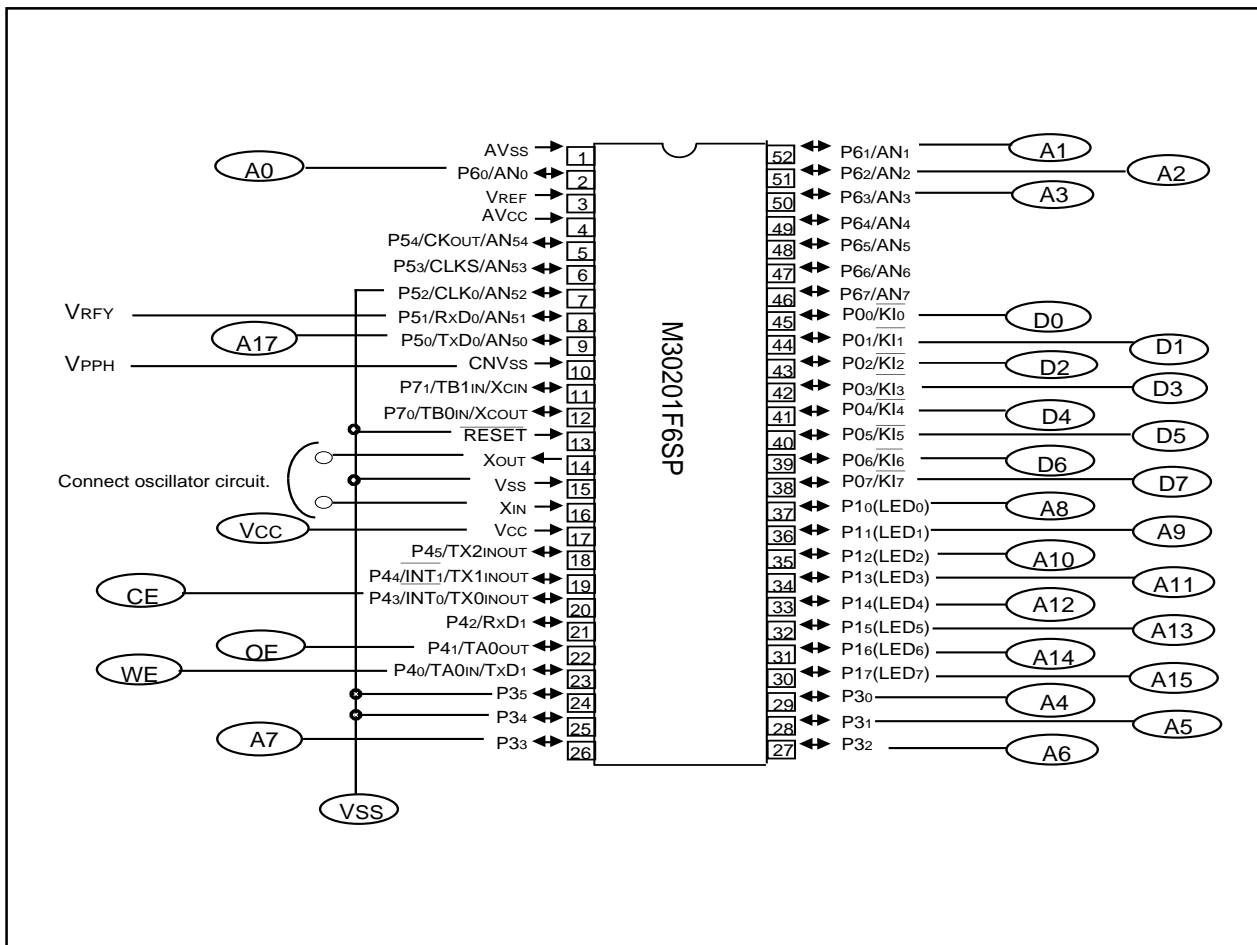


Figure 1.101. Pin connection diagram in parallel I/O mode (1)

## Appendix Parallel I/O Mode (Flash memory version)

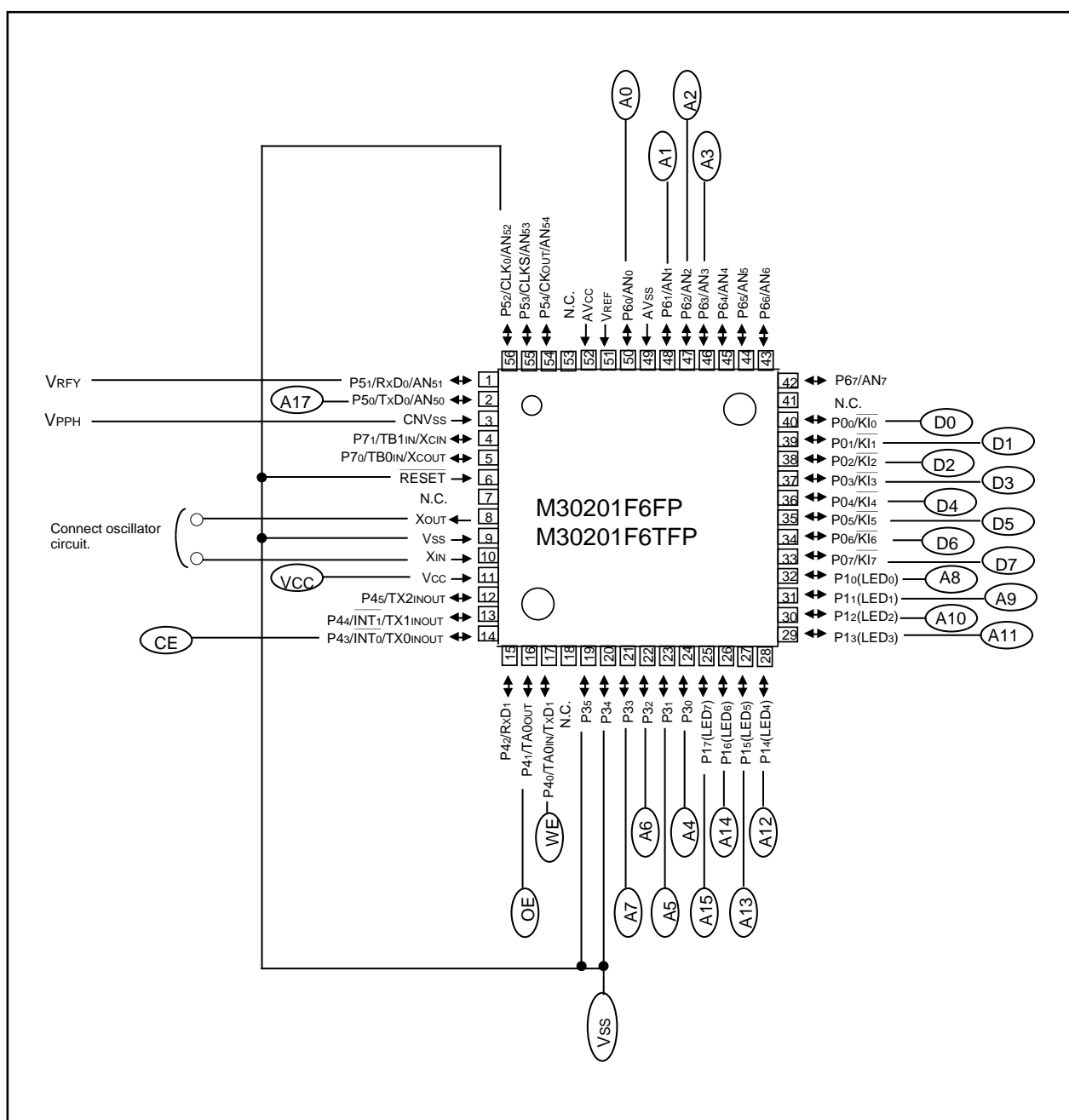


Figure 1.102. Pin connection diagram in parallel I/O mode (2)



## Appendix Parallel I/O Mode (Flash memory version)

### User ROM and Boot ROM Areas

In parallel I/O mode, the user ROM and boot ROM areas shown in Figure 1.100 can be rewritten.

In the boot ROM area, an erase block operation is applied to only one 3.5 K byte block. The boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the Mitsubishi factory. Therefore, using the device in standard serial input/output mode, the user does not need to write to the boot ROM area.

### Functional Outline (Parallel I/O Mode)

In parallel I/O mode, bus operation modes—Read, Output Disable, Standby, and Write—are selected by the status of the  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{WE}$ ,  $V_{RFY}$ , and  $CNV_{SS}$  input pins.

The contents of erase, program, and other operations are selected by writing a software command. The data in memory can only be read out by a read after software command input.

Program and erase operations are controlled using software commands.

**Table 1.77. Relationship between control signals and bus operation modes**

| Pin name   |                 | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $V_{RFY}$       | $V_{PP}$         | D0 to D7    |
|------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|-------------|
| Mode       |                 |                 |                 |                 |                 |                  |             |
| Read only  | Read            | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | V <sub>PPH</sub> | Data output |
|            | Output disabled | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>IL</sub> | V <sub>PPH</sub> | Hi-Z        |
|            | Stand by        | V <sub>IH</sub> | X               | X               | V <sub>IL</sub> | V <sub>PPH</sub> | Hi-Z        |
| Read/Write | Read            | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>PPH</sub> | Data output |
|            | Output disabled | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>PPH</sub> | Hi-Z        |
|            | Stand by        | V <sub>IH</sub> | X               | X               | V <sub>IH</sub> | V <sub>PPH</sub> | Hi-Z        |
|            | Write           | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>PPH</sub> | Data input  |

Note: X can be V<sub>IL</sub> or V<sub>IH</sub>.

## Appendix Parallel I/O Mode (Flash memory version)

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The following explains about bus operation modes, software commands, and status register.

### Bus Operation Modes

Read-only mode is entered by applying  $V_{PPH}$  to the CNVSS pin and a low voltage to the VRFY pin.

Read-only mode has three states: Read, Output Disable, and Standby which are selected by setting the  $\overline{CE}$ ,  $\overline{OE}$ , and  $\overline{WE}$  pins high or low.

Read-write mode is entered by applying  $V_{PPH}$  to the CNVSS pin and a high voltage to the VRFY pin.

Read-write mode has four states: Read, Output Disable, Standby, and Write which are selected by setting the  $\overline{CE}$ ,  $\overline{OE}$ , and  $\overline{WE}$  pins high or low.

#### Read

The Read mode is entered by pulling the  $\overline{WE}$  pin high when the  $\overline{CE}$  and  $\overline{OE}$  pins are low. In Read mode, the data corresponding to each software command entered is output from the data I/O pins D0–D7.

#### Output Disable

The Output Disable mode is entered by pulling the  $\overline{CE}$  pin low and the  $\overline{WE}$  and  $\overline{OE}$  pins high. Also, the data I/O pins are placed in the high-impedance state.

#### Standby

The Standby mode is entered by driving the  $\overline{CE}$  pin high. Also, the data I/O pins are placed in the high-impedance state.

#### Write

The Write mode is entered by applying  $V_{PPH}$  to the CNVSS pin and a high voltage to the VRFY pin and then pulling the  $\overline{WE}$  pin low when the  $\overline{CE}$  pin is low and  $\overline{OE}$  pin is high. In this mode, the device accepts the software commands or write data entered from the data I/O pins. A program, erase, or some other operation is initiated depending on the content of the software command entered here. The input data such as address is latched at the falling edge of  $\overline{WE}$  pin. The input data such as software command is latched at the rising edge of  $\overline{WE}$  pin.

## Appendix Parallel I/O Mode (Flash memory version)

### Software Commands

Table 1.78 lists the software commands available with the M30201 (flash memory version). By entering a software command from the data I/O pins (D<sub>0</sub>–D<sub>7</sub>) in Write mode, specify the content of the operation, such as erase or program operation, to be performed.

The following explains the content of each software command.

**Table 1.78. Software command list (parallel I/O mode)**

| Command        | First bus cycle |                |  | Second bus cycle |                 |  |
|----------------|-----------------|----------------|--|------------------|-----------------|--|
|                | Mode            | Address        | Data (D <sub>0</sub> to D <sub>7</sub> ) | Mode             | Address         | Data (D <sub>0</sub> to D <sub>7</sub> ) |
| Read           | Write           | x              | 00 <sub>16</sub>                         |                  |                 |  |
| Program        | Write           | x              | 40 <sub>16</sub>                         | Write            | Program address | Program data                             |
| Program verify | Write           | x              | C0 <sub>16</sub>                         | Read             | x               | Verify data                              |
| Erase          | Write           | x              | 20 <sub>16</sub>                         | Write            | x               | 20 <sub>16</sub>                         |
| Erase verify   | Write           | Verify address | A0 <sub>16</sub>                         | Read             | x               | Verify data                              |
| Reset          | Write           | x              | FF <sub>16</sub>                         | Write            | x               | FF <sub>16</sub>                         |

#### Read Command (00<sub>16</sub>)

The read mode is entered by writing the command code “00<sub>16</sub>” in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the content of the specified address is read out at the data I/O pins (D<sub>0</sub>–D<sub>7</sub>).

The read mode is retained intact until another command is written.

After reset and after the reset command is executed, the read mode is set.

#### Program Command (40<sub>16</sub>)

The program mode is entered by writing the command code “40<sub>16</sub>” in the first bus cycle. When an address and data to be program is write in the second bus cycle, the flash memory control circuit executes the program operation. The program operation requires approximately 20 μs. Wait for 20 μs or more before the user go to the next processing.

Note 1: The write operation is not completed immediately by writing a program command once. The user must always execute a program-verify command after each program command executed. And if verification fails, the user need to execute the program command repeatedly until the verification passes. See Figure 1.103 for an example of a programming flowchart.

## Appendix Parallel I/O Mode (Flash memory version)

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### Program-verify command (C016)

The program-verify mode is entered by writing the command code "C016" in the first bus cycle and the verify data is output from the data I/O pins (D0–D7) in the second bus cycle.

### Erase command (2016 + 2016)

The flash memory control circuit executes an erase operation by writing command code "2016" in the first bus cycle and the same command code again in the second bus cycle. The erase operation requires approximately 20 ms. Wait for 20 ms or more before the user go to the next processing. Before this erase command can be performed, all memory locations to be erased must have had data "0016" written to by using the program and program-verify commands.

Note 1: The erase operation is not completed immediately by writing an erase command once. The user must always execute an erase-verify command after each erase command executed. And if verification fails, the user need to execute the erase command repeatedly until the verification passes. See Figure 1.103 for an example of an erase flowchart.

### Erase-verify command (A016)

The erase-verify mode is entered by writing the command code "A016" in the first bus cycle and the verify data is output from the data I/O pins (D0–D7) in the second bus cycle.

Note 1: If any unerased memory location is encountered during erase-verify operation, be sure to execute erase and erase-verify operations one more time. In this case, however, the user does not need to write data "0016" to memory before erasing.

## Appendix Parallel I/O Mode (Flash memory version)

**Reset command (FF<sub>16</sub> + FF<sub>16</sub>)**

The reset command is used to stop the program command or the erase command in the middle of operation. After writing command code "40<sub>16</sub>" or "20<sub>16</sub>" twice, write command code "FF<sub>16</sub>" in the first bus cycle and the same command code again in the second bus cycle. The program command or erase command is disabled, with the flash memory placed in read mode.

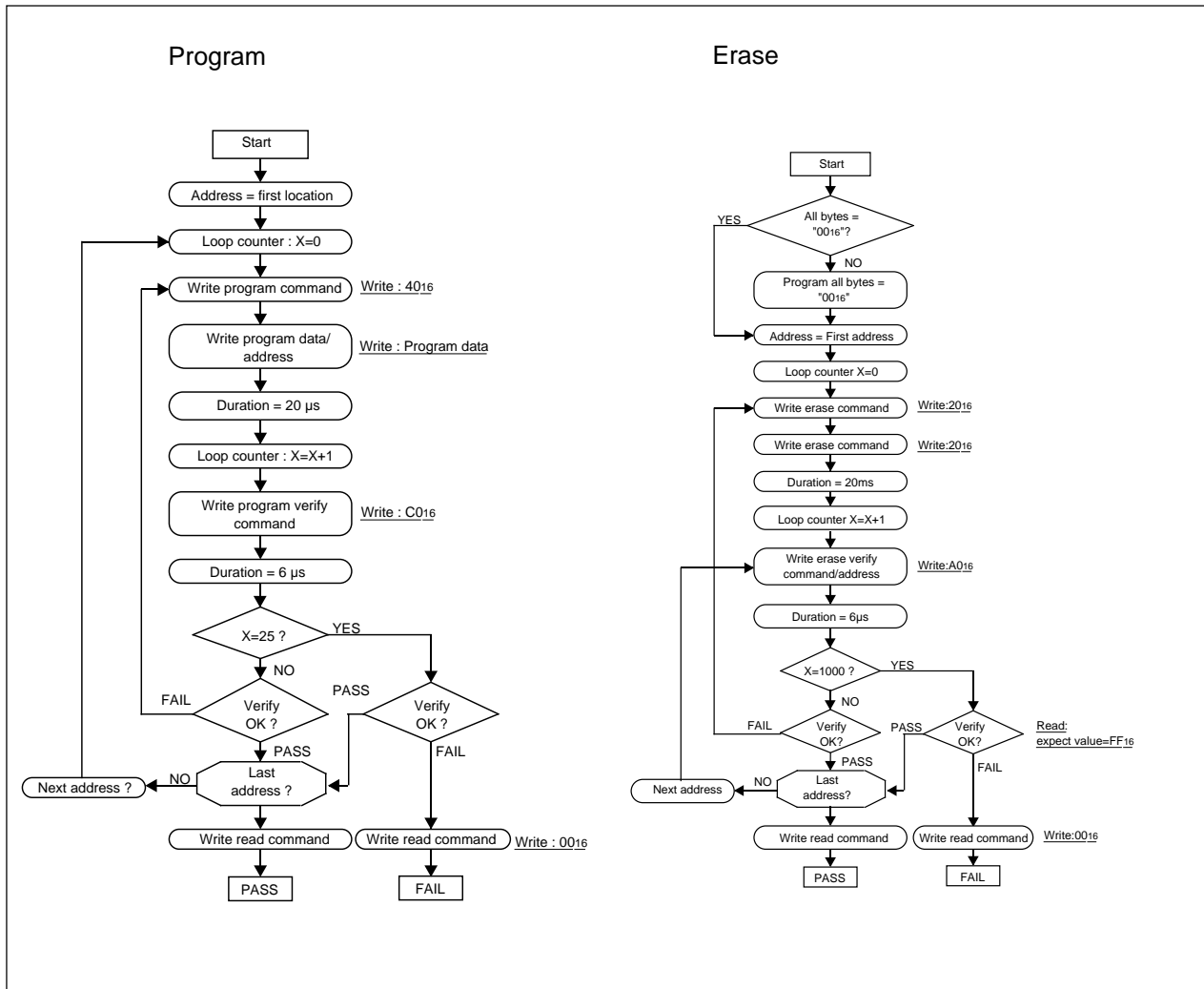


Figure 1.103. Program and erase execution flowchart in the CPU rewrite mode

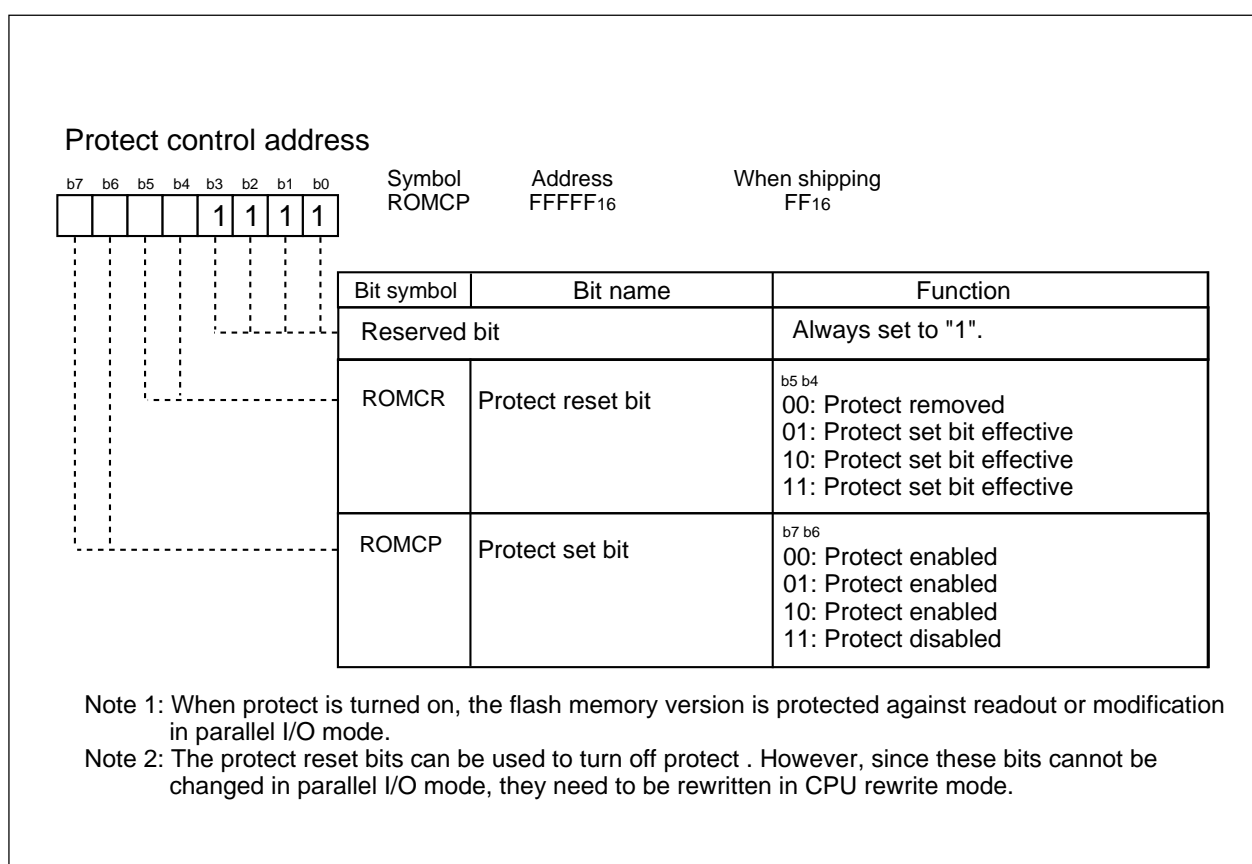
## Appendix Parallel I/O Mode (Flash memory version)

**Protect function**

In parallel I/O mode, the internal flash memory has the "protect function" available. This function protects the flash memory contents from being read or rewritten easily.

Depending on the content at the protect control address (FFFFF<sub>16</sub>) in parallel I/O mode, this function inhibits the flash memory contents against read or modification. The protect control address (FFFFF<sub>16</sub>) is shown in Figure 1.104. (This address exists in the user ROM area.)

The protect function is enabled by setting one of the two protect set bits to "0", so that the internal flash memory contents are inhibited against read or modification. The protect function is disabled by setting both of the two protect reset bits to "00", so that the internal flash memory contents can be read or modified. Once the protect function is set, the user cannot change settings of the protect clear bits while in parallel I/O mode. Settings of the protect reset bits can only be changed in CPU rewrite mode.



**Figure 1.104. Protect control address**

## Appendix Standard Serial I/O Mode (Flash Memory Version)

## Pin functions (Flash memory standard serial I/O mode)

| Pin        | Name                      | I/O               | Description  |
|------------|---------------------------|-------------------|--|
| Vcc,Vss    | Power input               |                   | Apply 5V $\pm$ 10 % to Vcc pin and 0 V to Vss pin.   |
| CNVss      | CNVss                     | I                 | Mode entry pin. Apply 12V $\pm$ 5 % to this pin.   |
| RESET      | Reset input               | I                 | Reset input pin. While reset is "L" level, a 20 cycle or longer clock must be input to XIN pin.  |
| XIN        | Clock input               | I                 | Connect a ceramic resonator or crystal oscillator between XIN and XOUT pins. To input an externally generated clock, input it to XIN pin and open XOUT pin.  |
| XOUT       | Clock output              | O                 |  |
| AVcc, AVss | Analog power supply input |                   | Connect AVss to Vss and AVcc to Vcc, respectively.   |
| VREF       | Reference voltage input   | I                 | Enter the reference voltage for AD from this pin.  |
| P00 to P07 | Input port P0             | I                 | Input "H" or "L" level signal or open.   |
| P10 to P17 | Input port P1             | I                 | Input "H" or "L" level signal or open.   |
| P30 to P35 | Input port P3             | I                 | Input "H" or "L" level signal or open.   |
| P40 to P45 | Input port P4             | I                 | Input "H" or "L" level signal or open.   |
| P54        | Input port P5             | I                 | Input "H" or "L" level signal or open.   |
| P50        | TxD output                | O                 | Serial data output pin.  |
| P51        | RxD input                 | I                 | Serial data input pin.   |
| P52        | SCLK input                | I                 | Mode entry pin. Supply "H" level when powering on MCU. When startup is completed this pin serves the serial input clock.   |
| P53        | BUSY                      | I $\rightarrow$ O | This pin sets the type of serial flash programming mode.<br>•An "H" level input (mode 1) sets the mode to clock synchronous.<br>•An "L" level input (mode 2) sets the mode to clock asynchronous.<br>This pin changes to "output" after entry into standard serial I/O mode. |
| P60 to P67 | Input port P6             | I                 | Input "H" or "L" level signal or open.   |
| P70 to P71 | Input port P7             | I                 | Input "H" or "L" level signal or open.   |

## Appendix Standard Serial I/O Mode (Flash Memory Version)

## Mode setup method

| Signal | Value                             |
|--------|-----------------------------------|
| CNVss  | V <sub>PPH</sub>                  |
| RESET  | V <sub>ss</sub> → V <sub>cc</sub> |
| SCLK   | V <sub>cc</sub> (Note)            |

Note: Apply V<sub>cc</sub> when powering on MCU.

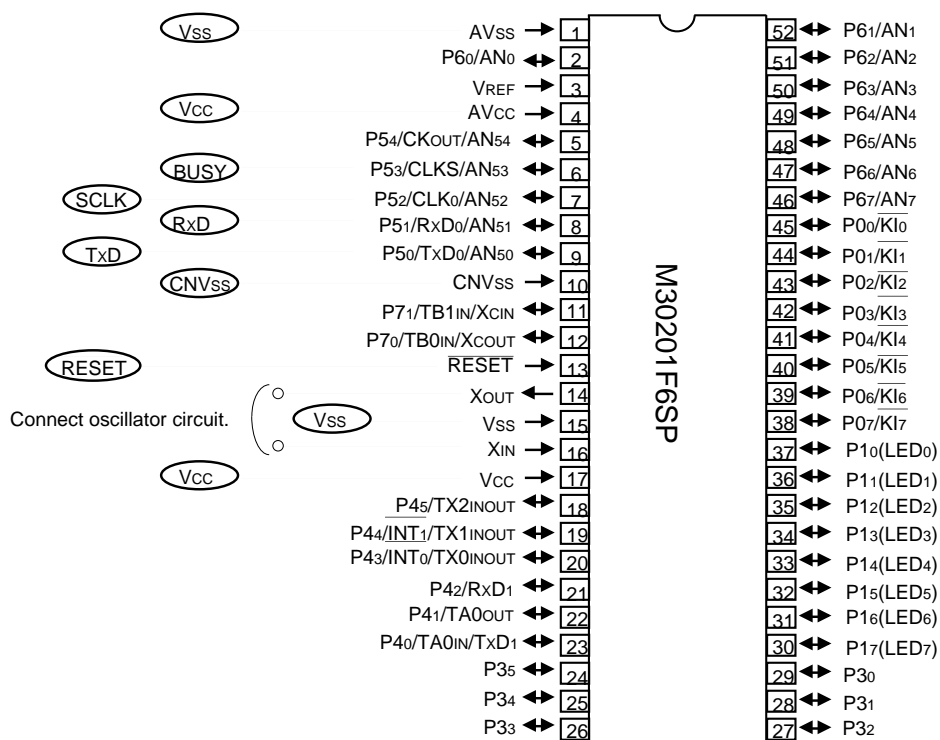


Figure 1.105. Pin connections for standard serial I/O mode (1)



## Appendix Standard Serial I/O Mode (Flash Memory Version)

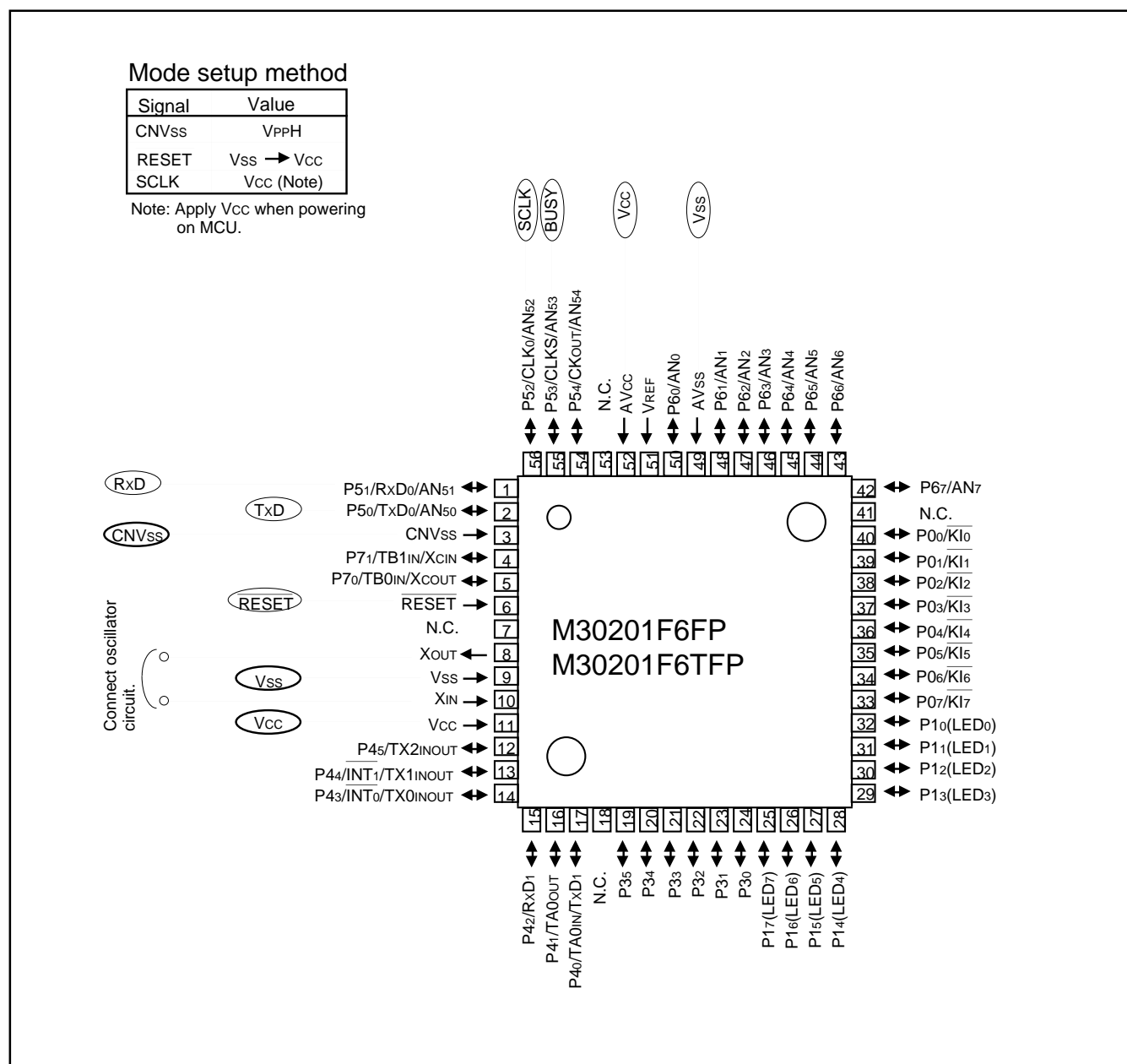


Figure 1.106. Pin connections for serial I/O mode (2)

## Appendix Standard Serial I/O Mode (Flash Memory Version)

**Standard serial I/O mode**

The standard serial I/O mode inputs and outputs the software commands, addresses and data needed to operate (read, program, erase, etc.) the internal flash memory. This I/O is serial. There are actually two standard serial I/O modes: mode 1, which is clock synchronized, and mode 2, which is asynchronous. Both modes require a purpose-specific peripheral unit.

The standard serial I/O mode is different from the parallel I/O mode in that the CPU controls flash memory rewrite (uses the CPU's rewrite mode), rewrite data input and so forth. It is started when the reset is released, which is done when the P52 (SCLK) pin is "H" level, the CNVss pin "VppH" level. (In the ordinary command mode, set CNVss pin to "L" level.)

This control program is written in the boot ROM area when the product is shipped from Mitsubishi. Accordingly, make note of the fact that the standard serial I/O mode cannot be used if the boot ROM area is rewritten in the parallel I/O mode. Figures 1.105 and 1.106 show the pin connections for the standard serial I/O mode. Serial data I/O uses UART0 and transfers the data serially in 8-bit units. Standard serial I/O switches between mode 1 (clock synchronized) and mode 2 (clock asynchronous) according to the level of P53 (BUSY) pin when the reset is released.

To use standard serial I/O mode 1 (clock synchronized), set the P53 (BUSY) pin to "H" level and release the reset. The operation uses the four UART0 pins CLK0, RxD0, TxD0 and P53 (BUSY). The CLK0 pin is the transfer clock input pin through which an external transfer clock is input. The TxD0 pin is for CMOS output. The P53 (BUSY) pin outputs an "L" level when ready for reception and an "H" level when reception starts.

To use standard serial I/O mode 2 (clock asynchronous), set the P53 (BUSY) pin to "L" level and release the reset. The operation uses the two UART0 pins RxD0 and TxD0.

In the standard serial I/O mode, only the user ROM area indicated in Figure 1.96 can be rewritten. The boot ROM cannot.

In the standard serial I/O mode, a 7-byte ID code is used. When there is data in the flash memory, commands sent from the peripheral unit are not accepted unless the ID code matches.

**Overview of standard serial I/O mode 1 (clock synchronized)**

In standard serial I/O mode 1, software commands, addresses and data are input and output between the MCU and peripheral units (serial programmer, etc.) using clock-synchronized serial I/O (UART0) and P53 (BUSY). Standard serial I/O mode 1 is engaged by releasing the reset with the P53 (BUSY) pin "H" level. In reception, software commands, addresses and program data are synchronized with the rise of the transfer clock that is input to the CLK0 pin, and are then input to the MCU via the RxDo pin. In transmission, the read data and status are synchronized with the fall of the transfer clock, and output from the TxDo pin.

The TxDo pin is for CMOS output. Transfer is in 8-bit units with LSB first.

When busy, such as during transmission, reception, erasing or program execution, the P53 (BUSY) pin is "H" level. Accordingly, always start the next transfer after the P53 (BUSY) pin is "L" level.

Also, data and status registers in memory can be read after inputting software commands. Status, such as the operating state of the flash memory or whether a program or erase operation ended successfully or not, can be checked by reading the status register. Here following are explained software commands, status registers, etc.

## Appendix Standard Serial I/O Mode 1 (Flash Memory Version)

## Software Commands

Table 1.79 lists software commands. In the standard serial I/O mode 1, erase operations, programs and reading are controlled by transferring software commands via the RxD<sub>0</sub> pin. Software commands are explained here below.

Table 1.79. Software commands (Standard serial I/O mode 1)

|    | Control command              |                  | 2nd byte            | 3rd byte            | 4th byte             | 5th byte            | 6th byte                    |                                 | When ID is not verificate |
|----|------------------------------|------------------|---------------------|---------------------|----------------------|---------------------|-----------------------------|---------------------------------|---------------------------|
| 1  | Page read                    | FF <sub>16</sub> | Address (middle)    | Address (high)      | Data output          | Data output         | Data output                 | Data output to 259th byte       | Not acceptable            |
| 2  | Page program                 | 41 <sub>16</sub> | Address (middle)    | Address (high)      | Data input           | Data input          | Data input                  | Data input to 259th byte        | Not acceptable            |
| 3  | Erase all unlocked blocks    | A7 <sub>16</sub> | D0 <sub>16</sub>    |                     |                      |                     |                             |                                 | Not acceptable            |
| 4  | Read status register         | 70 <sub>16</sub> | SRD output          | SRD1 output         |                      |                     |                             |                                 | Acceptable                |
| 5  | Clear status register        | 50 <sub>16</sub> |                     |                     |                      |                     |                             |                                 | Not acceptable            |
| 6  | Read lockbit status          | 71 <sub>16</sub> | Address (middle)    | Address (high)      | Lock bit data output |                     |                             |                                 | Not acceptable            |
| 7  | ID check function            | F5 <sub>16</sub> | Address (low)       | Address (middle)    | Address (high)       | ID size             | ID1                         | To ID7                          | Acceptable                |
| 8  | Download function            | FA <sub>16</sub> | Size (low)          | Size (high)         | Check-sum            | Data input          | To required number of times |                                 | Not acceptable            |
| 9  | Version data output function | FB <sub>16</sub> | Version data output | Version data output | Version data output  | Version data output | Version data output         | Version data output to 9th byte | Acceptable                |
| 10 | Boot area output function    | FC <sub>16</sub> | Address (middle)    | Address (high)      | Data output          | Data output         | Data output                 | Data output to 259th byte       | Not acceptable            |

Note 1: Shading indicates transfer from flash memory microcomputer to peripheral unit. All other data is transferred from the peripheral unit to the flash memory microcomputer.

Note 2: SRD refers to status register data. SRD1 refers to status register 1 data.

Note 3: All commands can be accepted when the flash memory is totally blank.

## Appendix Standard Serial I/O Mode 1 (Flash Memory Version)

**Page Read Command**

This command reads the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page read command as explained here following.

- (1) Transfer the "FF<sub>16</sub>" command code with the 1st byte.
- (2) Transfer addresses A<sub>8</sub> to A<sub>15</sub> and A<sub>16</sub> to A<sub>23</sub> with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, data (D<sub>0</sub>–D<sub>7</sub>) for the page (256 bytes) specified with addresses A<sub>8</sub> to A<sub>23</sub> will be output sequentially from the smallest address first in sync with the rise of the clock.

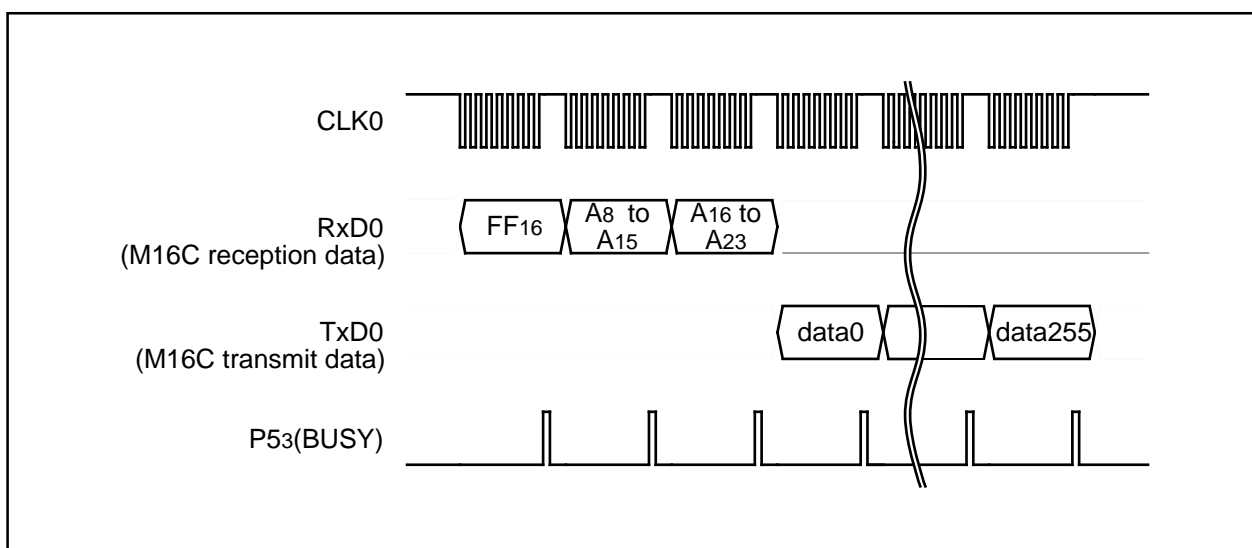


Figure 1.107. Timing for page read

**Read Status Register Command**

This command reads status information. When the "70<sub>16</sub>" command code is sent with the 1st byte, the contents of the status register (SRD) specified with the 2nd byte and the contents of status register 1 (SRD1) specified with the 3rd byte are read.

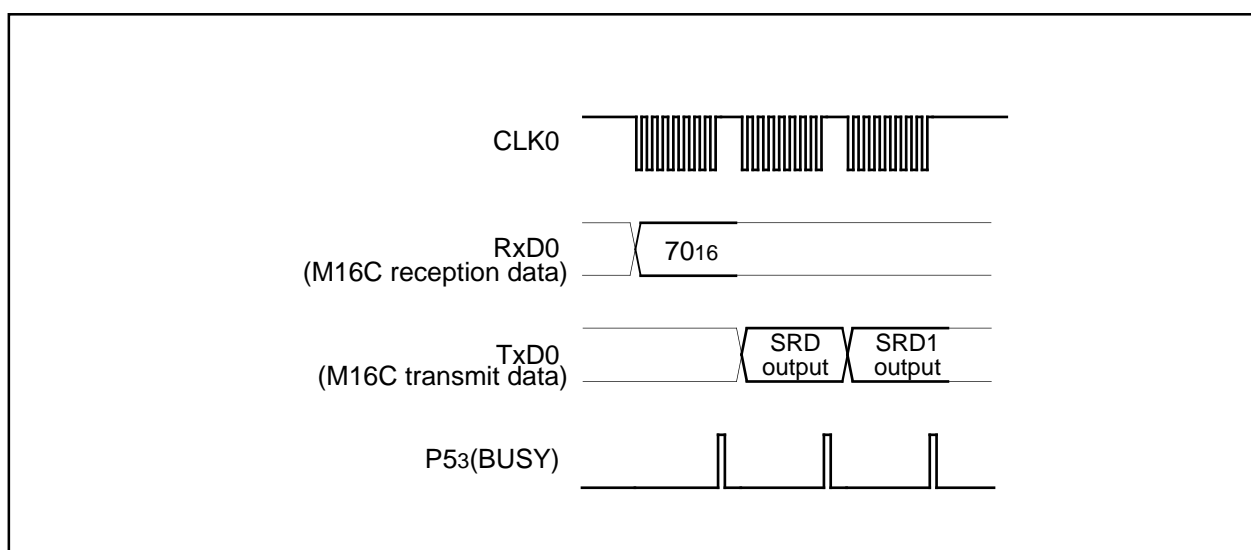


Figure 1.108. Timing for reading the status register

**Clear Status Register Command**

This command clears the bits (SR3–SR4) which are set when the status register operation ends in error. When the “5016” command code is sent with the 1st byte, the aforementioned bits are cleared. When the clear status register operation ends, the P53 (BUSY) signal changes from the “H” to the “L” level.

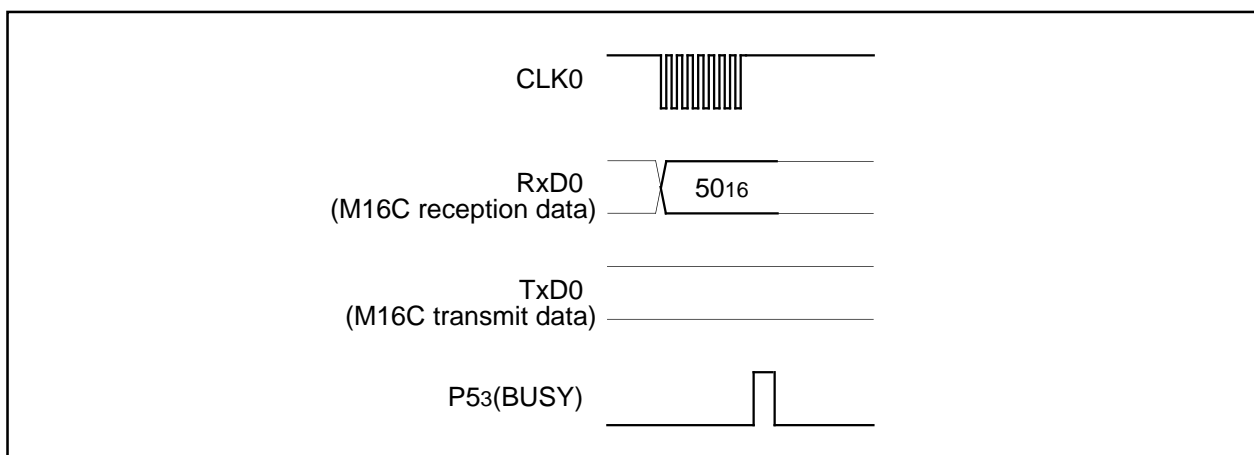


Figure 1.109. Timing for clearing the status register

**Page Program Command**

This command writes the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page program command as explained here following.

- (1) Transfer the “4116” command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, as write data (D0–D7) for the page (256 bytes) specified with addresses A8 to A23 is input sequentially from the smallest address first, that page is automatically written.

When reception setup for the next 256 bytes ends, the P53 (BUSY) signal changes from the “H” to the “L” level. The result of the page program can be known by reading the status register. For more information, see the section on the status register.

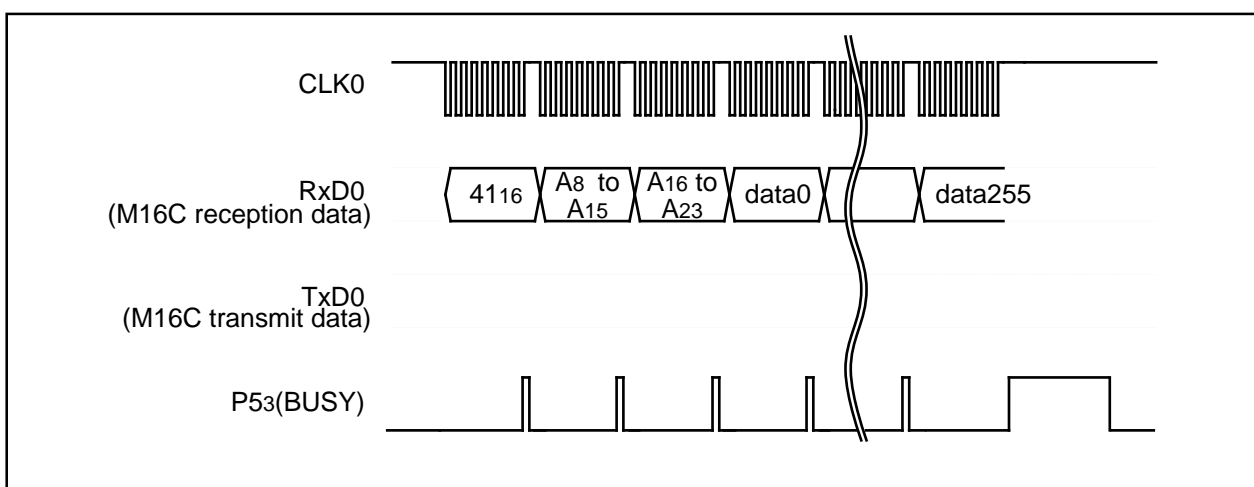


Figure 1.110. Timing for the page program

## Appendix Standard Serial I/O Mode 1 (Flash Memory Version)

**Erase All Unlocked Blocks Command**

This command erases the content of all blocks. Execute the erase all unlocked blocks command as explained here following.

- (1) Transfer the "A7<sub>16</sub>" command code with the 1st byte.
- (2) Transfer the verify command code "D0<sub>16</sub>" with the 2nd byte. With the verify command code, the erase operation will start and continue for all blocks in the flash memory.

When block erasing ends, the P53 (BUSY) signal changes from the "H" to the "L" level. The result of the erase operation can be known by reading the status register.

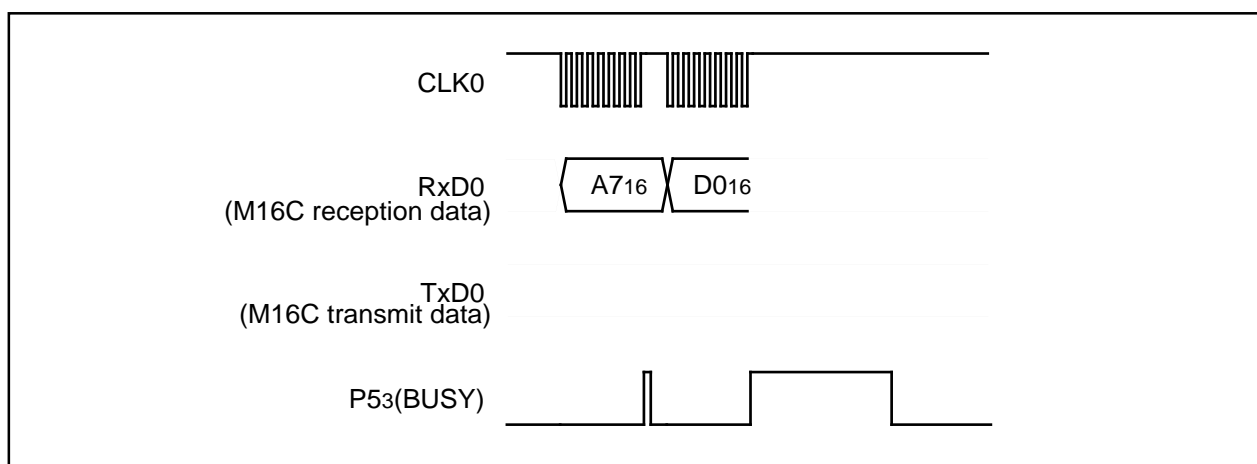


Figure 1.111. Timing for erasing all unlocked blocks

**Read Lock Bit Status Command**

This command reads the lock bit status of the specified block. Execute the read lock bit status command as explained here following.

- (1) Transfer the "71<sub>16</sub>" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) The lock bit data of the specified block is output with the 4th byte. Write the highest address of the specified block for addresses A8 to A23.

The M30201 (flash memory version) does not have the lock bit, so the read value is always "1" (block unlock).

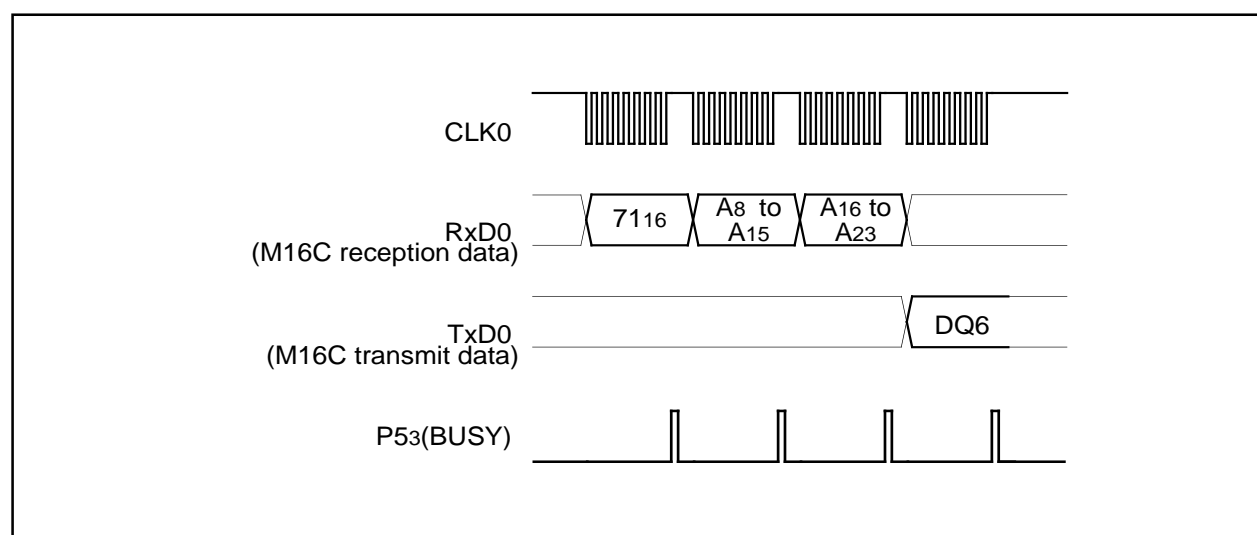


Figure 1.112. Timing for reading lock bit status

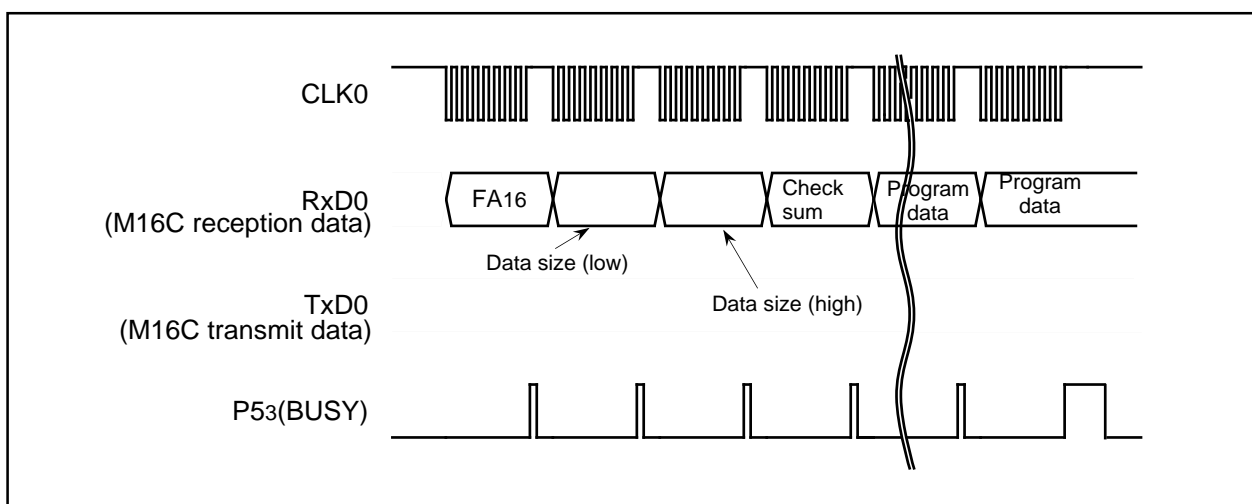
## Appendix Standard Serial I/O Mode 1 (Flash Memory Version)

**Download Command**

This command downloads a program to the RAM for execution. Execute the download command as explained here following.

- (1) Transfer the "FA16" command code with the 1st byte.
- (2) Transfer the program size with the 2nd and 3rd bytes.
- (3) Transfer the check sum with the 4th byte. The check sum is added to all data sent with the 5th byte onward.
- (4) The program to execute is sent with the 5th byte onward.

When all data has been transmitted, if the check sum matches, the downloaded program is executed. The size of the program will vary according to the internal RAM.



**Figure 1.113. Timing for download**



## Appendix Standard Serial I/O Mode 1 (Flash Memory Version)

**Version Information Output Command**

This command outputs the version information of the control program stored in the boot area. Execute the version information output command as explained here following.

- (1) Transfer the "FB16" command code with the 1st byte.
- (2) The version information will be output from the 2nd byte onward. This data is composed of 8 ASCII code characters.

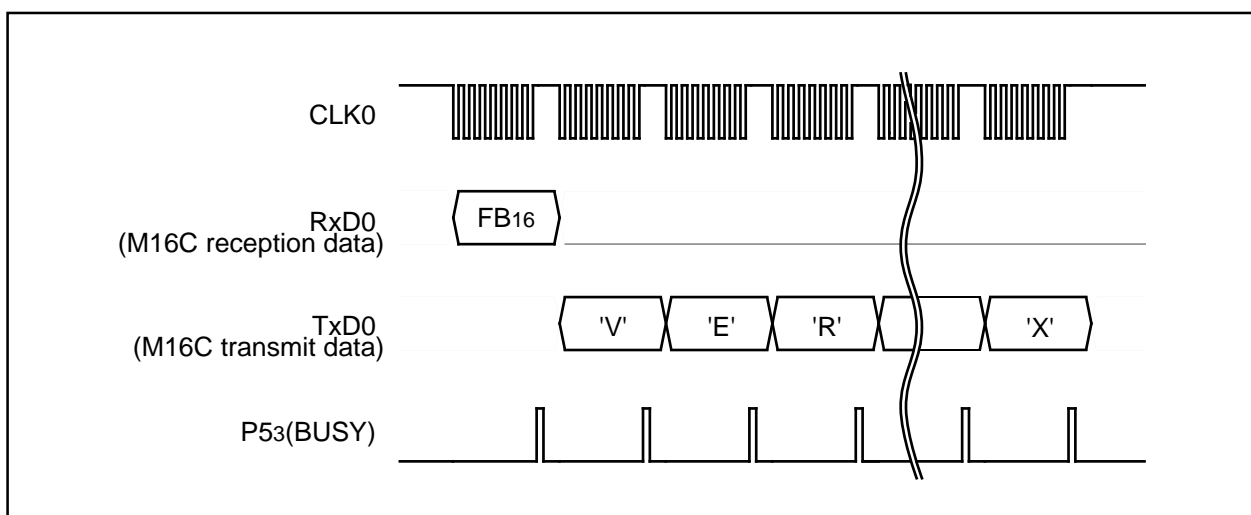


Figure 1.114. Timing for version information output

**Boot ROM Area Output Command**

This command outputs the control program stored in the boot ROM area in one page blocks (256 bytes). Execute the boot ROM area output command as explained here following.

- (1) Transfer the "FC16" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, data (D0–D7) for the page (256 bytes) specified with addresses A8 to A23 will be output sequentially from the smallest address first, in sync with the fall of the clock.

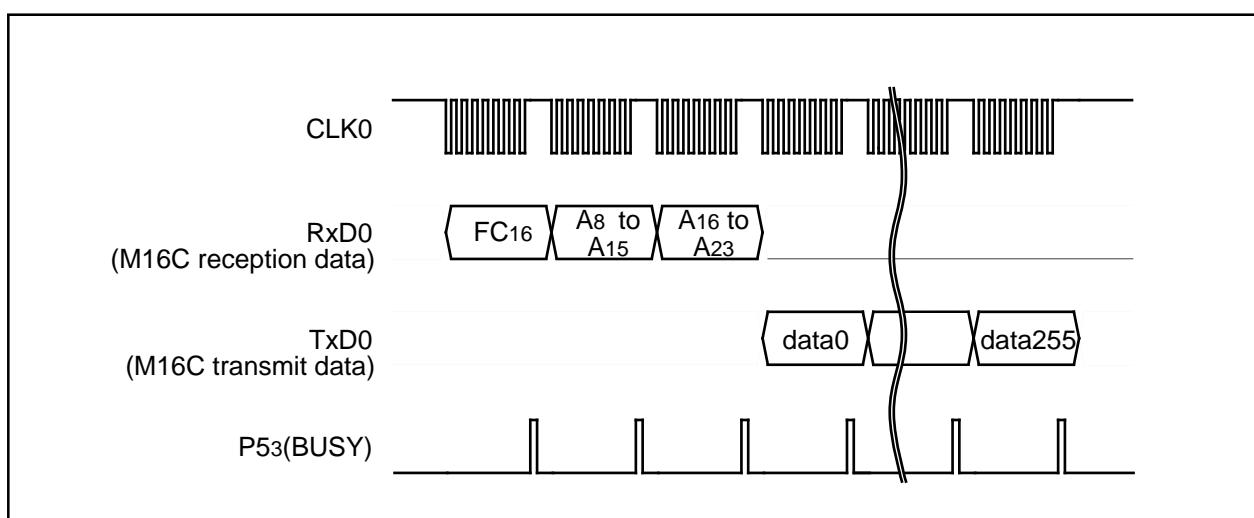


Figure 1.115. Timing for boot ROM area output

## Appendix Standard Serial I/O Mode 1 (Flash Memory Version)

**ID Check**

This command checks the ID code. Execute the boot ID check command as explained here following.

- (1) Transfer the "F5<sub>16</sub>" command code with the 1st byte.
- (2) Transfer addresses A0 to A7, A8 to A15 and A16 to A23 of the 1st byte of the ID code with the 2nd, 3rd and 4th bytes respectively.
- (3) Transfer the number of data sets of the ID code with the 5th byte.
- (4) The ID code is sent with the 6th byte onward, starting with the 1st byte of the code.

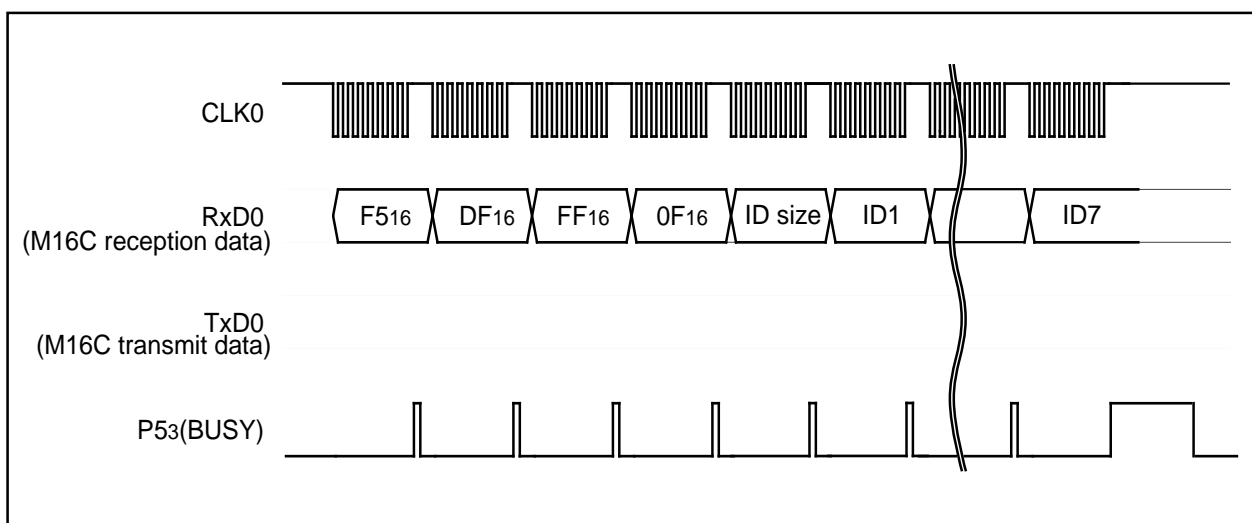


Figure 1.116. Timing for the ID check

**ID Code**

When the flash memory is not blank, the ID code sent from the peripheral units and the ID code written in the flash memory are compared to see if they match. If the codes do not match, the command sent from the peripheral units is not accepted. An ID code contains 8 bits of data. Area is, from the 1st byte, addresses 0FFFD<sub>16</sub>, 0FFFE<sub>316</sub>, 0FFFE<sub>B16</sub>, 0FFFE<sub>F16</sub>, 0FFFF<sub>316</sub>, 0FFFF<sub>716</sub> and 0FFFF<sub>B16</sub>. Write a program into the flash memory, which already has the ID code set for these addresses.

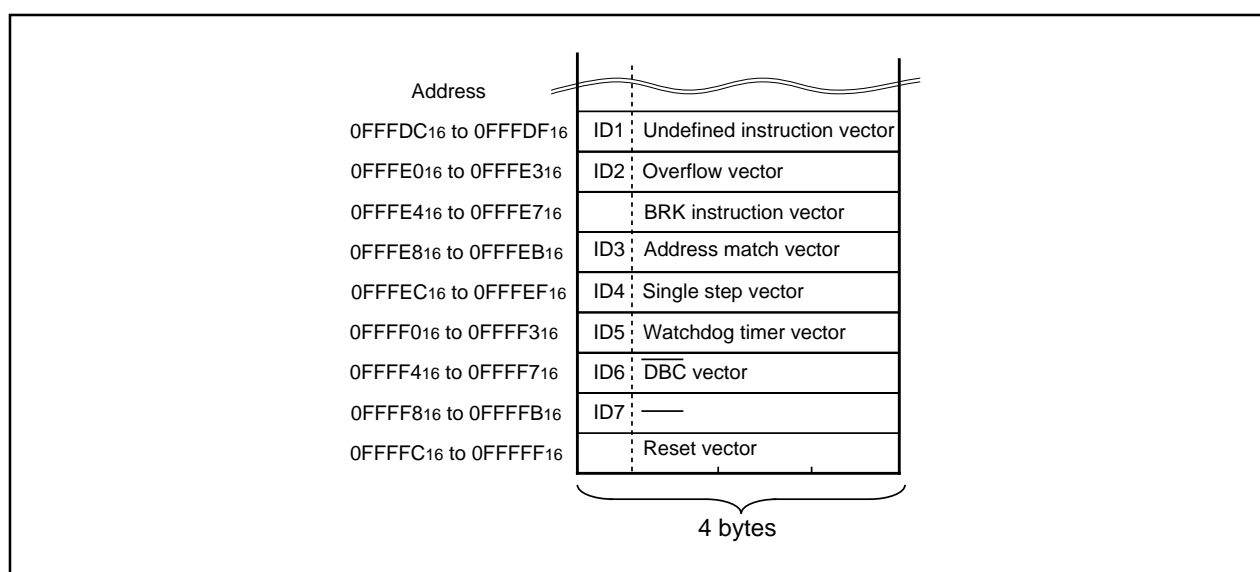


Figure 1.117. ID code storage addresses

## Status Register (SRD)

The status register indicates operating status of the flash memory and status such as whether an erase operation or a program ended successfully or in error. It can be read by writing the read status register command (70<sub>16</sub>). Also, the status register is cleared by writing the clear status register command (50<sub>16</sub>). Table 1.80 gives the definition of each status register bit. After clearing the reset, the status register outputs "80<sub>16</sub>".

**Table 1.80. Status register (SRD)**

| SRD0 bits  | Status name | Definition          |                     |
|------------|-------------|---------------------|---------------------|
|            |             | "1"                 | "0"                 |
| SR7 (bit7) | Status bit  | Ready               | Busy                |
| SR6 (bit6) | Reserved    | -                   | -                   |
| SR5 (bit5) | Erase bit   | Terminated in error | Terminated normally |
| SR4 (bit4) | Program bit | Terminated in error | Terminated normally |
| SR3 (bit3) | Reserved    | -                   | -                   |
| SR2 (bit2) | Reserved    | -                   | -                   |
| SR1 (bit1) | Reserved    | -                   | -                   |
| SR0 (bit0) | Reserved    | -                   | -                   |

### Status bit (SR7)

The status bit indicates the operating status of the flash memory. When power is turned on, "1" (ready) is set for it. The bit is set to "0" (busy) during an auto write or auto erase operation, but it is set back to "1" when the operation ends.

### Erase Status (SR5)

The erase status reports the operating status of the auto erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is set to "0".

### Program Status (SR4)

The program status reports the operating status of the auto write operation. If a write error occurs, it is set to "1". When the program status is cleared, it is set to "0".

## Status Register 1 (SRD1)

Status register 1 indicates the status of serial communications, results from ID checks and results from check sum comparisons. It can be read after the SRD by writing the read status register command (70<sub>16</sub>). Also, status register 1 is cleared by writing the clear status register command (50<sub>16</sub>).

Table 1.81 gives the definition of each status register 1 bit. "00<sub>16</sub>" is output when power is turned ON and the flag status is maintained even after the reset.

**Table 1.81. Status register 1 (SRD1)**

| SRD1 bits                  | Status name               | Definition           |   |
|----------------------------|---------------------------|----------------------|---|
|                            |                           | "1"                  | "0"   |
| SR15 (bit7)                | Boot update completed bit | Update completed     | Not update  |
| SR14 (bit6)                | Reserved                  | -                    | -   |
| SR13 (bit5)                | Reserved                  | -                    | -   |
| SR12 (bit4)                | Checksum match bit        | Match                | Mismatch  |
| SR11 (bit3)<br>SR10 (bit2) | ID check completed bits   | 00<br>01<br>10<br>11 | Not verified<br>Verification mismatch<br>Reserved<br>Verified |
| SR9 (bit1)                 | Data receive time out     | Time out             | Normal operation  |
| SR8 (bit0)                 | Reserved                  | -                    | -   |

### Boot Update Completed Bit (SR15)

This flag indicates whether the control program was downloaded to the RAM or not, using the download function.

### Check Sum Consistency Bit (SR12)

This flag indicates whether the check sum matches or not when a program, is downloaded for execution using the download function.

### ID Check Completed Bits (SR11 and SR10)

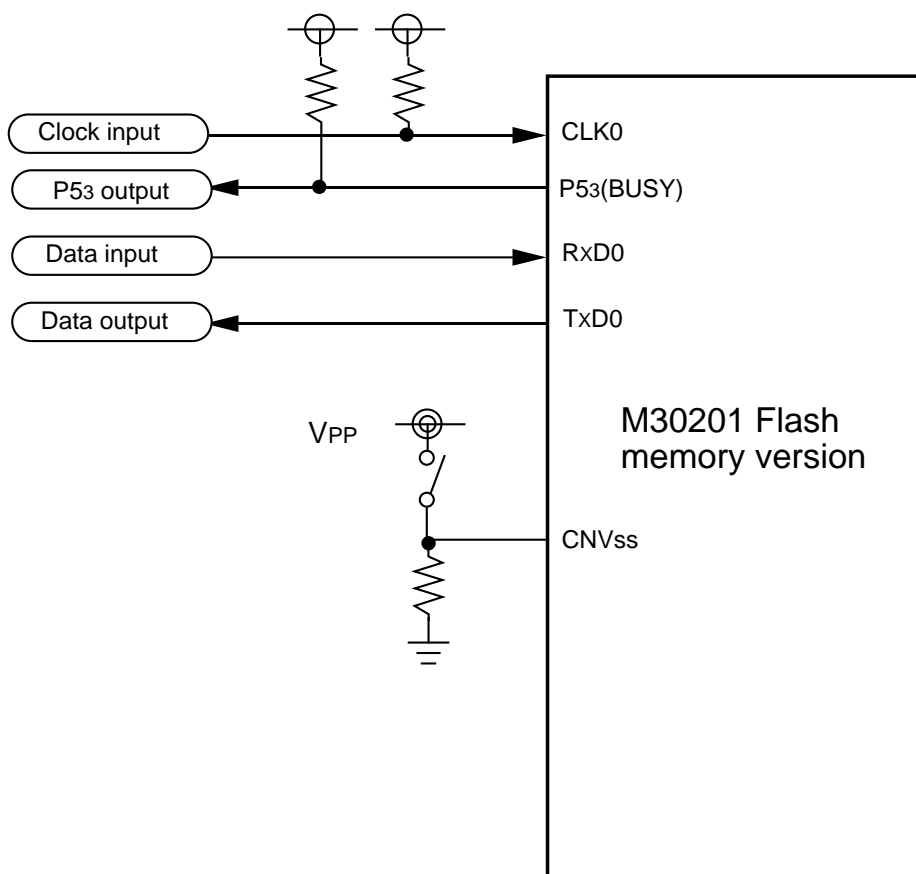
These flags indicate the result of ID checks. Some commands cannot be accepted without an ID check.

### Data Reception Time Out (SR9)

This flag indicates when a time out error is generated during data reception. If this flag is attached during data reception, the received data is discarded and the microcomputer returns to the command wait state.

### Example Circuit Application for The Standard Serial I/O Mode 1

The below figure shows a circuit application for the standard serial I/O mode 1. Control pins will vary according to programmer, therefore see the peripheral unit manual for more information.



- (1) Control pins and external circuitry will vary according to peripheral unit. For more information, see the peripheral unit manual.
- (2) In this example, the microprocessor mode and standard serial I/O mode are switched via a switch.

Figure 1.118. Example circuit application for the standard serial I/O mode 1

## Overview of standard serial I/O mode 2 (clock asynchronized)

In standard serial I/O mode 2, software commands, addresses and data are input and output between the MCU and peripheral units (serial programmer, etc.) using 2-wire clock-asynchronized serial I/O (UART0). Standard serial I/O mode 2 is engaged by releasing the reset with the P5<sub>3</sub> (BUSY) pin "L" level.

The TxD<sub>0</sub> pin is for CMOS output. Data transfer is in 8-bit units with LSB first, 1 stop bit and parity OFF.

After the reset is released, connections can be established at 9,600 bps when initial communications (Figure 1.119) are made with a peripheral unit. However, this requires a main clock with a minimum 2 MHz input oscillation frequency. Baud rate can also be changed from 9,600 bps to 19,200, 38,400 or 57,600 bps by executing software commands. However, communication errors may occur because of the oscillation frequency of the main clock. If errors occur, change the main clock's oscillation frequency and the baud rate. After executing commands from a peripheral unit that requires time to erase and write data, as with erase and program commands, allow a sufficient time interval or execute the read status command and check how processing ended, before executing the next command.

Data and status registers in memory can be read after transmitting software commands. Status, such as the operating state of the flash memory or whether a program or erase operation ended successfully or not, can be checked by reading the status register. Here following are explained initial communications with peripheral units, how frequency is identified and software commands.

## Initial communications with peripheral units

After the reset is released, the bit rate generator is adjusted to 9,600 bps to match the oscillation frequency of the main clock, by sending the code as prescribed by the protocol for initial communications with peripheral units (Figure 1.119).

- (1) Transmit "B016" from a peripheral unit. If the oscillation frequency input by the main clock is 10 MHz, the MCU with internal flash memory outputs the "B016" check code. If the oscillation frequency is anything other than 10 MHz, the MCU does not output anything.
- (2) Transmit "0016" from a peripheral unit 16 times. (The MCU with internal flash memory sets the bit rate generator so that "0016" can be successfully received.)
- (3) The MCU with internal flash memory outputs the "B016" check code and initial communications end successfully \*1. Initial communications must be transmitted at a speed of 9,600 bps and a transfer interval of a minimum 15 ms. Also, the baud rate at the end of initial communications is 9,600 bps.

\*1. If the peripheral unit cannot receive "B016" successfully, change the oscillation frequency of the main clock.

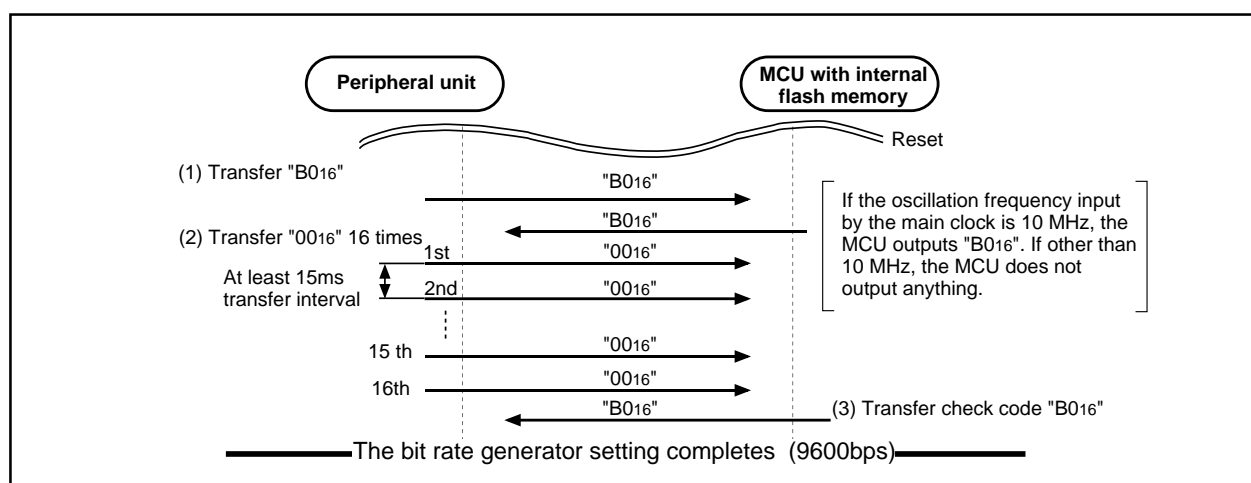


Figure 1.119. Peripheral unit and initial communication

## Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

**How frequency is identified**

When "0016" data is received 16 times from a peripheral unit at a baud rate of 9,600 bps, the value of the bit rate generator is set to match the operating frequency (2 - 10 MHz). The highest speed is taken from the first 8 transmissions and the lowest from the last 8. These values are then used to calculate the bit rate generator value for a baud rate of 9,600 bps.

Baud rate cannot be attained with some operating frequencies. Table 1.82 gives the operation frequency and the baud rate that can be attained for.

**Table 1.82 Operation frequency and the baud rate**

| Operation frequency<br>(MHz) | Baud rate<br>9,600bps | Baud rate<br>19,200bps | Baud rate<br>38,400bps | Baud rate<br>57,600bps |
|------------------------------|-----------------------|------------------------|------------------------|------------------------|
| 10MHz                        | √                     | √                      | —                      | √                      |
| 8MHz                         | √                     | √                      | —                      | √                      |
| 7.3728MHz                    | √                     | √                      | √                      | √                      |
| 6MHz                         | √                     | √                      | √                      | —                      |
| 5MHz                         | √                     | √                      | —                      | —                      |
| 4.5MHz                       | √                     | √                      | —                      | √                      |
| 4.194304MHz                  | √                     | √                      | √                      | —                      |
| 4MHz                         | √                     | √                      | —                      | —                      |
| 3.58MHz                      | √                     | √                      | √                      | √                      |
| 3MHz                         | √                     | √                      | √                      | —                      |
| 2MHz                         | √                     | —                      | —                      | —                      |

√ : Communications possible

— : Communications not possible

## Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

## Software Commands

Table 1.83 lists software commands. In the standard serial I/O mode 2, erase operations, programs and reading are controlled by transferring software commands via the RxD<sub>0</sub> pin. Standard serial I/O mode 2 adds four transmission speed commands - 9,600, 19,200, 38,400 and 57,600 bps - to the software commands of standard serial I/O mode 1. Software commands are explained here below.

Table 1.83. Software commands (Standard serial I/O mode 2)

|    | Control command               | 1st byte transfer | 2nd byte            | 3rd byte            | 4th byte             | 5th byte            | 6th byte                    |                                 | When ID is not verified |
|----|-------------------------------|-------------------|---------------------|---------------------|----------------------|---------------------|-----------------------------|---------------------------------|-------------------------|
| 1  | Page read                     | FF <sub>16</sub>  | Address (middle)    | Address (high)      | Data output          | Data output         | Data output                 | Data output to 259th byte       | Not acceptable          |
| 2  | Page program                  | 41 <sub>16</sub>  | Address (middle)    | Address (high)      | Data input           | Data input          | Data input                  | Data input to 259th byte        | Not acceptable          |
| 3  | Erase all unlocked blocks     | A7 <sub>16</sub>  | D0 <sub>16</sub>    |                     |                      |                     |                             |                                 | Not acceptable          |
| 4  | Read status register          | 70 <sub>16</sub>  | SRD output          | SRD1 output         |                      |                     |                             |                                 | Acceptable              |
| 5  | Clear status register         | 50 <sub>16</sub>  |                     |                     |                      |                     |                             |                                 | Not acceptable          |
| 6  | Read lock bit status          | 71 <sub>16</sub>  | Address (middle)    | Address (high)      | Lock bit data output |                     |                             |                                 | Not acceptable          |
| 7  | Code processing function      | F5 <sub>16</sub>  | Address (low)       | Address (middle)    | Address (high)       | ID size             | ID1                         | To ID7                          | Acceptable              |
| 8  | Download function             | FA <sub>16</sub>  | Size (low)          | Size (high)         | Check-sum            | Data input          | To required number of times |                                 | Not acceptable          |
| 9  | Version data output function  | FB <sub>16</sub>  | Version data output | Version data output | Version data output  | Version data output | Version data output         | Version data output to 9th byte | Acceptable              |
| 10 | Boot ROM area output function | FC <sub>16</sub>  | Address (middle)    | Address (high)      | Data output          | Data output         | Data output                 | Data output to 259th byte       | Not acceptable          |
| 11 | Baud rate 9600                | B0 <sub>16</sub>  | B0 <sub>16</sub>    |                     |                      |                     |                             |                                 | Acceptable              |
| 12 | Baud rate 19200               | B1 <sub>16</sub>  | B1 <sub>16</sub>    |                     |                      |                     |                             |                                 | Acceptable              |
| 13 | Baud rate 38400               | B2 <sub>16</sub>  | B2 <sub>16</sub>    |                     |                      |                     |                             |                                 | Acceptable              |
| 14 | Baud rate 57600               | B3 <sub>16</sub>  | B3 <sub>16</sub>    |                     |                      |                     |                             |                                 | Acceptable              |

Note 1: Shading indicates transfer from flash memory microcomputer to peripheral unit. All other data is transferred from the peripheral unit to the flash memory microcomputer.

Note 2: SRD refers to status register data. SRD1 refers to status register 1 data.

Note 3: All commands can be accepted when the flash memory is totally blank.



## Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

**Page Read Command**

This command reads the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page read command as explained here following.

- (1) Transfer the "FF<sub>16</sub>" command code with the 1st byte.
- (2) Transfer addresses A<sub>8</sub> to A<sub>15</sub> and A<sub>16</sub> to A<sub>23</sub> with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, data (D<sub>0</sub>–D<sub>7</sub>) for the page (256 bytes) specified with addresses A<sub>8</sub> to A<sub>23</sub> will be output sequentially from the smallest address first in sync with the fall of the clock.

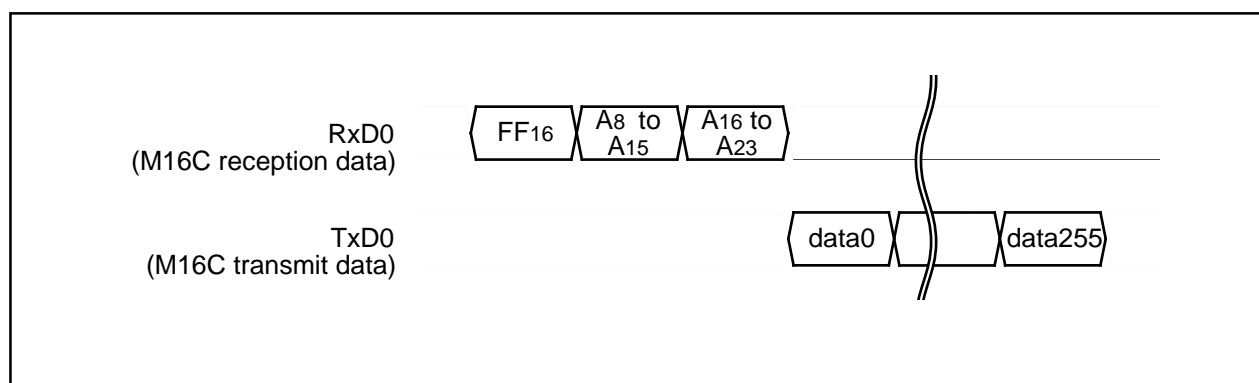


Figure 1.120. Timing for page read

**Read Status Register Command**

This command reads status information. When the "70<sub>16</sub>" command code is sent with the 1st byte, the contents of the status register (SRD) specified with the 2nd byte and the contents of status register 1 (SRD1) specified with the 3rd byte are read.

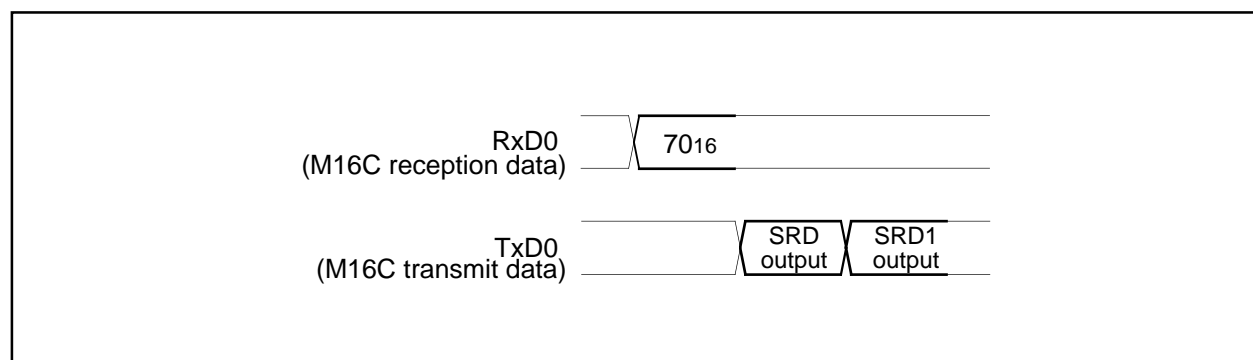


Figure 1.121. Timing for reading the status register

## Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

**Clear Status Register Command**

This command clears the bits (SR3–SR4) which are set when the status register operation ends in error. When the “5016” command code is sent with the 1st byte, the aforementioned bits are cleared. When the clear status register operation ends, the RTS<sub>1</sub> (BUSY) signal changes from the “H” to the “L” level.

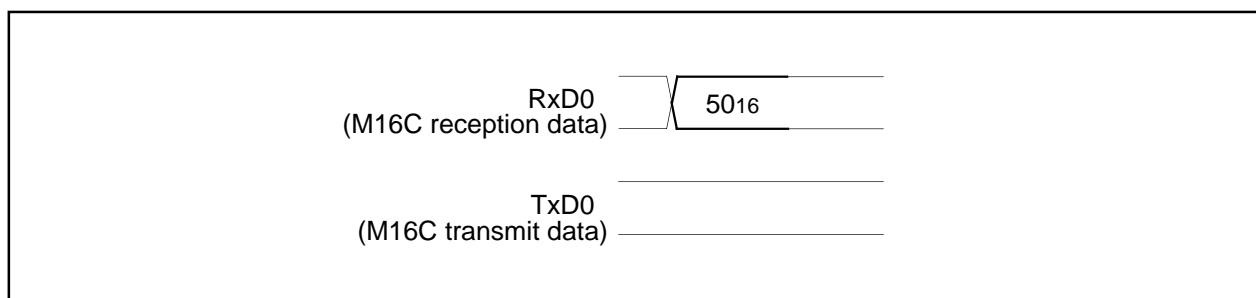


Figure 1.122. Timing for clearing the status register

**Page Program Command**

This command writes the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page program command as explained here following.

- (1) Transfer the “4116” command code with the 1st byte.
- (2) Transfer addresses A<sub>8</sub> to A<sub>15</sub> and A<sub>16</sub> to A<sub>23</sub> with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, as write data (D<sub>0</sub>–D<sub>7</sub>) for the page (256 bytes) specified with addresses A<sub>8</sub> to A<sub>23</sub> is input sequentially from the smallest address first, that page is automatically written.

When reception setup for the next 256 bytes ends, the RTS<sub>1</sub> (BUSY) signal changes from the “H” to the “L” level. The result of the page program can be known by reading the status register. For more information, see the section on the status register.

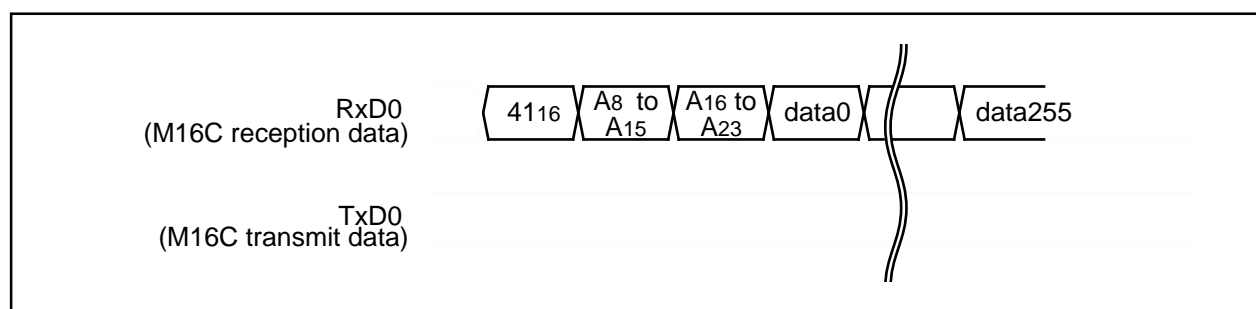


Figure 1.123. Timing for the page program

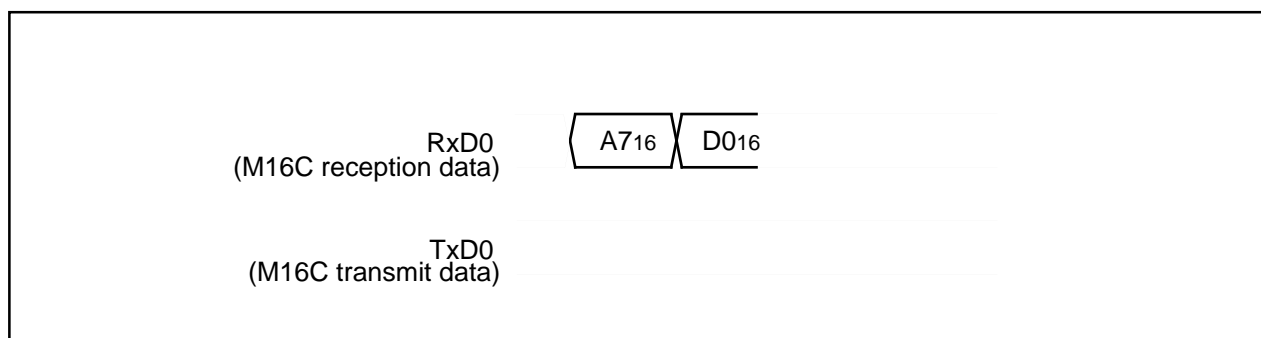
## Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

**Erase All Unlocked Blocks Command**

This command erases the content of all blocks. Execute the erase all unlocked blocks command as explained here following.

- (1) Transfer the "A7<sub>16</sub>" command code with the 1st byte.
- (2) Transfer the verify command code "D0<sub>16</sub>" with the 2nd byte. With the verify command code, the erase operation will start and continue for all blocks in the flash memory.

When block erasing ends, the RTS<sub>1</sub> (BUSY) signal changes from the "H" to the "L" level. The result of the erase operation can be known by reading the status register.



**Figure 1.124. Timing for erasing all unlocked blocks**

## Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

**Read Lock Bit Status Command**

This command reads the lock bit status of the specified block. Execute the read lock bit status command as explained here following.

- (1) Transfer the "7116" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) The lock bit data of the specified block is output with the 4th byte. Write the highest address of the specified block for addresses A8 to A23.

The M30201 (flash memory version) does not have the lock bit, so the read value is always "1" (block unlock).

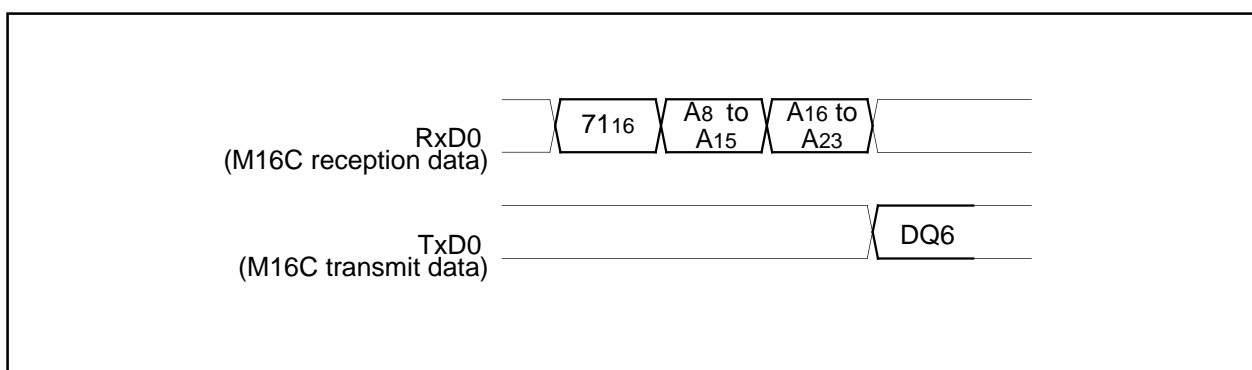


Figure 1.125. Timing for reading lock bit status

**Download Command**

This command downloads a program to the RAM for execution. Execute the download command as explained here following.

- (1) Transfer the "FA16" command code with the 1st byte.
- (2) Transfer the program size with the 2nd and 3rd bytes.
- (3) Transfer the check sum with the 4th byte. The check sum is added to all data sent with the 5th byte onward.
- (4) The program to execute is sent with the 5th byte onward.

When all data has been transmitted, if the check sum matches, the downloaded program is executed. The size of the program will vary according to the internal RAM.

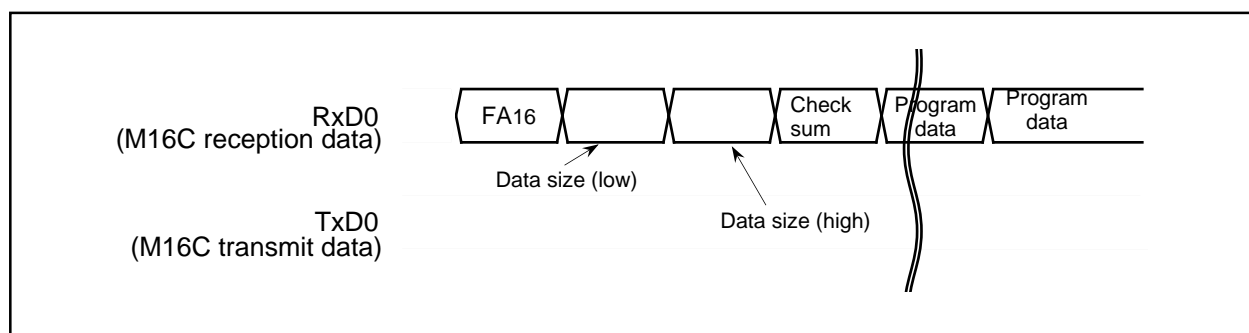


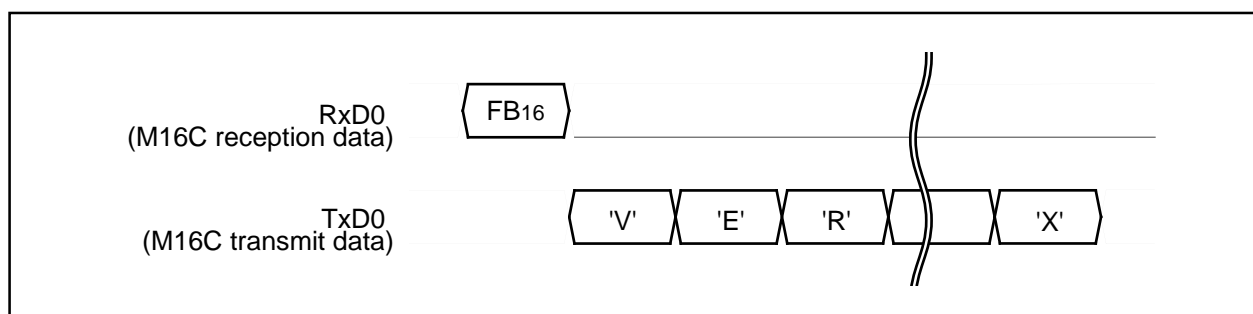
Figure 1.126. Timing for download

## Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

**Version Information Output Command**

This command outputs the version information of the control program stored in the boot area. Execute the version information output command as explained here following.

- (1) Transfer the "FB16" command code with the 1st byte.
- (2) The version information will be output from the 2nd byte onward. This data is composed of 8 ASCII code characters.

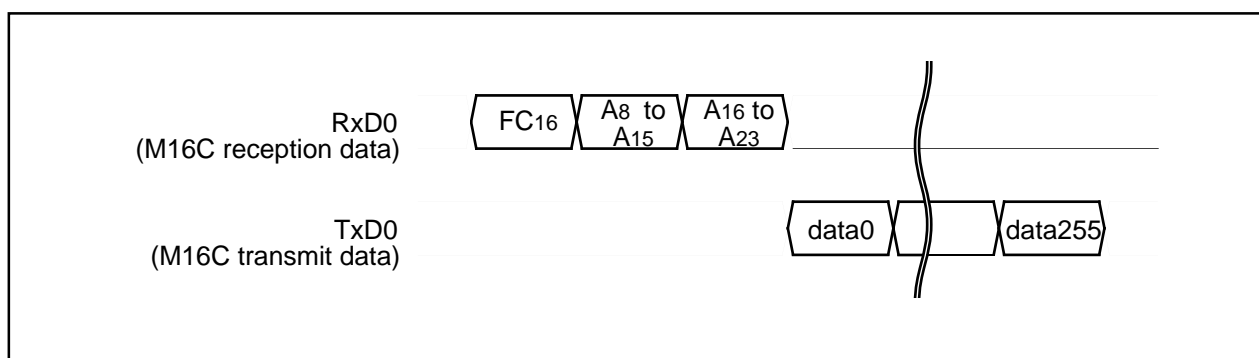


**Figure 1.127. Timing for version information output**

**Boot ROM Area Output Command**

This command outputs the control program stored in the boot ROM area in one page blocks (256 bytes). Execute the boot ROM area output command as explained here following.

- (1) Transfer the "FC16" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, data (D0–D7) for the page (256 bytes) specified with addresses A8 to A23 will be output sequentially from the smallest address first.



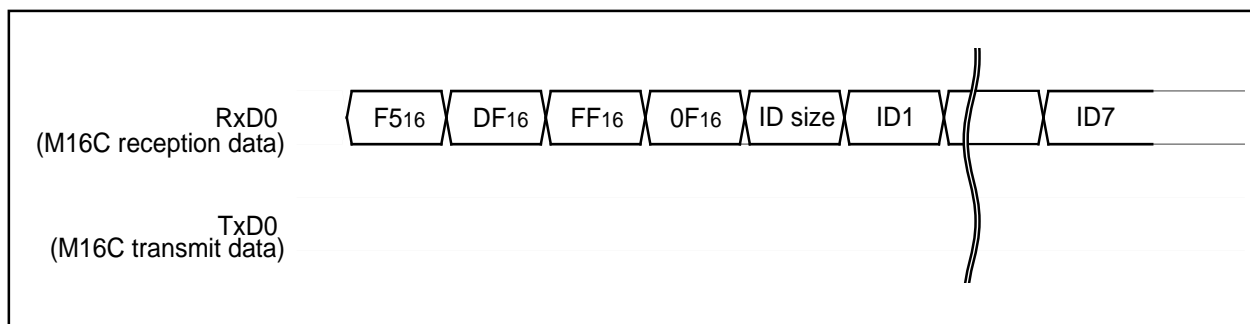
**Figure 1.128. Timing for boot ROM area output**

## Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

**ID Check**

This command checks the ID code. Execute the boot ID check command as explained here following.

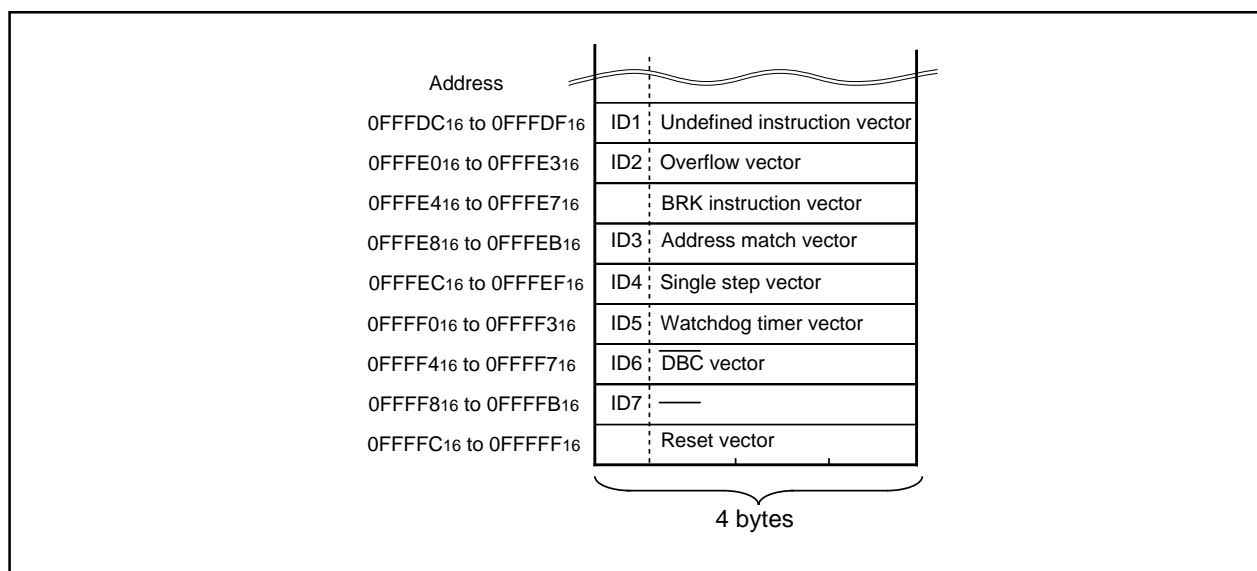
- (1) Transfer the "F5<sub>16</sub>" command code with the 1st byte.
- (2) Transfer addresses A0 to A7, A8 to A15 and A16 to A23 of the 1st byte of the ID code with the 2nd, 3rd and 4th bytes respectively.
- (3) Transfer the number of data sets of the ID code with the 5th byte.
- (4) The ID code is sent with the 6th byte onward, starting with the 1st byte of the code.



**Figure 1.129. Timing for the ID check**

**ID Code**

When the flash memory is not blank, the ID code sent from the peripheral units and the ID code written in the flash memory are compared to see if they match. If the codes do not match, the command sent from the peripheral units is not accepted. An ID code contains 8 bits of data. Area is, from the 1st byte, addresses 0FFFD<sub>16</sub>, 0FFFE<sub>316</sub>, 0FFFE<sub>B16</sub>, 0FFFE<sub>F16</sub>, 0FFFF<sub>316</sub>, 0FFFF<sub>716</sub> and 0FFFF<sub>B16</sub>. Write a program into the flash memory, which already has the ID code set for these addresses.



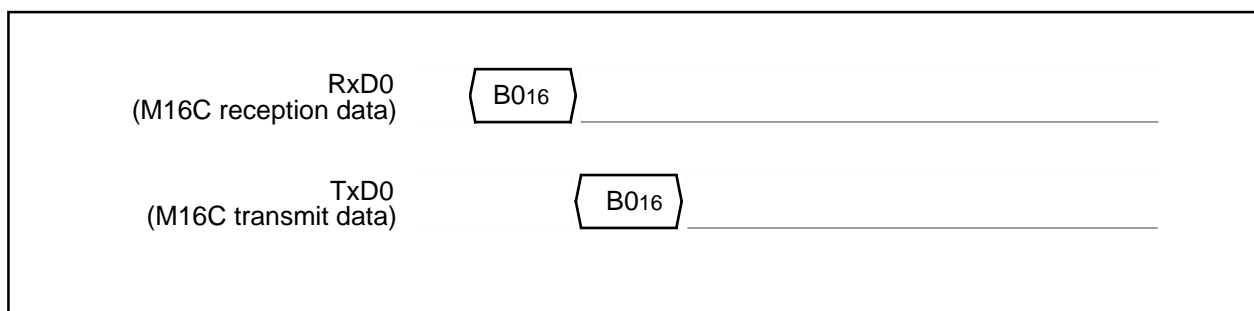
**Figure 1.130. ID code storage addresses**

## Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

**Baud Rate 9600**

This command changes baud rate to 9,600 bps. Execute it as follows.

- (1) Transfer the "B016" command code with the 1st byte.
- (2) After the "B016" check code is output with the 2nd byte, change the baud rate to 9,600 bps.



**Figure 1.131. Timing of baud rate 9600**

## Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

**Baud Rate 19200**

This command changes baud rate to 19,200 bps. Execute it as follows.

- (1) Transfer the "B116" command code with the 1st byte.
- (2) After the "B116" check code is output with the 2nd byte, change the baud rate to 19,200 bps.

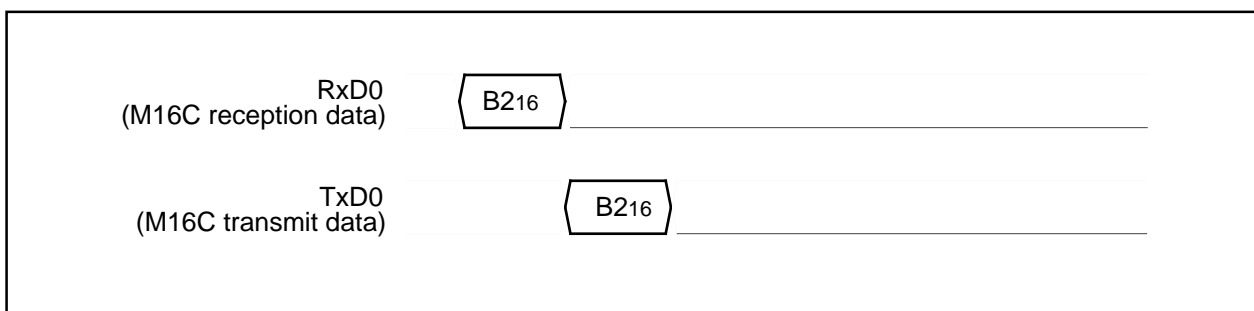


**Figure 1.132. Timing of baud rate 19200**

**Baud Rate 38400**

This command changes baud rate to 38,400 bps. Execute it as follows.

- (1) Transfer the "B216" command code with the 1st byte.
- (2) After the "B216" check code is output with the 2nd byte, change the baud rate to 38,400 bps.

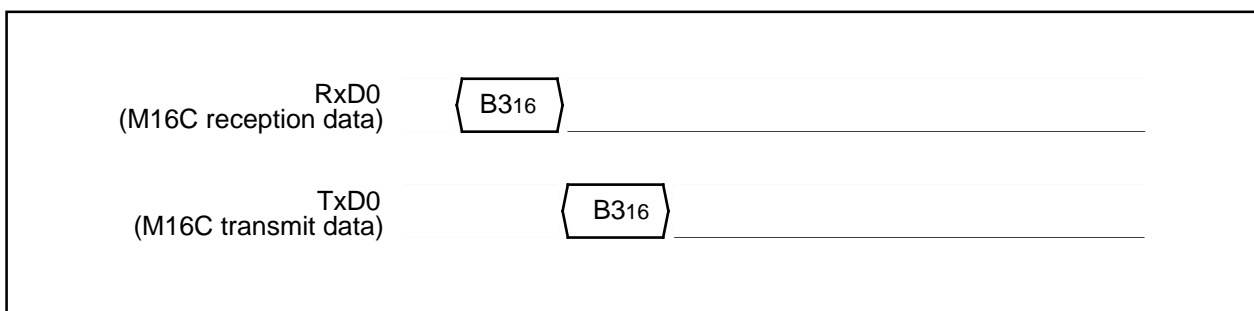


**Figure 1.133. Timing of baud rate 38400**

**Baud Rate 57600**

This command changes baud rate to 57,600 bps. Execute it as follows.

- (1) Transfer the "B316" command code with the 1st byte.
- (2) After the "B316" check code is output with the 2nd byte, change the baud rate to 57,600 bps.



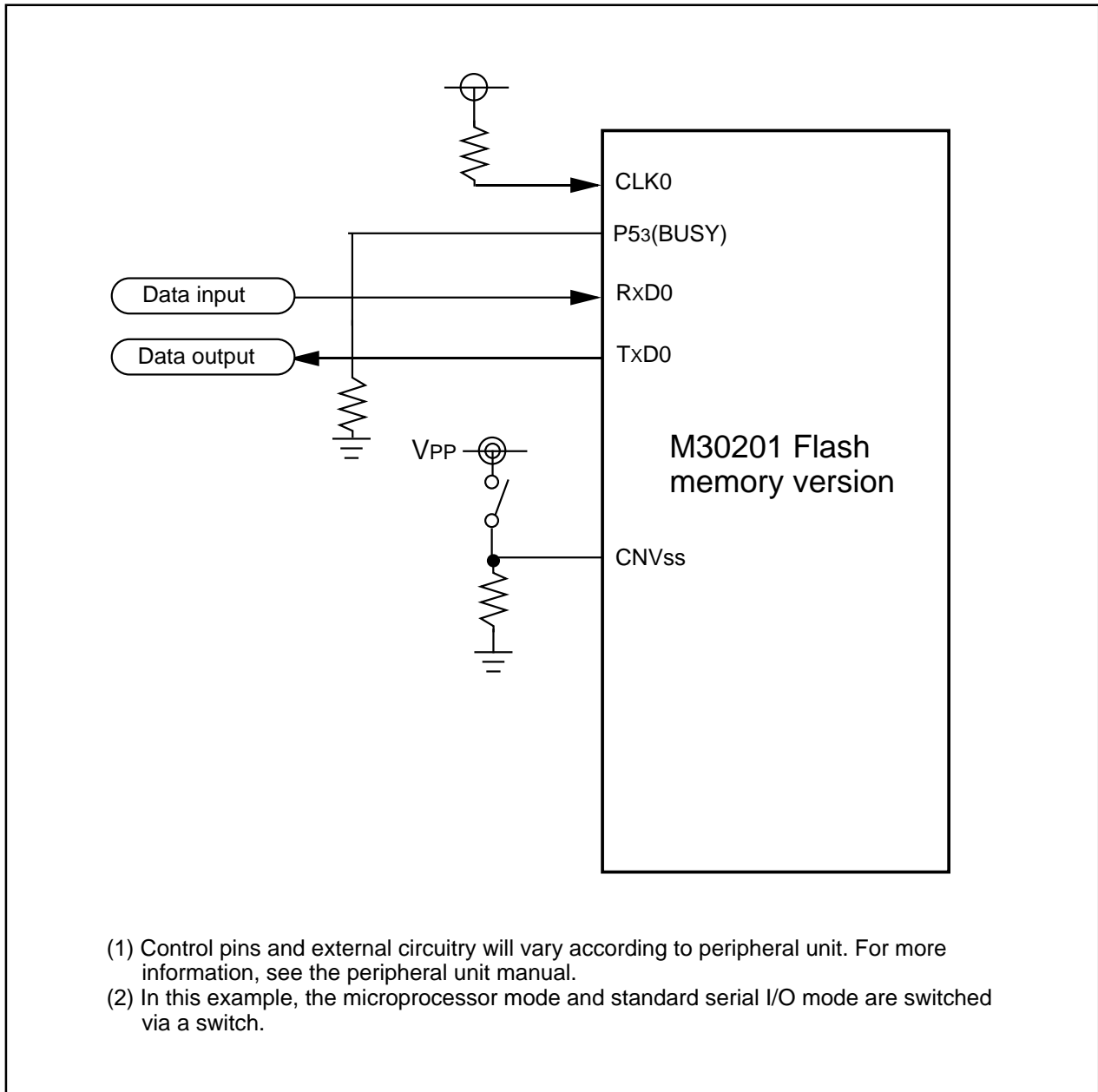
**Figure 1.134. Timing of baud rate 57600**



## Appendix Standard Serial I/O Mode 2 (Flash Memory Version)

**Example Circuit Application for The Standard Serial I/O Mode 2**

The below figure shows a circuit application for the standard serial I/O mode 2.



**Figure 1.135. Example circuit application for the standard serial I/O mode 2**

## Revision History

| Version          | Contents for change   | Revision date           |
|------------------|---|-------------------------|
| REV.E            | <p>Pages 1, 5<br/>internal interrupt 9 -&gt;13</p> <p>Pages 1, 5<br/>2.7 to 5.5V (f(XIN)=<u>7MHz with software one-wait</u>):mask ROM version<br/>-&gt;2.7 to 5.5V (f(XIN)=<u>3.5MHz</u>):mask ROM version</p> <p>Page 5<br/>Power consumption <u>18mA</u> (f(XIN)=<u>7MHz</u> with software one-wait, VCC=3V)<br/>-&gt;<u>11mA</u> (f(XIN)=<u>3.5MHz</u> , VCC=3V)</p> <p>Page 6<br/>M30201M2-XXXSP/FP, M30201M2T-XXXSP/FP -&gt;Delete<br/>M30201M4T-XXXSP, M30201F6T-XXXSP -&gt;Delete<br/>M30201M6-XXXFP, M30201M6T-XXXFP -&gt;Addition</p> <p>Pages 9, 10<br/>Figures 1.7 and 1.8 are partly revised.</p> <p>Page 14<br/>Figure 1.11 is partly revised.</p> <p>Page 16<br/>Figure 1.14 is partly revised (Bit 7 of the processor mode register 1).<br/>Wait bit -&gt;Reserved bit</p> <p>Page 17<br/><del>Software wait</del></p> <p>Page 20<br/>Figure 1.18 is partly revised (Note 8 is partly revised).</p> <p>Page 21<br/>Figure 1.19 is partly revised (n=0716 : approx. <u>16.5kHz</u> -&gt; <u>19.5kHz</u>).</p> <p>Page 33<br/>Figure 1.24 is partly revised (Note 2 is added).</p> <p>Page 49<br/>Figure 1.39 is partly revised.</p> <p>Page 77<br/>Figure 1.72 is partly revised (UARTi transmit/receive mode register).</p> <p>Page 78<br/>Figure 1.73 is partly revised.</p> <p>Page 80<br/>Figure 1.74 is partly revised.</p> <p>Page 85<br/>Figure 1.79 is partly revised.</p> <p>Pages 90 to 96<br/>Figures 1.83 to 1.89 are partly revised.</p> <p>Pages 110 to 113, 118 to 122<br/>Tables 1.36 to 1.39 and 1.56 to 1.71 are partly revised.</p> <p>Page 124<br/>Table 1.74 is partly revised (Boot ROM area <u>4 K</u> bytes -&gt; <u>3.5 K</u> bytes) .</p> <p>Page 142 to 168<br/>Standard serial I/O mode 2 is added.</p> | 01.4.12                 |
| Revision history |   | M30201 Group data sheet |

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