ACPL-267XL, ACPL-268KL, ACPL-560XL, ACPL-563XL, 5962-08242*

Hermetically Sealed, 3.3V High Speed, High CMR, Logic Gate Optocouplers

Data Sheet

*See Selection Guide for full matrix of part numbers.

Description

These units are single and dual channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard commercial product or with full MIL-PRF-38534 Class Level H or K testing or from DLA Drawing 5962-08242. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DLA Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

Truth Table (Positive Logic)

Multichannel Devices

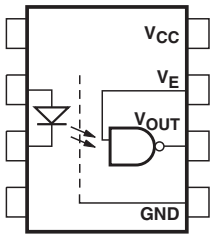
Input	Output
On (H)	L
Off (L)	H

Single Channel DIP

Input	Enable	Output
On (H)	H	L
Off (L)	H	H
On (H)	L	H
Off (L)	L	H

Functional Diagram

Multiple channel devices available



The connection of a 0.1 µF bypass capacitor between V_{CC} and GND is recommended.

Features

- Low power consumption
- 3.3V supply voltages
- Dual marked with device part number and DLA drawing number
- Manufactured and tested on a MIL-PRF-38534 Certified Line
- QML-38534, Class H and K
- Three hermetically sealed package configurations
- Performance guaranteed over full military temperature range: -55°C to +125°C
- High speed: 10 Mbd typical
- CMR: > 10,000 V/µs typical
- 1500 Vdc withstand test voltage
- TTL circuit compatibility
- HCPL-260L/060L/263L/063L function compatibility

Applications

- Military and aerospace
- High reliability systems
- Transportation, medical, and life critical systems
- Line receiver
- Voltage level shifting
- Isolated input line receiver
- Isolated output line driver
- Logic ground isolation
- Harsh industrial environments
- Isolation for computer, communication, and test equipment systems

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Each channel contains a GaAsP light emitting diode which is optically coupled to an integrated high speed photon detector. The output of the detector is an open collector Schottky clamped transistor. Internal shields provide a guaranteed common mode transient immunity specification of 1000 V/µs. Package styles for these parts are 8 and 16 pin DIP through hole (case outlines P and E respectively). Devices may be purchased with a variety of lead bend and plating options. See Selection Guide Table for details. Standard Microcircuit Drawing (SMD) parts are available for each package and lead style.

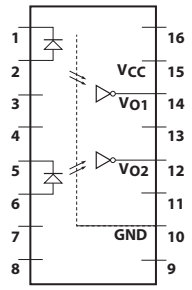
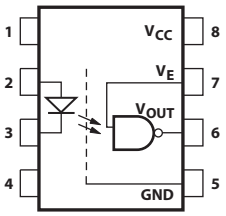
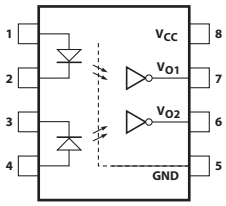
Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are identical for all parts. Occasional exceptions exist due to package variations and limitations, and are as noted. Additionally, the same package assembly processes and materials are used in all devices.

Selection Guide – Package Styles and Lead Configuration Options

Package	**16 Pin DIP**	**8 Pin DIP**	**8 Pin DIP**
Lead Style	Through Hole	Through Hole	Through Hole
Channels	2	1	2
Common Channel Wiring	VCC, GND	None	VCC, GND
Withstand Test Voltage	1500 Vdc	1500 Vdc	1500 Vdc
Avago Part # & Options			
Standard Commercial	ACPL-2670L	ACPL-5600L	ACPL-5630L
MIL-PRF-38534, Class H	ACPL-2672L	ACPL-5601L	ACPL-5631L
MIL-PRF-38534, Class K	ACPL-268KL	ACPL-560KL	ACPL-563KL
Standard Lead Finish	Gold Plate	Gold Plate	Gold Plate
Solder Dipped*	Option -200	Option -200	Option -200
Butt Cut/Gold Plate	Option -100	Option -100	Option -100
Gull Wing/Soldered*	Option -300	Option -300	Option -300
Class H SMD Part #			
Prescript for all below	*5962-*	*5962-*	*5962-*
Gold Plate	0824203HEC	0824201HPC	0824202HPC
Solder Dipped*	0824203HEA	0824201HPA	0824202HPA
Butt Cut/Gold Plate	0824203HUC	0824201HYC	0824202HYC
Butt Cut/Soldered*	0824203HUA	0824201HYA	0824202HYA
Gull Wing/Soldered*	0824203HTA	0824201HXA	0824202HXA
Class K SMD Part #			
Prescript for all below	*5962-*	*5962-*	*5962-*
Gold Plate	0824203KEC	0824201KPC	0824202KPC
Solder Dipped*	0824203KEA	0824201KPA	0824202KPA
Butt Cut/Gold Plate	0824203KUC	0824201KYC	0824202KYC
Butt Cut/Soldered*	0824203KUA	0824201KYA	0824202KYA
Gull Wing/Soldered*	0824203KTA	0824201KXA	0824202KXA

* Solder contains lead.

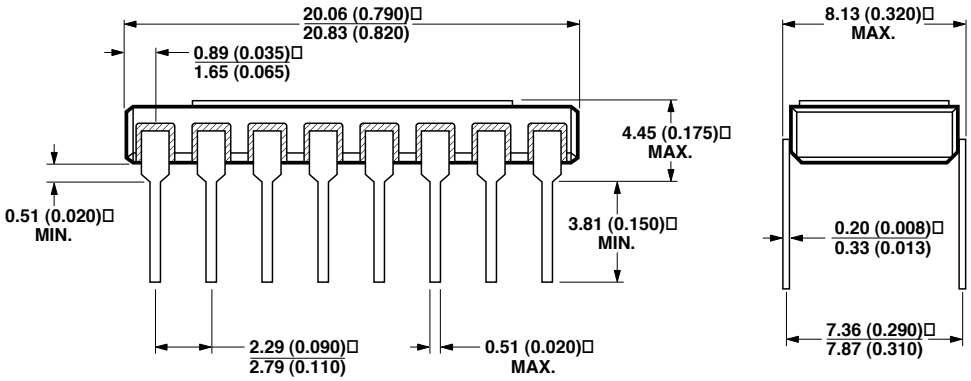
Functional Diagrams

16 Pin DIP	8 Pin DIP	8 Pin DIP
Through Hole	Through Hole	Through Hole
2 Channels	1 Channel	2 Channels
		

Note: Dual channel devices have common V_{CC} and ground. Single channel DIP has an enable pin 7. All diagrams are "top view."

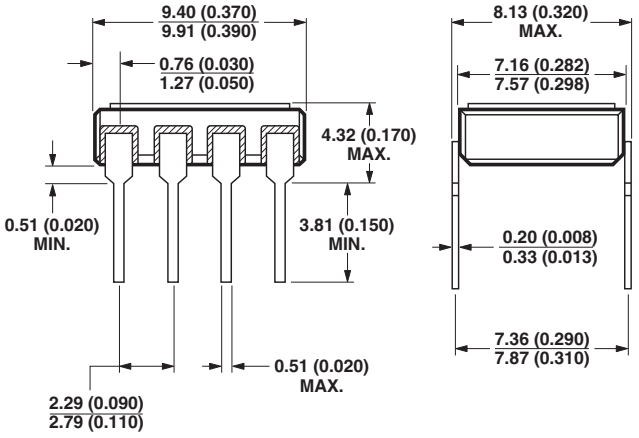
Outline Drawings

16 Pin DIP Through Hole, 2 Channels



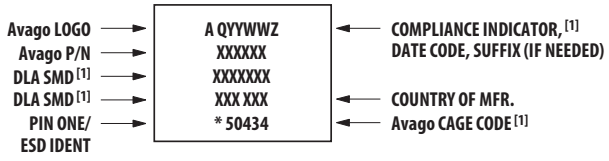
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

8 Pin DIP Through Hole, 1 and 2 Channels



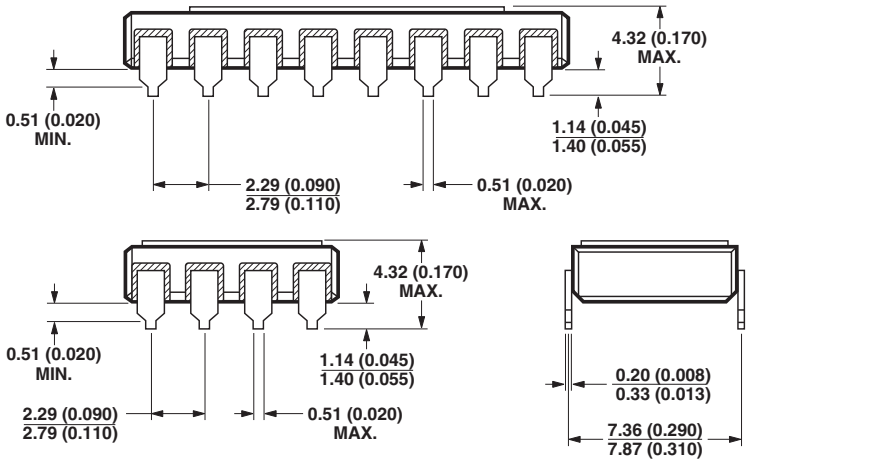
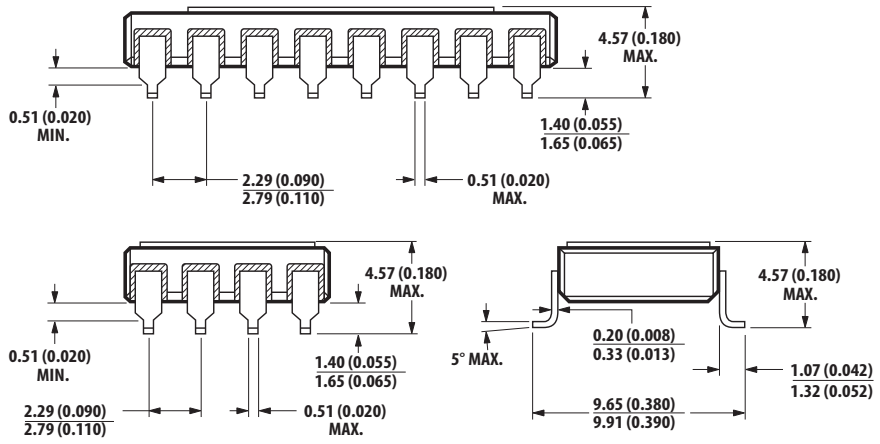
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Device Marking



Note 1. Qualified parts only

Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on standard commercial, class H & class K product in 8 and 16 pin DIP (see drawings below for details).  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
200	Lead finish is solder dipped rather than gold plated. This option is available on standard commercial, class H and class K products in 8 and 16 pin DIP. DLA Drawing part numbers contain provisions for lead finish.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on standard commercial, class H & class K product in 8 and 16 pin DIP (see drawings below for details). This option has solder dipped leads.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Solder contains lead.

Absolute Maximum Ratings

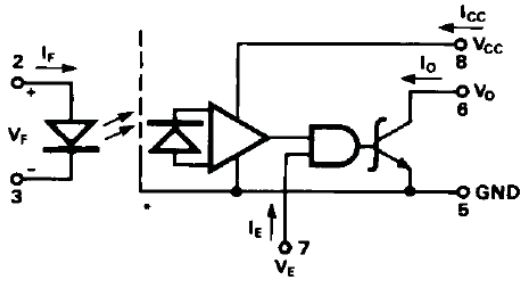
No derating required up to +125°C.

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-65	+150	°C
Operating Temperature	T_A	-55	+125	°C
Case Temperature	T_C		+170	°C
Junction Temperature	T_J		+175	°C
Lead Solder Temperature			260 for 10 sec	°C
Peak Forward Input Current (each channel, ≤1 ms duration)	$I_{F(PEAK)}$		40	mA
Average Input Forward Current (each channel)	$I_{F(AVG)}$		20	mA
Input Power Dissipation (each channel)			35	mW
Reverse Input Voltage (each channel	V_R		5	V
Supply Voltage (1 minute maximum)	V_{CC}		7.0	V
Output Current (each channel)	I_O		25	mA
Output Voltage (each channel)	V_O		7	V
Output Power Dissipation (each channel)	P_O		40	mW
Package Power Dissipation (each channel)	P_D		200	mW

Single Channel Product Only

Enable Input Voltage	V_E		3.6	V

8 Pin Ceramic DIP Single Channel Schematic



Note enable pin 7. An external 0.01 µF to 0.1 µF bypass capacitor must be connected between V_{CC} and ground for each package type.

ESD Classification

MIL-PRF-38534 and MIL-STD-883, Method 3015

ACPL-560L/01L/0KL, 5962-0824201	(▲B), Class 1B
ACPL-5630L/31L/3KL, 5962-0824202	(▲▲▲A), Class 3A
ACPL-2670L/72L/268KL, 5962-0824203	(▲▲), Class 2

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level, Each Channel	I_{FL}	0	250	µA
Input Current, High Level, Each Channel	I_{FH}	10	20	mA
Supply Voltage, Output	V_{CC}	3.0	3.6	V
Fan Out (TTL Load) Each Channel	N		6	

Recommended Operating Conditions (cont'd.)

Single Channel Product Only[10]

Parameter	Symbol	Min.	Max.	Units
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V

Electrical Characteristics (T_A = -55°C to +125°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Group A[13] Sub-groups	Limits Min.	Limits Typ.*	Limits Max.	Units	Fig.	Note
High Level Output Current		I_{OH}	V_{CC} = 3.3 V, V_O = 3.3 V, I_F = 250 µA	1, 2, 3		6	250	µA	1	1
Low Level Output Voltage		V_{OL}	V_{CC} = 3.3 V, I_F = 10 mA, I_{OL} (Sinking) = 10 mA	1, 2, 3		0.3	0.6	V	2	1, 8
Current Transfer Ratio		h_F CTR	V_O = 0.6 V, I_F = 10 mA, V_{CC} = 3.3 V	1, 2, 3	100			%		1
Logic High Supply Current	Single Channel	I_{CCH}	V_{CC} = 3.3 V, I_F = 0 mA	1, 2, 3		5	11	mA		1
	Dual Channel		V_{CC} = 3.3 V, I_{F1} = I_{F2} = 0 mA			10	22	mA		
Logic low Supply Current	Single Channel	I_{CCL}	V_{CC} = 3.3 V, I_F = 20 mA	1, 2, 3		6	15	mA		1
	Dual Channel		V_{CC} = 3.3 V, I_{F1} = I_{F2} = 20 mA			12	30	mA		
Input Forward Voltage		V_F	I_F = 20 mA	1, 2		1.55	1.75	V	3	1
				3			1.85			
Input Reverse Breakdown Voltage		BV_R	I_R = 10 µA	1, 2, 3	5			V		1
Input-Output Leakage Current		I_{I-O}	RH ≤ 65%, T_A = 25°C t = 5 s, V_{I-O} = 1500 Vdc	1			1.0	µA		2, 7
Capacitance Between Input/ Output		C_{I-O}	f = 1 MHz, T_C = 25°C	4		1.0	4.0	pF		1, 3, 13

*All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Electrical Characteristics (cont'd) T_A = -55°C to +125°C unless otherwise specified

Parameter	Symbol	Test Conditions	Group A[13] Subgroups	Limits Min.	Limits Typ.*	Limits Max.	Units	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	V_{CC} = 3.3 V, R_L = 510 Ω, C_L = 50 pF, I_F = 13 mA	9		43	100	ns	4, 5, 6	1, 5
			10, 11			140			
Propagation Delay Time to Low Output Level	t_{PHL}		9		54	100	ns		
			10, 11			120			
Output Rise Time	t_{LH}	R_L = 510 Ω, C_L = 50 pF, I_F = 13 mA	9, 10, 11		20	90	ns		1
Output Fall Time	t_{HL}				8	40			
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	V_{CM} = 50 V (PEAK), V_{CC} = 3.3 V, V_O (min.) = 2 V, R_L = 510 Ω, I_F = 0 mA	9, 10, 11	1000	>10000		V/µs	7	1, 6, 13
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	V_{CM} = 50 V (PEAK), V_{CC} = 3.3 V, V_O (max.) = 0.8 V, R_L = 510 Ω, I_F = 10 mA	9, 10, 11	1000	>10000		V/µs	7	1, 6, 13
Single Channel Product Only									
Low Level Enable Current	I_{EL}	V_{CC} = 3.3 V, V_E = 0.5 V	1, 2, 3	-2.0	-0.54		mA		
High Level Enable Voltage	V_{EH}		1, 2, 3	2.0			V		9
Low Level Enable Voltage	V_{EL}		1, 2, 3			0.8	V		

*All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Typical Characteristics, T_A = 25°C, V_{CC} = 3.3 V

Parameter	Sym.	Typ.	Units	Test Conditions	Fig.	Note
Input Capacitance	C_{IN}	60	pF	V_F = 0 V, f = 1 MHz		1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	-1.5	mV/°C	I_F = 20 mA		1
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 V		2
Single Channel Product Only						
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	32	ns	R_L = 510 Ω, C_L = 50 pF, I_F = 13 mA, V_{EH} = 3 V, V_{EL} = 0V	8, 9	1, 10
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	28	ns			1, 11
Dual Channel Product Only						
Input-Input Leakage Current	I_{I-I}	0.5	nA	Relative Humidity ≤ 65% V_{I-I} = 500 V, t = 5 s		4
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	V_{I-I} = 500 V		4
Capacitance (Input-Input)	C_{I-I}	0.55	pF	f = 1 MHz		4

Notes:

1. Each channel.
2. All devices are considered two-terminal devices; I_{I-O} is measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
3. Measured between each input pair shorted together and all output connections for that channel shorted together.
4. Measured between adjacent input pairs shorted together for each multichannel device.
5. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8$ V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0$ V).
7. This is a momentary withstand test, not an operating condition.
8. It is essential that a bypass capacitor (0.01 to 0.1 µF, ceramic) be connected from V_{CC} to ground. Total lead length between both ends of this external capacitor and the isolator connections should not exceed 20 mm.
9. No external pull up is required for a high logic state on the enable input.
10. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
11. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
12. Standard commercial parts receive 100% testing at 25°C (Subgroups 1 and 9). Class H and K parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
13. Parameters are tested as part of device initial characterization and after design and process changes. Parameters are guaranteed to limits specified for all lots not specifically tested.

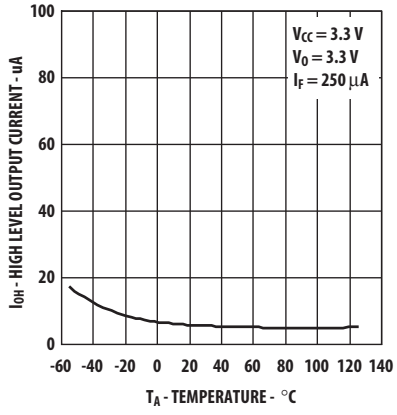


Figure 1. High Level Output Current vs. Temperature.

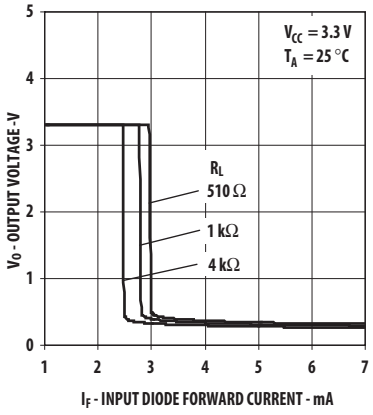


Figure 2. Input-Output Characteristics.

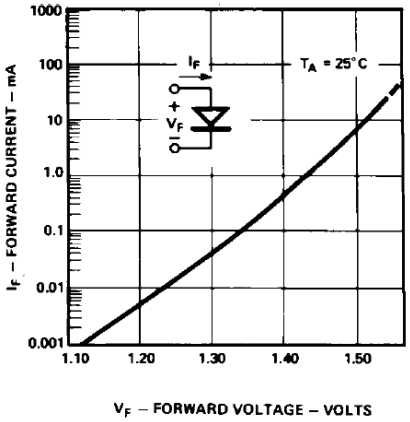


Figure 3. Input Diode Forward Characteristics.

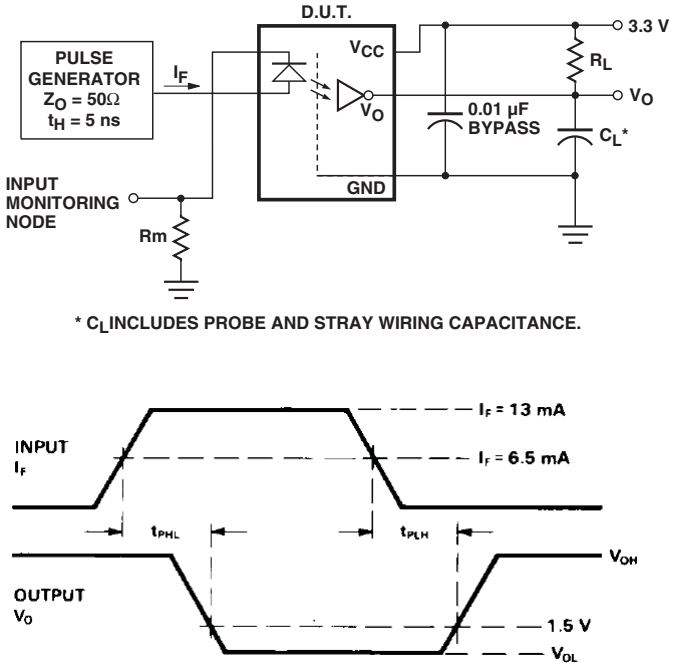


Figure 4. Test Circuit for t_{PHL} and t_{PLH}*.

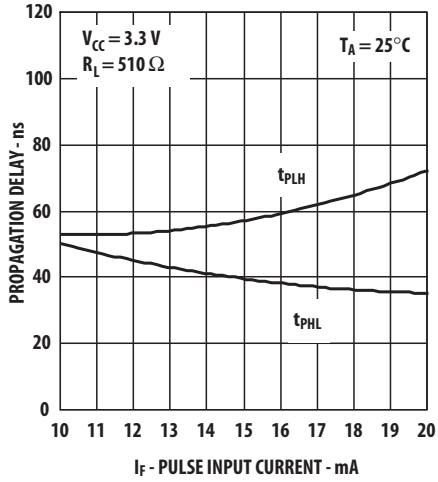


Figure 5. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}.

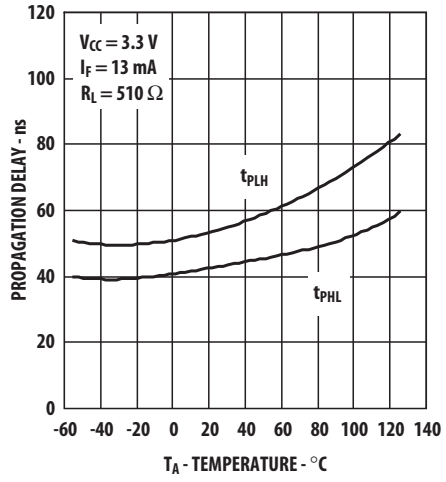


Figure 6. Propagation Delay vs. Temperature.

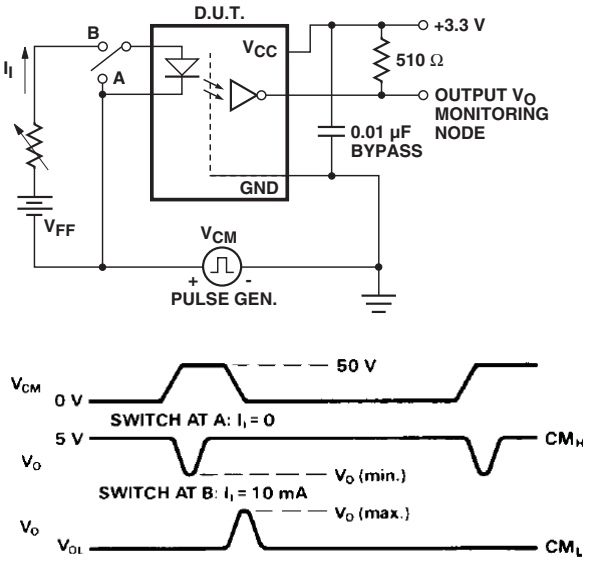


Figure 7. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

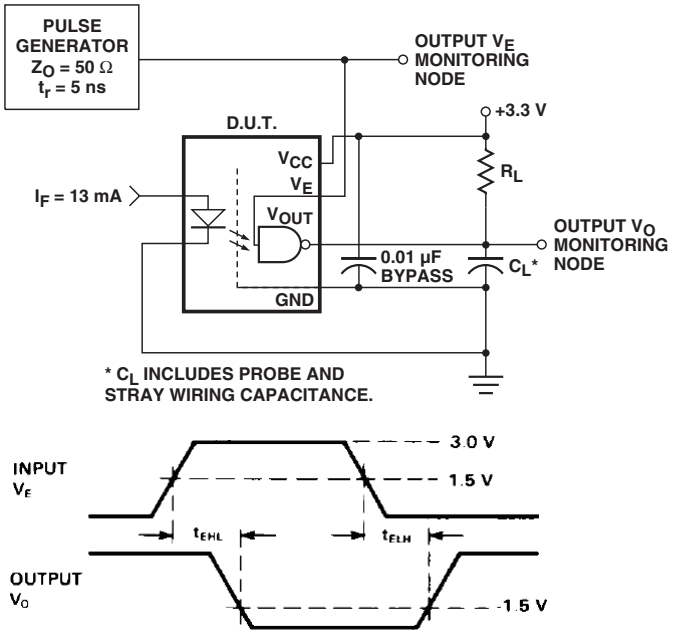


Figure 8. Test Circuit for t_{EHL} and t_{ELH}.

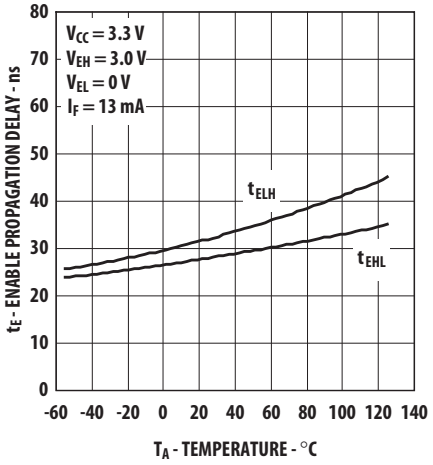


Figure 9. Enable Propagation Delay vs. Temperature.

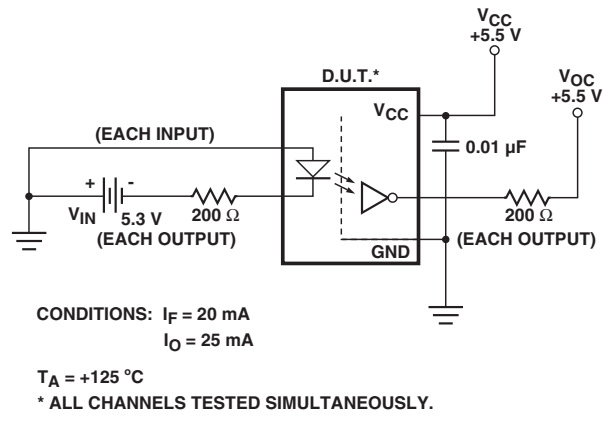


Figure 10. Operating Circuit for Burn-In and Steady State Life Tests.

MIL-PRF-38534 Class H, Class K, and DLA SMD Test Program

Avago's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Classes H and K. Class H and Class K devices are also in compliance with DLA drawing 5962-08242.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

AV02-1327EN - October 2, 2012

Стандарт Электрон Связь

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