

CD54AC273, CD74AC273 CD54ACT273, CD74ACT273

August 1998 - Revised July 2002

Octal D Flip-Flop with Reset

Features

- Buffered Inputs
- Typical Propagation Delay
 - 6.5ns at $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 50pF$
- Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption
- Balanced Propagation Delays
- AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply
- $\pm 24mA$ Output Drive Current
 - Fanout to 15 FAST™ ICs
 - Drives 50 Ω Transmission Lines

Pinout

CD54AC273, CD54ACT273
(CDIP)
CD74AC273, CD74ACT273
(PDIP, SOIC)
TOP VIEW



Description

The 'AC273 and 'ACT273 devices are octal D-type flip-flops with reset that utilize advanced CMOS logic technology. Information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. All eight flip-flops are controlled by a common clock (CP) and a common reset (\overline{MR}). Resetting is accomplished by a low voltage level independent of the clock.

Ordering Information

| PART NUMBER | TEMPERATURE RANGE | PACKAGE |
|---------------|--|------------|
| CD74AC273E | 0°C to 70°C -40°C to 85°C -55°C to 125°C | 20 Ld PDIP |
| CD54AC273F3A | -55°C to 125°C | 20 Ld CDIP |
| CD74ACT273E | 0°C to 70°C -40°C to 85°C -55°C to 125°C | 20 Ld PDIP |
| CD54ACT273F3A | -55°C to 125°C | 20 Ld CDIP |
| CD74AC273M | 0°C to 70°C -40°C to 85°C -55°C to 125°C | 20 Ld SOIC |
| CD74ACT273M | 0°C to 70°C -40°C to 85°C -55°C to 125°C | 20 Ld SOIC |

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office for ordering information.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram



TRUTH TABLE

| INPUTS | | | OUTPUTS |
|------------|----------|---------|---------|
| RESET (MR) | CLOCK CP | DATA Dn | Qn |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | Q0 |

H = High level (steady state), L = Low level (steady state), X = Irrelevant, ↑ = Transition from Low to High level, Q0 = The level of Q before the indicated steady-state input conditions were established.

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Absolute Maximum Ratings

| | |
|---|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 6V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 50mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 50mA$ |
| DC V_{CC} or Ground Current, I_{CC} or I_{GND} (Note 3) | $\pm 100mA$ |

Thermal Information

| | |
|--|----------------|
| Thermal Resistance, θ_{JA} (Typical, Note 5) | |
| E Package | 69°C/W |
| M Package | 58°C/W |
| Maximum Junction Temperature (Plastic Package) | 150°C |
| Maximum Storage Temperature Range | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C |

Operating Conditions

| | |
|---|----------------|
| Temperature Range, T_A | -55°C to 125°C |
| Supply Voltage Range, V_{CC} (Note 4) | |
| AC Types | 1.5V to 5.5V |
| ACT Types | 4.5V to 5.5V |
| DC Input or Output Voltage, V_I , V_O | 0V to V_{CC} |
| Input Rise and Fall Slew Rate, dt/dv | |
| AC Types, 1.5V to 3V | 50ns (Max) |
| AC Types, 3.6V to 5.5V | 20ns (Max) |
| ACT Types, 4.5V to 5.5V | 10ns (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. For up to 4 outputs per device, add $\pm 25mA$ for each additional output.
4. Unless otherwise specified, all voltages are referenced to ground.
5. The package thermal impedance is calculated in accordance with JESD 51.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS | |
|---------------------------|----------|----------------------|--------------------|--------------------|------|------|------------------|------|-------------------|------|-------|---|
| | | V_I (V) | I_O (mA) | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| AC TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 1.5 | 1.2 | - | 1.2 | - | 1.2 | - | V | |
| | | | | 3 | 2.1 | - | 2.1 | - | 2.1 | - | V | |
| | | | | 5.5 | 3.85 | - | 3.85 | - | 3.85 | - | V | |
| Low Level Input Voltage | V_{IL} | - | - | 1.5 | - | 0.3 | - | 0.3 | - | 0.3 | V | |
| | | | | 3 | - | 0.9 | - | 0.9 | - | 0.9 | V | |
| | | | | 5.5 | - | 1.65 | - | 1.65 | - | 1.65 | V | |
| High Level Output Voltage | V_{OH} | V_{IH} or V_{IL} | -0.05 | -0.05 | 1.5 | 1.4 | - | 1.4 | - | 1.4 | - | V |
| | | | -0.05 | -0.05 | 3 | 2.9 | - | 2.9 | - | 2.9 | - | V |
| | | | -0.05 | -0.05 | 4.5 | 4.4 | - | 4.4 | - | 4.4 | - | V |
| | | | -4 | -4 | 3 | 2.58 | - | 2.48 | - | 2.4 | - | V |
| | | | -24 | -24 | 4.5 | 3.94 | - | 3.8 | - | 3.7 | - | V |
| | | | -75 (Note 6, 7) | -75 (Note 6, 7) | 5.5 | - | - | 3.85 | - | - | - | V |
| | | | -50 (Note 6, 7) | -50 (Note 6, 7) | 5.5 | - | - | - | - | 3.85 | - | V |

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DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS | | |
|---|------------------|------------------------------------|---------------------|---------------------|------|------|---------------|------|----------------|------|-------|------|---|
| | | V _I (V) | I _O (mA) | | MIN | MAX | MIN | MAX | MIN | MAX | | | |
| Low Level Output Voltage | V _{OL} | V _{IH} or V _{IL} | 0.05 | 1.5 | - | 0.1 | - | 0.1 | - | 0.1 | V | | |
| | | | 0.05 | 3 | - | 0.1 | - | 0.1 | - | 0.1 | V | | |
| | | | 0.05 | 4.5 | - | 0.1 | - | 0.1 | - | 0.1 | V | | |
| | | | 12 | 3 | - | 0.36 | - | 0.44 | - | 0.5 | V | | |
| | | | 24 | 4.5 | - | 0.36 | - | 0.44 | - | 0.5 | V | | |
| | | | 75 (Note 6, 7) | 5.5 | - | - | - | 1.65 | - | - | V | | |
| | | | 50 (Note 6, 7) | 5.5 | - | - | - | - | - | 1.65 | V | | |
| Input Leakage Current | I _I | V _{CC} or GND | - | 5.5 | - | ±0.1 | - | ±1 | - | ±1 | µA | | |
| Quiescent Supply Current MSI | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | 8 | - | 80 | - | 160 | µA | | |
| ACT TYPES | | | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | 2 | - | 2 | - | V | | |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | 0.8 | - | 0.8 | - | 0.8 | V | | |
| High Level Output Voltage | V _{OH} | V _{IH} or V _{IL} | -0.05 | 4.5 | 4.4 | - | 4.4 | - | 4.4 | - | 4.4 | V | |
| | | | -24 | 4.5 | 3.94 | - | 3.8 | - | 3.7 | - | 3.7 | V | |
| | | | -75 (Note 6, 7) | 5.5 | - | - | 3.85 | - | - | - | - | - | V |
| | | | -50 (Note 6, 7) | 5.5 | - | - | - | - | - | 3.85 | - | 3.85 | V |
| Low Level Output Voltage | V _{OL} | V _{IH} or V _{IL} | 0.05 | 4.5 | - | 0.1 | - | 0.1 | - | 0.1 | V | | |
| | | | 24 | 4.5 | - | 0.36 | - | 0.44 | - | 0.5 | V | | |
| | | | 75 (Note 6, 7) | 5.5 | - | - | - | 1.65 | - | - | V | | |
| | | | 50 (Note 6, 7) | 5.5 | - | - | - | - | - | 1.65 | V | | |
| Input Leakage Current | I _I | V _{CC} or GND | - | 5.5 | - | ±0.1 | - | ±1 | - | ±1 | µA | | |
| Quiescent Supply Current MSI | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | 8 | - | 80 | - | 160 | µA | | |
| Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load | ΔI _{CC} | V _{CC} -2.1 | - | 4.5 to 5.5 | - | 2.4 | - | 2.8 | - | 3 | mA | | |

NOTES:

- Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

ACT Input Load Table

| INPUT | UNIT LOAD |
|-------|-----------|
| Dn | 0.5 |
| MR | 0.57 |
| CP | 1 |

NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

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Prerequisite For Switching Function

| PARAMETER | SYMBOL | V _{CC} (V) | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|-------------------------------------|------------------|---------------------|---------------|-----|----------------|-----|-------|
| | | | MIN | MAX | MIN | MAX | |
| AC TYPES | | | | | | | |
| Data to CP Set-Up Time | t _{SU} | 1.5 | 2 | - | 2 | - | ns |
| | | 3.3 (Note 9) | 2 | - | 2 | - | ns |
| | | 5 (Note 10) | 2 | - | 2 | - | ns |
| Hold Time | t _H | 1.5 | 2 | - | 2 | - | ns |
| | | 3.3 | 2 | - | 2 | - | ns |
| | | 5 | 2 | - | 2 | - | ns |
| Removal Time, \overline{MR} to CP | t _{REM} | 1.5 | 2 | - | 2 | - | ns |
| | | 3.3 | 2 | - | 2 | - | ns |
| | | 5 | 2 | - | 2 | - | ns |
| \overline{MR} Pulse Width | t _W | 1.5 | 55 | - | 63 | - | ns |
| | | 3.3 | 6.1 | - | 7 | - | ns |
| | | 5 | 4.4 | - | 5 | - | ns |
| CP Pulse Width | t _W | 1.5 | 55 | - | 63 | - | ns |
| | | 3.3 | 6.1 | - | 7 | - | ns |
| | | 5 | 4.4 | - | 5 | - | ns |
| CP Frequency | f _{MAX} | 1.5 | 9 | - | 8 | - | MHz |
| | | 3.3 | 81 | - | 71 | - | MHz |
| | | 5 | 114 | - | 100 | - | MHz |
| ACT TYPES | | | | | | | |
| Data to CP Set-Up Time | t _{SU} | 5 (Note 10) | 2 | - | 2 | - | ns |
| Hold Time | t _H | 5 | 2 | - | 2 | - | ns |
| Removal Time \overline{MR} to CP | t _{REM} | 5 | 2 | - | 2 | - | ns |
| \overline{MR} Pulse Width | t _W | 5 | 4.4 | - | 5 | - | ns |
| CP Pulse Width | t _W | 5 | 5.3 | - | 6 | - | ns |
| CP Frequency | f _{MAX} | 5 | 97 | - | 85 | - | MHz |

Switching Specifications Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

| PARAMETER | SYMBOL | V _{CC} (V) | -40°C TO 85°C | | | -55°C TO 125°C | | | UNITS |
|-----------------------------|-------------------------------------|---------------------|---------------|-----|------|----------------|-----|------|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| AC TYPES | | | | | | | | | |
| Propagation Delay, CP to Qn | t _{PLH} , t _{PHL} | 1.5 | - | - | 154 | - | - | 169 | ns |
| | | 3.3 (Note 9) | 4.9 | - | 17.2 | 4.7 | - | 18.9 | ns |
| | | 5 (Note 10) | 3.5 | - | 12.3 | 3.4 | - | 13.5 | ns |

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Switching Specifications Input $t_r, t_f = 3\text{ns}$, $C_L = 50\text{pF}$ (Worst Case) (Continued)

| PARAMETER | SYMBOL | V_{CC} (V) | -40°C TO 85°C | | | -55°C TO 125°C | | | UNITS |
|--------------------------------|-----------------------|----------------|---------------|-----|------|----------------|-----|------|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Propagation Delay, MR to Qn | t_{PLH}, t_{PHL} | 1.5 | - | - | 154 | - | - | 169 | ns |
| | | 3.3 | 4.9 | - | 17.2 | 4.7 | - | 18.9 | ns |
| | | 5 | 3.5 | - | 12.3 | 3.4 | - | 13.5 | ns |
| Input Capacitance | C_I | - | - | - | 10 | - | - | 10 | pF |
| Power Dissipation Capacitance | C_{PD} (Note 11) | - | - | 45 | - | - | 45 | - | pF |
| ACT TYPES | | | | | | | | | |
| Propagation Delay, CP to Qn | t_{PLH}, t_{PHL} | 5 (Note 10) | 3.5 | - | 12.3 | 3.4 | - | 13.5 | ns |
| Propagation Delay, MR to Qn | t_{PLH}, t_{PHL} | 5 | 3.5 | - | 12.3 | 3.4 | - | 13.5 | ns |
| Input Capacitance | C_I | - | - | - | 10 | - | - | 10 | pF |
| Power Dissipation Capacitance | C_{PD} (Note 11) | - | - | 45 | - | - | 45 | - | pF |

NOTES:

8. Limits tested 100%.
9. 3.3V Min is at 3.6V, Max is at 3V.
10. 5V Min is at 5.5V, Max is at 4.5V.
11. C_{PD} is used to determine the dynamic power consumption per flip-flop.
 AC: $P_D = C_{PD} V_{CC}^2 f_i = \sum (C_L V_{CC}^2 f_o)$
 ACT: $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

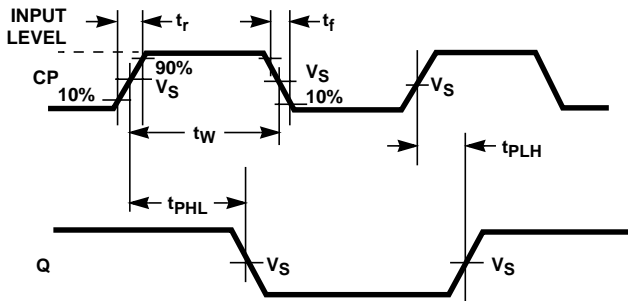


FIGURE 1. PROPAGATION DELAY TIMES AND CLOCK PULSE WIDTH

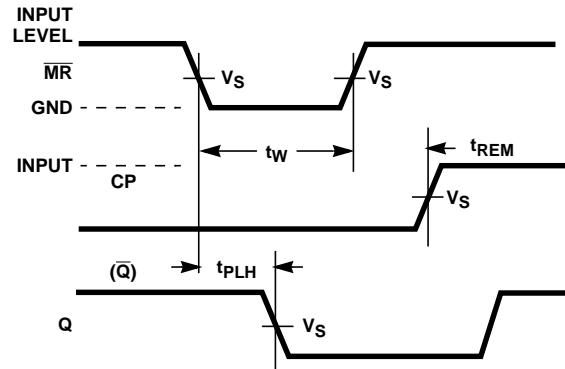


FIGURE 2. PREREQUISITE AND PROPAGATION DELAY TIMES FOR MASTER RESET

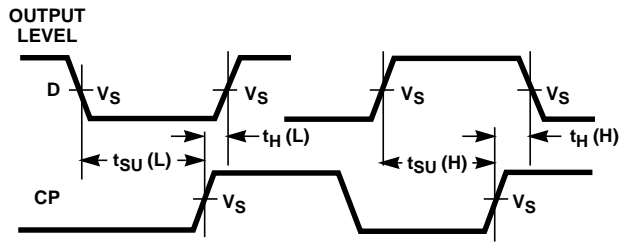


FIGURE 3. PREREQUISITE FOR CLOCK



NOTE: For AC Series Only: When $V_{CC} = 1.5V$, $R_L = 1k\Omega$.

| | AC | ACT |
|---------------------------------|--------------|--------------|
| Input Level | V_{CC} | 3V |
| Input Switching Voltage, V_S | $0.5 V_{CC}$ | 1.5V |
| Output Switching Voltage, V_S | $0.5 V_{CC}$ | $0.5 V_{CC}$ |

FIGURE 4. PROPAGATION DELAY TIMES

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD54AC273F3A | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| CD54ACT273F3A | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| CD74AC273E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74AC273EE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74AC273M | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC273M96 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC273M96E4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC273M96G4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC273ME4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74AC273MG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT273E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74ACT273EE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74ACT273M | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT273M96 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT273M96E4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT273M96G4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT273ME4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT273MG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT273PW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT273PWE4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT273PWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT273PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT273PWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT273PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT273SM96 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74ACT273SM96E4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| | | | | | | no Sb/Br) | | |
| CD74ACT273SM96G4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74AC273M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| CD74ACT273M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| CD74ACT273PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| CD74ACT273SM96 | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74AC273M96 | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| CD74ACT273M96 | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| CD74ACT273PWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| CD74ACT273SM96 | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

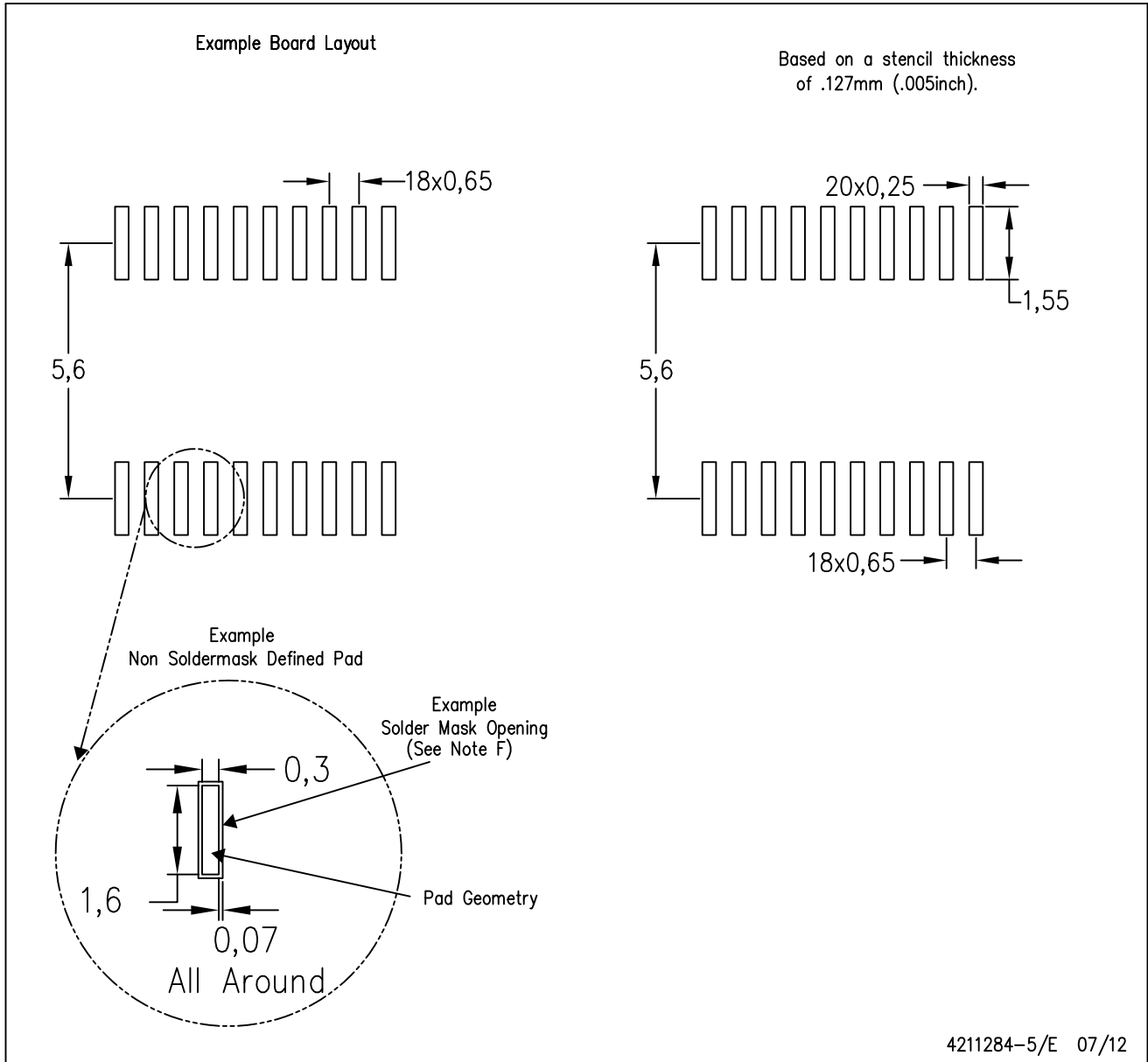


4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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