

# **TMS320C6457**

## ***Communications Infrastructure Digital Signal Processor***

### **Data Manual**



PRODUCTION DATA information is current as of publication date.  
Products conform to specifications per the terms of Texas  
Instruments standard warranty. Production processing does not  
necessarily include testing of all parameters.

Literature Number: SPRS582B  
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## Release History

|          | Additions/Modifications/Deletions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPRS582B | <ul style="list-style-type: none"> <li>• Added 850 mHz clock speed.</li> <li>• Added content to the Warm Reset section describing how to preserve contents of DDR2 SDRAM through a Warm Reset cycle with <i>Self-Refresh</i> mode enabled on the SDRAM.</li> <li>• Corrected typo in the Reset Timing Requirements table, parameter number 2: changed <math>\overline{\text{RESETx}}</math> to <math>\overline{\text{RESET}}</math> and POR to <math>\overline{\text{POR}}</math>.</li> <li>• Corrected 1.2-V to 1.1-V in last item of Features bullet list.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| SPRS582A | <ul style="list-style-type: none"> <li>• Corrected CORECLK(P N) and ALT CORECLK max frequency, minimum period time, duty cycle, and transition times</li> <li>• Corrected Period Jitter tolerance, duty cycle, and transition times for DDRREFCLK(P N) and ALTDDRCLK</li> <li>• Corrected PLL2 block diagram to include correct reference to PLLV<sub>2</sub> voltage net</li> <li>• Added DDR2CLKOUT0(N P) and DDR2CLKOUT0(N P) min and max frequency to PLL2 Clock Frequency Ranges table</li> <li>• Removed PLLOUT term from the PLL2 Clock Frequency ranges table</li> <li>• Clarified wording in the introduction of the PLL2 section and on the effective x5 multiplier that generates DDR2CLKOUT0(N P) and DDR2CLKOUT0(N P) from DDRREFCLK(P N) or ALTDDRCLK</li> <li>• Added Table 7-4 Power Supply to Peripheral I/O Mapping to clarify the exact I/O and reference clock buffers each power supply provides power for</li> <li>• Added Overshoot/Undershoot definition to Table 6-1 Absolute Maximum Ratings</li> <li>• Fixed typo in Table 2-1 under the 1.2 GHz space, "1.2 V, 1.8 V, and 3.3 V" now correctly reads "1.1 V, 1.8 V, and 3.3 V"</li> <li>• Fixed typo for the McBSP timing parameters. "P = 1/CORECLK" now correctly reads "P = 1/SYSREFCLK"</li> <li>• Fixed typo in 7.3.1 Power-Supply Sequencing - The SPRAAG5 reference now correctly references SPRAAV7</li> </ul> |
| SPRS582  | <ul style="list-style-type: none"> <li>• Initial version</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

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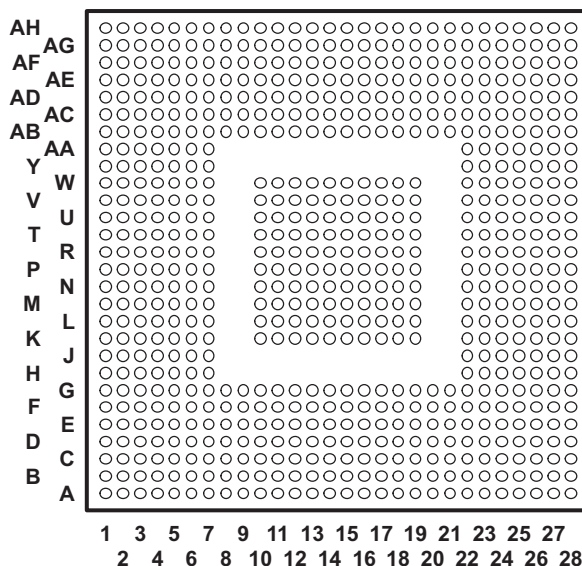
## 1 TMS320C6457 Features

- **High-Performance Fixed-Point DSP (C6457)**
  - 1.18-ns, 1-ns, and 0.83-ns Instruction Cycle Time
  - 850-MHz, 1-GHz, and 1.2-GHz Clock Rate
  - Eight 32-Bit Instructions/Cycle
  - 8000 and 9600 MIPS/MMACS (16-Bits)
  - Case Temperature
    - › Commercial:
      - » 0°C to 100°C (850 MHz)
      - » 0°C to 100°C (1 GHz)
      - » 0°C to 95°C (1.2 GHz)
    - › Extended:
      - » -40°C to 100°C (1 GHz)
      - » -40°C to 95°C (1.2 GHz)
- **TMS320C64x+™ DSP Core**
  - Dedicated SPLOOP Instruction
  - Compact Instructions (16-Bit)
  - Instruction Set Enhancements
  - Exception Handling
- **TMS320C64x+ Megamodule L1/L2 Memory Architecture:**
  - 256K-Bit (32K-Byte) L1P Program Cache [Direct Mapped]
  - 256K-Bit (32K-Byte) L1D Data Cache [2-Way Set-Associative]
  - 16M-Bit (2048K-Byte) L2 Unified Mapped Ram/Cache [Flexible Allocation]
    - › Configurable up to 1MB of L2 Cache
  - 512K-Bit (64K-Byte) L3 ROM
  - Time Stamp Counter
- **Enhanced VCP2**
  - Supports Over 694 7.95-Kbps AMR
  - Programmable Code Parameters
- **Two Enhanced Turbo Decoder Coprocessors (TCP2\_A and TCP2\_B)**
  - Each TCP2 Supports up to Eight 2-Mbps 3GPP (6 Iterations)
  - Programmable Turbo Code and Decoding Parameters
- **Endianess: Little Endian, Big Endian**
- **64-Bit External Memory Interface (EMIFA)**
  - Glueless Interface to Asynchronous Memories (SRAM, Flash, and EEPROM) and Synchronous Memories (SBSRAM, ZBT SRAM)
  - Supports Interface to Standard Sync Devices and Custom Logic (FPGA, CPLD, ASICs, etc.)
  - 32M-Byte Total Addressable External Memory Space
- **32-Bit DDR2 Memory Controller (DDR2-667 SDRAM)**
- **Four 1× Serial RapidIO® Links (or One 4×), v1.3 Compliant**
  - 1.25-, 2.5-, 3.125-Gbps Link Rates
  - Message Passing, DirectIO Support, Error Mgmt Extensions, Congestion Control
  - IEEE 1149.6 Compliant I/Os
- **EDMA3 Controller (64 Independent Channels)**
- **32-/16-Bit Host-Port Interface (HPI)**
- **Two 1.8-V McBSPs**
- **10/100/1000 Mb/s Ethernet MAC (EMAC)**
  - IEEE 802.3 Compliant
  - Supports SGMII, v1.8 Compliant
  - 8 Independent Transmit (TX) and 8 Independent Receive (RX) Channels
- **Two 64-Bit General-Purpose Timers**
  - Configurable as Four 32-Bit Timers
  - Configurable in a Watchdog Timer Mode
- **UTOPiA**
  - UTOPIA Level 2 Slave ATM Controller
  - 8-Bit Transmit and Receive Operations up to 50 MHz per Direction
  - User-Defined Cell Format up to 64 Bytes
- **One 1.8-V Inter-Integrated Circuit (I2C) Bus**
- **16 General-Purpose I/O (GPIO) Pins**
- **System PLL and PLL Controller**
- **DDR PLL, Dedicated to DDR2 Memory Controller**
- **Advanced Event Triggering (AET) Compatible**
- **Trace-Enabled Device**
- **Supports IP Security**
- **IEEE-1149.1 and IEEE-1149.6 (JTAG™) Boundary-Scan-Compatible**
- **688-Pin Ball Grid Array (BGA) Package (CMH or GMH Suffix), 0.8-mm Ball Pitch**
- **0.065-μm/7-Level Cu Metal Process (CMOS)**
- **3.3-V, 1.8-V, 1.1-V I/Os, 1.1-V and 1.2-V Internal**

## 1.1 TMS320C6457CMH/GMH BGA Package (Bottom View)

**Figure 1-1 CMH/GMH 688-Pin Ball Grid Array (BGA) Package**

**CMH/GMH 688-PIN BALL GRID ARRAY (BGA) PACKAGE  
(BOTTOM VIEW)**



(A) The CMH mechanical package designator represents the version of the GMH package with lead-free balls. For more detailed information, see “Mechanical Data” on page 209 of this document.

## 1.2 Description

The TMS320C64x+™ DSPs (including the TMS320C6457 device) are the highest-performance fixed-point DSP generation in the TMS320C6000™ DSP platform. The C6457 device is based on the third-generation high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making these DSPs an excellent choice for applications including video and telecom infrastructure, imaging/medical, and wireless infrastructure (WI). The C64x+ devices are upward code-compatible from previous devices that are part of the C6000™ DSP platform.

Based on 65-nm process technology and with performance of up to 9600 million instructions per second (MIPS) [or 9600 16-bit MMACs per cycle] at a 1.2-GHz clock rate, the C6457 device offers cost-effective solutions to high-performance DSP programming challenges. The C6457 DSP possesses the operational flexibility of high-speed controllers and the numerical capability of array processors.

The C64x+ DSP core employs eight functional units, two register files, and two data paths. Like the earlier C6000 devices, two of these eight functional units are multipliers or .M units. Each C64x+ .M unit doubles the multiply throughput versus the C64x core by performing four 16-bit × 16-bit multiply-accumulates (MACs) every clock cycle. Thus, eight 16-bit × 16-bit MACs can be executed every cycle on the C64x+ core. At a 1.2-GHz clock rate, this means 9600 16-bit MMACs can occur every second. Moreover, each multiplier on the C64x+ core can compute one 32-bit × 32-bit MAC or four 8-bit × 8-bit MACs every clock cycle.

The C6457 device includes Serial RapidIO®. This high-bandwidth peripheral dramatically improves system performance and reduces system cost for applications that include multiple DSPs on a board, such as video and telecom infrastructures and medical/imaging.

The C6457 DSP integrates a large amount of on-chip memory organized as a two-level memory system. The level-1 (L1) program and data memories on the C6457 device are 32KB each. This memory can be configured as mapped RAM, cache, or some combination of the two. When configured as cache, L1 program (L1P) is a direct mapped cache whereas L1 data (L1D) is a two-way set associative cache. The level 2 (L2) memory is shared between program and data space and is 2048KB in size. L2 memory can also be configured as mapped RAM, cache, or some combination of the two. L2 is configurable up to 1MB of cache. The C64x+ Megamodule also has a 32-bit peripheral configuration (CFG) port, an internal DMA (IDMA) controller, a system component with reset/boot control, interrupt/exception control, a power-down control, and a free-running 32-bit timer for time stamp.

The peripheral set includes: an inter-integrated circuit bus module ( $I^2C$ ); two multichannel buffered serial ports (McBSPs); an 8-bit Universal Test and Operations PHY Interface for Asynchronous Transfer Mode (ATM) Slave [UTOPIA Slave] port; two 64-bit general-purpose timers (also configurable as four 32-bit timers); a user-configurable 16-bit or 32-bit host-port interface (HPI16/HPI32); a 16-pin general-purpose input/output port (GPIO) with programmable interrupt/event generation modes; an 10/100/1000 Ethernet media access controller (EMAC), which provides an efficient interface between the C6457 DSP core processor and the network; a management data input/output (MDIO) module (also part of the EMAC) that continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system; a glueless external memory interface (64-bit EMIFA), which is capable of interfacing to synchronous and asynchronous peripherals; and a 32-bit DDR2 SDRAM interface.

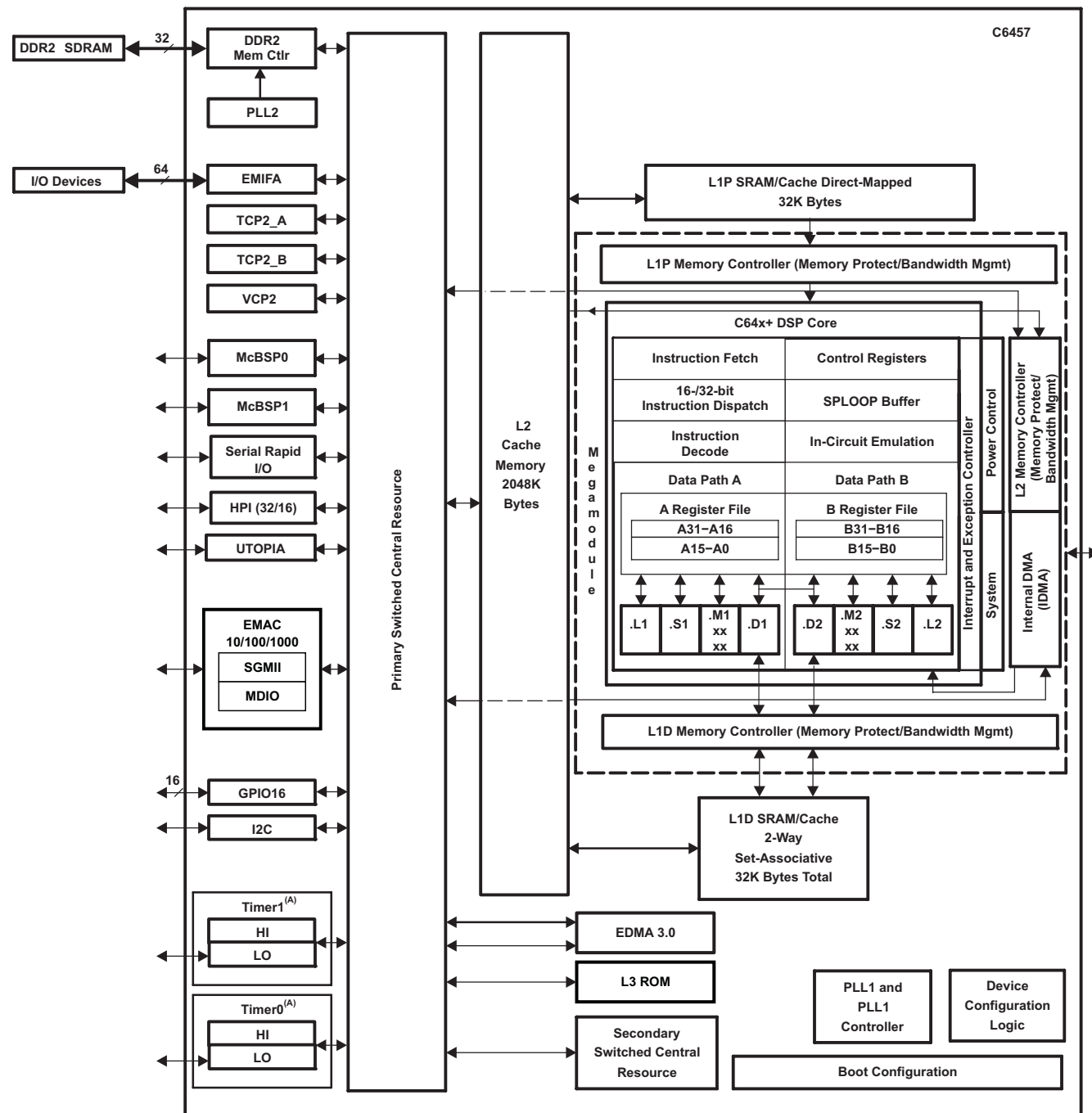
The C6457 device has three high-performance embedded coprocessors [one enhanced Viterbi Decoder Coprocessor (VCP2) and two enhanced Turbo Decoder Coprocessors (TCP2\_A and TCP2\_B)] that significantly speed up channel-decoding operations on-chip. The VCP2 operating at CPU clock  $\div 3$  can decode more than 694 7.95-Kbps adaptive multi-rate (AMR) [ $K = 9$ ,  $R = 1/3$ ] voice channels. The VCP2 supports constraint lengths  $K = 5, 6, 7, 8$ , and  $9$ , rates  $R = 3/4, 1/2, 1/3, 1/4$ , and  $1/5$ , and flexible polynomials, while generating hard decisions or soft decisions. Each TCP2 operating at CPU clock  $\div 3$  can decode up to fifty 384-Kbps or eight 2-Mbps turbo encoded channels (assuming 6 iterations). The TCP2 implements the max\*log-map algorithm and is designed to support all polynomials and rates required by Third-Generation Partnership Projects (3GPP and 3GPP2), with fully programmable frame length and turbo interleaver. Decoding parameters such as the number of iterations and stopping criteria are also programmable. Communications between the VCP2/TCP2s and the CPU are carried out through the EDMA3 controller.

The C6457 device has a complete set of development tools, which includes: a new C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows® debugger interface for visibility into source code execution.

## 1.3 Functional Block Diagram

Figure 1-2 Shows the functional block diagram of the TMS320C6457 device.

Figure 1-2 Functional Block Diagram



(A) Each of the TIMER peripherals (TIMER1 and TIMER0) is configurable as either one 64-bit general-purpose timer or two 32-bit general-purpose timers or a watchdog timer.



## 2 Device Overview

### 2.1 Device Characteristics

Table 2-1 provides an overview of the TMS320C6457 DSP. The table shows significant features of the C6457 device, including the capacity of on-chip RAM, the peripherals, the CPU frequency, and the package and pin count.

### 2.2 CPU (DSP Core) Description

**Table 2-1 Characteristics of the C6457 Processor (Part 1 of 2)**

| HARDWARE FEATURES                |                                                                                      |             | TMS320C6457                                                                                                                                 |
|----------------------------------|--------------------------------------------------------------------------------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| Peripherals                      | EMIFA (64-bit bus width) (clock source = AECLKIN or SYSCLK7)                         |             | 1                                                                                                                                           |
|                                  | DDR2 Memory Controller (32-bit bus width) [1.8 V I/O] (clock source = DDRREFCLKN[P]) |             | 1                                                                                                                                           |
|                                  | EDMA3 (64 independent channels) [CPU/3 clock rate]                                   |             | 1                                                                                                                                           |
|                                  | High-speed 1×/4× Serial RapidIO Port (4 lanes)                                       |             | 1                                                                                                                                           |
|                                  | I <sup>2</sup> C                                                                     |             | 1                                                                                                                                           |
|                                  | HPI (32-or 16-bit user selectable)                                                   |             | 1 (HPI16 or HPI32)                                                                                                                          |
|                                  | McBSPs (internal or external clock source up to 100 Mbps)                            |             | 2                                                                                                                                           |
|                                  | UTOPiA (8-bit mode, 50-MHz, slave-only)                                              |             | 1                                                                                                                                           |
|                                  | 10/100/1000 Ethernet MAC (EMAC)                                                      |             | 1                                                                                                                                           |
|                                  | Management Data Input/Output (MDIO)                                                  |             | 1                                                                                                                                           |
|                                  | 64-Bit Timers (configurable) (internal clock source = CPU/6 clock frequency)         |             | 2 64-bit <b>or</b> 4 32-bit                                                                                                                 |
|                                  | General-Purpose Input/Output Port (GPIO)                                             |             | 16                                                                                                                                          |
| Decoder Coprocessors             | VCP2 (clock source = CPU/3 clock frequency)                                          |             | 1                                                                                                                                           |
|                                  | TCP2 (clock source = CPU/3 clock frequency)                                          |             | 2                                                                                                                                           |
| On-Chip Memory                   | Size (Bytes)                                                                         |             | 2176K                                                                                                                                       |
|                                  | Organization                                                                         |             | 32KB L1 Program Memory Controller [SRAM/Cache]<br>32KB L1 Data Memory Controller [SRAM/Cache]<br>2048KB L2 Unified Memory/Cache 64KB L3 ROM |
| C64x+ Megamodule Revision ID     | Megamodule Revision ID Register (address location: 0181 2000h)                       |             | See Section 5.6 <a href="#">“Megamodule Revision”</a> on page 77                                                                            |
| JTAG BSDL_ID                     | JTAGID register (address location: 0288 0818h)                                       |             | See Section 3.5 <a href="#">“JTAG ID (JTAGID) Register Description”</a> on page 62                                                          |
| Frequency                        | MHz                                                                                  |             | 850, 1000 (1 GHz), and 1200 (1.2 GHz)                                                                                                       |
| Cycle Time                       | ns                                                                                   |             | 1.18 ns, 1 ns, and 0.83 ns (0.85, 1.0, & 1.2-GHz CPU)                                                                                       |
| Voltage                          | Core (V)                                                                             | 850-MHz CPU | 1.1 V                                                                                                                                       |
|                                  |                                                                                      | 1-GHz CPU   | 1.1 V                                                                                                                                       |
|                                  |                                                                                      | 1.2-GHz CPU | 1.2 V                                                                                                                                       |
|                                  | I/O (V)                                                                              | 850-MHz CPU | 1.1 V, 1.8 V, and 3.3 V                                                                                                                     |
|                                  |                                                                                      | 1-GHz CPU   | 1.1 V, 1.8 V, and 3.3 V                                                                                                                     |
|                                  |                                                                                      | 1.2-GHz CPU | 1.1 V, 1.8 V, and 3.3 V                                                                                                                     |
| PLL1 and PLL1 Controller Options | CLKIN1 frequency multiplier                                                          |             | Bypass (×1), (×4 to ×32)                                                                                                                    |
| PLL2                             | DDR2 Clock                                                                           |             | ×10                                                                                                                                         |
| BGA Package                      | 23 mm × 23 mm                                                                        |             | 688-Pin Flip-Chip Plastic BGA (CMH/GMH)                                                                                                     |
| Process Technology               | μm                                                                                   |             | 0.065 μm                                                                                                                                    |

**Table 2-1 Characteristics of the C6457 Processor (Part 2 of 2)**

| HARDWARE FEATURES   |                                                                                       | TMS320C6457        |
|---------------------|---------------------------------------------------------------------------------------|--------------------|
| Product Status      | Production Data (PD)                                                                  | PD                 |
| Device Part Numbers | (For more details on the C64x+™ DSP part numbering, see <a href="#">Figure 2-12</a> ) | TMS320C6457CMH/GMH |
| End of Table 2-1    |                                                                                       |                    |

The C64x+ Central Processing Unit (CPU) consists of eight functional units, two register files, and two data paths as shown in Figure 2-1. The two general-purpose register files (A and B) each contain 32 32-bit registers for a total of 64 registers. The general-purpose registers can be used for data or can be data address pointers. The data types supported include packed 8-bit data, packed 16-bit data, 32-bit data, 40-bit data, and 64-bit data. Values larger than 32 bits, such as 40-bit-long or 64-bit-long values are stored in register pairs, with the 32 LSBs of data placed in an even register and the remaining 8 or 32 MSBs in the next upper register (which is always an odd-numbered register).

The eight functional units (.M1, .L1, .D1, .S1, .M2, .L2, .D2, and .S2) are each capable of executing one instruction every clock cycle. The .M functional units perform all multiply operations. The .S and .L units perform a general set of arithmetic, logical, and branch functions. The .D units primarily load data from memory to the register file and store results from the register file into memory.

The C64x+ CPU extends the performance of the C64x core through enhancements and new features.

Each C64x+ .M unit can perform one of the following each clock cycle: one  $32 \times 32$  bit multiply, two  $16 \times 16$  bit multiplies, two  $16 \times 32$  bit multiplies, four  $8 \times 8$  bit multiplies, four  $8 \times 8$  bit multiplies with add operations, and four  $16 \times 16$  multiplies with add/subtract capabilities (including a complex multiply). There is also support for Galois field multiplication for 8-bit and 32-bit data. Many communications algorithms such as FFTs and modems require complex multiplication. The complex multiply (CMPY) instruction takes four 16-bit inputs and produces a 32-bit real and a 32-bit imaginary output. There are also complex multiplies with rounding capability that produces one 32-bit packed output that contain 16-bit real and 16-bit imaginary values. The  $32 \times 32$  bit multiply instructions provide the extended precision necessary for audio and other high-precision algorithms on a variety of signed and unsigned 32-bit data types.

The .L or (Arithmetic Logic Unit) now incorporates the ability to do parallel add/subtract operations on a pair of common inputs. Versions of this instruction exist to work on 32-bit data or on pairs of 16-bit data performing dual 16-bit add and subtracts in parallel. There are also saturated forms of these instructions. The C64x+ core enhances the .S unit in several ways. In the C64x core, dual 16-bit MIN2 and MAX2 comparisons were only available on the .L units. On the C64x+ core they are also available on the .S unit which increases the performance of algorithms that do searching and sorting. Finally, to increase data packing and unpacking throughput, the .S unit allows sustained high performance for the quad 8-bit/16-bit and dual 16-bit instructions. Unpack instructions prepare 8-bit data for parallel 16-bit operations. Pack instructions return parallel results to output precision including saturation support.

Other new features include:

- **SPLOOP** — A small instruction buffer in the CPU that aids in creation of software pipelining loops where multiple iterations of a loop are executed in parallel. The SPLOOP buffer reduces the code size associated with software pipelining. Furthermore, loops in the SPLOOP buffer are fully interruptible.
- **Compact Instructions** — The native instruction size for the C6000 devices is 32 bits. Many common instructions such as MPY, AND, OR, ADD, and SUB can be expressed as 16 bits if the C64x+ compiler can restrict the code to use certain registers in the register file. This compression is performed by the code generation tools.
- **Instruction Set Enhancements** — As noted above, there are new instructions such as 32-bit multiplications, complex multiplications, packing, sorting, bit manipulation, and 32-bit Galois field multiplication.



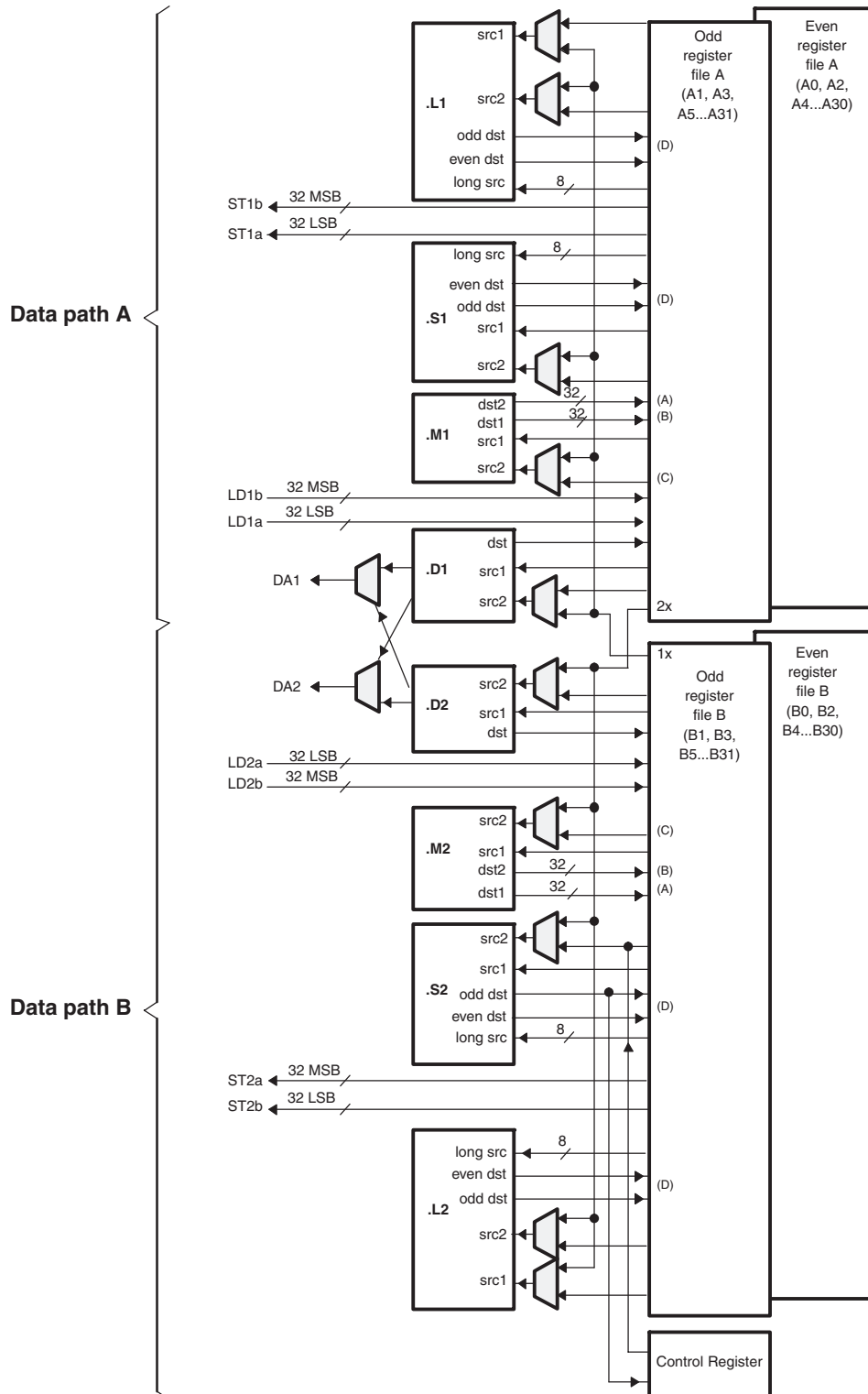
- **Exception Handling** — Intended to aid the programmer in isolating bugs. The C64x+ CPU is able to detect and respond to exceptions, both from internally detected sources (such as illegal op-codes) and from system events (such as a watchdog time expiration).
- **Privilege** — Defines user and supervisor modes of operation, allowing the operating system to give a basic level of protection to sensitive resources. Local memory is divided into multiple pages, each with read, write, and execute permissions.
- **Time-Stamp Counter** — Primarily targeted for Real-Time Operating System (RTOS) robustness, a free-running time-stamp counter is implemented in the CPU, which is *not* sensitive to system stalls.

For more details on the C64x+ CPU and its enhancements over the C64x architecture, see the following documents:

- *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (literature number [SPRU732](#))
- *TMS320C64x+ DSP Cache User's Guide* (literature number [SPRU862](#))
- *TMS320C64x+ Megamodule Reference Guide* (literature number [SPRU871](#))
- *TMS320C64x to TMS320C64x+ CPU Migration Guide* (literature number [SPRAA84](#))

Figure 2-1 shows the DSP core functional units and data paths.

**Figure 2-1 TMS320C64x+ CPU (DSP Core) Data Paths**



(A) On .M unit, dst2 is 32 MSB. \_\_\_\_ (B) On .M unit, dst1 is 32 LSB. \_\_\_\_ (C) On C64x CPU .M unit, src2 is 32 bits; on C64x+ CPU .M unit, src2 is 64 bits.  
 (D) On .L and .S units, odd dst connects to odd register files and even dst connects to even register files.

## 2.3 Memory Map Summary

Table 2-2 shows the memory map address ranges of the TMS320C6457 device. The external memory configuration register address ranges in the C6457 device begin at the hex address location 0x7000 0000 for EMIFA and hex address location 0x7800 0000 for DDR2 Memory Controller.

**Table 2-2 TMS320C6457 Memory Map Summary (Part 1 of 3)**

| MEMORY BLOCK DESCRIPTION                              | BLOCK SIZE (BYTES) | HEX ADDRESS RANGE     |
|-------------------------------------------------------|--------------------|-----------------------|
| Reserved                                              | 8M                 | 0000 0000 - 007F FFFF |
| L2 SRAM                                               | 2M                 | 0080 0000 - 009F FFFF |
| Reserved                                              | 4M                 | 00A0 0000 - 00DF FFFF |
| L1P SRAM                                              | 32K                | 00E0 0000 - 00E0 7FFF |
| Reserved                                              | 1M - 32K           | 00E0 8000 - 00EF FFFF |
| L1D SRAM                                              | 32K                | 00F0 0000 - 00F0 7FFF |
| Reserved                                              | 1M - 32K           | 00F0 8000 - 00FF FFFF |
| Reserved                                              | 8M                 | 0100 0000 - 017F FFFF |
| C64x+ Megamodule Registers                            | 4M                 | 0180 0000 - 01BF FFFF |
| Reserved                                              | 12.5M              | 01C0 0000 - 0287 FFFF |
| HPI Control Registers                                 | 256                | 0288 0000 - 0288 00FF |
| Reserved                                              | 2K - 256           | 0288 0100 - 0288 07FF |
| Chip-Level Registers                                  | 1K                 | 0288 0800 - 0288 0BFF |
| Reserved                                              | 253K               | 0288 0C00 - 028B FFFF |
| McBSP 0 Registers                                     | 256                | 028C 0000 - 028C 00FF |
| Reserved                                              | 256K - 256         | 028C 0100 - 028F FFFF |
| McBSP 1 Registers                                     | 256                | 0290 0000 - 0290 00FF |
| Reserved                                              | 256K - 256         | 0290 0100 - 0293 FFFF |
| Timer 0 Registers                                     | 128                | 0294 0000 - 0294 007F |
| Reserved                                              | 256K - 128         | 0294 0080 - 0297 FFFF |
| Timer 1 Registers                                     | 128                | 0298 0000 - 0298 007F |
| Reserved                                              | 128K - 128         | 0298 0080 - 0299 FFFF |
| PLL Controller (including Reset Controller) Registers | 512                | 029A 0000 - 029A 01FF |
| Reserved                                              | 384K - 512         | 029A 0200 - 029F FFFF |
| EDMA3 Channel Controller Registers                    | 32K                | 02A0 0000 - 02A0 7FFF |
| Reserved                                              | 96K                | 02A0 8000 - 02A1 FFFF |
| EDMA3 Transfer Controller 0 Registers                 | 1K                 | 02A2 0000 - 02A2 03FF |
| Reserved                                              | 31K                | 02A2 0400 - 02A2 7FFF |
| EDMA3 Transfer Controller 1 Registers                 | 1K                 | 02A2 8000 - 02A2 83FF |
| Reserved                                              | 31K                | 02A2 8400 - 02A2 FFFF |
| EDMA3 Transfer Controller 2 Registers                 | 1K                 | 02A3 0000 - 02A3 03FF |
| Reserved                                              | 31K                | 02A3 0400 - 02A3 7FFF |
| EDMA3 Transfer Controller 3 Registers                 | 1K                 | 02A3 8000 - 02A3 83FF |
| Reserved                                              | 31K                | 02A3 8400 - 02A3 FFFF |
| EDMA3 Transfer Controller 4 Registers                 | 1K                 | 02A4 0000 - 02A4 03FF |
| Reserved                                              | 31K                | 02A4 0400 - 02A4 7FFF |
| EDMA3 Transfer Controller 5 Registers                 | 1K                 | 02A4 8000 - 02A4 83FF |
| Reserved                                              | 479K               | 02A4 8400 - 02AB FFFF |
| Power / Sleep Controller (PSC)                        | 4K                 | 02AC 0000 - 02AC 0FFF |

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**Table 2-2 TMS320C6457 Memory Map Summary (Part 2 of 3)**

| MEMORY BLOCK DESCRIPTION       | BLOCK SIZE (BYTES) | HEX ADDRESS RANGE     |
|--------------------------------|--------------------|-----------------------|
| Reserved                       | 60K                | 02AC 1000 - 02AC FFFF |
| Embedded Trace Buffer (ETB)    | 8K                 | 02AD 0000 - 02AD 1FFF |
| Reserved                       | 184K               | 02AD 2000 - 02AF FFFF |
| GPIO Registers                 | 256                | 02B0 0000 - 02B0 00FF |
| Reserved                       | 16K - 256          | 02B0 0100 - 02B0 3FFF |
| I2C Data and Control Registers | 128                | 02B0 4000 - 02B0 407F |
| Reserved                       | 240K - 128         | 02B0 4080 - 02B3 FFFF |
| UTOPiA Control Registers       | 512                | 02B4 0000 - 02B4 01FF |
| Reserved                       | 256K - 512         | 02B4 0200 - 02B7 FFFF |
| VCP2 Control Registers         | 256                | 02B8 0000 - 02B8 00FF |
| Reserved                       | 128K - 256         | 02B8 0100 - 02B9 FFFF |
| TCP2_A Control Registers       | 256                | 02BA 0000 - 02BA 00FF |
| TCP2_B Control Registers       | 256                | 02BA 0100 - 02BA 01FF |
| Reserved                       | 640K - 512         | 02BA 0200 - 02C3 FFFF |
| SGMII Control                  | 256                | 02C4 0000 - 02C4 00FF |
| Reserved                       | 256K - 256         | 02C4 0100 - 02C7 FFFF |
| EMAC Control                   | 2K                 | 02C8 0000 - 02C8 07FF |
| Reserved                       | 2K                 | 02C8 0800 - 02C8 0FFF |
| EMAC Interrupt Controller      | 256                | 02C8 1000 - 02C8 10FF |
| Reserved                       | 2K - 256           | 02C8 1100 - 02C8 17FF |
| MDIO Control Registers         | 256                | 02C8 1800 - 02C8 18FF |
| Reserved                       | 2K - 256           | 02C8 1900 - 02C8 1FFF |
| EMAC Descriptor Memory         | 8K                 | 02C8 2000 - 02C8 3FFF |
| Reserved                       | 496K               | 02C8 4000 - 02CF FFFF |
| RapidIO Control Registers      | 132K               | 02D0 0000 - 02D2 0FFF |
| Reserved                       | 892K               | 02D2 1000 - 02DF FFFF |
| RapidIO Descriptor Memory      | 16K                | 02E0 0000 - 02E0 3FFF |
| Reserved                       | 1M - 16K           | 02E0 4000 - 02EF FFFF |
| Reserved                       | 1M                 | 02F0 0000 - 02FF FFFF |
| Reserved                       | 208M               | 0300 0000 - 0FFF FFFF |
| Reserved                       | 512M               | 1000 0000 - 2FFF FFFF |
| McBSP 0 Data                   | 256                | 3000 0000 - 3000 00FF |
| Reserved                       | 64M - 256          | 3000 0100 - 33FF FFFF |
| McBSP 1 Data                   | 256                | 3400 0000 - 3400 00FF |
| Reserved                       | 128M - 256         | 3400 0100 - 3BFF FFFF |
| L3 ROM                         | 64K                | 3C00 0000 - 3C00 FFFF |
| Reserved                       | 16M - 64K          | 3C01 0000 - 3CFF FFFF |
| UTOPiA Receive (RX) Data       | 128                | 3D00 0000 - 3D00 007F |
| Reserved                       | 896                | 3D00 0080 - 3D00 03FF |
| UTOPiA Transmit (TX) Data      | 128                | 3D00 0400 - 3D00 047F |
| Reserved                       | 304M - 1152        | 3D00 0480 - 4FFF FFFF |
| TCP2_A Data                    | 1M                 | 5000 0000 - 500F FFFF |
| TCP2_B Data                    | 1M                 | 5010 0000 - 501F FFFF |
| Reserved                       | 126M               | 5020 0000 - 57FF FFFF |

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**Table 2-2 TMS320C6457 Memory Map Summary (Part 3 of 3)**

| MEMORY BLOCK DESCRIPTION               | BLOCK SIZE (BYTES) | HEX ADDRESS RANGE     |
|----------------------------------------|--------------------|-----------------------|
| VCP2 Data                              | 64K                | 5800 0000 - 5800 FFFF |
| Reserved                               | 384M - 64K         | 5801 0000 - 6FFF FFFF |
| EMIFA (EMIF64) Configuration Registers | 256                | 7000 0000 - 7000 00FF |
| Reserved                               | 128M - 256         | 7000 0100 - 77FF FFFF |
| DDR2 EMIF Configuration Registers      | 256                | 7800 0000 - 7800 00FF |
| Reserved                               | 128M - 256         | 7800 0100 - 7FFF FFFF |
| Reserved                               | 512M               | 8000 0000 - 9FFF FFFF |
| EMIFA CE2 Data -SBSRAM/Async           | 8M                 | A000 0000 - A07F FFFF |
| Reserved                               | 256M - 8M          | A080 0000 - AFFF FFFF |
| EMIFA CE3 Data -SBSRAM/Async           | 8M                 | B000 0000 - B07F FFFF |
| Reserved                               | 256M - 8M          | B080 0000 - BFFF FFFF |
| EMIFA CE4 Data -SBSRAM/Async           | 8M                 | C000 0000 - C07F FFFF |
| Reserved                               | 256M - 8M          | C080 0000 - CFFF FFFF |
| EMIFA CE5 Data -SBSRAM/Async           | 8M                 | D000 0000 - D07F FFFF |
| Reserved                               | 256M - 8M          | D080 0000 - DFFF FFFF |
| DDR2 EMIF CE0 Data                     | 512M               | E000 0000 - FFFF FFFF |
| <b>End of Table 2-2</b>                |                    |                       |

## 2.4 Boot Sequence

The boot sequence is a process by which the DSP's internal memory is loaded with program and data sections. The DSP's internal registers are programmed with predetermined values. The boot sequence is started automatically after each power-on reset, warm reset, and system reset. A local reset to an individual C64x+ Megamodule should not affect the state of the hardware boot controller on the device. For more details on the initiators of the resets, see Section 7.6 “Reset Controller” on page 123.

The C6457 supports several boot processes begins execution at the ROM base address, which contains the bootloader code necessary to support various device boot modes. The boot processes are software driven; using the BOOTMODE[3:0] device configuration inputs to determine the software configuration that must be completed.

## 2.5 Boot Modes Supported

The device supports several boot processes, which leverage the internal boot ROM. Most boot processes are software driven, using the BOOTMODE[3:0] device configuration inputs to determine the software configuration that must be completed. From a hardware perspective, there are two possible boot modes:

- **Public ROM Boot** - C64x+ Megamodule is released from reset and begins executing from the L3 ROM base address. After performing the boot process (e.g., from I<sup>2</sup>C ROM, Ethernet, or RapidIO), the C64x+ Megamodule then begins execution from the L2 RAM base address.
- **Secure ROM Boot** - On secure devices, the C64x+ Megamodule is released from reset and begin executing from secure ROM. Software in the secure ROM will free up internal RAM pages, after which the C64x+ Megamodule initiates the boot process. The C64x+ Megamodule performs any authentication and decryption required on the bootloaded image prior to beginning execution.

The boot process performed by the C64x+ Megamodule in public ROM boot and secure ROM boot are determined by the BOOTMODE[3:0] value in the DEVSTAT register. The C64x+ Megamodule reads this value, and then executes the associated boot process in software. [Table 2-3](#) shows the supported boot modes.

**Table 2-3 TMS320C6457 Supported Boot Modes**

| Mode Name                      | Bootmode[3:0] | Description                                                                                                                                                                                                                                                                                                                                                     |
|--------------------------------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| No Boot                        | 0000b         | No Boot                                                                                                                                                                                                                                                                                                                                                         |
| I <sup>2</sup> C Master Boot A | 0001b         | Slave I <sup>2</sup> C address is 0x50. The C64x+ Megamodule configures I <sup>2</sup> C, acts as a master to the I <sup>2</sup> C bus and copies data from an I <sup>2</sup> C EEPROM or a device acting as an I <sup>2</sup> C slave to the DSP using a predefined boot table format. The destination address and length are contained within the boot table. |
| I <sup>2</sup> C Master Boot B | 0010b         | Similar to I <sup>2</sup> C boot A except the slave I <sup>2</sup> C address is 0x51.                                                                                                                                                                                                                                                                           |
| I <sup>2</sup> C Slave Boot    | 0011b         | The C64x+ Megamodule configures I <sup>2</sup> C and acts as a slaye and will accept data and code section packets through the I2C interface. It is required that an I <sup>2</sup> C master is present in the system.                                                                                                                                          |
| HPI Boot                       | 0100b         | Host boot.                                                                                                                                                                                                                                                                                                                                                      |
| EMIFA Boot                     | 0101b         | External memory boot from ACE3 space (0xB0000000 address).                                                                                                                                                                                                                                                                                                      |
| EMAC Master Boot               | 0110b         | TI Ethernet Boot. The C64x+ Megamodule configures EMAC and EDMA, if required, and brings the code image into the internal on-chip memory via the protocol defined by the boot method (EMAC bootloader).                                                                                                                                                         |
| EMAC Slave Boot                | 0111b         |                                                                                                                                                                                                                                                                                                                                                                 |
| EMAC Forced-Mode Boot          | 1000b         |                                                                                                                                                                                                                                                                                                                                                                 |
| Reserved                       | 1001b         | Reserved                                                                                                                                                                                                                                                                                                                                                        |
| RapidIO Boot (Config 0)        | 1010b         | The C64x+ Megamodule configures the SRIO and an external host loads the application via SRIO peripheral, using directIO protocol. A doorbell interrupt is used to indicate that the code has been loaded. For more details on the RapidIO configurations, see <a href="#">Table 2-4</a> .                                                                       |
| RapidIO Boot (Config 1)        | 1011b         |                                                                                                                                                                                                                                                                                                                                                                 |
| RapidIO Boot (Config 2)        | 1100b         |                                                                                                                                                                                                                                                                                                                                                                 |
| RapidIO Boot (Config 3)        | 1101b         |                                                                                                                                                                                                                                                                                                                                                                 |
| End of Table 2-3               |               |                                                                                                                                                                                                                                                                                                                                                                 |

The C64x+ Megamodule configures Serial RapidIO, EMAC, and EDMA, if required, and brings the code image into the internal on-chip memory via the protocol defined by the boot method (SRIO EMAC bootloader).

**Table 2-4 Serial RapidIO (SRIO) Supported Boot Modes**

| SRIO Boot Mode          | SerDes Clock | Link Rate  | SRIO Boot Configuration |
|-------------------------|--------------|------------|-------------------------|
| Bootmode 10 - Config 0  | 125 MHz      | 1.25 Gbps  | Four 1× SRIO links      |
| Bootmode 11 - Config 1  | 125 MHz      | 3.125 Gbps | One 4× SRIO link        |
| Bootmode 12 - Config 2  | 156.25 MHz   | 1.25 Gbps  | One 4× SRIO link        |
| Bootmode 13 - Config 3  | 156.25 MHz   | 3.125 Gbps | One 4× SRIO link        |
| <b>End of Table 2-4</b> |              |            |                         |

All the other BOOTMODE[3:0] modes are reserved.

### 2.5.1 Second-Level Bootloaders

Any of the boot modes can be used to download a second-level bootloader. A second-level bootloader allows for any level of customization to current boot methods as well as the definition of a completely customized boot.

## 2.6 Pin Assignments

### 2.6.1 Pin Map

Figure 2-2 through Figure 2-5 show the C6457 pin assignments in four quadrants (A, B, C, and D).

**Figure 2-2 TMS320C6457 Pin Map (Bottom View) [Quadrant A]**

|    | 1                    | 2               | 3                    | 4     | 5                    | 6                    | 7                    | 8                    | 9                | 10                | 11               | 12               | 13               | 14               |    |
|----|----------------------|-----------------|----------------------|-------|----------------------|----------------------|----------------------|----------------------|------------------|-------------------|------------------|------------------|------------------|------------------|----|
| AH | V <sub>DDS18_1</sub> | V <sub>SS</sub> | TCLK                 | EMU4  | EMU2                 | CORECLKP             | CORECLKN             | V <sub>SS</sub>      | RIOTXN1          | RIOTXP1           | V <sub>SS</sub>  | RIORXN1          | RIORXP1          | SGMIITXP         | AH |
| AG | V <sub>SS</sub>      | EMU7            | EMU8                 | EMU5  | V <sub>DDS18_1</sub> | RIOSGMII CLK         | RIOSGMII CLKP        | RIORXN0              | RIORXP0          | V <sub>SS</sub>   | V <sub>DDT</sub> | V <sub>SS</sub>  | RIOTXN3          | RIOTXP3          | AG |
| AF | TDO                  | EMU11           | EMU13                | EMU6  | V <sub>SS</sub>      | ALTCORE CLK          | RSV09                | V <sub>SS</sub>      | V <sub>DDT</sub> | RIORXP1           | RIORXN1          | RSV16            | RIOTXN2          | RIOTXP2          | AF |
| AE | EMU12                | TRST            | EMU10                | EMU3  | EMU1                 | CORE CLKSEL          | RSV08                | RIOTXP0              | RIOTXN0          | V <sub>DDR4</sub> | V <sub>SS</sub>  | RIORXP3          | RIORXN3          | V <sub>SS</sub>  | AE |
| AD | EMU15                | V <sub>SS</sub> | EMU16                | EMU9  | EMU0                 | RSV24                | SYSCLOCK OUT         | V <sub>SS</sub>      | V <sub>DDT</sub> | V <sub>SS</sub>   | V <sub>DDT</sub> | V <sub>SS</sub>  | V <sub>DDT</sub> | V <sub>SS</sub>  | AD |
| AC | EMU14                | EMU18           | V <sub>DDS18_1</sub> | RSV01 | V <sub>DDA18V1</sub> | RSV20                | RSV21                | V <sub>DDS18_1</sub> | V <sub>SS</sub>  | V <sub>DDA</sub>  | V <sub>SS</sub>  | V <sub>DDA</sub> | V <sub>SS</sub>  | V <sub>DDA</sub> | AC |
| AB | TDI                  | RSV02           | CLKX0                | RSV03 | RSV12                | V <sub>SS</sub>      | V <sub>DDS18_1</sub> | V <sub>SS</sub>      | V <sub>SS</sub>  | V <sub>SS</sub>   | V <sub>SS</sub>  | V <sub>SS</sub>  | V <sub>SS</sub>  | V <sub>SS</sub>  | AB |
| AA | EMU17                | V <sub>SS</sub> | CLKX1                | CLKS0 | RSV13                | V <sub>DDS18_1</sub> | V <sub>SS</sub>      |                      |                  |                   |                  |                  |                  |                  | AA |
| Y  | CLKS1                | TMS             | DX1                  | CLKR1 | CLKR0                | DR0                  | V <sub>DDS18_1</sub> |                      |                  |                   |                  |                  |                  |                  | Y  |
| W  | HD11                 | HD00            | DR1                  | FSX0  | FSX1                 | DX0                  | V <sub>SS</sub>      |                      |                  | V <sub>SS</sub>   | V <sub>DDD</sub> | V <sub>SS</sub>  | V <sub>DDD</sub> | V <sub>SS</sub>  | W  |
| V  | HD22                 | HD25            | V <sub>DDS33</sub>   | FSR0  | FSR1                 | V <sub>DDS18_1</sub> | V <sub>SS</sub>      |                      |                  | V <sub>DD</sub>   | V <sub>SS</sub>  | V <sub>DDD</sub> | V <sub>SS</sub>  | V <sub>DDD</sub> | V  |
| U  | HD21                 | HD13            | V <sub>SS</sub>      | HD05  | HD27                 | HD23                 | V <sub>DDS33</sub>   |                      |                  | V <sub>SS</sub>   | V <sub>DD</sub>  | V <sub>SS</sub>  | V <sub>DDD</sub> | V <sub>SS</sub>  | U  |
| T  | HD19                 | HD15            | HD09                 | HD03  | HD29                 | HD06                 | V <sub>SS</sub>      |                      |                  | RSV23             | V <sub>SS</sub>  | V <sub>DD</sub>  | V <sub>SS</sub>  | V <sub>DD</sub>  | T  |
| R  | HD17                 | V <sub>SS</sub> | V <sub>DDS33</sub>   | HD07  | HD10                 | HD04                 | V <sub>DDS33</sub>   |                      |                  | RSV23             | V <sub>DD</sub>  | V <sub>SS</sub>  | V <sub>DD</sub>  | V <sub>SS</sub>  | R  |

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**Figure 2-3 TMS320C6457 Pin Map (Bottom View) [Quadrant B]**

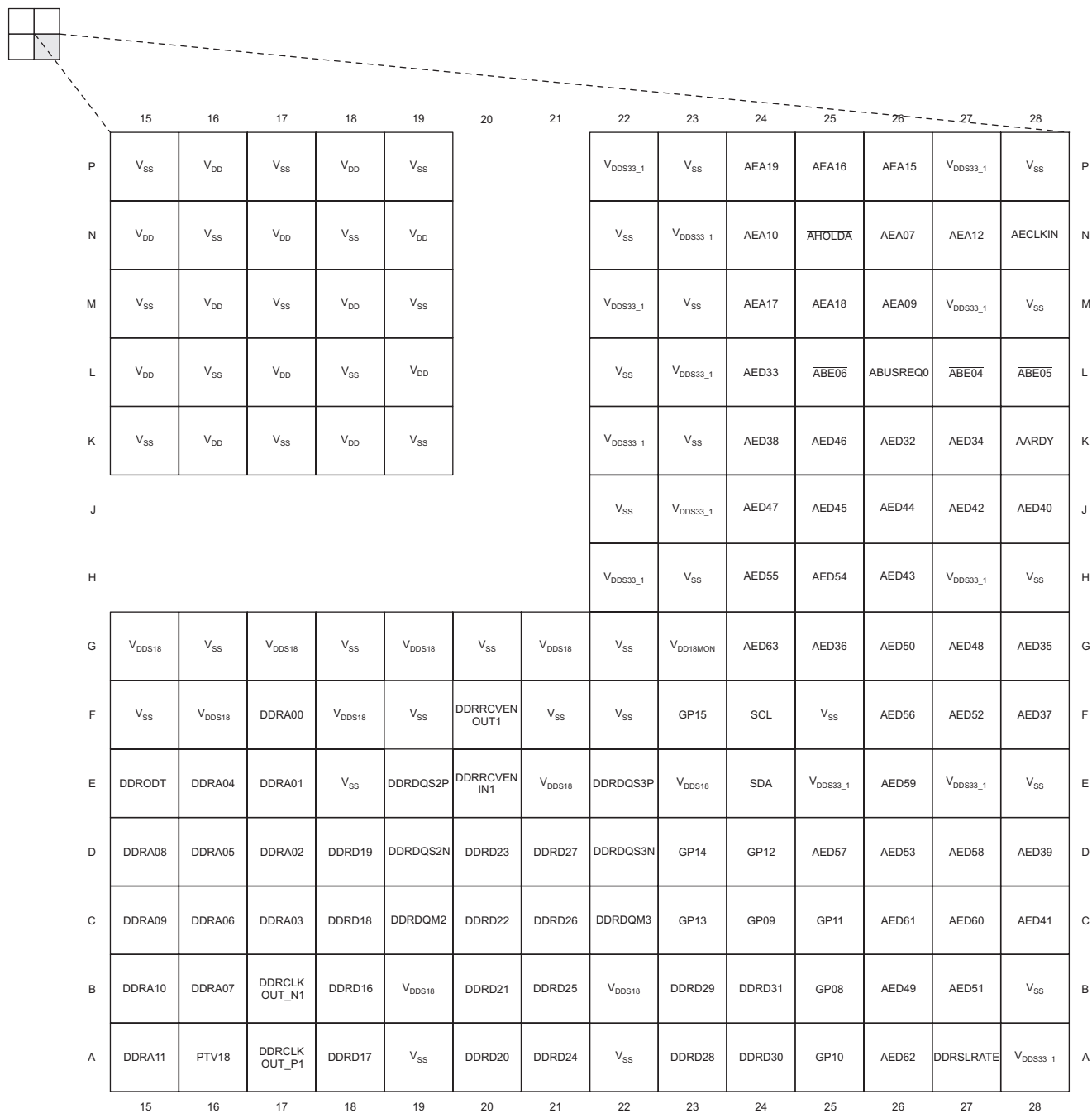
|    | 15               | 16                | 17               | 18                   | 19                   | 20                   | 21                   | 22                   | 23                  | 24                  | 25    | 26    | 27              | 28                  |    |
|----|------------------|-------------------|------------------|----------------------|----------------------|----------------------|----------------------|----------------------|---------------------|---------------------|-------|-------|-----------------|---------------------|----|
| AH | SGMIITXN         | V <sub>SS</sub>   | V <sub>DDT</sub> | MDCLK                | MDIO                 | TINPOL               | RSV18                | RSV29                | RESET               | V <sub>DD33_1</sub> | AED05 | AED06 | V <sub>SS</sub> | V <sub>DD33_1</sub> | AH |
| AG | V <sub>SS</sub>  | RSV17             | V <sub>SS</sub>  | V <sub>SS</sub>      | TINP1L               | TOUT0L               | RSV19                | POR                  | RSV28               | V <sub>SS</sub>     | AED14 | AED02 | AED20           | V <sub>SS</sub>     | AG |
| AF | V <sub>DDT</sub> | SGMIIRXN          | SGMIIRXP         | V <sub>DD318_2</sub> | TOUT1L               | RSV14                | RSV15                | RSV27                | RESETSTAT           | AED03               | AED09 | AED16 | AED18           | AED30               | AF |
| AE | V <sub>SS</sub>  | V <sub>DDR3</sub> | V <sub>SS</sub>  | V <sub>SS</sub>      | NMI                  | RSV06                | RSV07                | RSV26                | RSV22               | AED01               | AOE   | AED10 | AED15           | AED19               | AE |
| AD | V <sub>DDT</sub> | V <sub>SS</sub>   | V <sub>DDT</sub> | V <sub>DD318_2</sub> | V <sub>SS</sub>      | RSV04                | RSV05                | V <sub>DD318_2</sub> | V <sub>SS</sub>     | V <sub>DD33_1</sub> | AED07 | AED12 | AED04           | AED17               | AD |
| AC | V <sub>SS</sub>  | V <sub>DDA</sub>  | V <sub>SS</sub>  | V <sub>SS</sub>      | V <sub>DD318_2</sub> | V <sub>SS</sub>      | V <sub>DD318_2</sub> | V <sub>SS</sub>      | V <sub>DD33_1</sub> | AED00               | AED11 | AED08 | AED13           | AED21               | AC |
| AB | V <sub>SS</sub>  | V <sub>SS</sub>   | V <sub>SS</sub>  | V <sub>DD318_2</sub> | V <sub>SS</sub>      | V <sub>DD318_2</sub> | V <sub>SS</sub>      | V <sub>DD33_1</sub>  | V <sub>SS</sub>     | AED24               | AED26 | AED28 | V <sub>SS</sub> | V <sub>DD33_1</sub> | AB |
| AA |                  |                   |                  |                      |                      |                      |                      | V <sub>SS</sub>      | V <sub>DD33_1</sub> | ASDWE               | AED23 | AED25 | AED22           | AED29               | AA |
| Y  |                  |                   |                  |                      |                      |                      |                      | V <sub>DD33_1</sub>  | V <sub>SS</sub>     | ABE0T               | ABE00 | AED31 | AED27           | ABE03               | Y  |
| W  | V <sub>DDD</sub> | V <sub>SS</sub>   | V <sub>DD</sub>  | V <sub>SS</sub>      | V <sub>DD</sub>      |                      |                      | V <sub>SS</sub>      | V <sub>DD33_1</sub> | ARNW                | ACE3  | ACE2  | ABE02           | ABE07               | W  |
| V  | V <sub>SS</sub>  | V <sub>DD</sub>   | V <sub>SS</sub>  | V <sub>DD</sub>      | V <sub>SS</sub>      |                      |                      | V <sub>DD33_1</sub>  | V <sub>SS</sub>     | ABA1                | ABA0  | ACE5  | V <sub>SS</sub> | AECLKOUT            | V  |
| U  | V <sub>DD</sub>  | V <sub>SS</sub>   | V <sub>DD</sub>  | V <sub>SS</sub>      | V <sub>DDMON</sub>   |                      |                      | V <sub>DD33MON</sub> | V <sub>SS</sub>     | V <sub>SS</sub>     | AEA00 | AEA01 | ACE4            | AEA05               | U  |
| T  | V <sub>SS</sub>  | V <sub>DD</sub>   | V <sub>SS</sub>  | V <sub>DD</sub>      | V <sub>SS</sub>      |                      |                      | V <sub>DD33_1</sub>  | V <sub>SS</sub>     | AEA14               | AEA11 | AEA02 | AEA03           | AEA06               | T  |
| R  | V <sub>DD</sub>  | V <sub>SS</sub>   | V <sub>DD</sub>  | V <sub>SS</sub>      | V <sub>DD</sub>      |                      |                      | V <sub>SS</sub>      | V <sub>DD33_1</sub> | AEA08               | AADS  | AEA13 | AEA04           | AHOLD               | R  |



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**Figure 2-4 TMS320C6457 Pin Map (Bottom View) [Quadrant C]**



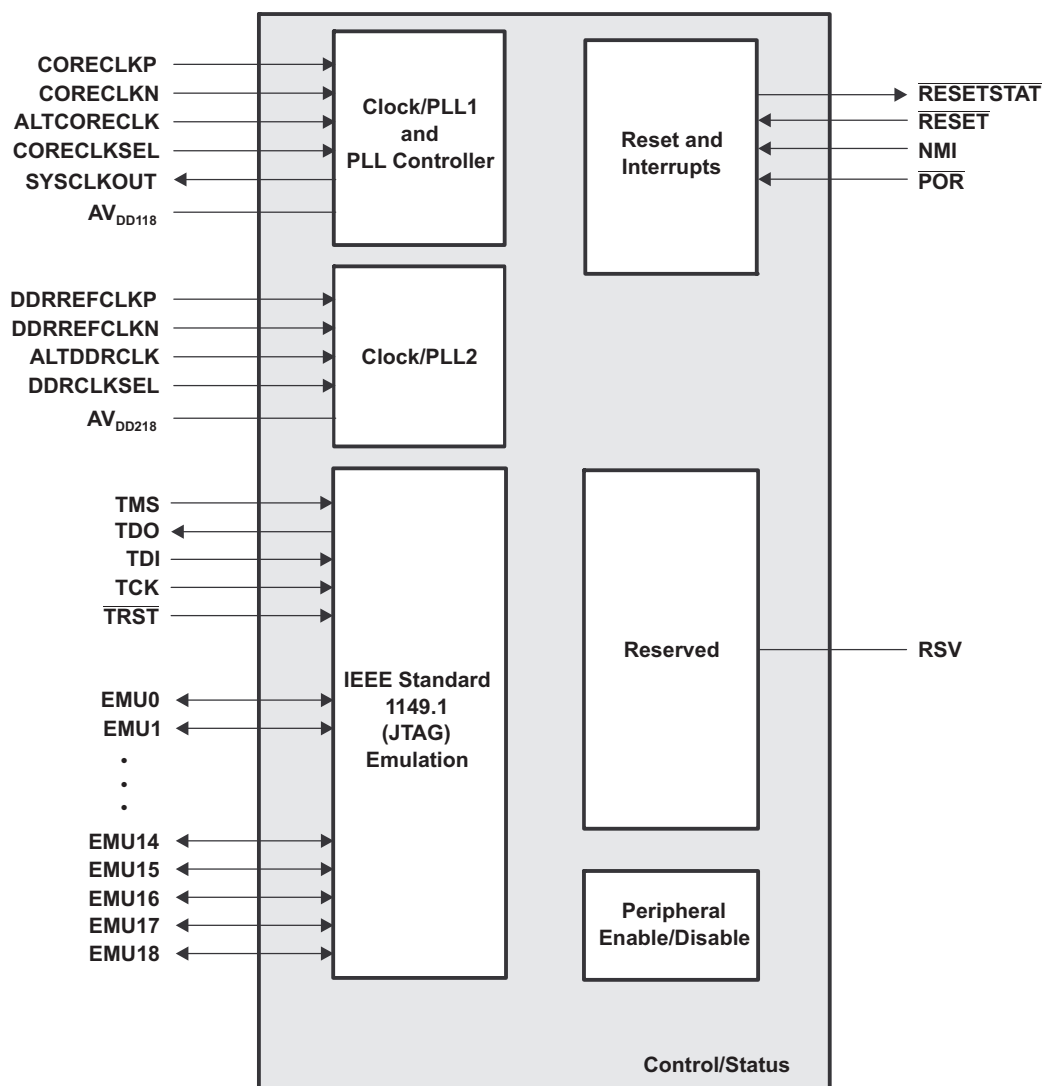
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|   | 1                   | 2               | 3                   | 4               | 5       | 6           | 7                     | 8                   | 9                   | 10                  | 11                  | 12                  | 13                   | 14                  |   |
|---|---------------------|-----------------|---------------------|-----------------|---------|-------------|-----------------------|---------------------|---------------------|---------------------|---------------------|---------------------|----------------------|---------------------|---|
| P | V <sub>DD</sub> S33 | HD18            | HD31                | HD14            | HD02    | HD28        | V <sub>SS</sub>       |                     |                     | V <sub>DD</sub>     | V <sub>SS</sub>     | V <sub>DD</sub>     | V <sub>SS</sub>      | V <sub>DD</sub>     | P |
| N | HD26                | HD20            | HD16                | HD12            | HD08    | HD30        | V <sub>DD</sub> S33   |                     |                     | V <sub>SS</sub>     | V <sub>DD</sub>     | V <sub>SS</sub>     | V <sub>DD</sub>      | V <sub>SS</sub>     | N |
| M | HD24                | V <sub>SS</sub> | HCS                 | HAS             | HCNTL1  | HRDY        | V <sub>SS</sub>       |                     |                     | V <sub>DD</sub>     | V <sub>SS</sub>     | V <sub>DD</sub>     | V <sub>SS</sub>      | V <sub>DD</sub>     | M |
| L | V <sub>DD</sub> S33 | HDS1            | HHWIL               | HINT            | HDS2    | HCNTL0      | V <sub>DD</sub> S33   |                     |                     | V <sub>SS</sub>     | V <sub>DD</sub>     | V <sub>SS</sub>     | V <sub>DD</sub>      | V <sub>SS</sub>     | L |
| K | URADDR4             | URADDR3         | UXADDR2             | URENB           | HR/W    | HD01        | V <sub>SS</sub>       |                     |                     | V <sub>DD</sub>     | V <sub>SS</sub>     | V <sub>DD</sub>     | V <sub>SS</sub>      | V <sub>DD</sub>     | K |
| J | URADDR2             | V <sub>SS</sub> | URADDR1             | UXADDR4         | UXADDR1 | RSV11       | V <sub>DD</sub> S18   |                     |                     |                     |                     |                     |                      |                     | J |
| H | V <sub>DD</sub> S33 | URADDR0         | UXDATA3             | UXADDR0         | UXADDR3 | RSV10       | V <sub>SS</sub>       |                     |                     |                     |                     |                     |                      |                     | H |
| G | URDATA7             | URSOC           | UXDATA2             | UXSOC           | RSV25   | DDRCLKSEL   | V <sub>DD</sub> S18   | V <sub>SS</sub>     | V <sub>DD</sub> S18 | V <sub>SS</sub>     | V <sub>DD</sub> S18 | V <sub>SS</sub>     | V <sub>DD</sub> S18  | V <sub>SS</sub>     | G |
| F | URDATA5             | URDATA6         | UXDATA7             | UXDATA1         | GP07    | GP05        | V <sub>DD</sub> A18V2 | DDR11               | V <sub>SS</sub>     | V <sub>DD</sub> S18 | V <sub>SS</sub>     | V <sub>DD</sub> S18 | V <sub>SS</sub>      | V <sub>DD</sub> S18 | F |
| E | URDATA3             | URDATA4         | UXDATA0             | UXDATA6         | GP01    | DDRREF CLKN | DDRQ51P               | DDR10               | V <sub>DD</sub> S18 | DDRQ50P             | V <sub>DD</sub> S18 | DDRCA5              | DDRCE                | DDRBA2              | E |
| D | URDATA1             | URDATA2         | V <sub>DD</sub> S33 | V <sub>SS</sub> | GP02    | DDRREF CLKP | DDRQ51N               | DDR09               | DDR07               | DDRQ50N             | DDR03               | DDRRA5              | DDRCKE               | DDRBA1              | D |
| C | URCLK               | URDATA0         | UXCLAV              | UXDATA5         | GP06    | ALTDDRCLK   | DDRQ0M1               | DDR08               | DDR06               | DDRQ0M0             | DDR02               | DDRWE               | V <sub>REF</sub> STL | DDRBA0              | C |
| B | V <sub>SS</sub>     | URCLAV          | UXENB               | GP03            | GP04    | DDR14       | DDR12                 | V <sub>DD</sub> S18 | DDRRCVEN OUT0       | DDR05               | V <sub>DD</sub> S18 | DDR01               | DDRCLK OUT_N0        | DDR13               | B |
| A | V <sub>DD</sub> S33 | V <sub>SS</sub> | UXDATA4             | UXCLK           | GP00    | DDR15       | DDR13                 | V <sub>SS</sub>     | DDRRCVEN IN0        | DDR04               | V <sub>SS</sub>     | DDR00               | DDRCLK OUT_P0        | DDR12               | A |

## 2.7 Signal Groups Description

Figure 2-6 shows the CPU and core peripheral signal groups.

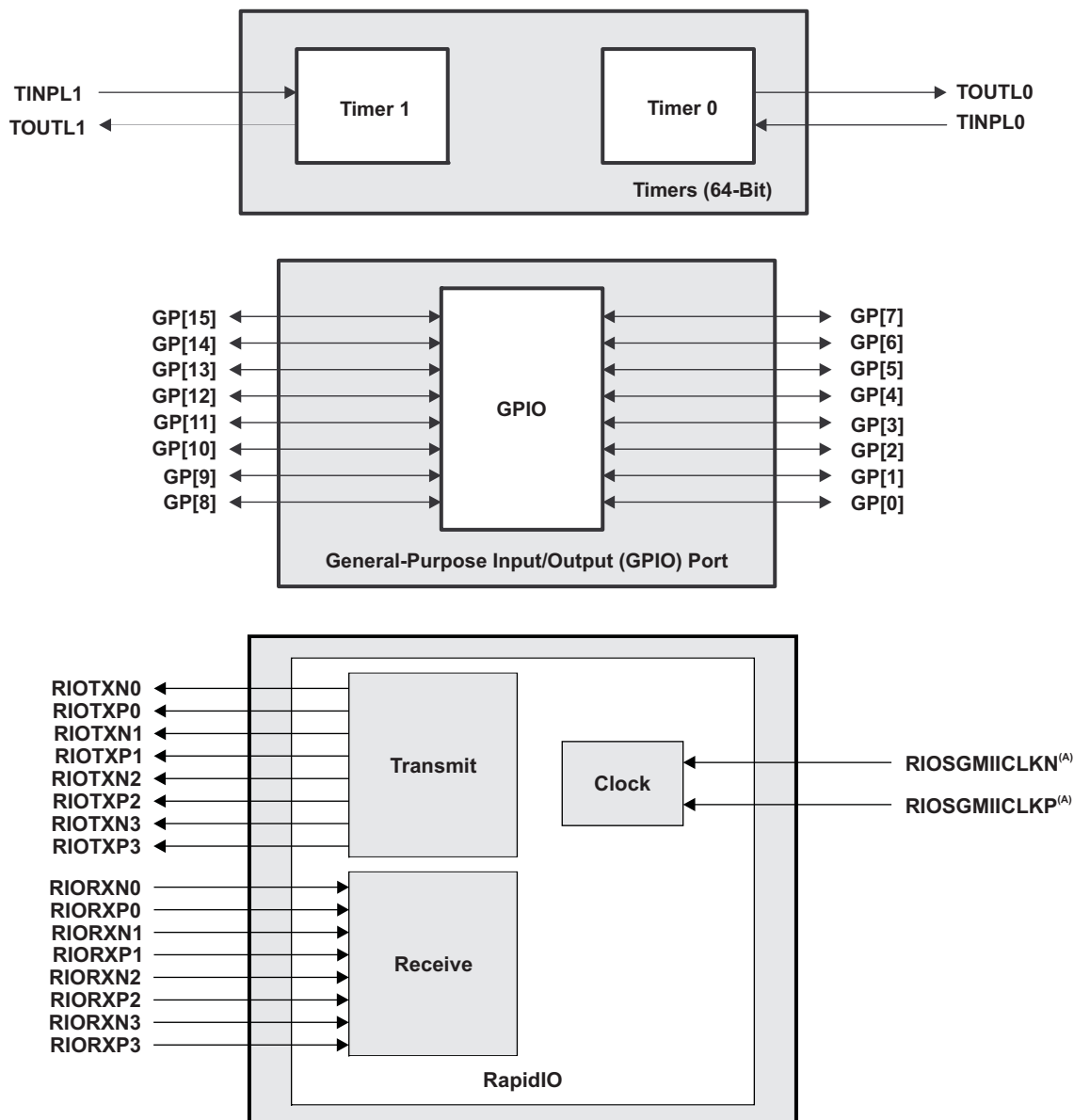
Figure 2-6 CPU and Peripheral Signals



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Figure 2-7 shows the timer peripheral I/O, the general purpose I/O, the Serial RapidIO, and the general purpose I/O reference clock, transmit, and receive signals.

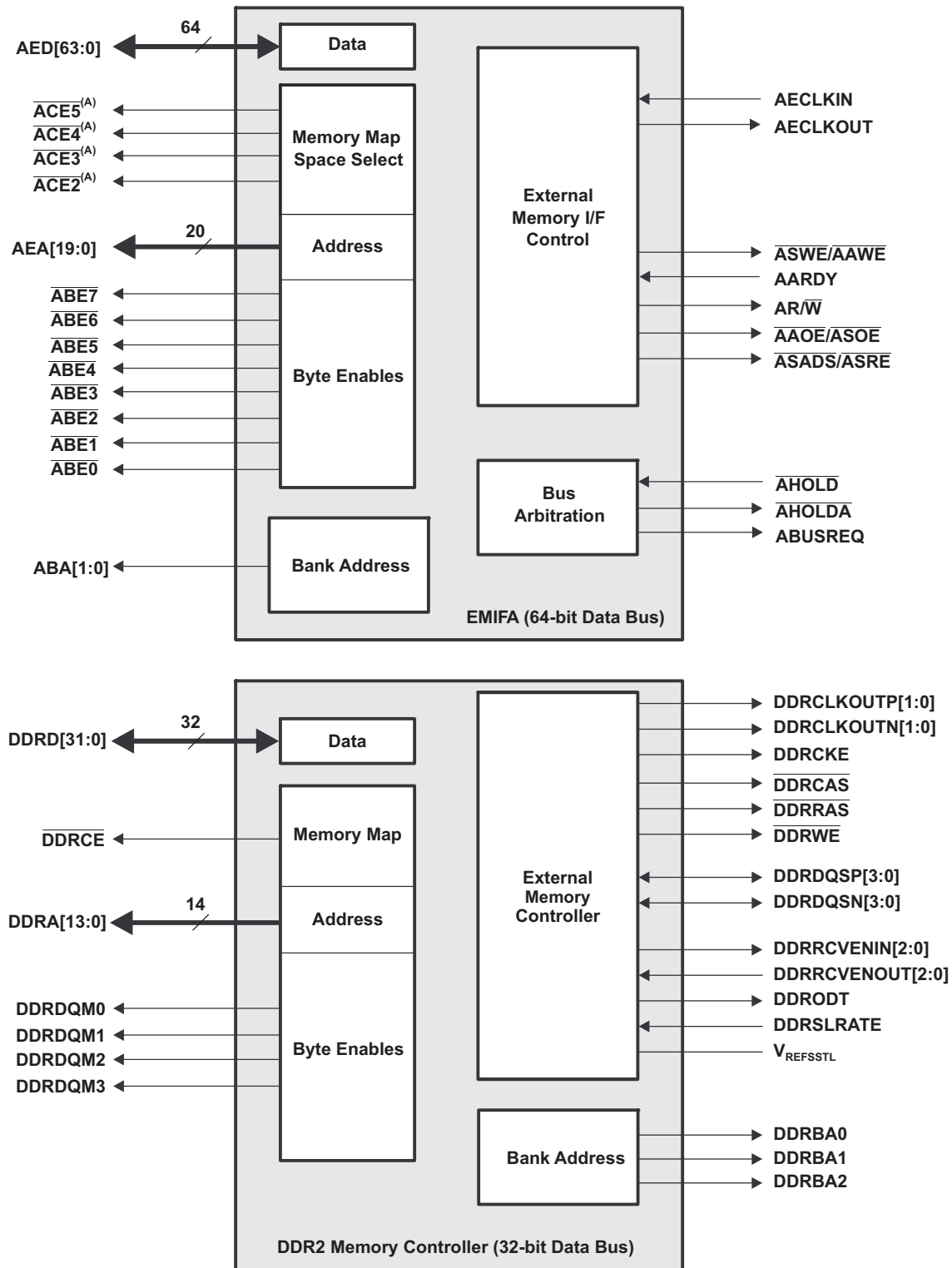
**Figure 2-7 Timers/GPIO/RapidIO Peripheral Signals**



(A) Reference clock to drive RapidIO and SGMII.

Figure 2-8 shows the EMIFA and DDR2 peripheral interfaces.

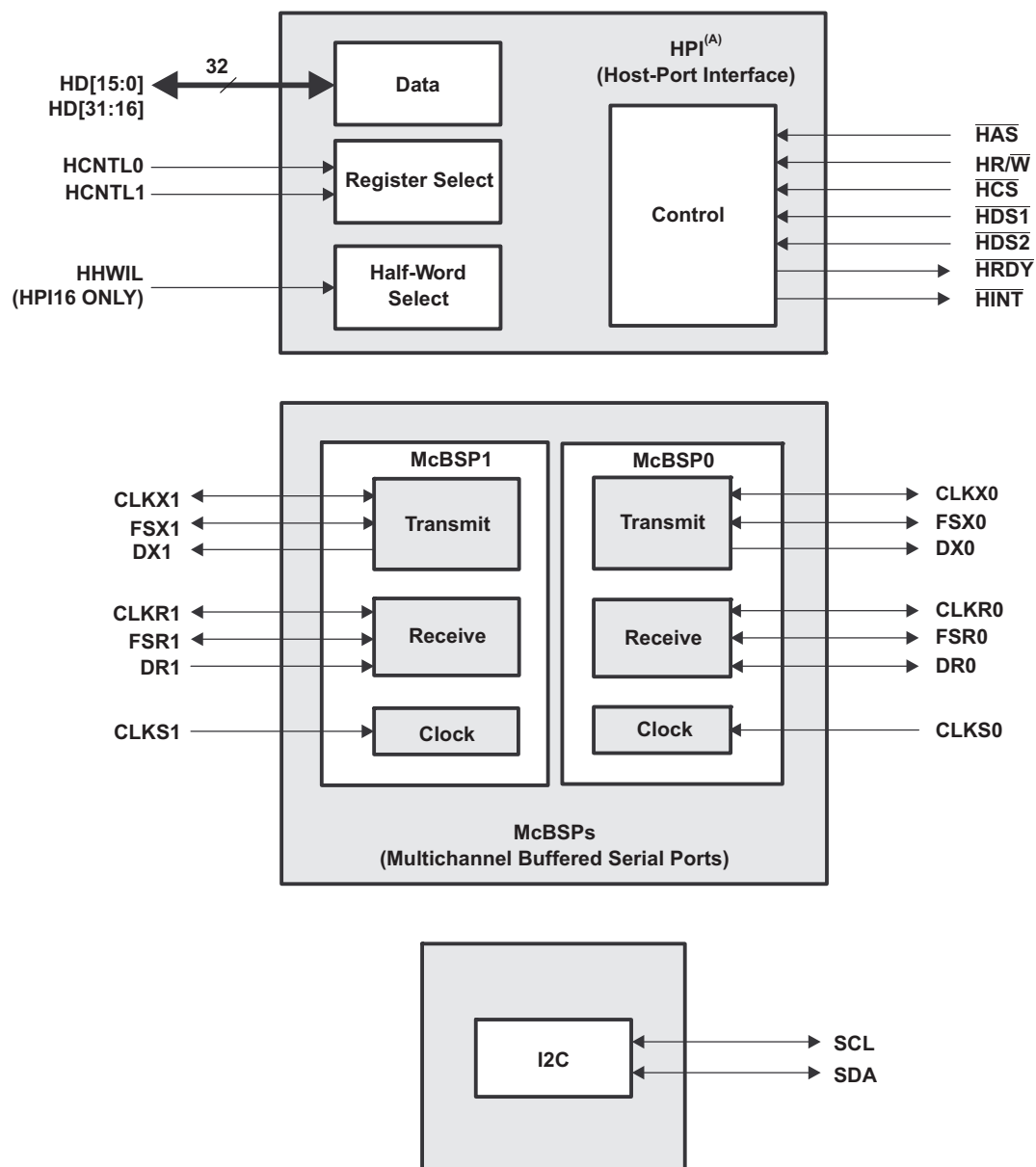
Figure 2-8 EMIFA and DDR2 Memory Controller Peripheral Signals



(A) The EMIFA ACE0 and ACE1 are not functionally supported on C6457 devices.

Figure 2-9 shows the HPI, McBSP, and I<sup>2</sup>C peripheral signals.

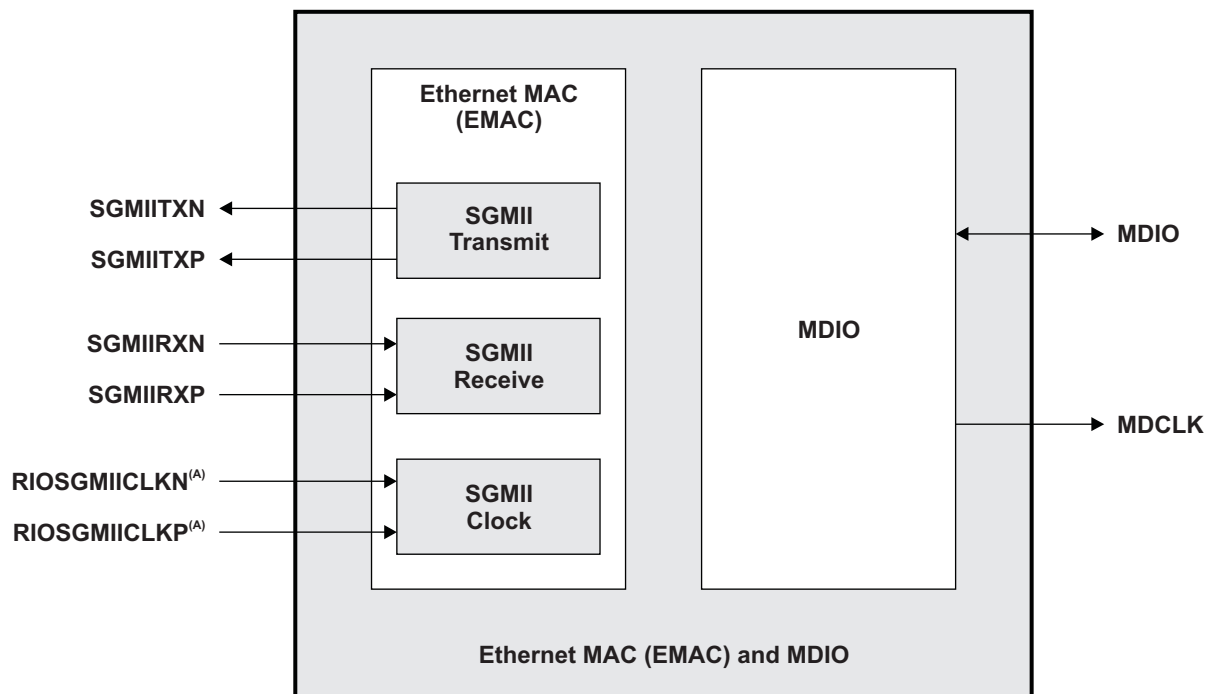
**Figure 2-9 HPI/McBSP/I<sup>2</sup>C Peripheral Signals**



(A) When the HPI is enabled, the number of HPI pins used depends on the HPI configuration (HPI16 or HPI32).

Figure 2-10 shows the EMAC/MDIO (SGMII) peripheral signals.

**Figure 2-10 EMAC/MDIO (SGMII) Peripheral Signals**

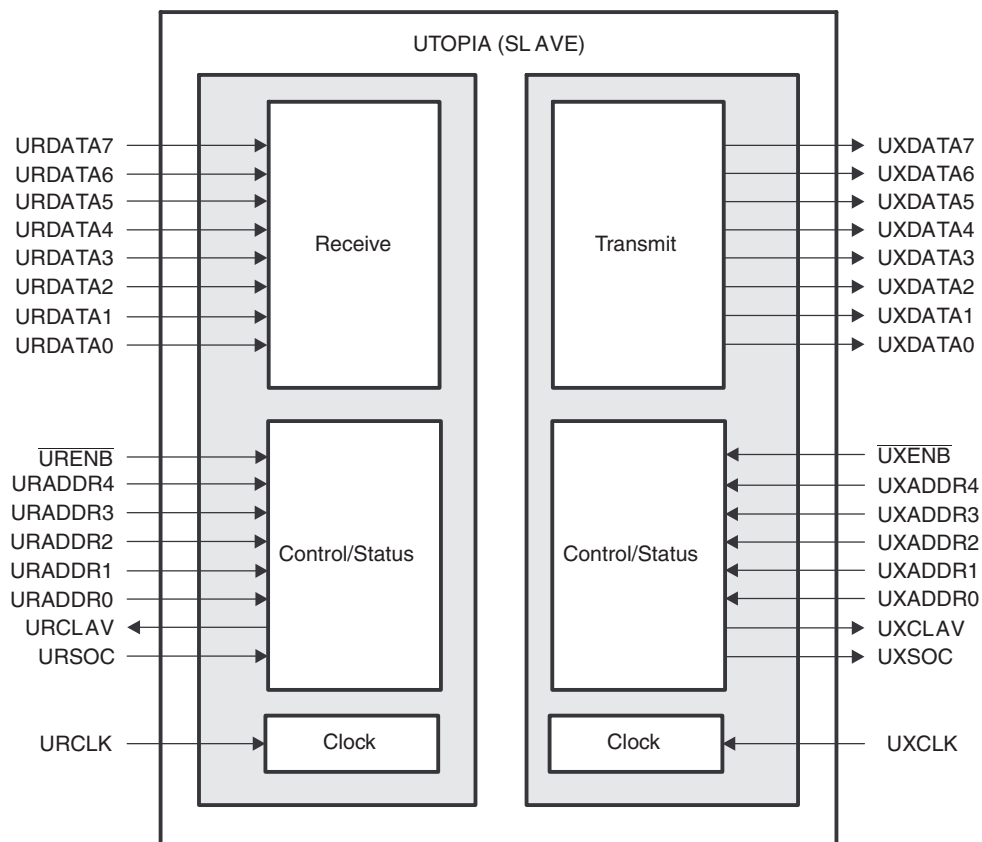


(A) Reference clock to drive RapidIO and SGMII.

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Figure 2-11 shows the UTOPIA peripheral signals.

**Figure 2-11 UTOPIA Peripheral Signals**





## 2.8 Terminal Functions

The terminal functions table [Table 2-6](#) identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type (I, O/Z, or I/O/Z), whether the pin has any internal pullup/pulldown resistors, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed/shared pins, and pullup/pulldown resistors, see Section 3 “[Device Configuration](#)” on page 59.

Use the symbol definitions in [Table 2-5](#) when reading [Table 2-6](#).

**Table 2-5 I/O Functional Symbol Definitions**

| Functional Symbol       | Definition                                                                                                                                                                                                                                                                                                                                                        | <a href="#">Table 2-6</a><br>Column Heading |
|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|
| IPD or IPU              | Internal 100- $\mu$ A pulldown or pullup is provided for this terminal. In most systems, a 1-k $\Omega$ resistor can be used to oppose the IPD/IPU. For more detailed information on pulldown/pullup resistors and situations in which external pulldown/pullup resistors are required, see Section 3.6 “ <a href="#">Pullup/Pulldown Resistors</a> ” on page 63. | IPD/IPU                                     |
| A                       | Analog signal                                                                                                                                                                                                                                                                                                                                                     | Type                                        |
| GND                     | Ground                                                                                                                                                                                                                                                                                                                                                            | Type                                        |
| I                       | Input terminal                                                                                                                                                                                                                                                                                                                                                    | Type                                        |
| O                       | Output terminal                                                                                                                                                                                                                                                                                                                                                   | Type                                        |
| S                       | Supply voltage                                                                                                                                                                                                                                                                                                                                                    | Type                                        |
| Z                       | Three-state terminal or high impedance                                                                                                                                                                                                                                                                                                                            | Type                                        |
| <b>End of Table 2-5</b> |                                                                                                                                                                                                                                                                                                                                                                   |                                             |

**Table 2-6 Terminal Functions (Part 1 of 22)**

| Signal Name                     | Ball No. | Type | IPD/IPU | Description                                                                                                                                                                                                                           |
|---------------------------------|----------|------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>CLOCK/PLL CONFIGURATIONS</b> |          |      |         |                                                                                                                                                                                                                                       |
| CORECLKN                        | AH7      | I    |         | Clock Input for PLL1 (differential).                                                                                                                                                                                                  |
| CORECLKP                        | AH6      | I    |         | Clock Input for PLL1 (differential).                                                                                                                                                                                                  |
| ALTCORECLK                      | AF6      |      |         | Alternate Core Clock (single-ended) input to main PLL [vs. CORECLK(N P)].                                                                                                                                                             |
| CORECLKSEL                      | AE6      |      |         | Core Clock Select. Selects between CORECLK(N P) and ALTCORECLK to the Main PLL.<br>• When CORECLKSEL = 0, it selects the differential clock [CORECLK(N P)].<br>• When CORECLKSEL = 1, it selects the single-ended clock [ALTCORECLK]. |
| SYSCLKOUT                       | AD7      | O/Z  | IPD     | SYSCLKOUT is the clock output at 1/10 (default rate) of the device speed.                                                                                                                                                             |
| DDRREFCLKN                      | E6       | I    |         | DDR Reference Clock Input to DDR PLL (differential).                                                                                                                                                                                  |
| DDRREFCLKP                      | D6       | I    |         | DDR Reference Clock Input to DDR PLL (differential).                                                                                                                                                                                  |
| ALTDDRCLK                       | C6       | I    |         | Alternate DDR Clock (single-ended) input to DDR PLL [vs. DDRREFCLK(N P)].                                                                                                                                                             |
| DDRCLKSEL                       | G6       | I    |         | DDR Clock Select. Selects between DDRREFCLK(N P) and ALTDDRCLK to the DDR PLL.<br>• When DDRCLKSEL = 0, it selects the differential clock [DDRREFCLK(N P)].<br>• When DDRCLKSEL = 1, it selects the single-ended clock [ALTDDRCLK].   |
| RIOSGMIICLKN                    | AG6      |      |         | RapidIO/SGMII Reference Clock to drive the RapidIO and SGMII SerDes (differential).                                                                                                                                                   |
| RIOSGMIICLKP                    | AG7      |      |         | RapidIO/SGMII Reference Clock to drive the RapidIO and SGMII SerDes (differential).                                                                                                                                                   |

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**Table 2-6 Terminal Functions (Part 2 of 22)**

| Signal Name                                           | Ball No. | Type  | IPD/IPU | Description                                                                                                                                                                                                                                   |
|-------------------------------------------------------|----------|-------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| JTAG EMULATION                                        |          |       |         |                                                                                                                                                                                                                                               |
| TMS                                                   | Y2       | I     | IPU     | JTAG test-port mode select                                                                                                                                                                                                                    |
| TDO                                                   | AF1      | O/Z   |         | JTAG test-port data out                                                                                                                                                                                                                       |
| TDI                                                   | AB1      | I     | IPU     | JTAG test-port data in                                                                                                                                                                                                                        |
| TCK                                                   | AH3      | I     | IPU     | JTAG test-port clock                                                                                                                                                                                                                          |
| TRST                                                  | AE2      | I     | IPD     | JTAG test-port reset. For IEEE 1149.1 JTAG compatibility, see 7.22.3.1 <a href="#">“IEEE 1149.1 JTAG Compatibility Statement”</a> on page 206.                                                                                                |
| EMU0(3)                                               | AD5      | I/O/Z | IPU     | Emulation pin 0                                                                                                                                                                                                                               |
| EMU1(3)                                               | AE5      |       |         | Emulation pin 1                                                                                                                                                                                                                               |
| EMU2                                                  | AH5      |       |         | Emulation pin 2                                                                                                                                                                                                                               |
| EMU3                                                  | AE4      |       |         | Emulation pin 3                                                                                                                                                                                                                               |
| EMU4                                                  | AH4      |       |         | Emulation pin 4                                                                                                                                                                                                                               |
| EMU5                                                  | AG4      |       |         | Emulation pin 5                                                                                                                                                                                                                               |
| EMU6                                                  | AF4      |       |         | Emulation pin 6                                                                                                                                                                                                                               |
| EMU7                                                  | AG2      |       |         | Emulation pin 7                                                                                                                                                                                                                               |
| EMU8                                                  | AG3      |       |         | Emulation pin 8                                                                                                                                                                                                                               |
| EMU9                                                  | AD4      |       |         | Emulation pin 9                                                                                                                                                                                                                               |
| EMU10                                                 | AE3      |       |         | Emulation pin 10                                                                                                                                                                                                                              |
| EMU11                                                 | AF2      |       |         | Emulation pin 11                                                                                                                                                                                                                              |
| EMU12                                                 | AE1      |       |         | Emulation pin 12                                                                                                                                                                                                                              |
| EMU13                                                 | AF3      |       |         | Emulation pin 13                                                                                                                                                                                                                              |
| EMU14                                                 | AC1      |       |         | Emulation pin 14                                                                                                                                                                                                                              |
| EMU15                                                 | AD1      |       |         | Emulation pin 15                                                                                                                                                                                                                              |
| EMU16                                                 | AD3      |       |         | Emulation pin 16                                                                                                                                                                                                                              |
| EMU17                                                 | AA1      |       |         | Emulation pin 17                                                                                                                                                                                                                              |
| EMU18                                                 | AC2      |       |         | Emulation pin 18                                                                                                                                                                                                                              |
| RESETS, INTERRUPTS, AND GENERAL-PURPOSE INPUT/OUTPUTS |          |       |         |                                                                                                                                                                                                                                               |
| RESET                                                 | AH23     | I     |         | Device reset                                                                                                                                                                                                                                  |
| NMI                                                   | AE19     | I     | IPD     | Nonmaskable interrupt, edge-driven (rising edge).<br><b>NOTE:</b> Any noise on the NMI pin may trigger an NMI interrupt. Therefore, if the NMI pin is not used, it is recommended that the NMI pin be grounded instead of relying on the IPD. |
| RESETSTAT                                             | AF23     | O     |         | Reset Status pin. The RESETSTAT pin indicates when the device is in reset                                                                                                                                                                     |
| POR                                                   | AG22     | I     |         | Power on reset.                                                                                                                                                                                                                               |

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**Table 2-6 Terminal Functions (Part 3 of 22)**

| Signal Name               | Ball No. | Type  | IPD/IPU | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------------------------|----------|-------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GP15                      | F23      | I/O/Z | IPD     | General-purpose input/output (GPIO) pins (I/O/Z). GPIO[15:0] pins are multiplexed at power-on reset for configuration latching: <ul style="list-style-type: none"><li>• GPIO[0] is mapped to LENDIAN</li><li>• GPIO[4:1] are mapped to BOOTMODE[3:0] (see Section 2.5 “Boot Modes Supported” on page 21)</li><li>• GPIO[8:5] are mapped to DEVNUM[3:0]</li><li>• GPIO[13:9] are mapped to CFGGPP[4:0]</li><li>• GPIO[14] is mapped to HPIWIDTH</li><li>• GPIO[15] is mapped to ECLKINSEL</li></ul> |
| GP14                      | D23      |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GP13                      | C23      |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GP12                      | D24      |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GP11                      | C25      |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GP10                      | A25      |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GP09                      | C24      |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GP08                      | B25      |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GP07                      | F5       |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GP06                      | C5       |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GP05                      | F6       |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GP04                      | B5       |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GP03                      | B4       |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GP02                      | D5       |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GP01                      | E5       |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GP00                      | A5       |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| HOST PORT INTERFACE (HPI) |          |       |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| HINT                      | L4       | I/O/Z |         | Host interrupt from DSP to host (O/Z)                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| HCNTL1                    | M5       | I/O/Z |         | Host control -selects between control, address, or data registers (I) [default]                                                                                                                                                                                                                                                                                                                                                                                                                    |
| HCNTL0                    | L6       | I/O/Z |         | Host control -selects between control, address, or data registers (I) [default]                                                                                                                                                                                                                                                                                                                                                                                                                    |
| HHWIL                     | L3       | I/O/Z |         | Host half-word select — first or second half-word (not necessarily high or low order). For HPI16 bus width selection only] (I) [default]                                                                                                                                                                                                                                                                                                                                                           |
| HR/W                      | K5       | I/O/Z |         | Host read or write select (I) [default]                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| HAS                       | M4       | I/O/Z |         | Host address strobe (I) [default]                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| HCS                       | M3       | I/O/Z |         | Host chip select (I) [default]                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| HDS1                      | L2       | I/O/Z |         | Host data strobe 1 (I) [default]                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| HDS2                      | L5       | I/O/Z |         | Host data strobe 2 (I) [default]                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| HRDY                      | M6       | I/O/Z |         | Host ready from DSP to host (O/Z) [default]                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

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**Table 2-6 Terminal Functions (Part 4 of 22)**

| Signal Name | Ball No. | Type  | IPD/IPU | Description                                  |
|-------------|----------|-------|---------|----------------------------------------------|
| HD31        | P3       | I/O/Z |         | Host-port data [31:16] pin (I/O/Z) [default] |
| HD30        | N6       |       |         |                                              |
| HD29        | T5       |       |         |                                              |
| HD28        | P6       |       |         |                                              |
| HD27        | U5       |       |         |                                              |
| HD26        | N1       |       |         |                                              |
| HD25        | V2       |       |         |                                              |
| HD24        | M1       |       |         |                                              |
| HD23        | U6       |       |         |                                              |
| HD22        | V1       |       |         |                                              |
| HD21        | U1       |       |         |                                              |
| HD20        | N2       |       |         |                                              |
| HD19        | T1       |       |         |                                              |
| HD18        | P2       |       |         |                                              |
| HD17        | R1       | I/O/Z |         | Host-port data [15:0] pin (I/O/Z) [default]  |
| HD16        | N3       |       |         |                                              |
| HD15        | T2       |       |         |                                              |
| HD14        | P4       |       |         |                                              |
| HD13        | U2       |       |         |                                              |
| HD12        | N4       |       |         |                                              |
| HD11        | W1       |       |         |                                              |
| HD10        | R5       |       |         |                                              |
| HD09        | T3       |       |         |                                              |
| HD08        | N5       |       |         |                                              |
| HD07        | R4       |       |         |                                              |
| HD06        | T6       |       |         |                                              |
| HD05        | U4       |       |         |                                              |
| HD04        | R6       |       |         |                                              |
| HD03        | T4       |       |         |                                              |
| HD02        | P5       |       |         |                                              |
| HD01        | K6       |       |         |                                              |
| HD00        | W2       |       |         |                                              |

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**Table 2-6 Terminal Functions (Part 5 of 22)**

| Signal Name                                                    | Ball No. | Type | IPD/IPU | Description                                                                                                                                                                                                                                                                                                                                                       |
|----------------------------------------------------------------|----------|------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EMIFA (64-BIT) — CONTROL SIGNALS COMMON TO ALL TYPES OF MEMORY |          |      |         |                                                                                                                                                                                                                                                                                                                                                                   |
| ABA1                                                           | V24      | O/Z  | IPD     | EMIFA bank address control (ABA[1:0]). Active-low bank selects for the 64-bit EMIFA.<br>• When interfacing to 16-bit Asynchronous devices, ABA1 carries bit 1 of the byte address.<br>• For an 8-bit Asynchronous interface, ABA[1:0] are used to carry bits 1 and 0 of the byte address.                                                                         |
| ABA0                                                           | V25      | O/Z  | IPD     |                                                                                                                                                                                                                                                                                                                                                                   |
| $\overline{ACE5}$                                              | V26      | O/Z  | IPU     | EMIFA memory space enables.<br>• Enabled by bits 28 through 31 of the word address<br>• Only one pin is asserted during any external data access<br><b>NOTE:</b> The C6457 device does not have ACE0 and ACE1 pins.                                                                                                                                               |
| $\overline{ACE4}$                                              | U27      |      |         |                                                                                                                                                                                                                                                                                                                                                                   |
| $\overline{ACE3}$                                              | W25      |      |         |                                                                                                                                                                                                                                                                                                                                                                   |
| $\overline{ACE2}$                                              | W26      |      |         |                                                                                                                                                                                                                                                                                                                                                                   |
| $\overline{ABE07}$                                             | W28      | O/Z  | IPU     | EMIFA byte-enable control.<br>• Decoded from the low-order address bits. The number of address bits or byte enables used depends on the width of external memory.<br>• Byte-write enables for most types of memory.                                                                                                                                               |
| $\overline{ABE06}$                                             | L25      |      |         |                                                                                                                                                                                                                                                                                                                                                                   |
| $\overline{ABE05}$                                             | L28      |      |         |                                                                                                                                                                                                                                                                                                                                                                   |
| $\overline{ABE04}$                                             | L27      |      |         |                                                                                                                                                                                                                                                                                                                                                                   |
| $\overline{ABE03}$                                             | Y28      |      |         |                                                                                                                                                                                                                                                                                                                                                                   |
| $\overline{ABE02}$                                             | W27      |      |         |                                                                                                                                                                                                                                                                                                                                                                   |
| $\overline{ABE01}$                                             | Y24      |      |         |                                                                                                                                                                                                                                                                                                                                                                   |
| $\overline{ABE00}$                                             | Y25      |      |         |                                                                                                                                                                                                                                                                                                                                                                   |
| EMIFA (64-BIT) — BUS ARBITRATION                               |          |      |         |                                                                                                                                                                                                                                                                                                                                                                   |
| $\overline{AHOLDA}$                                            | N25      | O    | IPU     | EMIFA hold-request-acknowledge to the host                                                                                                                                                                                                                                                                                                                        |
| $\overline{AHOLD}$                                             | R28      | I    | IPU     | EMIFA hold request from the host                                                                                                                                                                                                                                                                                                                                  |
| ABUSREQ                                                        | L26      | O    | IPU     | EMIFA bus request output                                                                                                                                                                                                                                                                                                                                          |
| EMIFA (64-BIT) — ASYNCHRONOUS/SYNCHRONOUS MEMORY CONTROL       |          |      |         |                                                                                                                                                                                                                                                                                                                                                                   |
| AECLKIN                                                        | N28      | I    | IPD     | EMIFA external input clock. The EMIFA input clock (AECLKIN or SYSCLK7 clock) is selected at reset via the pullup/pulldown resistor on the GPIO[15] pin.<br><b>NOTE:</b> AECLKIN is the default for the EMIFA input clock.                                                                                                                                         |
| AECLKOUT                                                       | V28      | O/Z  | IPD     | EMIFA output clock [at EMIFA input clock (AECLKIN or SYSCLK7) frequency]                                                                                                                                                                                                                                                                                          |
| $\overline{AAWE}/\overline{ASWE}$                              | AA24     | O/Z  | IPU     | Asynchronous memory write-enable/Programmable synchronous interface write-enable                                                                                                                                                                                                                                                                                  |
| AARDY                                                          | K28      | I    | IPU     | Asynchronous memory ready input                                                                                                                                                                                                                                                                                                                                   |
| $\overline{AR}/\overline{W}$                                   | W24      | O/Z  | IPU     | Asynchronous memory read/write                                                                                                                                                                                                                                                                                                                                    |
| $\overline{AAOE}/\overline{ASOE}$                              | AE25     | O/Z  | IPU     | Asynchronous/Programmable synchronous memory output-enable                                                                                                                                                                                                                                                                                                        |
| $\overline{ASADS}/\overline{ASRE}$                             | R25      | O/Z  | IPU     | Programmable synchronous address strobe or read-enable<br>• For programmable synchronous interface, the R_ENABLE field in the Chip Select x Configuration Register selects between ASADS and ASRE:<br>– If R_ENABLE = 0, then the ASADS/ASRE signal functions as the ASADS signal.<br>– If R_ENABLE = 1, then the ASADS/ASRE signal functions as the ASRE signal. |

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**Table 2-6 Terminal Functions (Part 6 of 22)**

| Signal Name              | Ball No. | Type | IPD/IPU | Description                                          |
|--------------------------|----------|------|---------|------------------------------------------------------|
| EMIFA (64-BIT) — ADDRESS |          |      |         |                                                      |
| AEA19                    | P24      | O/Z  | IPD     | EMIFA external address (word address) ( <b>O/Z</b> ) |
| AEA18                    | M25      |      |         |                                                      |
| AEA17                    | M24      |      |         |                                                      |
| AEA16                    | P25      |      |         |                                                      |
| AEA15                    | P26      |      |         |                                                      |
| AEA14                    | T24      |      |         |                                                      |
| AEA13                    | R26      | O/Z  | IPU     |                                                      |
| AEA12                    | N27      | O/Z  | IPD     |                                                      |
| AEA11                    | T25      |      |         |                                                      |
| AEA10                    | N24      | O/Z  | IPD     |                                                      |
| AEA09                    | M26      |      |         |                                                      |
| AEA08                    | R24      |      |         |                                                      |
| AEA07                    | N26      |      |         |                                                      |
| AEA06                    | T28      |      |         |                                                      |
| AEA05                    | U28      |      |         |                                                      |
| AEA04                    | R27      |      |         |                                                      |
| AEA03                    | T27      |      |         |                                                      |
| AEA02                    | T26      |      |         |                                                      |
| AEA01                    | U26      |      |         |                                                      |
| AEA00                    | U25      |      |         |                                                      |

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**Table 2-6 Terminal Functions (Part 7 of 22)**

| Signal Name                  | Ball No. | Type  | IPD/IPU | Description         |
|------------------------------|----------|-------|---------|---------------------|
| <b>EMIFA (64-BIT) — DATA</b> |          |       |         |                     |
| AED63                        | G24      | I/O/Z | IPU     | EMIFA external data |
| AED62                        | A26      |       |         |                     |
| AED61                        | C26      |       |         |                     |
| AED60                        | C27      |       |         |                     |
| AED59                        | E26      |       |         |                     |
| AED58                        | D27      |       |         |                     |
| AED57                        | D25      |       |         |                     |
| AED56                        | F26      |       |         |                     |
| AED55                        | H24      |       |         |                     |
| AED54                        | H25      |       |         |                     |
| AED53                        | D26      |       |         |                     |
| AED52                        | F27      |       |         |                     |
| AED51                        | B27      |       |         |                     |
| AED50                        | G26      |       |         |                     |
| AED49                        | B26      |       |         |                     |
| AED48                        | G27      |       |         |                     |
| AED47                        | J24      |       |         |                     |
| AED46                        | K25      |       |         |                     |
| AED45                        | J25      |       |         |                     |
| AED44                        | J26      |       |         |                     |
| AED43                        | H26      |       |         |                     |
| AED42                        | J27      |       |         |                     |
| AED41                        | C28      |       |         |                     |
| AED40                        | J28      |       |         |                     |
| AED39                        | D28      |       |         |                     |
| AED38                        | K24      |       |         |                     |
| AED37                        | F28      |       |         |                     |
| AED36                        | G25      |       |         |                     |
| AED35                        | G28      |       |         |                     |
| AED34                        | K27      |       |         |                     |
| AED33                        | L24      |       |         |                     |
| AED32                        | K26      |       |         |                     |
| AED31                        | Y26      |       |         |                     |
| AED30                        | AF28     |       |         |                     |
| AED29                        | AA28     |       |         |                     |
| AED28                        | AB26     |       |         |                     |
| AED27                        | Y27      |       |         |                     |
| AED26                        | AB25     |       |         |                     |

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**Table 2-6 Terminal Functions (Part 8 of 22)**

| Signal Name | Ball No. | Type  | IPD/IPU | Description         |
|-------------|----------|-------|---------|---------------------|
| AED25       | AA26     | I/O/Z | IPU     | EMIFA external data |
| AED24       | AB24     |       |         |                     |
| AED23       | AA25     |       |         |                     |
| AED22       | AA27     |       |         |                     |
| AED21       | AC28     |       |         |                     |
| AED20       | AG27     |       |         |                     |
| AED19       | AE28     |       |         |                     |
| AED18       | AF27     |       |         |                     |
| AED17       | AD28     |       |         |                     |
| AED16       | AF26     |       |         |                     |
| AED15       | AE27     |       |         |                     |
| AED14       | AG25     |       |         |                     |
| AED13       | AC27     |       |         |                     |
| AED12       | AD26     |       |         |                     |
| AED11       | AC25     |       |         |                     |
| AED10       | AE26     |       |         |                     |
| AED09       | AF25     |       |         |                     |
| AED08       | AC26     |       |         |                     |
| AED07       | AD25     |       |         |                     |
| AED06       | AH26     |       |         |                     |
| AED05       | AH25     |       |         |                     |
| AED04       | AD27     |       |         |                     |
| AED03       | AF24     |       |         |                     |
| AED02       | AG26     |       |         |                     |
| AED01       | AE24     |       |         |                     |
| AED00       | AC24     |       |         |                     |

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**Table 2-6 Terminal Functions (Part 9 of 22)**

| Signal Name                   | Ball No. | Type | IPD/IPU | Description                                                        |
|-------------------------------|----------|------|---------|--------------------------------------------------------------------|
| <b>DDR2 MEMORY CONTROLLER</b> |          |      |         |                                                                    |
| DDRQDM0                       | C10      | O/Z  |         | DDR2 EMIF Data Masks                                               |
| DDRQDM1                       | C7       |      |         |                                                                    |
| DDRQDM2                       | C19      |      |         |                                                                    |
| DDRQDM3                       | C22      |      |         |                                                                    |
| DDRBA0                        | C14      | O/Z  |         | DDR Bank Address                                                   |
| DDRBA1                        | D14      |      |         |                                                                    |
| DDRBA2                        | E14      |      |         |                                                                    |
| DDRA00                        | F17      | O/Z  |         | DDR2 EMIF Address Bus                                              |
| DDRA01                        | E17      |      |         |                                                                    |
| DDRA02                        | D17      |      |         |                                                                    |
| DDRA03                        | C17      |      |         |                                                                    |
| DDRA04                        | E16      |      |         |                                                                    |
| DDRA05                        | D16      |      |         |                                                                    |
| DDRA06                        | C16      |      |         |                                                                    |
| DDRA07                        | B16      |      |         |                                                                    |
| DDRA08                        | D15      |      |         |                                                                    |
| DDRA09                        | C15      |      |         |                                                                    |
| DDRA10                        | B15      |      |         |                                                                    |
| DDRA11                        | A15      |      |         |                                                                    |
| DDRA12                        | A14      |      |         |                                                                    |
| DDRA13                        | B14      |      |         |                                                                    |
| DDRCLKOUTP0                   | A13      | O/Z  |         | DDR2 EMIF Output Clocks to drive SDRAMs (one clock pair per SDRAM) |
| DDRCLKOUTN0                   | B13      |      |         |                                                                    |
| DDRCLKOUTP1                   | A17      |      |         |                                                                    |
| DDRCLKOUTN1                   | B17      |      |         |                                                                    |

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**Table 2-6 Terminal Functions (Part 10 of 22)**

| Signal Name                | Ball No. | Type | IPD/IPU | Description                     |
|----------------------------|----------|------|---------|---------------------------------|
| DDR00                      | A12      | O/Z  |         | DDR2 EMIF Data Bus              |
| DDR01                      | B12      |      |         |                                 |
| DDR02                      | C11      |      |         |                                 |
| DDR03                      | D11      |      |         |                                 |
| DDR04                      | A10      |      |         |                                 |
| DDR05                      | B10      |      |         |                                 |
| DDR06                      | C9       |      |         |                                 |
| DDR07                      | D9       |      |         |                                 |
| DDR08                      | C8       |      |         |                                 |
| DDR09                      | D8       |      |         |                                 |
| DDR10                      | E8       |      |         |                                 |
| DDR11                      | F8       |      |         |                                 |
| DDR12                      | B7       |      |         |                                 |
| DDR13                      | A7       |      |         |                                 |
| DDR14                      | B6       |      |         |                                 |
| DDR15                      | A6       |      |         |                                 |
| DDR16                      | B18      |      |         |                                 |
| DDR17                      | A18      |      |         |                                 |
| DDR18                      | C18      |      |         |                                 |
| DDR19                      | D18      |      |         |                                 |
| DDR20                      | A20      |      |         |                                 |
| DDR21                      | B20      |      |         |                                 |
| DDR22                      | C20      |      |         |                                 |
| DDR23                      | D20      |      |         |                                 |
| DDR24                      | A21      |      |         |                                 |
| DDR25                      | B21      |      |         |                                 |
| DDR26                      | C21      |      |         |                                 |
| DDR27                      | D21      |      |         |                                 |
| DDR28                      | A23      |      |         |                                 |
| DDR29                      | B23      |      |         |                                 |
| DDR30                      | A24      |      |         |                                 |
| DDR31                      | B24      |      |         |                                 |
| $\overline{\text{DDRCAS}}$ | E12      | O/Z  |         | DDR2 EMIF Column Address Strobe |
| $\overline{\text{DDRRAS}}$ | D12      | O/Z  |         | DDR2 EMIF Row Address Strobe    |
| $\overline{\text{DDRC E}}$ | E13      | O/Z  |         | DDR2 EMIF Chip Enable           |
| $\overline{\text{DDRWE}}$  | C12      | O/Z  |         | DDR2 EMIF Write Enable          |
| DDRCKE                     | D13      | O/Z  |         | DDR2 EMIF Clock Enable          |

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**Table 2-6 Terminal Functions (Part 11 of 22)**

| Signal Name                                      | Ball No. | Type  | IPD/IPU | Description                                                                                        |
|--------------------------------------------------|----------|-------|---------|----------------------------------------------------------------------------------------------------|
| DDRQ50P                                          | E10      | I/O/Z |         | DDR2 EMIF Data Strobe                                                                              |
| DDRQ50N                                          | D10      |       |         |                                                                                                    |
| DDRQ51P                                          | E7       |       |         |                                                                                                    |
| DDRQ51N                                          | D7       |       |         |                                                                                                    |
| DDRQ52P                                          | E19      |       |         |                                                                                                    |
| DDRQ52N                                          | D19      |       |         |                                                                                                    |
| DDRQ53P                                          | E22      |       |         |                                                                                                    |
| DDRQ53N                                          | D22      |       |         |                                                                                                    |
| DDRRVCENIN0                                      | A9       | I     |         | DDR2 EMIF Data Strobe Gate Input/Outputs to help meet DDR Timing                                   |
| DDRRVCENOUT0                                     | B9       | O/Z   |         |                                                                                                    |
| DDRRVCENIN1                                      | E20      | I     |         |                                                                                                    |
| DDRRVCENOUT1                                     | F20      | O/Z   |         |                                                                                                    |
| DDRODT                                           | E15      | O/Z   |         | DDR2 EMIF On Die Termination Outputs used to set termination on the SDRAMs                         |
| DDSLRATE                                         | A27      | I     |         | DDR2 Slew rate control                                                                             |
| V <sub>REFSSTL</sub>                             | C13      | A     |         | Reference Voltage Input for SSTL18 buffers used by DDR2 EMIF (V <sub>DD518_2</sub> )               |
| <b>TIMER 1</b>                                   |          |       |         |                                                                                                    |
| TOUT1L                                           | AF19     | O/Z   | IPD     | Timer 1 output pin for lower 32-bit counter                                                        |
| TINP1L                                           | AG19     | I     | IPD     | Timer 1 input pin for lower 32-bit counter                                                         |
| <b>TIMER 0</b>                                   |          |       |         |                                                                                                    |
| TOUT0L                                           | AG20     | O/Z   | IPD     | Timer 0 output pin for lower 32-bit counter                                                        |
| TINP0L                                           | AH20     | I     | IPD     | Timer 0 input pin for lower 32-bit counter                                                         |
| <b>INTER-INTEGRATED CIRCUIT (I<sup>2</sup>C)</b> |          |       |         |                                                                                                    |
| SCL                                              | F24      | I/O/Z |         | I <sup>2</sup> C clock. When the I <sup>2</sup> C module is used, use an external pullup resistor. |
| SDA                                              | E24      | I/O/Z |         | I <sup>2</sup> C data. When I <sup>2</sup> C is used, ensure there is an external pullup resistor. |
| <b>MULTICHANNEL BUFFERED SERIAL PORT (McBSP)</b> |          |       |         |                                                                                                    |
| CLKS0                                            | AA4      | I     | IPD     | McBSP0 Module Clock                                                                                |
| CLKR0                                            | Y5       | I/O/Z | IPD     | McBSP0 Receive Clock                                                                               |
| CLKX0                                            | AB3      | I/O/Z | IPD     | McBSP0 Transmit Clock                                                                              |
| DR0                                              | Y6       | I     | IPD     | McBSP0 Receive Data                                                                                |
| DX0                                              | W6       | O/Z   | IPD     | McBSP0 Transmit Data                                                                               |
| FSR0                                             | V4       | I/O/Z | IPD     | McBSP0 Receive Frame Sync                                                                          |
| FSX0                                             | W4       | I/O/Z | IPD     | McBSP0 Transmit Frame Sync                                                                         |
| CLKS1                                            | Y1       | I     | IPD     | McBSP1 Module Clock                                                                                |
| CLKR1                                            | Y4       | I/O/Z | IPD     | McBSP1 Receive Clock                                                                               |
| CLKX1                                            | AA3      | I/O/Z | IPD     | McBSP1 Transmit Clock                                                                              |
| DR1                                              | W3       | I     | IPD     | McBSP1 Receive Data                                                                                |
| DX1                                              | Y3       | O/Z   | IPD     | McBSP1 Transmit Data                                                                               |
| FSR1                                             | V5       | I/O/Z | IPD     | McBSP1 Receive Frame Sync                                                                          |
| FSX1                                             | W5       | I/O/Z | IPD     | McBSP1 Transmit Frame Sync                                                                         |

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**Table 2-6 Terminal Functions (Part 12 of 22)**

| Signal Name                                                                                     | Ball No. | Type | IPD/IPU | Description                                                                                                                                                                                                                               |
|-------------------------------------------------------------------------------------------------|----------|------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| UNIVERSAL TEST AND OPERATIONS PHY INTERFACE for ASYNCHRONOUS TRANSFER MODE (ATM) [UTOPIA SLAVE] |          |      |         |                                                                                                                                                                                                                                           |
| UTOPIA SLAVE (ATM CONTROLLER) — TRANSMIT INTERFACE                                              |          |      |         |                                                                                                                                                                                                                                           |
| UXCLK                                                                                           | A4       | I    |         | Source clock for UTOPIA transmit driven by Master ATM Controller.                                                                                                                                                                         |
| UXCLAV                                                                                          | C3       | O/Z  |         | Transmit cell available status output signal from UTOPIA Slave.<br>• 0 indicates a complete cell is NOT available for transmit<br>• 1 indicates a complete cell is available for transmit                                                 |
| $\overline{\text{UXENB}}$                                                                       | B3       | I    |         | UTOPIA transmit interface enable input signal. Asserted by the Master ATM Controller to indicate that the UTOPIA Slave should put out on the Transmit Data Bus the first byte of valid data and the UXSOC signal in the next clock cycle. |
| UXSOC                                                                                           | G4       | O/Z  |         | Transmit Start-of-Cell signal. This signal is output by the UTOPIA Slave on the rising edge of the UXCLK, indicating that the first valid byte of the cell is available on the 8-bit Transmit Data Bus (UXDATA[7:0]).                     |
| UXADDR4                                                                                         | J4       | I    |         | UTOPIA transmit address pins (UXADDR[4:0]) (I) 5-bit Slave transmit address input pins driven by the Master ATM Controller to identify and select one of the Slave devices (up to 31 possible) in the ATM System.                         |
| UXADDR3                                                                                         | H5       |      |         |                                                                                                                                                                                                                                           |
| UXADDR2                                                                                         | K3       |      |         |                                                                                                                                                                                                                                           |
| UXADDR1                                                                                         | J5       |      |         |                                                                                                                                                                                                                                           |
| UXADDR0                                                                                         | H4       |      |         |                                                                                                                                                                                                                                           |
| UXDATA7                                                                                         | F3       | O/Z  |         | UTOPIA 8-bit transmit data bus (I/O/Z) Using the Transmit Data Bus, the UTOPIA Slave (on the rising edge of the UXCLK) transmits the 8-bit ATM cells to the Master ATM Controller.                                                        |
| UXDATA6                                                                                         | E4       |      |         |                                                                                                                                                                                                                                           |
| UXDATA5                                                                                         | C4       |      |         |                                                                                                                                                                                                                                           |
| UXDATA4                                                                                         | A3       |      |         |                                                                                                                                                                                                                                           |
| UXDATA3                                                                                         | H3       |      |         |                                                                                                                                                                                                                                           |
| UXDATA2                                                                                         | G3       |      |         |                                                                                                                                                                                                                                           |
| UXDATA1                                                                                         | F4       |      |         |                                                                                                                                                                                                                                           |
| UXDATA0                                                                                         | E3       |      |         |                                                                                                                                                                                                                                           |
| UTOPIA SLAVE (ATM CONTROLLER) — RECEIVE INTERFACE                                               |          |      |         |                                                                                                                                                                                                                                           |
| URCLK                                                                                           | C1       | I    |         | Source clock for UTOPIA receive driven by Master ATM Controller.                                                                                                                                                                          |
| URCLAV                                                                                          | B2       | O/Z  |         | Receive cell available status output signal from UTOPIA Slave.<br>• 0 indicates NO space is available to receive a cell from Master ATM Controller.<br>• 1 indicates space is available to receive a cell from Master ATM Controller.     |
| $\overline{\text{URENB}}$                                                                       | K4       | I    |         | UTOPIA receive interface enable input signal. Asserted by the Master ATM Controller to indicate to the UTOPIA Slave to sample the Receive Data Bus (URDATA[7:0]) and URSOC signal in the next clock cycle or thereafter.                  |
| URSOC                                                                                           | G2       | I    |         | Receive Start-of-Cell signal. This signal is output by the Master ATM Controller to indicate to the UTOPIA Slave that the first valid byte of the cell is available to sample on the 8-bit Receive Data Bus (URDATA[7:0]).                |
| URADDR4                                                                                         | K1       | I    |         | UTOPIA receive address pins [URADDR[4:0] (I)]: 5-bit Slave receive address input pins driven by the Master ATM Controller to identify and select one of the Slave devices (up to 31 possible) in the ATM System.                          |
| URADDR3                                                                                         | K2       |      |         |                                                                                                                                                                                                                                           |
| URADDR2                                                                                         | J1       |      |         |                                                                                                                                                                                                                                           |
| URADDR1                                                                                         | J3       |      |         |                                                                                                                                                                                                                                           |
| URADDR0                                                                                         | H2       |      |         |                                                                                                                                                                                                                                           |

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**Table 2-6 Terminal Functions (Part 13 of 22)**

| Signal Name                         | Ball No. | Type  | IPD/IPU | Description                                                                                                                                                                               |
|-------------------------------------|----------|-------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| URDATA7                             | G1       | I     |         | UTOPIA 8-bit Receive Data Bus (I/O/Z). Using the Receive Data Bus, the UTOPIA Slave (on the rising edge of the URCLK) can receive the 8-bit ATM cell data from the Master ATM Controller. |
| URDATA6                             | F2       |       |         |                                                                                                                                                                                           |
| URDATA5                             | F1       |       |         |                                                                                                                                                                                           |
| URDATA4                             | E2       |       |         |                                                                                                                                                                                           |
| URDATA3                             | E1       |       |         |                                                                                                                                                                                           |
| URDATA2                             | D2       |       |         |                                                                                                                                                                                           |
| URDATA1                             | D1       |       |         |                                                                                                                                                                                           |
| URDATA0                             | C2       |       |         |                                                                                                                                                                                           |
| SERIAL RAPIDIO (SRIO)               |          |       |         |                                                                                                                                                                                           |
| RIORXN0                             | AG8      | I     |         | Serial RapidIO Receive Data (4 links)                                                                                                                                                     |
| RIORXP0                             | AG9      |       |         |                                                                                                                                                                                           |
| RIORXN1                             | AF11     |       |         |                                                                                                                                                                                           |
| RIORXP1                             | AF10     |       |         |                                                                                                                                                                                           |
| RIORXN2                             | AH13     |       |         |                                                                                                                                                                                           |
| RIORXP2                             | AH12     |       |         |                                                                                                                                                                                           |
| RIORXN3                             | AE13     |       |         |                                                                                                                                                                                           |
| RIORXP3                             | AE12     |       |         |                                                                                                                                                                                           |
| RIOTXN0                             | AE9      | O     |         | Serial RapidIO Transmit data (4 links)                                                                                                                                                    |
| RIOTXP0                             | AE8      |       |         |                                                                                                                                                                                           |
| RIOTXN1                             | AH9      |       |         |                                                                                                                                                                                           |
| RIOTXP1                             | AH10     |       |         |                                                                                                                                                                                           |
| RIOTXN2                             | AF13     |       |         |                                                                                                                                                                                           |
| RIOTXP2                             | AF14     |       |         |                                                                                                                                                                                           |
| RIOTXN3                             | AG13     |       |         |                                                                                                                                                                                           |
| RIOTXP3                             | AG14     |       |         |                                                                                                                                                                                           |
| ETHERNET MAC (EMAC) AND SGMII       |          |       |         |                                                                                                                                                                                           |
| SGMIIRXN                            | AF16     | I     |         | Ethernet MAC SGMII Receive Data                                                                                                                                                           |
| SGMIIRXP                            | AF17     |       |         |                                                                                                                                                                                           |
| SGMIITXN                            | AH15     | O     |         | Ethernet MAC SGMII Transmit Data                                                                                                                                                          |
| SGMIITXP                            | AH14     |       |         |                                                                                                                                                                                           |
| MANAGEMENT DATA INPUT/OUTPUT (MDIO) |          |       |         |                                                                                                                                                                                           |
| MDIO                                | AH19     | I/O/Z | IPU     | MDIO Data                                                                                                                                                                                 |
| MDCLK                               | AH18     | O     | IPD     | MDIO Clock                                                                                                                                                                                |
| VOLTAGE CONTROL TERMINALS           |          |       |         |                                                                                                                                                                                           |
| PTV18                               | A16      | A     |         | PTV Compensation NMOS Reference Input. Install with 47-Ω, 5% resistor to GND                                                                                                              |
| SUPPLY VOLTAGE MONITOR TERMINALS    |          |       |         |                                                                                                                                                                                           |
| CV <sub>DDMON</sub>                 | U19      | A     |         | 1.1-V CV <sub>DD</sub> Supply Monitor                                                                                                                                                     |
| DV <sub>DD33MON</sub>               | U22      | A     |         | 3.3-V DV <sub>DD</sub> Supply Monitor                                                                                                                                                     |
| DV <sub>DD18MON</sub>               | G23      | A     |         | 1.8-V DV <sub>DD</sub> Supply Monitor                                                                                                                                                     |

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**Table 2-6 Terminal Functions (Part 14 of 22)**

| Signal Name                     | Ball No. | Type | IPD/IPU | Description                                                                                  |
|---------------------------------|----------|------|---------|----------------------------------------------------------------------------------------------|
| <b>SUPPLY VOLTAGE TERMINALS</b> |          |      |         |                                                                                              |
| V <sub>DDR18</sub>              | AE10     | S    |         | 1.8-V I/O supply voltage (SRIO/SGMII SerDes regulator supply).                               |
|                                 | AE16     |      |         |                                                                                              |
| V <sub>DDA11</sub>              | AC10     | S    |         | SRIO/SGMII analog supply:<br>1.1-V I/O supply voltage<br>Do not use core supply.             |
|                                 | AC12     |      |         |                                                                                              |
|                                 | AC14     |      |         |                                                                                              |
|                                 | AC16     |      |         |                                                                                              |
| V <sub>DDD11</sub>              | U13      | S    |         | SRIO/SGMII SerDes digital supply:<br>1.1-V I/O supply voltage<br>Do not use core supply.     |
|                                 | V12      |      |         |                                                                                              |
|                                 | V14      |      |         |                                                                                              |
|                                 | W11      |      |         |                                                                                              |
|                                 | W13      |      |         |                                                                                              |
|                                 | W15      |      |         |                                                                                              |
| V <sub>DDT11</sub>              | AD9      | S    |         | SRIO/SGMII SerDes termination supply:<br>1.1-V I/O supply voltage<br>Do not use core supply. |
|                                 | AD11     |      |         |                                                                                              |
|                                 | AD13     |      |         |                                                                                              |
|                                 | AD15     |      |         |                                                                                              |
|                                 | AD17     |      |         |                                                                                              |
|                                 | AF9      |      |         |                                                                                              |
|                                 | AF15     |      |         |                                                                                              |
|                                 | AG11     |      |         |                                                                                              |
| DV <sub>DD18</sub>              | AH17     | S    |         | 1.8-V I/O supply voltage                                                                     |
|                                 | AA6      |      |         |                                                                                              |
|                                 | AB18     |      |         |                                                                                              |
|                                 | AB20     |      |         |                                                                                              |
|                                 | AB7      |      |         |                                                                                              |
|                                 | AC19     |      |         |                                                                                              |
|                                 | AC21     |      |         |                                                                                              |
|                                 | AC3      |      |         |                                                                                              |
|                                 | AC8      |      |         |                                                                                              |
|                                 | AD18     |      |         |                                                                                              |
|                                 | AD22     |      |         |                                                                                              |
|                                 | AF18     |      |         |                                                                                              |
|                                 | AG5      |      |         |                                                                                              |
|                                 | AH1      |      |         |                                                                                              |
|                                 | B11      |      |         |                                                                                              |
|                                 | B19      |      |         |                                                                                              |
|                                 | B22      |      |         |                                                                                              |
|                                 | B8       |      |         |                                                                                              |

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**Table 2-6 Terminal Functions (Part 15 of 22)**

| Signal Name        | Ball No. | Type | IPD/IPU | Description              |
|--------------------|----------|------|---------|--------------------------|
| DV <sub>DD18</sub> | E11      | S    |         | 1.8-V I/O supply voltage |
|                    | E21      |      |         |                          |
|                    | E23      |      |         |                          |
|                    | E9       |      |         |                          |
|                    | F10      |      |         |                          |
|                    | F12      |      |         |                          |
|                    | F14      |      |         |                          |
|                    | F16      |      |         |                          |
|                    | F18      |      |         |                          |
|                    | G11      |      |         |                          |
|                    | G13      |      |         |                          |
|                    | G15      |      |         |                          |
|                    | G17      |      |         |                          |
|                    | G19      |      |         |                          |
|                    | G21      |      |         |                          |
|                    | G7       |      |         |                          |
|                    | G9       |      |         |                          |
|                    | J7       |      |         |                          |
|                    | V6       |      |         |                          |
|                    | Y7       |      |         |                          |

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**Table 2-6 Terminal Functions (Part 16 of 22)**

| Signal Name        | Ball No. | Type | IPD/IPU | Description              |
|--------------------|----------|------|---------|--------------------------|
| DV <sub>DD33</sub> | A1       | S    |         | 3.3-V I/O supply voltage |
|                    | A28      |      |         |                          |
|                    | AA23     |      |         |                          |
|                    | AB22     |      |         |                          |
|                    | AB28     |      |         |                          |
|                    | AC23     |      |         |                          |
|                    | AD24     |      |         |                          |
|                    | AH24     |      |         |                          |
|                    | AH28     |      |         |                          |
|                    | D3       |      |         |                          |
|                    | E25      |      |         |                          |
|                    | E27      |      |         |                          |
|                    | H1       |      |         |                          |
|                    | H22      |      |         |                          |
|                    | H27      |      |         |                          |
|                    | J23      |      |         |                          |
|                    | K22      |      |         |                          |
|                    | L1       |      |         |                          |
|                    | L23      |      |         |                          |
|                    | L7       |      |         |                          |
|                    | M22      |      |         |                          |
|                    | M27      |      |         |                          |
|                    | N23      |      |         |                          |
|                    | N7       |      |         |                          |
|                    | P1       |      |         |                          |
|                    | P22      |      |         |                          |
|                    | P27      |      |         |                          |
|                    | R23      |      |         |                          |
|                    | R3       |      |         |                          |
|                    | R7       |      |         |                          |
|                    | T22      |      |         |                          |
|                    | U7       |      |         |                          |
|                    | V22      |      |         |                          |
|                    | V3       |      |         |                          |
|                    | W23      |      |         |                          |
|                    | Y22      |      |         |                          |

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**Table 2-6 Terminal Functions (Part 17 of 22)**

| Signal Name       | Ball No. | Type | IPD/IPU | Description               |
|-------------------|----------|------|---------|---------------------------|
| CV <sub>DD</sub>  | K10      | S    |         | 1.1-V core supply voltage |
|                   | K12      |      |         |                           |
|                   | K14      |      |         |                           |
|                   | K16      |      |         |                           |
|                   | K18      |      |         |                           |
|                   | L11      |      |         |                           |
|                   | L13      |      |         |                           |
|                   | L15      |      |         |                           |
|                   | L17      |      |         |                           |
|                   | L19      |      |         |                           |
|                   | M10      |      |         |                           |
|                   | M12      |      |         |                           |
|                   | M14      |      |         |                           |
|                   | M16      |      |         |                           |
|                   | M18      |      |         |                           |
|                   | N11      |      |         |                           |
|                   | N13      |      |         |                           |
|                   | N15      |      |         |                           |
|                   | N17      |      |         |                           |
| CV <sub>DD</sub>  | N19      | S    |         | 1.1-V core supply voltage |
|                   | P10      |      |         |                           |
|                   | P12      |      |         |                           |
|                   | P14      |      |         |                           |
|                   | P16      |      |         |                           |
|                   | P18      |      |         |                           |
|                   | R11      |      |         |                           |
|                   | R13      |      |         |                           |
|                   | R15      |      |         |                           |
|                   | R17      |      |         |                           |
|                   | R19      |      |         |                           |
|                   | T12      |      |         |                           |
|                   | T14      |      |         |                           |
|                   | T16      |      |         |                           |
|                   | T18      |      |         |                           |
|                   | U11      |      |         |                           |
|                   | U15      |      |         |                           |
|                   | U17      |      |         |                           |
|                   | V10      |      |         |                           |
|                   | V16      |      |         |                           |
|                   | V18      |      |         |                           |
|                   | W17      |      |         |                           |
|                   | W19      |      |         |                           |
| PLL <sub>V1</sub> | AC5      | S    |         | 1.8-V PLL Supply          |
| PLL <sub>V2</sub> | F7       | S    |         | 1.8-V PLL Supply          |

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**Table 2-6 Terminal Functions (Part 18 of 22)**

| Signal Name        | Ball No. | Type | IPD/IPU | Description |
|--------------------|----------|------|---------|-------------|
| <b>GROUND PINS</b> |          |      |         |             |
| VSS                | A11      | GND  |         | Ground pins |
|                    | A19      |      |         |             |
|                    | A2       |      |         |             |
|                    | A22      |      |         |             |
|                    | A8       |      |         |             |
|                    | AA2      |      |         |             |
|                    | AA22     |      |         |             |
|                    | AA7      |      |         |             |
|                    | AB10     |      |         |             |
|                    | AB11     |      |         |             |
|                    | AB12     |      |         |             |
|                    | AB13     |      |         |             |
|                    | AB14     |      |         |             |
|                    | AB15     |      |         |             |
|                    | AB16     |      |         |             |
|                    | AB17     |      |         |             |
|                    | AB19     |      |         |             |
|                    | AB21     |      |         |             |
|                    | AB23     |      |         |             |
|                    | AB27     |      |         |             |
|                    | AB6      |      |         |             |
|                    | AB8      |      |         |             |
|                    | AB9      |      |         |             |
|                    | AC11     |      |         |             |
|                    | AC13     |      |         |             |
|                    | AC15     |      |         |             |
|                    | AC17     |      |         |             |
|                    | AC18     |      |         |             |
|                    | AC20     |      |         |             |
|                    | AC22     |      |         |             |
|                    | AC9      |      |         |             |
|                    | AD10     |      |         |             |
|                    | AD12     |      |         |             |
|                    | AD14     |      |         |             |
|                    | AD16     |      |         |             |
|                    | AD19     |      |         |             |
|                    | AD2      |      |         |             |

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**Table 2-6 Terminal Functions (Part 19 of 22)**

| Signal Name | Ball No. | Type | IPD/IPU | Description |
|-------------|----------|------|---------|-------------|
| VSS         | AD23     | GND  |         | Ground pins |
|             | AD8      |      |         |             |
|             | AE11     |      |         |             |
|             | AE14     |      |         |             |
|             | AE15     |      |         |             |
|             | AE17     |      |         |             |
|             | AE18     |      |         |             |
|             | AF5      |      |         |             |
|             | AF8      |      |         |             |
|             | AG1      |      |         |             |
|             | AG10     |      |         |             |
|             | AG12     |      |         |             |
|             | AG15     |      |         |             |
|             | AG17     |      |         |             |
|             | AG18     |      |         |             |
|             | AG24     |      |         |             |
|             | AG28     |      |         |             |
|             | AH11     |      |         |             |
|             | AH16     |      |         |             |
|             | AH2      |      |         |             |
|             | AH27     |      |         |             |
|             | AH8      |      |         |             |
|             | B1       |      |         |             |
|             | B28      |      |         |             |
|             | D4       |      |         |             |
|             | E18      |      |         |             |
|             | E28      |      |         |             |
|             | F11      |      |         |             |
|             | F13      |      |         |             |
|             | F15      |      |         |             |
|             | F19      |      |         |             |
|             | F21      |      |         |             |
|             | F22      |      |         |             |
|             | F25      |      |         |             |
|             | F9       |      |         |             |
|             | G10      |      |         |             |
|             | G12      |      |         |             |
|             | G14      |      |         |             |

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**Table 2-6 Terminal Functions (Part 20 of 22)**

| Signal Name | Ball No. | Type | IPD/IPU | Description |
|-------------|----------|------|---------|-------------|
| VSS         | G16      | GND  |         | Ground pins |
|             | G18      |      |         |             |
|             | G20      |      |         |             |
|             | G22      |      |         |             |
|             | G8       |      |         |             |
|             | H23      |      |         |             |
|             | H28      |      |         |             |
|             | H7       |      |         |             |
|             | J2       |      |         |             |
|             | J22      |      |         |             |
|             | K11      |      |         |             |
|             | K13      |      |         |             |
|             | K15      |      |         |             |
|             | K17      |      |         |             |
|             | K19      |      |         |             |
|             | K23      |      |         |             |
|             | K7       |      |         |             |
|             | L10      |      |         |             |
|             | L12      |      |         |             |
|             | L14      |      |         |             |
|             | L16      |      |         |             |
|             | L18      |      |         |             |
|             | L22      |      |         |             |
|             | M11      |      |         |             |
|             | M13      |      |         |             |
|             | M15      |      |         |             |
|             | M17      |      |         |             |
|             | M19      |      |         |             |
|             | M2       |      |         |             |
|             | M23      |      |         |             |
|             | M28      |      |         |             |
|             | M7       |      |         |             |
|             | N10      |      |         |             |
|             | N12      |      |         |             |
|             | N14      |      |         |             |
|             | N16      |      |         |             |
|             | N18      |      |         |             |
|             | N22      |      |         |             |

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**Table 2-6 Terminal Functions (Part 21 of 22)**

| Signal Name | Ball No. | Type | IPD/IPU | Description |
|-------------|----------|------|---------|-------------|
| VSS         | P11      | GND  |         | Ground pins |
|             | P13      |      |         |             |
|             | P15      |      |         |             |
|             | P17      |      |         |             |
|             | P19      |      |         |             |
|             | P23      |      |         |             |
|             | P28      |      |         |             |
|             | P7       |      |         |             |
|             | R12      |      |         |             |
|             | R14      |      |         |             |
|             | R16      |      |         |             |
|             | R18      |      |         |             |
|             | R2       |      |         |             |
|             | R22      |      |         |             |
|             | T11      |      |         |             |
|             | T13      |      |         |             |
|             | T15      |      |         |             |
|             | T17      |      |         |             |
|             | T19      |      |         |             |
|             | T23      |      |         |             |
|             | T7       |      |         |             |
|             | U10      |      |         |             |
|             | U12      |      |         |             |
|             | U14      |      |         |             |
|             | U16      |      |         |             |
|             | U18      |      |         |             |
|             | U23      |      |         |             |
|             | U24      |      |         |             |
|             | U3       |      |         |             |
|             | V11      |      |         |             |
|             | V13      |      |         |             |
|             | V15      |      |         |             |
|             | V17      |      |         |             |
|             | V19      |      |         |             |
|             | V23      |      |         |             |
|             | V27      |      |         |             |
|             | V7       |      |         |             |
|             | W10      |      |         |             |
|             | W12      |      |         |             |
|             | W14      |      |         |             |
|             | W16      |      |         |             |

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**Table 2-6 Terminal Functions (Part 22 of 22)**

| Signal Name      | Ball No. | Type  | IPD/IPU | Description                                                  |
|------------------|----------|-------|---------|--------------------------------------------------------------|
| VSS              | W18      | GND   |         | Ground pins                                                  |
|                  | W22      |       |         |                                                              |
|                  | W7       |       |         |                                                              |
|                  | Y23      |       |         |                                                              |
| RESERVED PINS    |          |       |         |                                                              |
| RSV01            | AC4      | I/O/Z | IPU     | Reserved - Unconnected                                       |
| RSV02            | AB2      | I/O/Z | IPU     | Reserved - Unconnected                                       |
| RSV03            | AB4      | I/O/Z | IPU     | Reserved - Unconnected                                       |
| RSV04            | AD20     | O/Z   | IPD     | Reserved - Unconnected                                       |
| RSV05            | AD21     | O/Z   | IPD     | Reserved - Unconnected                                       |
| RSV06            | AE20     | A     |         | Reserved - Unconnected                                       |
| RSV07            | AE21     | A     |         | Reserved - Unconnected                                       |
| RSV08            | AE7      | O     |         | Reserved - Unconnected                                       |
| RSV09            | AF7      | O     |         | Reserved - Unconnected                                       |
| RSV10            | H6       | O     |         | Reserved - Unconnected                                       |
| RSV11            | J6       | O     |         | Reserved - Unconnected                                       |
| RSV12            | AB5      | A     |         | Reserved - Connect to GND                                    |
| RSV13            | AA5      | A     |         | Reserved - Unconnected                                       |
| RSV14            | AF20     | I/O/Z | IPU     | Reserved - Unconnected                                       |
| RSV15            | AF21     | I/O/Z | IPU     | Reserved - Unconnected                                       |
| RSV16            | AF12     | A     |         | Reserved - Unconnected                                       |
| RSV17            | AG16     | A     |         | Reserved - Unconnected                                       |
| RSV18            | AH21     | A     |         | Reserved - Unconnected                                       |
| RSV19            | AG21     | A     |         | Reserved - Unconnected                                       |
| RSV20            | AC6      | A     |         | Reserved - Unconnected                                       |
| RSV21            | AC7      | A     |         | Reserved - Unconnected                                       |
| RSV22            | AE23     | I     | IPU     | Reserved - Pullup to DV <sub>DD18</sub> with 10-kΩ resistor. |
| RSV23            | R10      | S     |         | Reserved - Connected to CV <sub>DD</sub>                     |
| RSV23            | T10      | S     |         | Reserved - Connected to CV <sub>DD</sub>                     |
| RSV24            | AD6      | O/Z   | IPD     | Reserved - Unconnected                                       |
| RSV25            | G5       | O/Z   | IPD     | Reserved - Unconnected                                       |
| RSV26            | AE22     |       |         | Reserved - Unconnected                                       |
| RSV27            | AF22     |       |         | Reserved - Unconnected                                       |
| RSV28            | AG23     |       |         | Reserved - Unconnected                                       |
| RSV29            | AH22     |       |         | Reserved - Unconnected                                       |
| End of Table 2-6 |          |       |         |                                                              |

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## 2.9 Development

### 2.9.1 Development Support

In case the customer would like to develop their own features and software on the C6457 device, TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of C6000™ DSP-based applications:

- **Software Development Tools:**
  - Code Composer Studio™ Integrated Development Environment (IDE), including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools
  - Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any DSP application.
- **Hardware Development Tools:**
  - Extended Development System (XDS™) Emulator (supports C6000™ DSP multiprocessor system debug)
  - EVM (Evaluation Module)

### 2.9.2 Device Support

#### 2.9.2.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., TMX320C6457CMH). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

- **TMX:** Experimental device that is not necessarily representative of the final device's electrical specifications
- **TMP:** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
- **TMS:** Fully qualified production device

Support tool development evolutionary flow:

- **TMDX:** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- **TMDS:** Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, CMH), the temperature range (for example, blank is the default case temperature range), and the device speed range, in megahertz (for example, blank is 1000 MHz [1 GHz]).

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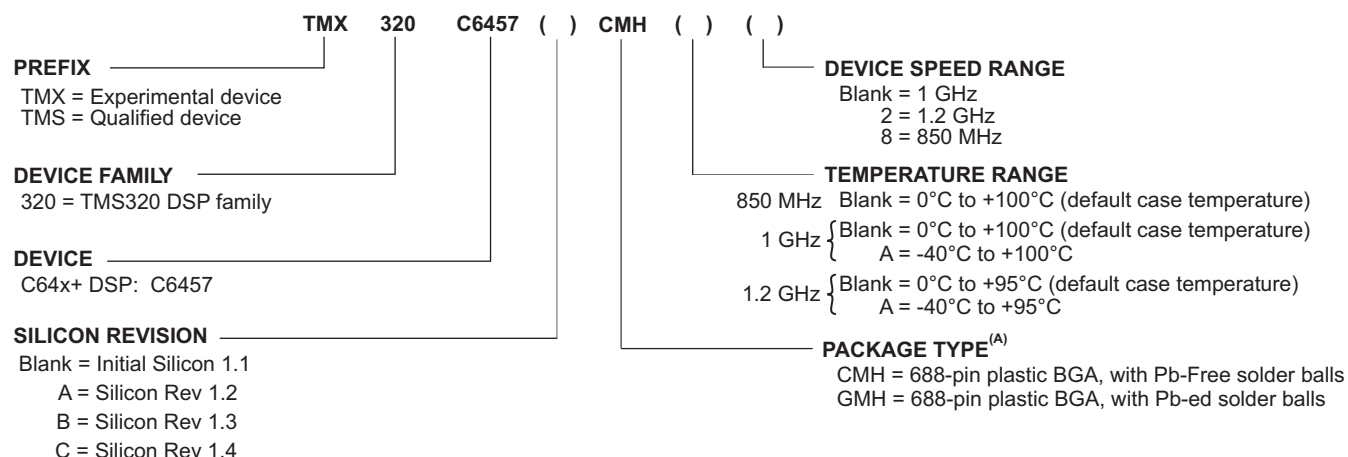


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provides a legend for reading the complete device name for any TMS320C64x+™ DSP generation member.

For device part numbers and further ordering information for TMS320C6457 in the CMH package type, see the TI website [www.ti.com](http://www.ti.com) or contact your TI sales representative.

**Figure 2-12 TMS320C64x+™ DSP Device Nomenclature (including the TMS320C6457 DSP)**



(A) BGA = Ball Grid Array

### 2.9.2.2 Documentation Support

The documents shown in [Table 2-7](#) describe the TMS320C6457 Communications Infrastructure Digital Signal Processor. Copies of these documents are available on the Internet at [www.ti.com](http://www.ti.com). Tip: Enter the literature number in the search box provided at [www.ti.com](http://www.ti.com).

The current documentation that describes the TMS320C6457, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: [www.ti.com/c6000](http://www.ti.com/c6000).

**Table 2-7 Relevant Documents (Part 1 of 2)**

| TI Literature No.       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <a href="#">SPRU732</a> | <i>TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.</i> Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set. |
| <a href="#">SPRU871</a> | <i>TMS320C64x+ Megamodule Reference Guide.</i> Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.                                                                                                                       |
| <a href="#">SPRAA84</a> | <i>TMS320C64x to TMS320C64x+ CPU Migration Guide.</i> Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.                                                                                                                            |
| <a href="#">SPRU889</a> | <i>High-Speed DSP Systems Design Reference Guide.</i> Provides recommendations for meeting the many challenges of high-speed DSP system design. These recommendations include information about DSP audio, video, and communications systems for the C5000 and C6000 DSP platforms.                                                                                                                                                                |
| <a href="#">SPRUGK5</a> | <i>TMS320C6457 DSP DDR2 Memory Controller User's Guide.</i> This document describes the DDR2 memory controller in the TMS320C6457 digital-signal processors (DSPs).                                                                                                                                                                                                                                                                                |
| <a href="#">SPRUGK6</a> | <i>TMS320C6457 DSP Enhanced DMA (EDMA3) Controller User's Guide.</i> This document describes the Enhanced DMA (EDMA3) Controller on the TMS320C6457 device.                                                                                                                                                                                                                                                                                        |
| <a href="#">SPRUGK2</a> | <i>TMS320C6457 DSP External Memory Interface (EMIF) User's Guide.</i> This document describes the operation of the external memory interface (EMIF) in the digital signal processors (DSPs) of the TMS320C6457 DSP family.                                                                                                                                                                                                                         |



**Table 2-7 Relevant Documents (Part 2 of 2)**

| TI Literature No.       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <a href="#">SPRUGL2</a> | <i>TMS320C6457 DSP General-Purpose Input/Output (GPIO) User's Guide.</i> This document describes the general-purpose input/output (GPIO) peripheral in the digital signal processors (DSPs) of the TMS320C6457 DSP family. The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of the input by reading the state of an internal register. When configured as an output, you can write to an internal register to control the state driven on the output pin.                                                                                                                                                                                                                     |
| <a href="#">SPRUGK7</a> | <i>TMS320C6457 DSP Host Port Interface (HPI) User's Guide.</i> This guide describes the host port interface (HPI) on the TMS320C6457 digital signal processors (DSPs). The HPI enables an external host processor (host) to directly access DSP resources (including internal and external memory) using a 16-bit (HPI16) or 32-bit (HPI32) interface.                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| <a href="#">SPRUGK3</a> | <i>TMS320C6457 DSP Inter-Integrated Circuit (I<sup>2</sup>C) Module User's Guide.</i> This document describes the inter-integrated circuit (I <sup>2</sup> C) module in the TMS320C6457 Digital Signal Processor (DSP). The I <sup>2</sup> C provides an interface between the TMS320C6457 device and other devices compliant with Philips Semiconductors Inter-IC bus (I <sup>2</sup> C-bus) specification version 2.1 and connected by way of an I <sup>2</sup> C-bus. This document assumes the reader is familiar with the I <sup>2</sup> C-bus specification.                                                                                                                                                                                                                                 |
| <a href="#">SPRUGK4</a> | <i>TMS320C6457 Serial RapidIO (SRIO) User's Guide.</i> This document describes the Serial RapidIO (SRIO) on the TMS320C6457 devices.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| <a href="#">SPRUGL3</a> | <i>TMS320C6457 DSP Software-Programmable Phase-Locked Loop (PLL) Controller UG.</i> This document describes the operation of the software-programmable phase-locked loop (PLL) controller in the TMS320C6457 digital signal processors (DSPs). The PLL controller offers flexibility and convenience by way of software-configurable multipliers and dividers to modify the input signal internally. The resulting clock outputs are passed to the TMS320C6457 DSP core, peripherals, and other modules inside the TMS320C6457 DSP.                                                                                                                                                                                                                                                                |
| <a href="#">SPRUGL0</a> | <i>TMS320C6457 DSP 64-Bit Timer User's Guide.</i> This document provides an overview of the 64-bit timer in the TMS320C6457 DSP. The timer can be configured as a general-purpose 64-bit timer, dual general-purpose 32-bit timers, or a watchdog timer. When configured as a dual 32-bit timers, each half can operate in conjunction (chain mode) or independently (unchained mode) of each other.                                                                                                                                                                                                                                                                                                                                                                                               |
| <a href="#">SPRUGK1</a> | <i>TMS320C6457 DSP Turbo-Decoder Coprocessor 2 (TCP2) Reference Guide.</i> Channel decoding of high bit-rate data channels found in third generation (3G) cellular standards requires decoding of turbo-encoded data. The turbo-decoder coprocessor (TCP) in some of the digital signal processor (DSPs) of the TMS320C6000™ DSP family has been designed to perform this operation for IS2000 and 3GPP wireless standards. This document describes the operation and programming of the TCP.                                                                                                                                                                                                                                                                                                      |
| <a href="#">SPRUGL1</a> | <i>TMS320C6457 DSP Universal Test &amp; Operations PHY Interface for ATM 2 (UTOPIA2) User's Guide.</i> This document describes the universal test and operations PHY interface for asynchronous transfer mode (ATM) 2 (UTOPIA2) in the TMS320C6457 digital signal processors (DSPs) of the TMS320C6000™ DSP family.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <a href="#">SPRUGK0</a> | <i>TMS320C6457 DSP Viterbi-Decoder Coprocessor 2 (VCP2) Reference Guide.</i> Channel decoding of voice and low bit-rate data channels found in third generation (3G) cellular standards requires decoding of convolutional encoded data. The Viterbi-decoder coprocessor 2 (VCP2) provided in TMS320C6457 devices has been designed to perform Viterbi-Decoding for IS2000 and 3GPP wireless standards. The VCP2 coprocessor has been designed to perform forward error correction for 2G and 3G wireless systems. The VCP2 coprocessor offers a very cost effective and synergistic solution when combined with Texas Instruments (TI) DSPs. The VCP2 can support 1941 12.2 Kbps class A 3G voice channels running at 333 MHz. This document describes the operation and programming of the VCP2. |
| <a href="#">SPRUGK9</a> | <i>TMS320C6457 DSP Ethernet Media Access Controller (EMAC) / Management Data Input Output (MDIO) User's Guide.</i> This document provides a functional description of the Ethernet Media Access Controller (EMAC) and Physical layer (PHY) device Management Data Input/Output (MDIO) module integrated with TMS320C6457 devices. Included are the features of the EMAC and MDIO modules, a discussion of their architecture and operation, how these modules connect to the outside world, and the registers description for each module.                                                                                                                                                                                                                                                         |
| <a href="#">SPRUGK8</a> | <i>TMS320C6457 DSP Multichannel Buffered Serial Port (McBSP) Reference Guide.</i> This document describes the operation of the multichannel buffered serial port (McBSP) in the digital signal processors (DSPs) of the TMS320C6000™ DSP family.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <a href="#">SPRUGL4</a> | <i>TMS320C6457 DSP Power/Sleep Controller (PSC) User's Guide.</i> This document covers the usage of the Power/Sleep Controller (PSC) in the TMS320C6457 device.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <a href="#">SPRUGL5</a> | <i>TMS320C6457 DSP Bootloader User's Guide.</i> This document describes the features of the on-chip bootloader provided with the TMS320C6457 Digital Signal Processor (DSP).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>End of Table 2-7</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

# PRODUCT PREVIEW

## 3 Device Configuration

On the TMS320C6457 device, certain device configurations like boot mode and endianness, are selected at device power-on reset. The status of the peripherals (enabled/disabled) is determined after device power-on reset. By default, the peripherals on the C6457 device are disabled and need to be enabled by software before being used.

### 3.1 Device Configuration at Device Reset

Table 3-1 describes the C6457 device configuration pins. The logic level is latched at power-on reset to determine the device configuration. The logic level on the device configuration pins can be set by using external pullup/pulldown resistors or by using some control device (e.g., FPGA/CPLD) to intelligently drive these pins. When using a control device, care should be taken to ensure there is no contention on the lines when the device is out of reset. The device configuration pins are sampled during power-on reset and are driven after the reset is removed. To avoid contention, the control device must stop driving the device configuration pins of the DSP.



**Note**—If a configuration pin must be routed out from the device and it is not driven (Hi-Z state), the internal pullup/pulldown (IPU/IPD) resistor should not be relied upon. TI recommends the use of an external pullup/pulldown resistor. For more detailed information on pullup/pulldown resistors and situations in which external pullup/pulldown resistors are required, see Section 3.6 “Pullup/Pulldown Resistors” on page 63.

**Table 3-1 TMS320C6457 Device Configuration Pins**

| Configuration Pin | No.                                   | IPD/IPU <sup>(1)</sup> | Functional Description                                                                                                                                                                                                                                                                                  |
|-------------------|---------------------------------------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO[0]           | A5                                    | IPU                    | Device Endian mode (LENDIAN)<br>0 = Device operates in Big Endian mode.<br>1 = Device operates in Little Endian mode (default).                                                                                                                                                                         |
| GPIO[4:1]         | [B5,<br>B4,D5,<br>E5]                 | IPD                    | Boot Mode Selection (BOOTMODE [3:0])<br>These pins select the boot mode for the device. For more information on the boot modes, see Section 2.4 “Boot Sequence” on page 21.                                                                                                                             |
| GPIO[8:5]         | [B25,<br>F5,C5,<br>F6]                | IPD                    | Device Number (DEVNUM[3:0])                                                                                                                                                                                                                                                                             |
| GPIO[13:9]        | [C23,<br>D24,<br>C25,<br>A25,<br>C24] | IPD                    | Configuration General-Purpose Inputs (CFGGP[4:0])<br>The value of these pins is latched to the Device Status Register following power-on reset and is used by the software.                                                                                                                             |
| GPIO[14]          | D23                                   | IPD                    | HPI peripheral bus width select (HPIWIDTH)<br>0 = HPI operates in HPI16 mode (default).<br>HPI bus is 16 bits wide; HD[15:0] pins are used and the remaining HD[31:16] pins are reserved pins in the Hi-Z state.<br>1 = HPI operates in HPI32 mode.<br>HPI bus is 32 bits wide; HD[31:0] pins are used. |
| GPIO[15]          | F23                                   | IPD                    | EMIFA input clock source select (ECLKINSEL).<br>0 = ECLKIN (default mode)<br>1 = SYSCLK7 (CPU/x) Clock Rate.<br>The SYSCLK7 clock rate is software selectable via the Software PLL1 Controller. By default, SYSCLK7 is selected as CPU ÷ 10 clock rate.                                                 |
| CORECLKSEL        | AE6                                   |                        | Core Clock Select<br>0 = CORECLK(N P) is the input to main PLL.<br>1 = ALT CORECLK is used as the input to main PLL.                                                                                                                                                                                    |
| DDRCLKSEL         | G6                                    |                        | DDR Clock Select<br>0 = DDRREFCLK(N P) is the input to DDR PLL.<br>1 = ALTDDRCLK is used as the input to DDR PLL.                                                                                                                                                                                       |

**End of Table 3-1**

<sup>1</sup> Internal 100-μA pulldown or pullup is provided for this terminal. In most systems, a 1-kΩ resistor can be used to oppose the IPD/IPU. For more detailed information on pulldown/pullup resistors and situations in which external pulldown/pullup resistors are required, see Section 3.6 “Pullup/Pulldown Resistors” on page 63.

## 3.2 Peripheral Selection After Device Reset

Several of the peripherals on the TMS320C6457 are controlled by the Power Sleep Controller (PSC). By default, the SRIO, TCP2\_A, TCP2\_B, and VCP are held in reset and clock-gated. The memories in these modules are also in a low-leakage sleep mode. Software is required to turn these memories on. Then, the software enables the modules (turns on clocks and de-asserts reset) before these modules can be used.

In addition, the EMIFA, HPI, and UTOPIA come up clock-gated and held in reset. Memories in these modules are already enabled. Software is required to enable these modules before they are used as well.

If one of the above modules is used in the selected ROM boot mode, the ROM code will automatically enable the module.

All other modules come up enabled by default and there is no special software sequence to enable. For more detailed information on the PSC usage, see the *TMS320C6457 DSP Power/Sleep Controller PSC User's Guide* (literature number [SPRUGL4](#)).

## 3.3 Device State Control Registers

The C6457 device has a set of registers that are used to control the status of its peripherals. These registers are shown in [Table 3-2](#) and described in the next sections.

**Table 3-2 Device State Control Registers<sup>(1)</sup>**

| Hex Address Range       | Acronym       | Description                                                                                                                                                                                                                                                                                                        |
|-------------------------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0288 0818               | JTAGID        | Parameters for DSP device ID. Also referred to as JTAG or BSDL ID. These are readable by the configuration bus and can be accessed via the JTAG and the CPU.                                                                                                                                                       |
| 0288 081C               | -             | Reserved                                                                                                                                                                                                                                                                                                           |
| 0288 0820               | DEVSTAT       | Stores parameters latched from configuration pins                                                                                                                                                                                                                                                                  |
| 0288 0824 - 0288 0837   | -             | Reserved                                                                                                                                                                                                                                                                                                           |
| 0288 0838               | KICK0         | Two successive key writes are required to get write access to any of the device state control registers. KICK0 is the first key register. The written data must be 0x83E70B13 to unlock it and it must be written before the KICK1 register. Writing any other value will lock the device state control registers. |
| 0288 083C               | KICK1         | KICK1 is the second key register to be unlocked in order to get write access to any of the device state control registers. The written data must be 0x95A4F1E0 to unlock it and it must be written after the KICK0 register. Writing any other value will lock the device state control registers.                 |
| 0288 0840               | DSP_BOOT_ADDR | DSP boot address                                                                                                                                                                                                                                                                                                   |
| 0288 0844 - 0288 090F   | -             | Reserved                                                                                                                                                                                                                                                                                                           |
| 0288 0910               | DEVCFG        | Parameters set through software for device configuration                                                                                                                                                                                                                                                           |
| 0288 0914               | MACID1        | EFUSE derived MAC address for C6457                                                                                                                                                                                                                                                                                |
| 0288 0918               | MACID2        | EFUSE derived MAC address for C6457                                                                                                                                                                                                                                                                                |
| 0288 0922 - 0288 091B   | -             | Reserved                                                                                                                                                                                                                                                                                                           |
| 0288 091C               | PRI_ALLOC     | Sets priority for Master peripherals                                                                                                                                                                                                                                                                               |
| 0288 0920               | WDRSTSEL      | Reset select for Watchdog (Timer1)                                                                                                                                                                                                                                                                                 |
| <b>End of Table 3-2</b> |               |                                                                                                                                                                                                                                                                                                                    |

<sup>1</sup> Writes are conditional based on valid keys written to both the KICK0 and KICK1 registers.

### 3.4 Device Status Register Description

The device status register depicts the device configuration selected upon power-on reset. Once set, these bits will remain set until a power-on reset. For the actual register bit names and their associated bit field descriptions, see [Table 3-4](#) and [Table 3-5](#).

[Table 3-3](#) shows the parameters that are set through software to configure different components on the device. The configuration is done through the device configuration DEVCFG register, which is one-time writeable through software. The register is reset on all hard resets and is locked after the first write.

**Table 3-3 Device Configuration Register Fields**

| Field                                         | Reset | Description        | Settings                                            |
|-----------------------------------------------|-------|--------------------|-----------------------------------------------------|
| <b>Device Configuration 1 Register Fields</b> |       |                    |                                                     |
| CLKS0                                         | 0b    | McBSP0 CLKS Select | 0 = CLKS0 device pin<br>1 = chip_clks from Main.PLL |
| CLKS1                                         | 0b    | McBSP1 CLKS Select | 0 = CLKS1 device pin<br>1 = chip_clks from Main.PLL |
| SYSCLKOUTEN                                   | 1b    | SYSCLKOUT Enable   | 0 = No clock output<br>1 = Clock output enabled     |
| <b>End of Table 3-3</b>                       |       |                    |                                                     |

**Table 3-4 Device Configuration Status Register (DEVSTAT)**

| HEX ADDRESS - 0288 0820h |           |          |       |    |    |    |    |        |    |    |    |          |    |    |         |    |
|--------------------------|-----------|----------|-------|----|----|----|----|--------|----|----|----|----------|----|----|---------|----|
| Bit                      | 31        | 30       | 29    | 28 | 27 | 26 | 25 | 24     | 23 | 22 | 21 | 20       | 19 | 18 | 17      | 16 |
| Acronym                  | Reserved  |          |       |    |    |    |    |        |    |    |    |          |    |    |         |    |
| Reset <sup>(1)</sup>     | R-0       |          |       |    |    |    |    |        |    |    |    |          |    |    |         |    |
| Bit                      | 15        | 14       | 13    | 12 | 11 | 10 | 9  | 8      | 7  | 6  | 5  | 4        | 3  | 2  | 1       | 0  |
| Acronym                  | ECLKINSEL | HPIWIDTH | CFGGP |    |    |    |    | DEVNUM |    |    |    | BOOTMODE |    |    | LENDIAN |    |
| Reset <sup>(1)</sup>     | 0         | 0        | R-n   |    |    |    |    | R      |    |    |    | R        |    |    | R-1     |    |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 3-5 Device Configuration Status Register Field Descriptions (Part 1 of 2)**

| Bit   | Acronym     | Description                                                                                                                                                                                                                                                                                       |
|-------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | Reserved    | Reserved. Read only, writes have no effect.                                                                                                                                                                                                                                                       |
| 15    | ECLKINSEL   | EMIFA input clock select — shows the status of what clock mode is enabled or disabled for EMIFA.<br>0 = ECLKIN (default mode)<br>1 = SYSCLK7 (CPU ÷ x) Clock Rate. The SYSCLK7 clock rate is software selectable via the PLL1 Controller. By default, SYSCLK7 is selected as CPU ÷ 10 clock rate. |
| 14    | HPIWIDTH    | HPI bus width control bit — shows the status of whether the HPI bus operates in 32-bit mode or in 16-bit mode.<br>0 = HPI operates in 16-bit mode. (default)<br>1 = HPI operates in 32-bit mode                                                                                                   |
| 13:9  | CFGGP[4:0]  | Used as general-purpose inputs for configuration purposes. These pins are latched at power-on reset. These values can be used by software routines for boot operations.                                                                                                                           |
| 8:5   | DEVNUM[3:0] | Device number.                                                                                                                                                                                                                                                                                    |

| Bit | Acronym       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:1 | BOOTMODE[3:0] | <p>Determines the boot method for the device. For more information on bootmode, see Section 2.4 <a href="#">“Boot Sequence”</a> on page 21.</p> <p>0000 = No Boot</p> <p>0001 = I<sup>2</sup>C Master Boot (Slave Address 0x50)</p> <p>0010 = I<sup>2</sup>C Master Boot (Slave Address 0x51)</p> <p>0011 = I<sup>2</sup>C Slave Boot</p> <p>0100 = HPI Boot</p> <p>0101 = EMIFA Boot</p> <p>0110 = EMAC Master Boot</p> <p>0111 = EMAC Slave Boot</p> <p>1000 = EMAC Forced Mode Boot</p> <p>1001 = Reserved</p> <p>1010 = RapidIO Boot (Configuration 0)</p> <p>1011 = RapidIO Boot (Configuration 1)</p> <p>1100 = RapidIO Boot (Configuration 2)</p> <p>1101 = RapidIO Boot (Configuration 3)</p> <p>111x = Reserved</p> |
| 0   | LENDIAN       | <p>Device Endian mode (LENDIAN) — Shows the status of whether the system is operating in Big Endian mode or Little Endian mode (default).</p> <p>0 = System is operating in Big Endian mode</p> <p>1 = System is operating in Little Endian mode (default)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

**End of Table 3-5**

The JTAG ID register is a read-only register that identifies to the customer the JTAG/Device ID. For the C6457 device, the JTAG ID register resides at address location 0x0288 0818. For the actual register bit names and their associated bit field descriptions, see [Table 3-6](#) and [Table 3-7](#).

| HEX ADDRESS - 0288 0818h |                         |    |    |    |                        |    |    |    |    |    |    |    |    |    |    |    |     |
|--------------------------|-------------------------|----|----|----|------------------------|----|----|----|----|----|----|----|----|----|----|----|-----|
| Bit                      | 31                      | 30 | 29 | 28 | 27                     | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |     |
| Acronym                  | VARIANT                 |    |    |    | PART NUMBER (16-bit)   |    |    |    |    |    |    |    |    |    |    |    |     |
| Reset <sup>(1)</sup>     | R-0000                  |    |    |    | R-0000 0000 1001 0110b |    |    |    |    |    |    |    |    |    |    |    |     |
| Bit                      | 15                      | 14 | 13 | 12 | 11                     | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |     |
| Acronym                  | PART NUMBER (Continued) |    |    |    | MANUFACTURER           |    |    |    |    |    |    |    |    |    |    |    | LSB |
| Reset <sup>(1)</sup>     |                         |    |    |    | 0000 0010 111b         |    |    |    |    |    |    |    |    |    |    |    | R-1 |

1 R/W = Read/Write; R = Read only; -n = value after reset

| Bit   | Acronym      | Value                | Description                                                                                |
|-------|--------------|----------------------|--------------------------------------------------------------------------------------------|
| 31:28 | VARIANT      | 0000                 | Variant (4-Bit) value. The value of this field depends on the silicon revision being used. |
| 27:12 | PART NUMBER  | 0000 0000 1001 0110b | Part Number for boundary scan                                                              |
| 11:1  | MANUFACTURER | 0000 0010 111b       | Manufacturer                                                                               |
| 0     | LSB          | 1b                   | This bit is read as a 1 for TMS320C6457                                                    |

**End of Table 3-7**

### 3.6 Pullup/Pulldown Resistors

Proper board design should ensure that input pins to the C6457 device always be at a valid logic level and not floating. This may be achieved via pullup/pulldown resistors. The C6457 device features internal pullup (IPU) and internal pulldown (IPD) resistors on most pins to eliminate the need, unless otherwise noted, for external pullup/pulldown resistors.

An external pullup/pulldown resistor needs to be used in the following situations:

- **Device Configuration Pins:** If the pin is both routed out and are not driven (in Hi-Z state), an external pullup/pulldown resistor must be used, even if the IPU/IPD matches the desired value/state.
- **Other Input Pins:** If the IPU/IPD does not match the desired value/state, use an external pullup/pulldown resistor to pull the signal to the opposite rail.

For the device configuration pins (listed in [Table 3-1](#)), if they are both routed out and are not driven (in Hi-Z state), it is strongly recommended that an external pullup/pulldown resistor be implemented. Although, internal pullup/pulldown resistors exist on these pins and they may match the desired configuration value, providing external connectivity can help ensure that valid logic levels are latched on these device configuration pins. In addition, applying external pullup/pulldown resistors on the device configuration pins adds convenience to the user in debugging and flexibility in switching operating modes.

Tips for choosing an external pullup/pulldown resistor:

- Consider the total amount of current that may pass through the pullup or pulldown resistor. Make sure to include the leakage currents of all the devices connected to the net, as well as any internal pullup or pulldown resistors.
- Decide a target value for the net. For a pulldown resistor, this should be below the lowest  $V_{IL}$  level of all inputs connected to the net. For a pullup resistor, this should be above the highest  $V_{IH}$  level of all inputs on the net. A reasonable choice would be to target the  $V_{OL}$  or  $V_{OH}$  levels for the logic family of the limiting device; which, by definition, have margin to the  $V_{IL}$  and  $V_{IH}$  levels.
- Select a pullup/pulldown resistor with the largest possible value that can still ensure that the net will reach the target pulled value when maximum current from all devices on the net is flowing through the resistor. The current to be considered includes leakage current plus, any other internal and external pullup/pulldown resistors on the net.
- For bidirectional nets, there is an additional consideration that sets a lower limit on the resistance value of the external resistor. Verify that the resistance is small enough that the weakest output buffer can drive the net to the opposite logic level (including margin).
- Remember to include tolerances when selecting the resistor value.
- For pullup resistors, also remember to include tolerances on the  $DV_{DD}$  rail.

For most systems:

- A 1-k $\Omega$  resistor can be used to oppose the IPU/IPD while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.
- A 20-k $\Omega$  resistor can be used to compliment the IPU/IPD on the device configuration pins while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For more detailed information on input current ( $I_I$ ), and the low-level/high-level input voltages ( $V_{IL}$  and  $V_{IH}$ ) for the TMS320C6457 device, see Section 6.3 “[Electrical Characteristics](#)” on page 89.

To determine which pins on the C6457 device include internal pullup/pulldown resistors, see Table 2-6 “[Terminal Functions](#)” on page 33.





## 4 System Interconnect

On the TMS320C6457 device, the C64x+ Megamodule, the EDMA3 transfer controllers, and the system peripherals are interconnected through two switch fabrics. The switch fabrics allow for low-latency, concurrent data transfers between master peripherals and slave peripherals; for example, through a switch fabric the CPU can send data to the Viterbi co-processor (VCP2) without affecting a data transfer between the HPI and the DDR2 memory controller. The switch fabrics also allow for seamless arbitration between the system masters when accessing system slaves.

### 4.1 Internal Buses, Bridges, and Switch Fabrics

Two types of buses exist in the C6457 device: data buses and configuration buses. Some C6457 peripherals have both a data bus and a configuration bus interface, while others only have one type of interface. Furthermore, the bus interface width and speed varies from peripheral to peripheral. Configuration buses are mainly used to access the register space of a peripheral and the data buses are used mainly for data transfers. However, in some cases, the configuration bus is also used to transfer data. For example, data is transferred to the VCP2 and TCP2 via their configuration bus. Similarly, the data bus can also be used to access the register space of a peripheral. For example, the EMIFA and DDR2 memory controller registers are accessed through their data bus interface.

The C64x+ Megamodule, the EDMA3 traffic controllers, and the various system peripherals can be classified into two categories: masters and slaves.

Masters are capable of initiating read and write transfers in the system and do not rely on the EDMA3 for their data transfers. Slaves on the other hand rely on the EDMA3 to perform transfers to and from them. Examples of masters include the EDMA3 traffic controllers, SRIO, EMAC, and HPI. Examples of slaves include the McBSP, UTOPIA, and I<sup>2</sup>C.

The C6457 device contains two switch fabrics through which masters and slaves communicate. The data switch fabric, known as the data switched central resource (SCR), is a high-throughput interconnect mainly used to move data across the system (for more information, see Section 4.2 “[Data Switch Fabric Connections](#)”). The data SCR connects masters to slaves via 128-bit data buses running at a SYSCLK4 frequency (SYSCLK4 is generated from PLL controller). Peripherals that have a 128-bit data bus interface running at this speed can connect directly to the data SCR; other peripherals require a bridge.

The configuration switch fabric, also known as the configuration switch central resource (SCR), is mainly used by the C64x+ Megamodule to access peripheral registers (for more information, see Section 4.3 “[Configuration Switch Fabric](#)”). The configuration SCR connects C64x+ Megamodule to slaves via 32-bit configuration buses running at a SYSCLK4 frequency (SYSCLK4 is generated from PLL controller). As with the data SCR, some peripherals require the use of a bridge to interface to the configuration SCR. Note that the data SCR also connects to the configuration SCR.

Bridges perform a variety of functions:

- Conversion between configuration bus and data bus.
- Width conversion between peripheral bus width and SCR bus width.
- Frequency conversion between peripheral bus frequency and SCR bus frequency.

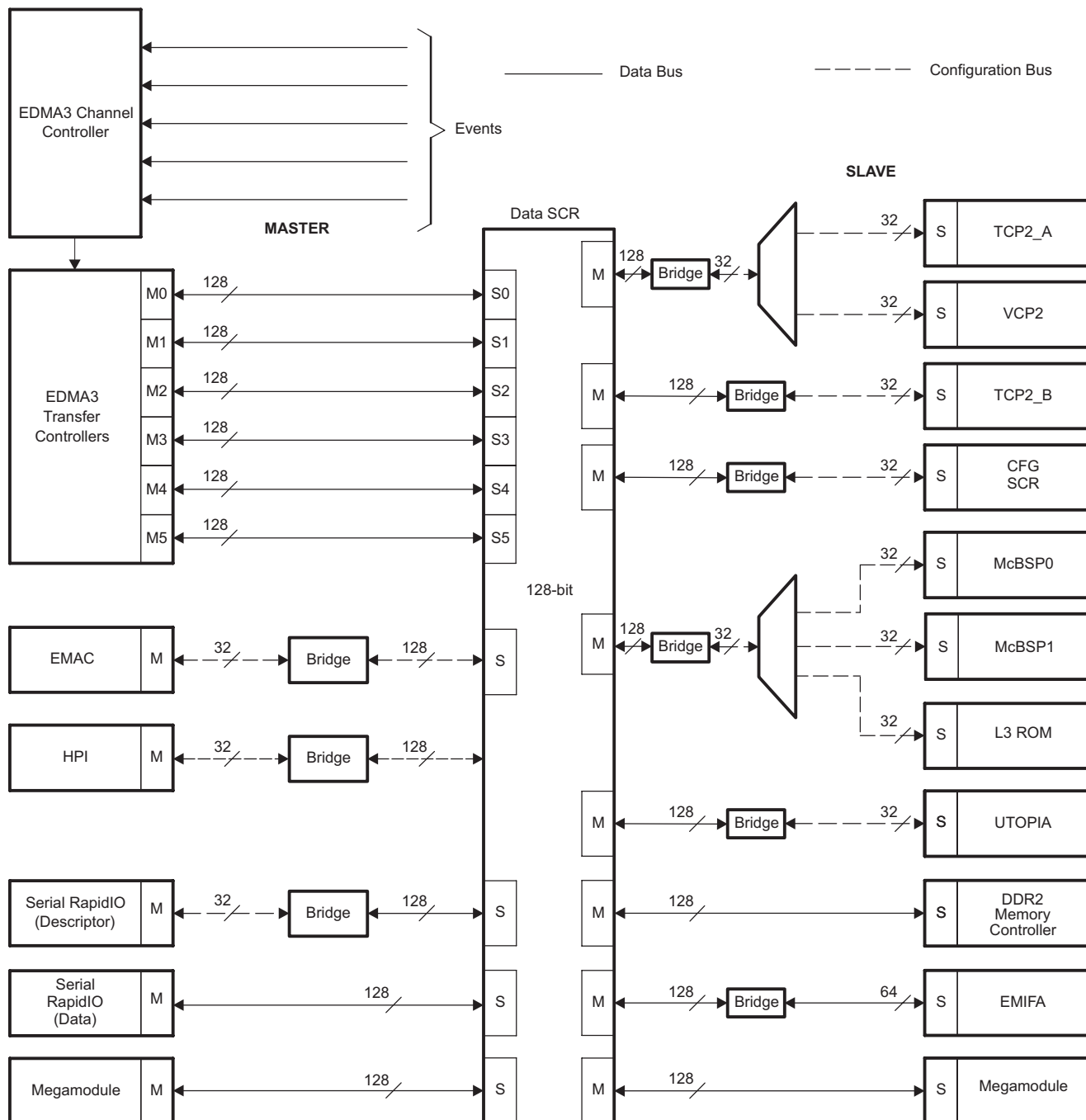
For example, the EMIFA requires a bridge to convert its 64-bit data bus interface into a 128-bit interface so that it can connect to the data SCR. In the case of the TCP2 and VCP2, a bridge is required to connect the data SCR to the 64-bit configuration bus interface.

Note that some peripherals can be accessed through the data SCR and also through the configuration SCR.

## 4.2 Data Switch Fabric Connections

Figure 4-1 shows the connection between slaves and masters through the data switched central resource (SCR). Masters are shown on the left and slaves on the right. The data SCR connects masters to slaves via 128-bit data buses running at a SYSCLK4 frequency. SYSCLK4 is supplied by the PLL controller and is fixed at a frequency equal to the CPU frequency divided by 3.

**Figure 4-1 Data Switched Central Resource Block Diagram**



Masters are shown on the left and slaves on the right. The data SCR connects masters to slaves via 128-bit data buses running at a SYSCLK4 frequency. SYSCLK4 is supplied by the PLL controller and is fixed at a frequency equal to the CPU frequency divided by 3.

Some peripherals and the C64x+ Megamodule have both slave and master ports. Note that each EDMA3 transfer controller has an independent connection to the data SCR.

The Serial RapidIO (SRIO) peripheral has two connections to the data SCR. The first connection is used when descriptors are being fetched from system memory. The other connection is used for all other data transfers.

Note that masters can access the configuration SCR through the data SCR. The configuration SCR is described in Section 4.3 “[Configuration Switch Fabric](#)”.

Not all masters on the C6457 DSP may connect to all slaves. Allowed connections are summarized in [Table 4-1](#).

**Table 4-1**      **SCR Connection Matrix**

|                           | VCP2 | TCP2_A | TCP2_B | McBSPs | L3 ROM | UTOPIA | Configuration SCR | DDR2 Memory Controller | EMIFA | Megamodule |
|---------------------------|------|--------|--------|--------|--------|--------|-------------------|------------------------|-------|------------|
| <b>TC0</b>                | Y    | Y      | Y      | N      | N      | N      | N                 | Y                      | Y     | Y          |
| <b>TC1</b>                | N    | N      | Y      | Y      | Y      | N      | N                 | Y                      | Y     | Y          |
| <b>TC2</b>                | N    | N      | N      | Y      | Y      | Y      | Y                 | Y                      | Y     | Y          |
| <b>TC3</b>                | N    | N      | N      | N      | N      | Y      | Y                 | Y                      | Y     | Y          |
| <b>TC4</b>                | N    | N      | N      | N      | N      | N      | Y                 | Y                      | Y     | Y          |
| <b>TC5</b>                | N    | N      | N      | N      | N      | N      | Y                 | Y                      | Y     | Y          |
| <b>EMAC</b>               | N    | N      | N      | N      | N      | N      | N                 | Y                      | Y     | Y          |
| <b>HPI</b>                | N    | N      | N      | N      | N      | N      | Y                 | Y                      | Y     | Y          |
| <b>SRIO<sup>(1)</sup></b> | N    | N      | N      | N      | N      | N      | Y                 | Y                      | Y     | Y          |
| <b>Megamodule</b>         | Y    | Y      | Y      | Y      | Y      | Y      | N                 | Y                      | Y     | N          |
| <b>End of Table 4-1</b>   |      |        |        |        |        |        |                   |                        |       |            |

1 Applies to both descriptor and data accesses by the SRIO peripheral.

### 4.3 Configuration Switch Fabric

[Figure 4-2](#) shows the connection between the C64x+ Megamodule and the configuration switched central resource (SCR). The configuration SCR is mainly used by the C64x+ Megamodule to access peripheral registers. The data SCR also has a connection to the configuration SCR which allows masters to access most peripheral registers. The only registers not accessible by the data SCR through the configuration SCR are the device configuration registers and the PLL controller registers; these can only be accessed by the C64x+ Megamodule.

The configuration SCR uses 32-bit configuration buses running at SYSCLK4 frequency. SYSCLK4 is supplied by the PLL controller and is fixed at a frequency equal to the CPU frequency divided by 3.

Figure 10: C64x+ Megamodule Peripheral Access Diagram

Legend:

- Configuration Bus
- Data Bus

The diagram shows the internal structure of the C64x+ Megamodule, including the CFG SCR, 32-bit Data Bus, and various peripheral modules. The Megamodule is connected to the Data Bus via a MUX and a Bridge. The Megamodule is also connected to the Configuration Bus via a MUX and a Bridge.

Peripheral modules and their connections:

- CFG SCR: MUX, Bridge, MUX
- 32-bit Data Bus: MUX, Bridge, MUX
- Peripheral modules: TCP2\_A, TCP2\_B, VCP2, ETB, McBSPs (x2), GPIO, UTOPIA, GPSC, I2C, Timers (x2), HPI, EMAC (MDIO, CP-GMAC, Ethernet CPPI, CP-SGMII, SERDES), PLL Controller (A), Device Configuration Registers (A), Serial RapidIO (Data), Serial RapidIO (Descriptor), EDMA3 CC, EDMA3 TC0, EDMA3 TC1, EDMA3 TC2, EDMA3 TC3, EDMA3 TC4, EDMA3 TC5

Note A: Only accessible by the C64x+ Megamodule

Note A: Only accessible by the C64x+ Megamodule

## 4.4 Bus Priorities

On the TMS320C6457 device, bus priority is programmable for each master. The register bit fields and default priority levels for C6457 bus masters are shown in [Table 4-2](#).

**Table 4-2 TMS320C6457 Default Bus Master Priorities**

| Bus Master                   | Default Priority Level | Priority Control                           |
|------------------------------|------------------------|--------------------------------------------|
| EDMA3TC0                     | 0                      | QUEPRI.PRIQ0 (EDMA3 register)              |
| EDMA3TC1                     | 0                      | QUEPRI.PRIQ1 (EDMA3 register)              |
| EDMA3TC2                     | 0                      | QUEPRI.PRIQ2 (EDMA3 register)              |
| EDMA3TC3                     | 0                      | QUEPRI.PRIQ3 (EDMA3 register)              |
| EDMA3TC4                     | 0                      | QUEPRI.PRIQ4 (EDMA3 register)              |
| EDMA3TC5                     | 0                      | QUEPRI.PRIQ5 (EDMA3 register)              |
| EMAC                         | 1                      | PRI_ALLOC.EMAC                             |
| SRIO (Data Access)           | 0                      | PER_SET_CNTL.CBA_TRANS_PRI (SRIO register) |
| SRIO (Descriptor Access)     | 1                      | PRI_ALLOC.SRIO_CPPI                        |
| HPI                          | 2                      | PRI_ALLOC.HOST                             |
| C64x+ Megamodule (MDMA port) | 7                      | MDMAARBE.PRI (C64x+ Megamodule Register)   |
| <b>End of Table 4-2</b>      |                        |                                            |

The priority levels should be tuned to obtain the best system performance for a particular application. Lower values indicate higher priorities. For some masters, the priority values are programmed at the system level by configuring the PRI\_ALLOC register. Details on the PRI\_ALLOC register are shown in [Table 4-3](#) and [Table 4-4](#). The C64x+ megamodule, SRIO, and EDMA masters contain registers that control their own priority values.

**Table 4-3 Priority Allocation Register (PRI\_ALLOC)**

|                      |                       |    |    |    |    |    |    |         |    |    |           |    |    |         |    |    |
|----------------------|-----------------------|----|----|----|----|----|----|---------|----|----|-----------|----|----|---------|----|----|
| 0x0288 091C          |                       |    |    |    |    |    |    |         |    |    |           |    |    |         |    |    |
| Bit                  | 31                    | 30 | 29 | 28 | 27 | 26 | 25 | 24      | 23 | 22 | 21        | 20 | 19 | 18      | 17 | 16 |
| Acronym              | Reserved              |    |    |    |    |    |    |         |    |    |           |    |    |         |    |    |
| Reset <sup>(1)</sup> | R-0000 0000 0000 0000 |    |    |    |    |    |    |         |    |    |           |    |    |         |    |    |
| Bit                  | 15                    | 14 | 13 | 12 | 11 | 10 | 9  | 8       | 7  | 6  | 5         | 4  | 3  | 2       | 1  | 0  |
| Acronym              | Reserved              |    |    |    |    |    |    | HPI     |    |    | SRIO_CPPI |    |    | EMAC    |    |    |
| Reset <sup>(1)</sup> | R-0000 000            |    |    |    |    |    |    | R/W-010 |    |    | R/W-001   |    |    | R/W-001 |    |    |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 4-4 Priority Allocation Register (PRI\_ALLOC) Field Descriptions**

| Bit                     | Acronym   | Value               | Description                                                                                                                   |
|-------------------------|-----------|---------------------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:16                   | Reserved  | 0000 0000 0000 0000 | Reserved.                                                                                                                     |
| 15:9                    | Reserved  | 0000 000            | Reserved.                                                                                                                     |
| 8:6                     | HOST      | 010                 | Priority of the HPI peripheral.                                                                                               |
| 5:3                     | SRIO_CPPI | 001                 | Priority of the Serial RapidIO when accessing descriptors from system memory. This priority is set in the peripheral, itself. |
| 2:0                     | EMAC      | 001                 | Priority of the EMAC peripheral.                                                                                              |
| <b>End of Table 4-4</b> |           |                     |                                                                                                                               |

The priority is enforced when several masters in the system are vying for the same endpoint. Note that the configuration SCR port on the data SCR is considered a single endpoint meaning priority will be enforced when multiple masters try to access the configuration SCR. Priority is also enforced on the configuration SCR side when a master (through the data SCR) tries to access the same endpoint as the C64x+ megamodule.

In the PRI\_ALLOC register, the HOST field applies to the priority of the HPI peripheral. The EMAC fields specify the priority of the EMAC peripheral. The SRIO\_CPPI field is used to specify the priority of the Serial RapidIO when accessing descriptors from system memory. The priority for Serial RapidIO data accesses is set in the peripheral itself.

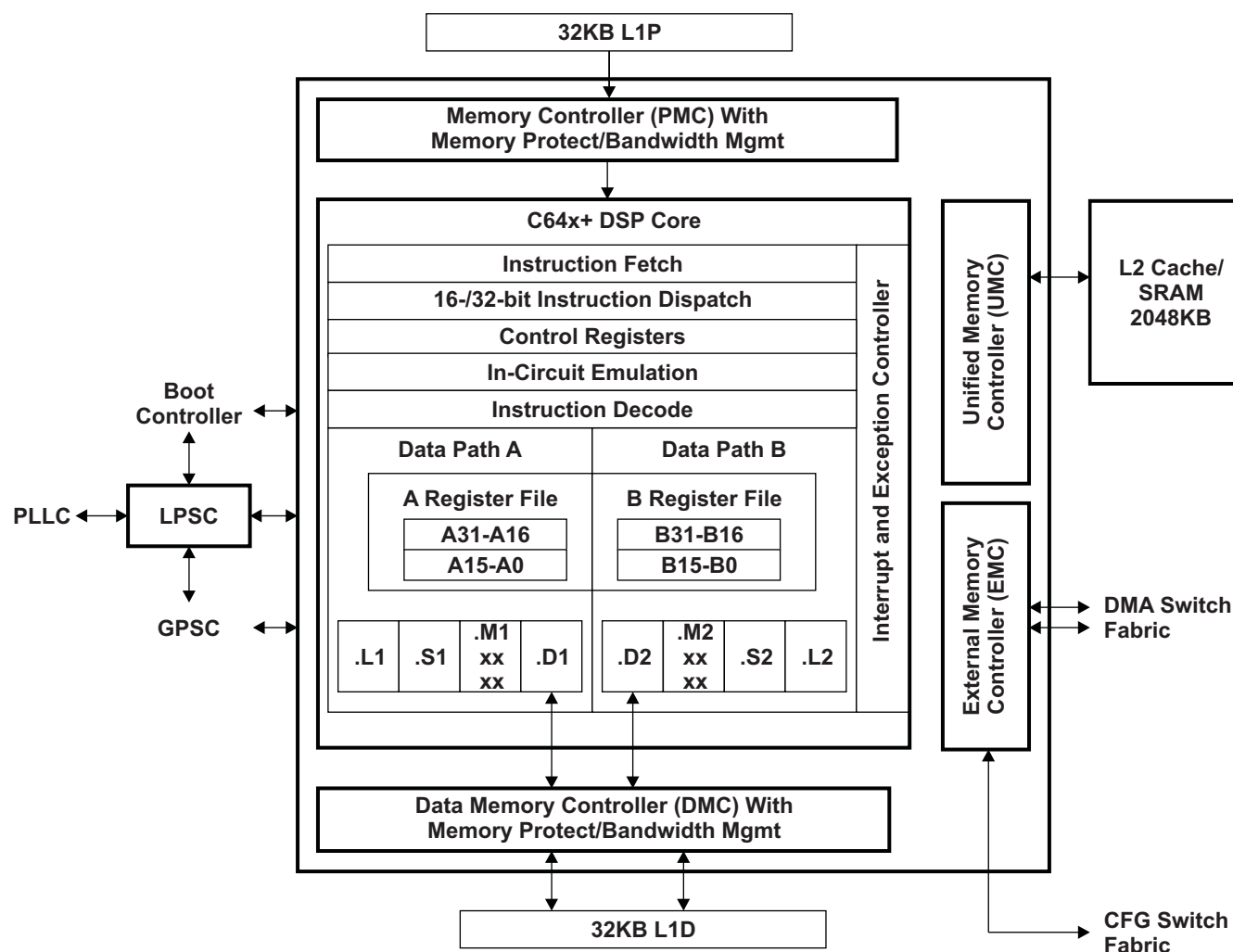
## 5 C64x+ Megamodule

The C64x+ Megamodule consists of several components:

- The C64x+ CPU and associated C64x+ Megamodule core
- Level-one and level-two memories (L1P, L1D, L2)
- Interrupt controller
- Power-down controller
- External memory controller
- A dedicated power/sleep controller (LPSC)

The C64x+ Megamodule also provides support for memory protection and bandwidth management (for resources local to the C64x+ Megamodule). [Figure 5-1](#) shows a block diagram of the C64x+ Megamodule.

**Figure 5-1** 64x+ Megamodule Block Diagram



For more detailed information on the TMS320C64x+ megamodule on the C6457 device, see the *TMS320C64x+ Megamodule Reference Guide* (literature number [SPRU871](#)).

## 5.1 Memory Architecture

The TMS320C6457 device contains a 2048KB level-2 memory (L2), a 32KB level-1 program memory (L1P), and a 32KB level-1 data memory (L1D). All memory on the C6457 has a unique location in the memory map (see Table 2-2 “TMS320C6457 Memory Map Summary” on page 19).

After device reset, L1P and L1D cache are configured as all cache, by default. The L1P and L1D cache can be reconfigured via software through the L1PMODE field of the L1P Configuration Register (L1PMODE) and the L1DMODE field of the L1D Configuration Register (L1DCFG) of the C64x+ Megamodule. L1D is a two-way set-associative cache, while L1P is a direct-mapped cache.

The on-chip bootloader changes the reset configuration for L1P and L1D. For more information, see the *TMS320C6457 Bootloader User's Guide* (literature number [SPRUGL5](#)).

For more information on the operation L1 and L2 caches, see the *TMS320C64x+ DSP Cache User's Guide* (literature number [SPRU862](#)).

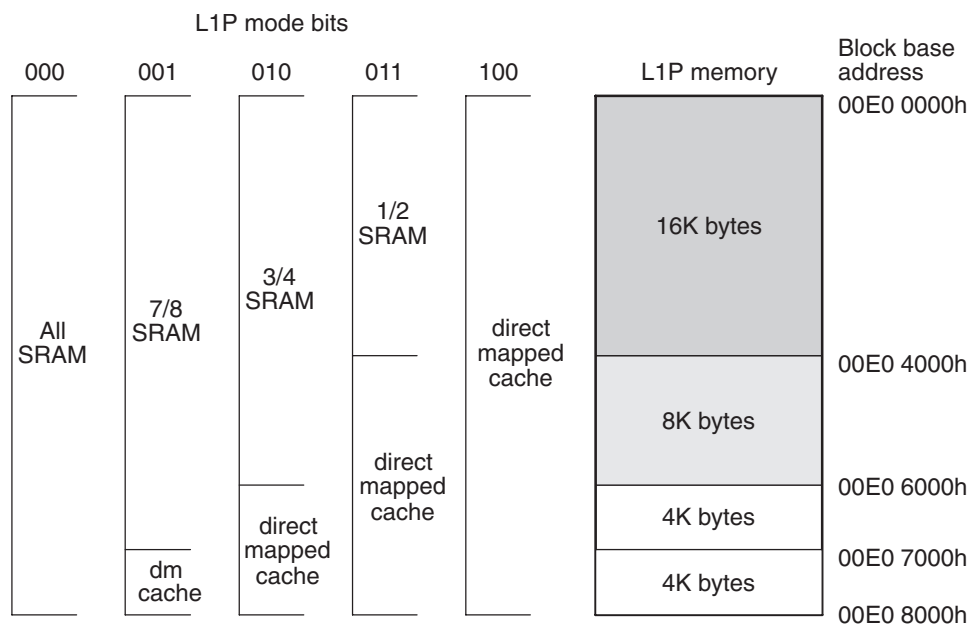
### 5.1.1 L1P Memory

The L1P memory configuration for the C6457 device is as follows:

- Region 0 size is 0K bytes (disabled)
- Region 1 size is 32K bytes with no wait states

[Figure 5-2](#) shows the available SRAM/cache configurations for L1P.

**Figure 5-2 TMS320C6457 L1P Memory Configurations**





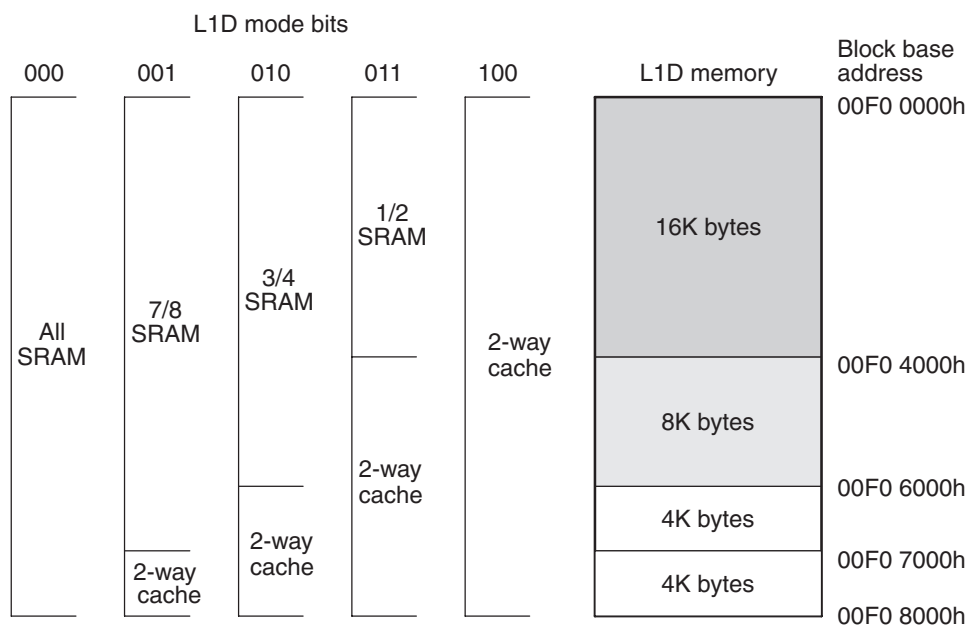
## 5.1.2 L1D Memory

The L1D memory configuration for the C6457 device is as follows:

- Region 0 size is 0K bytes (disabled)
- Region 1 size is 32K bytes with no wait states

Figure 5-3 shows the available SRAM/cache configurations for L1D.

**Figure 5-3 TMS320C6457 L1D Memory Configurations**



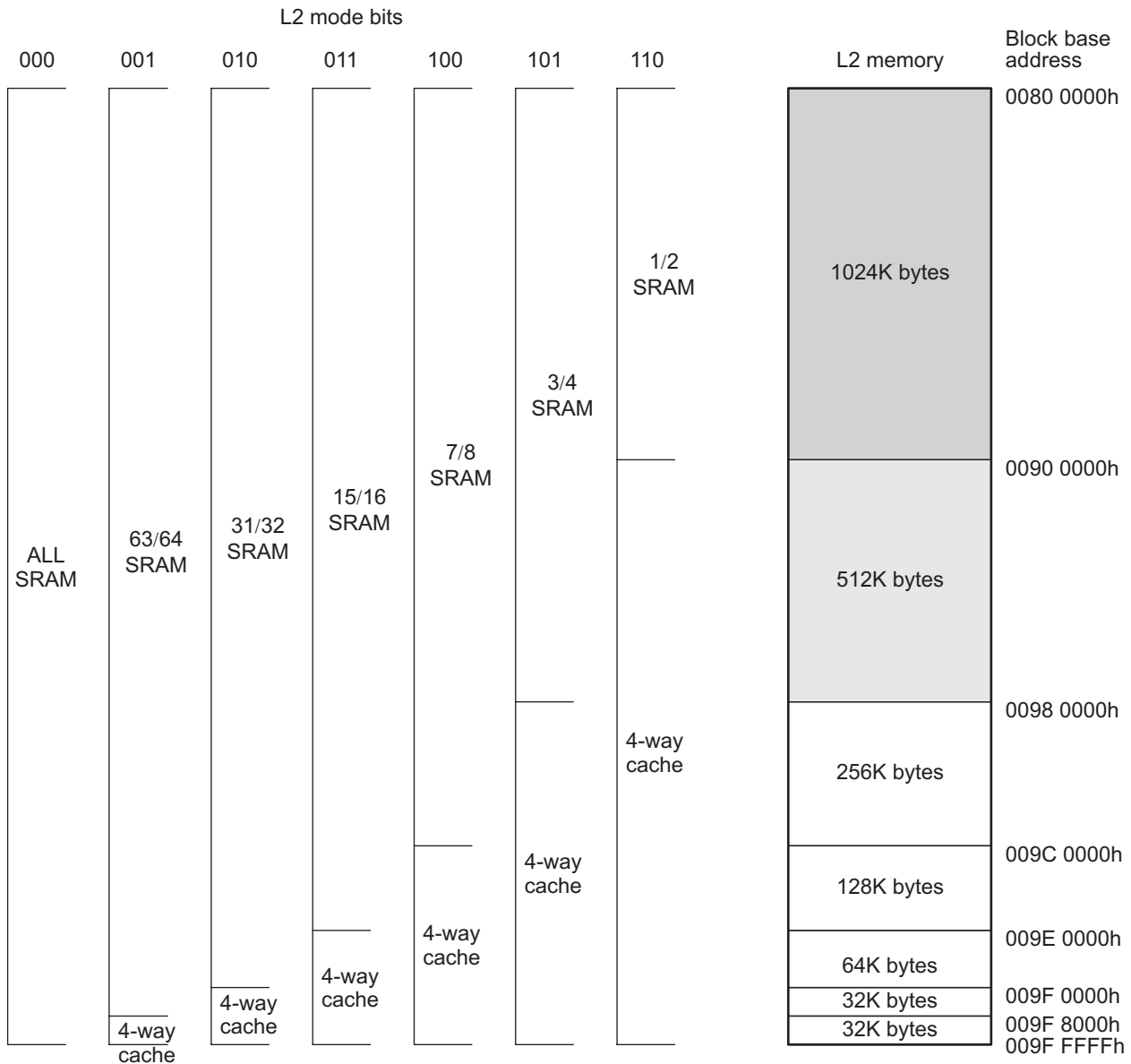
### 5.1.3 L2 Memory

The L2 memory configuration for the C6457 device is as follows:

- Memory size is 2048KB
- Starting address is 0080 0000h

L2 memory can be configured as all SRAM or as part 4-way set-associative cache. The amount of L2 memory that is configured as cache is controlled through the L2MODE field of the L2 Configuration Register (L2CFG) of the C64x+ Megamodule. [Figure 5-4](#) shows the available SRAM/cache configurations for L2. By default, L2 is configured as all SRAM after device reset.

**Figure 5-4 TMS320C6457 L2 Memory Configurations**



### 5.1.4 L3 Memory

The L3 ROM on the device is 64KB. The contents of the ROM are divided into two partitions. The first is the ROM bootloader with the primary purpose of containing software to boot the device. There is no requirement to block accesses from this portion to the ROM. The second partition is the secure portion of ROM, which has a secure kernel that is necessary for support of security features on the device. The secure portion of ROM cannot be accessed both on secure, and non-secure parts. Only secure supervisors should have access.

Emulation accesses follows the same rules of the secure portion of the ROM. Emulation can access the non-secure portion of the ROM, but cannot read the secure portion of the ROM.

## 5.2 Memory Protection

Memory protection allows an operating system to define who or what is authorized to access L1D, L1P, and L2 memory. To accomplish this, the L1D, L1P, and L2 memories are divided into pages. There are 16 pages of L1P (2KB each), 16 pages of L1D (2KB each), and 64 pages of L2 (32KB each). The L1D, L1P, and L2 memory controllers in the C64x+ Megamodule are equipped with a set of registers that specify the permissions for each memory page.

Each page may be assigned with fully orthogonal user and supervisor read, write, and execute permissions. In addition, a page may be marked as either (or both) locally accessible or globally accessible. A local access is a direct CPU access to L1D, L1P, and L2, while a global access is initiated by a DMA (either IDMA or the EDMA3) or by other system masters. Note that EDMA or IDMA transfers programmed by the CPU count as global accesses. On a secure device, pages can be restricted to secure access only (default) or opened up for public, non-secure access.

The CPU and each of the system masters on the device are all assigned a privilege ID (see [Table 5-1](#)). It is only possible to specify whether memory pages are locally or globally accessible.

**Table 5-1 Available Memory Page Protection Scheme With Privilege ID**

| Privid Module    | Description              |
|------------------|--------------------------|
| 0                | C64x+ Megamodule         |
| 1                | Reserved                 |
| 2                | Reserved                 |
| 3                | EMAC                     |
| 4                | RapidIO and RapidIO CPPI |
| 5                | HPI                      |
| End of Table 5-1 |                          |

The AID0 and LOCAL bits of the memory protection page attribute registers specify the memory page protection scheme, see [Table 5-2](#).

**Table 5-2 Available Memory Page Protection Schemes**

| AID0 Bit | Local Bit | Description                                                                                                    |
|----------|-----------|----------------------------------------------------------------------------------------------------------------|
| 0        | 0         | No access to memory page is permitted.                                                                         |
| 0        | 1         | Only direct access by CPU is permitted.                                                                        |
| 1        | 0         | Only accesses by system masters and IDMA are permitted (includes EDMA and IDMA accesses initiated by the CPU). |
| 1        | 1         | All accesses permitted                                                                                         |

Faults are handled by software in an interrupt (or an exception, programmable within the C64x+ megamodule interrupt controller) service routine. A CPU or DMA access to a page without the proper permissions will:

- Block the access — reads return zero, writes are ignored
- Capture the initiator in a status register — ID, address, and access type are stored
- Signal event to CPU interrupt controller

The software is responsible for taking corrective action to respond to the event and resetting the error status in the memory controller. For more information on memory protection for L1D, L1P, and L2, see the *TMS320C64x+ Megamodule Reference Guide* (literature number [SPRU871](#)).

### 5.3 Bandwidth Management

When multiple requestors contend for a single C64x+ Megamodule resource, the conflict is resolved by granting access to the highest priority requestor. The following four resources are managed by the Bandwidth Management control hardware:

- Level 1 Program (L1P) SRAM/Cache
- Level 1 Data (L1D) SRAM/Cache
- Level 2 (L2) SRAM/Cache
- Memory-mapped registers configuration bus

The priority level for operations initiated within the C64x+ Megamodule are declared through registers in the C64x+ Megamodule. These operations are:

- CPU-initiated transfers
- User-programmed cache coherency operations
- IDMA-initiated transfers

The priority level for operations initiated outside the C64x+ Megamodule by system peripherals is declared through the Priority Allocation Register (PRI\_ALLOC), see Section 4.4 “[Bus Priorities](#)” on page 69. System peripherals with no fields in PRI\_ALLOC have their own registers to program their priorities.

More information on the bandwidth management features of the C64x+ Megamodule can be found in the *TMS320C64x+ Megamodule Reference Guide* (literature number [SPRU871](#).)

### 5.4 Power-Down Control

The C64x+ Megamodule supports the ability to power-down various parts of the C64x+ Megamodule. The power-down controller (PDC) of the C64x+ Megamodule can be used to power down L1P, the cache control hardware, the CPU, and the entire C64x+ Megamodule. These power-down features can be used to design systems for lower overall system power requirements.



**Note**—The C6457 does not support power-down modes for the L2 memory at this time.

More information on the power-down features of the C64x+ Megamodule can be found in the *TMS320C64x+ Megamodule Reference Guide* (literature number [SPRU871](#)).

## 5.5 Megamodule Resets

Table 5-3 shows the reset types supported on the C6457 device and they affect the resetting of the Megamodule, either both globally or just locally.

**Table 5-3 Megamodule Reset (Global or Local)**

| Reset Type              | Global Megamodule Reset | Local Megamodule Reset |
|-------------------------|-------------------------|------------------------|
| Power-On Reset          | Y                       | Y                      |
| Warm Reset              | Y                       | Y                      |
| System Reset            | Y                       | Y                      |
| CPU Reset               | N                       | Y                      |
| <b>End of Table 5-3</b> |                         |                        |

For more detailed information on the global and local Megamodule resets, see the *TMS320C64x+ Megamodule Reference Guide* (literature number [SPRU871](#)). And for more detailed information on device resets, see Section 7.6 “Reset Controller” on page 123.

## 5.6 Megamodule Revision

The version and revision of the C64x+ Megamodule can be read from the Megamodule Revision ID Register (MM\_REVID) located at address 0181 2000h. The MM\_REVID register is shown in Table 5-4 and described in Table 5-5. The C64x+ Megamodule revision is dependant on the silicon revision being used.

**Table 5-4 Megamodule Revision ID Register (MM\_REVID)**

| Address - 0181 2000h |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|----------------------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Bit                  | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Acronym              | VERSION  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset <sup>(1)</sup> | R-5h     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Bit                  | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Acronym              | REVISION |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset <sup>(1)</sup> | R-n      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 5-5 Megamodule Revision ID Register (MM\_REVID) Field Descriptions**

| Bit                     | Acronym  | Value | Description                                                                                 |
|-------------------------|----------|-------|---------------------------------------------------------------------------------------------|
| 31:16                   | VERSION  | 5h    | Version of the C64x+ Megamodule implemented on the device. This field is always read as 5h. |
| 15:0                    | REVISION | -     | Revision of the C64x+ Megamodule version implemented on the device.                         |
| <b>End of Table 5-5</b> |          |       |                                                                                             |

## 5.7 C64x+ Megamodule Register Descriptions

**Table 5-6 Megamodule Interrupt Registers (Part 1 of 2)**

| Hex Address Range     | Acronym  | Register Name                         |
|-----------------------|----------|---------------------------------------|
| 0180 0000             | EVTFLAG0 | Event Flag Register 0 (Events [31:0]) |
| 0180 0004             | EVTFLAG1 | Event Flag Register 1                 |
| 0180 0008             | EVTFLAG2 | Event Flag Register 2                 |
| 0180 000C             | EVTFLAG3 | Event Flag Register 3                 |
| 0180 0010 - 0180 001C | -        | Reserved                              |
| 0180 0020             | EVTSET0  | Event Set Register 0 (Events [31:0])  |
| 0180 0024             | EVTSET1  | Event Set Register 1                  |

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**Table 5-6 Megamodule Interrupt Registers (Part 2 of 2)**

| Hex Address Range       | Acronym   | Register Name                                       |
|-------------------------|-----------|-----------------------------------------------------|
| 0180 0028               | EVTSET2   | Event Set Register 2                                |
| 0180 002C               | EVTSET3   | Event Set Register 3                                |
| 0180 0030 - 0180 003C   | -         | Reserved                                            |
| 0180 0040               | EVTCLR0   | Event Clear Register 0 (Events [31:0])              |
| 0180 0044               | EVTCLR1   | Event Clear Register 1                              |
| 0180 0048               | EVTCLR2   | Event Clear Register 2                              |
| 0180 004C               | EVTCLR3   | Event Clear Register 3                              |
| 0180 0050 - 0180 007C   | -         | Reserved                                            |
| 0180 0080               | EVTMASK0  | Event Mask Register 0 (Events [31:0])               |
| 0180 0084               | EVTMASK1  | Event Mask Register 1                               |
| 0180 0088               | EVTMASK2  | Event Mask Register 2                               |
| 0180 008C               | EVTMASK3  | Event Mask Register 3                               |
| 0180 0090 - 0180 009C   | -         | Reserved                                            |
| 0180 00A0               | MEVTFLAG0 | Masked Event Flag Status Register 0 (Events [31:0]) |
| 0180 00A4               | MEVTFLAG1 | Masked Event Flag Status Register 1                 |
| 0180 00A8               | MEVTFLAG2 | Masked Event Flag Status Register 2                 |
| 0180 00AC               | MEVTFLAG3 | Masked Event Flag Status Register 3                 |
| 0180 00B0 - 0180 00BC   | -         | Reserved                                            |
| 0180 00C0               | EXPMASK0  | Exception Mask Register 0 (Events [31:0])           |
| 0180 00C4               | EXPMASK1  | Exception Mask Register 1                           |
| 0180 00C8               | EXPMASK2  | Exception Mask Register 2                           |
| 0180 00CC               | EXPMASK3  | Exception Mask Register 3                           |
| 0180 00D0 - 0180 00DC   | -         | Reserved                                            |
| 0180 00E0               | MEXPFLAG0 | Masked Exception Flag Register 0                    |
| 0180 00E4               | MEXPFLAG1 | Masked Exception Flag Register 1                    |
| 0180 00E8               | MEXPFLAG2 | Masked Exception Flag Register 2                    |
| 0180 00EC               | MEXPFLAG3 | Masked Exception Flag Register 3                    |
| 0180 00F0 - 0180 00FC   | -         | Reserved                                            |
| 0180 0100               | -         | Reserved                                            |
| 0180 0104               | INTMUX1   | Interrupt Multiplexor Register 1                    |
| 0180 0108               | INTMUX2   | Interrupt Multiplexor Register 2                    |
| 0180 010C               | INTMUX3   | Interrupt Multiplexor Register 3                    |
| 0180 0110 - 0180 013C   | -         | Reserved                                            |
| 0180 0140               | AEGMUX0   | Advanced Event Generator Mux Register 0             |
| 0180 0144               | AEGMUX1   | Advanced Event Generator Mux Register 1             |
| 0180 0148 - 0180 017C   | -         | Reserved                                            |
| 0180 0180               | INTXSTAT  | Interrupt Exception Status Register                 |
| 0180 0184               | INTXCLR   | Interrupt Exception Clear Register                  |
| 0180 0188               | INTDMASK  | Dropped Interrupt Mask Register                     |
| 0180 0188 - 0180 01BC   | -         | Reserved                                            |
| 0180 01C0               | EVTASRT   | Event Asserting Register                            |
| 0180 01C4 - 0180 FFFF   | -         | Reserved                                            |
| <b>End of Table 5-6</b> |           |                                                     |

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**Table 5-7 Megamodule Powerdown Control Registers**

| Hex Address Range       | Acronym | Register Name                          |
|-------------------------|---------|----------------------------------------|
| 0181 0000               | PDCCMD  | Power-down controller command register |
| 0181 0004 - 0181 1FFF   | -       | Reserved                               |
| <b>End of Table 5-7</b> |         |                                        |

**Table 5-8 Megamodule Revision Register**

| Hex Address Range       | Acronym  | Register Name                   |
|-------------------------|----------|---------------------------------|
| 0181 2000               | MM_REVID | Megamodule Revision ID Register |
| 0181 2004 - 0181 2FFF   | -        | Reserved                        |
| <b>End of Table 5-8</b> |          |                                 |

**Table 5-9 Megamodule IDMA Registers**

| Hex Address Range       | Acronym   | Register Name                               |
|-------------------------|-----------|---------------------------------------------|
| 0182 0000               | IDMA0STAT | IDMA Channel 0 Status Register              |
| 0182 0004               | IDMA0MASK | IDMA Channel 0 Mask Register                |
| 0182 0008               | IMDA0SRC  | IDMA Channel 0 Source Address Register      |
| 0182 000C               | IDMA0DST  | IDMA Channel 0 Destination Address Register |
| 0182 0010               | IDMA0CNT  | IDMA Channel 0 Count Register               |
| 0182 0014 - 0182 00FC   | -         | Reserved                                    |
| 0182 0100               | IDMA1STAT | IDMA Channel 1 Status Register              |
| 0182 0104               | -         | Reserved                                    |
| 0182 0108               | IMDA1SRC  | IDMA Channel 1 Source Address Register      |
| 0182 010C               | IDMA1DST  | IDMA Channel 1 Destination Address Register |
| 0182 0110               | IDMA1CNT  | IDMA Channel 1 Count Register               |
| 0182 0114 - 0182 017C   | -         | Reserved                                    |
| 0182 0180               | -         | Reserved                                    |
| 0182 0184 - 0182 01FF   | -         | Reserved                                    |
| <b>End of Table 5-9</b> |           |                                             |

**Table 5-10 Megamodule Cache Configuration Registers (Part 1 of 4)**

| Hex Address Range     | Acronym | Register Name                                                                  |
|-----------------------|---------|--------------------------------------------------------------------------------|
| 0184 0000             | L2CFG   | L2 Cache Configuration Register                                                |
| 0184 0004 - 0184 001F | -       | Reserved                                                                       |
| 0184 0020             | L1PCFG  | L1P Configuration Register                                                     |
| 0184 0024             | L1PCC   | L1P Cache Control Register                                                     |
| 0184 0028 - 0184 003F | -       | Reserved                                                                       |
| 0184 0040             | L1DCFG  | L1D Configuration Register                                                     |
| 0184 0044             | L1DCC   | L1D Cache Control Register                                                     |
| 0184 0048 - 0184 0FFF | -       | Reserved                                                                       |
| 0184 1000 - 0184 104F | -       | See <a href="#">Table 5-13 "CPU Megamodule Bandwidth Management Registers"</a> |
| 0184 1050 - 0184 3FFF | -       | Reserved                                                                       |
| 0184 4000             | L2WBAR  | L2 Writeback Base Address Register — for Block Writebacks                      |
| 0184 4004             | L2WWC   | L2 Writeback Word Count Register                                               |
| 0184 4008 - 0184 400C | -       | Reserved                                                                       |

**Table 5-10 Megamodule Cache Configuration Registers (Part 2 of 4)**

| Hex Address Range     | Acronym          | Register Name                                                            |
|-----------------------|------------------|--------------------------------------------------------------------------|
| 0184 4010             | L2WIBAR          | L2 Writeback and Invalidate Base Address Register — for Block Writebacks |
| 0184 4014             | L2WIWC           | L2 Writeback and Invalidate word count register                          |
| 0184 4018             | L2IBAR           | L2 Invalidate Base Address Register                                      |
| 0184 401C             | L2IWC            | L2 Invalidate Word Count Register                                        |
| 0184 4020             | L1PIBAR          | L1P Invalidate Base Address Register                                     |
| 0184 4024             | L1PIWC           | L1P Invalidate Word Count Register                                       |
| 0184 4030             | L1DWIBAR         | L1D Writeback and Invalidate Base Address Register                       |
| 0184 4034             | L1DWIWC          | L1D Writeback and Invalidate Word Count Register                         |
| 0184 4038             | -                | Reserved                                                                 |
| 0184 4040             | L1DWBAR          | L1D Writeback Base Address Register — for Block Writebacks               |
| 0184 4044             | L1DWWC           | L1D Writeback Word Count Register                                        |
| 0184 4048             | L1DIBAR          | L1D Invalidate Base Address Register                                     |
| 0184 404C             | L1DIWC           | L1D Invalidate Word Count Register                                       |
| 0184 4050 - 0184 4FFF | -                | Reserved                                                                 |
| 0184 5000             | L2WB             | L2 Global Writeback Register                                             |
| 0184 5004             | L2WBINV          | L2 Global Writeback and Invalidate Register                              |
| 0184 5008             | L2INV            | L2 Global Invalidate Register                                            |
| 0184 500C - 0184 5024 | -                | Reserved                                                                 |
| 0184 5028             | L1PINV           | L1P Global Invalidate Register                                           |
| 0184 502C - 0184 503C | -                | Reserved                                                                 |
| 0184 5040             | L1DWB            | L1D Global Writeback Register                                            |
| 0184 5044             | L1DWBINV         | L1D Global Writeback and Invalidate Register                             |
| 0184 5048             | L1DINV           | L1D Global Invalidate Register                                           |
| 0184 504C - 0184 5FFF | -                | Reserved                                                                 |
| 0184 6000 - 0184 640F | -                | See Table 5-11 “Megamodule Error Detection Correct Registers”            |
| 0184 6410 - 0184 7FFF | -                | Reserved                                                                 |
| 0184 8000 - 0184 81FC | MAR0 to MAR127   | Reserved                                                                 |
| 0184 8200 - 0184 823C | MAR128 to MAR143 | Reserved                                                                 |
| 0184 8240 - 0184 827C | MAR144 to MAR159 | Reserved                                                                 |
| 0184 8280             | MAR160           | Controls EMIFA CE2 Range A000 0000 - A0FF FFFF                           |
| 0184 8284             | MAR161           | Controls EMIFA CE2 Range A100 0000 - A1FF FFFF                           |
| 0184 8288             | MAR162           | Controls EMIFA CE2 Range A200 0000 - A2FF FFFF                           |
| 0184 828C             | MAR163           | Controls EMIFA CE2 Range A300 0000 - A3FF FFFF                           |
| 0184 8290             | MAR164           | Controls EMIFA CE2 Range A400 0000 - A4FF FFFF                           |
| 0184 8294             | MAR165           | Controls EMIFA CE2 Range A500 0000 - A5FF FFFF                           |
| 0184 8298             | MAR166           | Controls EMIFA CE2 Range A600 0000 - A6FF FFFF                           |
| 0184 829C             | MAR167           | Controls EMIFA CE2 Range A700 0000 - A7FF FFFF                           |
| 0184 82A0             | MAR168           | Controls EMIFA CE2 Range A800 0000 - A8FF FFFF                           |
| 0184 82A4             | MAR169           | Controls EMIFA CE2 Range A900 0000 - A9FF FFFF                           |
| 0184 82A8             | MAR170           | Controls EMIFA CE2 Range AA00 0000 - AAFF FFFF                           |
| 0184 82AC             | MAR171           | Controls EMIFA CE2 Range AB00 0000 - ABFF FFFF                           |
| 0184 82B0             | MAR172           | Controls EMIFA CE2 Range AC00 0000 - ACFF FFFF                           |
| 0184 82B4             | MAR173           | Controls EMIFA CE2 Range AD00 0000 - ADFF FFFF                           |
| 0184 82B8             | MAR174           | Controls EMIFA CE2 Range AE00 0000 - AEFF FFFF                           |



**Table 5-10 Megamodule Cache Configuration Registers (Part 3 of 4)**

| Hex Address Range | Acronym | Register Name                                  |
|-------------------|---------|------------------------------------------------|
| 0184 82BC         | MAR175  | Controls EMIFA CE2 Range AF00 0000 - AFFF FFFF |
| 0184 82C0         | MAR176  | Controls EMIFA CE3 Range B000 0000 - B0FF FFFF |
| 0184 82C4         | MAR177  | Controls EMIFA CE3 Range B100 0000 - B1FF FFFF |
| 0184 82C8         | MAR178  | Controls EMIFA CE3 Range B200 0000 - B2FF FFFF |
| 0184 82CC         | MAR179  | Controls EMIFA CE3 Range B300 0000 - B3FF FFFF |
| 0184 82D0         | MAR180  | Controls EMIFA CE3 Range B400 0000 - B4FF FFFF |
| 0184 82D4         | MAR181  | Controls EMIFA CE3 Range B500 0000 - B5FF FFFF |
| 0184 82D8         | MAR182  | Controls EMIFA CE3 Range B600 0000 - B6FF FFFF |
| 0184 82DC         | MAR183  | Controls EMIFA CE3 Range B700 0000 - B7FF FFFF |
| 0184 82E0         | MAR184  | Controls EMIFA CE3 Range B800 0000 - B8FF FFFF |
| 0184 82E4         | MAR185  | Controls EMIFA CE3 Range B900 0000 - B9FF FFFF |
| 0184 82E8         | MAR186  | Controls EMIFA CE3 Range BA00 0000 - BAFF FFFF |
| 0184 82EC         | MAR187  | Controls EMIFA CE3 Range BB00 0000 - BBFF FFFF |
| 0184 82F0         | MAR188  | Controls EMIFA CE3 Range BC00 0000 - BCFF FFFF |
| 0184 82F4         | MAR189  | Controls EMIFA CE3 Range BD00 0000 - BDFF FFFF |
| 0184 82F8         | MAR190  | Controls EMIFA CE3 Range BE00 0000 - BEFF FFFF |
| 0184 82FC         | MAR191  | Controls EMIFA CE3 Range BF00 0000 - BFFF FFFF |
| 0184 8300         | MAR192  | Controls EMIFA CE4 Range C000 0000 - C0FF FFFF |
| 0184 8304         | MAR193  | Controls EMIFA CE4 Range C100 0000 - C1FF FFFF |
| 0184 8308         | MAR194  | Controls EMIFA CE4 Range C200 0000 - C2FF FFFF |
| 0184 830C         | MAR195  | Controls EMIFA CE4 Range C300 0000 - C3FF FFFF |
| 0184 8310         | MAR196  | Controls EMIFA CE4 Range C400 0000 - C4FF FFFF |
| 0184 8314         | MAR197  | Controls EMIFA CE4 Range C500 0000 - C5FF FFFF |
| 0184 8318         | MAR198  | Controls EMIFA CE4 Range C600 0000 - C6FF FFFF |
| 0184 831C         | MAR199  | Controls EMIFA CE4 Range C700 0000 - C7FF FFFF |
| 0184 8320         | MAR200  | Controls EMIFA CE4 Range C800 0000 - C8FF FFFF |
| 0184 8324         | MAR201  | Controls EMIFA CE4 Range C900 0000 - C9FF FFFF |
| 0184 8328         | MAR202  | Controls EMIFA CE4 Range CA00 0000 - CAFF FFFF |
| 0184 832C         | MAR203  | Controls EMIFA CE4 Range CB00 0000 - CBFF FFFF |
| 0184 8330         | MAR204  | Controls EMIFA CE4 Range CC00 0000 - CCFF FFFF |
| 0184 8334         | MAR205  | Controls EMIFA CE4 Range CD00 0000 - CDFF FFFF |
| 0184 8338         | MAR206  | Controls EMIFA CE4 Range CE00 0000 - CEFF FFFF |
| 0184 833C         | MAR207  | Controls EMIFA CE4 Range CF00 0000 - CFFF FFFF |
| 0184 8340         | MAR208  | Controls EMIFA CE5 Range D000 0000 - D0FF FFFF |
| 0184 8344         | MAR209  | Controls EMIFA CE5 Range D100 0000 - D1FF FFFF |
| 0184 8348         | MAR210  | Controls EMIFA CE5 Range D200 0000 - D2FF FFFF |
| 0184 834C         | MAR211  | Controls EMIFA CE5 Range D300 0000 - D3FF FFFF |
| 0184 8350         | MAR212  | Controls EMIFA CE5 Range D400 0000 - D4FF FFFF |
| 0184 8354         | MAR213  | Controls EMIFA CE5 Range D500 0000 - D5FF FFFF |
| 0184 8358         | MAR214  | Controls EMIFA CE5 Range D600 0000 - D6FF FFFF |
| 0184 835C         | MAR215  | Controls EMIFA CE5 Range D700 0000 - D7FF FFFF |
| 0184 8360         | MAR216  | Controls EMIFA CE5 Range D800 0000 - D8FF FFFF |
| 0184 8364         | MAR217  | Controls EMIFA CE5 Range D900 0000 - D9FF FFFF |
| 0184 8368         | MAR218  | Controls EMIFA CE5 Range DA00 0000 - DAFF FFFF |

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**Table 5-10 Megamodule Cache Configuration Registers (Part 4 of 4)**

| Hex Address Range        | Acronym          | Register Name                                  |
|--------------------------|------------------|------------------------------------------------|
| 0184 836C                | MAR219           | Controls EMIFA CE5 Range DB00 0000 - DBFF FFFF |
| 0184 8370                | MAR220           | Controls EMIFA CE5 Range DC00 0000 - DCFF FFFF |
| 0184 8374                | MAR221           | Controls EMIFA CE5 Range DD00 0000 - DDFF FFFF |
| 0184 8378                | MAR222           | Controls EMIFA CE5 Range DE00 0000 - DEFF FFFF |
| 0184 837C                | MAR223           | Controls EMIFA CE5 Range DF00 0000 - DFFF FFFF |
| 0184 8380                | MAR224           | Controls DDR2 CE0 Range E000 0000 - E0FF FFFF  |
| 0184 8384                | MAR225           | Controls DDR2 CE0 Range E100 0000 - E1FF FFFF  |
| 0184 8388                | MAR226           | Controls DDR2 CE0 Range E200 0000 - E2FF FFFF  |
| 0184 838C                | MAR227           | Controls DDR2 CE0 Range E300 0000 - E3FF FFFF  |
| 0184 8390                | MAR228           | Controls DDR2 CE0 Range E400 0000 - E4FF FFFF  |
| 0184 8394                | MAR229           | Controls DDR2 CE0 Range E500 0000 - E5FF FFFF  |
| 0184 8398                | MAR230           | Controls DDR2 CE0 Range E600 0000 - E6FF FFFF  |
| 0184 839C                | MAR231           | Controls DDR2 CE0 Range E700 0000 - E7FF FFFF  |
| 0184 83A0                | MAR232           | Controls DDR2 CE0 Range E800 0000 - E8FF FFFF  |
| 0184 83A4                | MAR233           | Controls DDR2 CE0 Range E900 0000 - E9FF FFFF  |
| 0184 83A8                | MAR234           | Controls DDR2 CE0 Range EA00 0000 - EAFF FFFF  |
| 0184 83AC                | MAR235           | Controls DDR2 CE0 Range EB00 0000 - EBFF FFFF  |
| 0184 83B0                | MAR236           | Controls DDR2 CE0 Range EC00 0000 - ECFF FFFF  |
| 0184 83B4                | MAR237           | Controls DDR2 CE0 Range ED00 0000 - EDFF FFFF  |
| 0184 83B8                | MAR238           | Controls DDR2 CE0 Range EE00 0000 - EEFF FFFF  |
| 0184 83BC                | MAR239           | Controls DDR2 CE0 Range EF00 0000 - EFFF FFFF  |
| 0184 83C0 - 0184 83FC    | MAR240 to MAR255 | Reserved                                       |
| <b>End of Table 5-10</b> |                  |                                                |

**Table 5-11 Megamodule Error Detection Correct Registers**

| Hex Address Range        | Acronym   | Register Name                                                    |
|--------------------------|-----------|------------------------------------------------------------------|
| 0184 6000                | -         | Reserved                                                         |
| 0184 6004                | L2EDSTAT  | L2 Error Detection Status Register                               |
| 0184 6008                | L2EDCMD   | L2 Error Detection Command Register                              |
| 0184 600C                | L2EDADDR  | L2 Error Detection Address Register                              |
| 0184 6010                | L2EDEN0   | L2 Error Detection Enable Map 0 Register                         |
| 0184 6014                | L2EDEN1   | L2 Error Detection Enable Map 1 Register                         |
| 0184 6018                | L2EDCPEC  | L2 Error Detection — Correctable Parity Error Count Register     |
| 0184 601C                | L2EDNPEC  | L2 Error Detection — Non-Correctable Parity Error Count Register |
| 0184 6020 - 0184 6400    | -         | Reserved                                                         |
| 0184 6404                | L1PEDSTAT | L1P Error Detection Status Register                              |
| 0184 6408                | L1PEDCMD  | L1P Error Detection Command Register                             |
| 0184 640C                | L1PEDADDR | L1P Error Detection Address Register                             |
| <b>End of Table 5-11</b> |           |                                                                  |

**Table 5-12 Megamodule L1/L2 Memory Protection Registers (Part 1 of 3)**

| Hex Address Range                    | Acronym    | Register Name                                   |
|--------------------------------------|------------|-------------------------------------------------|
| 0184 A000                            | L2MPFAR    | L2 memory protection fault address register     |
| 0184 A004                            | L2MPFSR    | L2 memory protection fault status register      |
| 0184 A008                            | L2MPFCR    | L2 memory protection fault command register     |
| 0184 A00C - 0184 A0FF                | -          | Reserved                                        |
| 0184 A100                            | L2MPLK0    | L2 memory protection lock key bits [31:0]       |
| 0184 A104                            | L2MPLK1    | L2 memory protection lock key bits [63:32]      |
| 0184 A108                            | L2MPLK2    | L2 memory protection lock key bits [95:64]      |
| 0184 A10C                            | L2MPLK3    | L2 memory protection lock key bits [127:96]     |
| 0184 A110                            | L2MPLKCMD  | L2 memory protection lock key command register  |
| 0184 A114                            | L2MPLKSTAT | L2 memory protection lock key status register   |
| 0184 A118 - 0184 A1FF                | -          | Reserved                                        |
| 0184 A200                            | L2MPPA0    | L2 memory protection page attribute register 0  |
| 0184 A204                            | L2MPPA1    | L2 memory protection page attribute register 1  |
| 0184 A208                            | L2MPPA2    | L2 memory protection page attribute register 2  |
| 0184 A20C                            | L2MPPA3    | L2 memory protection page attribute register 3  |
| 0184 A210                            | L2MPPA4    | L2 memory protection page attribute register 4  |
| 0184 A214                            | L2MPPA5    | L2 memory protection page attribute register 5  |
| 0184 A218                            | L2MPPA6    | L2 memory protection page attribute register 6  |
| 0184 A21C                            | L2MPPA7    | L2 memory protection page attribute register 7  |
| 0184 A220                            | L2MPPA8    | L2 memory protection page attribute register 8  |
| 0184 A224                            | L2MPPA9    | L2 memory protection page attribute register 9  |
| 0184 A228                            | L2MPPA10   | L2 memory protection page attribute register 10 |
| 0184 A22C                            | L2MPPA11   | L2 memory protection page attribute register 11 |
| 0184 A230                            | L2MPPA12   | L2 memory protection page attribute register 12 |
| 0184 A234                            | L2MPPA13   | L2 memory protection page attribute register 13 |
| 0184 A238                            | L2MPPA14   | L2 memory protection page attribute register 14 |
| 0184 A23C                            | L2MPPA15   | L2 memory protection page attribute register 15 |
| 0184 A240                            | L2MPPA16   | L2 memory protection page attribute register 16 |
| 0184 A244                            | L2MPPA17   | L2 memory protection page attribute register 17 |
| 0184 A248                            | L2MPPA18   | L2 memory protection page attribute register 18 |
| 0184 A24C                            | L2MPPA19   | L2 memory protection page attribute register 19 |
| 0184 A250                            | L2MPPA20   | L2 memory protection page attribute register 20 |
| 0184 A254                            | L2MPPA21   | L2 memory protection page attribute register 21 |
| 0184 A258                            | L2MPPA22   | L2 memory protection page attribute register 22 |
| 0184 A25C                            | L2MPPA23   | L2 memory protection page attribute register 23 |
| 0184 A260                            | L2MPPA24   | L2 memory protection page attribute register 24 |
| 0184 A264                            | L2MPPA25   | L2 memory protection page attribute register 25 |
| 0184 A268                            | L2MPPA26   | L2 memory protection page attribute register 26 |
| 0184 A26C                            | L2MPPA27   | L2 memory protection page attribute register 27 |
| 0184 A270                            | L2MPPA28   | L2 memory protection page attribute register 28 |
| 0184 A274                            | L2MPPA29   | L2 memory protection page attribute register 29 |
| 0184 A278                            | L2MPPA30   | L2 memory protection page attribute register 30 |
| 0184 A27C                            | L2MPPA31   | L2 memory protection page attribute register 31 |
| 0184 A280 - 0184 A2FC <sup>(1)</sup> | -          | Reserved                                        |

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**Table 5-12 Megamodule L1/L2 Memory Protection Registers (Part 2 of 3)**

| Hex Address Range                    | Acronym     | Register Name                                             |
|--------------------------------------|-------------|-----------------------------------------------------------|
| 0184 0300 - 0184 A3FF                | -           | Reserved                                                  |
| 0184 A400                            | L1PMPFAR    | L1 program (L1P) memory protection fault address register |
| 0184 A404                            | L1PMPFSR    | L1P memory protection fault status register               |
| 0184 A408                            | L1PMPFCR    | L1P memory protection fault command register              |
| 0184 A40C - 0184 A4FF                | -           | Reserved                                                  |
| 0184 A500                            | L1PMPLK0    | L1P memory protection lock key bits [31:0]                |
| 0184 A504                            | L1PMPLK1    | L1P memory protection lock key bits [63:32]               |
| 0184 A508                            | L1PMPLK2    | L1P memory protection lock key bits [95:64]               |
| 0184 A50C                            | L1PMPLK3    | L1P memory protection lock key bits [127:96]              |
| 0184 A510                            | L1PMPLKCMD  | L1P memory protection lock key command register           |
| 0184 A514                            | L1PMPLKSTAT | L1P memory protection lock key status register            |
| 0184 A518 - 0184 A5FF                | -           | Reserved                                                  |
| 0184 A600 - 0184 A63C <sup>(2)</sup> | -           | Reserved                                                  |
| 0184 A640                            | L1PMPPA16   | L1P memory protection page attribute register 16          |
| 0184 A644                            | L1PMPPA17   | L1P memory protection page attribute register 17          |
| 0184 A648                            | L1PMPPA18   | L1P memory protection page attribute register 18          |
| 0184 A64C                            | L1PMPPA19   | L1P memory protection page attribute register 19          |
| 0184 A650                            | L1PMPPA20   | L1P memory protection page attribute register 20          |
| 0184 A654                            | L1PMPPA21   | L1P memory protection page attribute register 21          |
| 0184 A658                            | L1PMPPA22   | L1P memory protection page attribute register 22          |
| 0184 A65C                            | L1PMPPA23   | L1P memory protection page attribute register 23          |
| 0184 A660                            | L1PMPPA24   | L1P memory protection page attribute register 24          |
| 0184 A664                            | L1PMPPA25   | L1P memory protection page attribute register 25          |
| 0184 A668                            | L1PMPPA26   | L1P memory protection page attribute register 26          |
| 0184 A66C                            | L1PMPPA27   | L1P memory protection page attribute register 27          |
| 0184 A670                            | L1PMPPA28   | L1P memory protection page attribute register 28          |
| 0184 A674                            | L1PMPPA29   | L1P memory protection page attribute register 29          |
| 0184 A678                            | L1PMPPA30   | L1P memory protection page attribute register 30          |
| 0184 A67C                            | L1PMPPA31   | L1P memory protection page attribute register 31          |
| 0184 A680 - 0184 ABFF                | -           | Reserved                                                  |
| 0184 AC00                            | L1DMPFAR    | L1 data (L1D) memory protection fault address register    |
| 0184 AC04                            | L1DMPFSR    | L1D memory protection fault status register               |
| 0184 AC08                            | L1DMPFCR    | L1D memory protection fault command register              |
| 0184 AC0C - 0184 ACFF                | -           | Reserved                                                  |
| 0184 AD00                            | L1DMPLK0    | L1D memory protection lock key bits [31:0]                |
| 0184 AD04                            | L1DMPLK1    | L1D memory protection lock key bits [63:32]               |
| 0184 AD08                            | L1DMPLK2    | L1D memory protection lock key bits [95:64]               |
| 0184 AD0C                            | L1DMPLK3    | L1D memory protection lock key bits [127:96]              |
| 0184 AD10                            | L1DMPLKCMD  | L1D memory protection lock key command register           |
| 0184 AD14                            | L1DMPLKSTAT | L1D memory protection lock key status register            |
| 0184 AD18 - 0184 ADFF                | -           | Reserved                                                  |
| 0184 AE00 - 0184 AE3C <sup>(3)</sup> | -           | Reserved                                                  |
| 0184 AE40                            | L1DMPPA16   | L1D memory protection page attribute register 16          |
| 0184 AE44                            | L1DMPPA17   | L1D memory protection page attribute register 17          |

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**Table 5-12 Megamodule L1/L2 Memory Protection Registers (Part 3 of 3)**

| Hex Address Range     | Acronym   | Register Name                                    |
|-----------------------|-----------|--------------------------------------------------|
| 0184 AE48             | L1DMPPA18 | L1D memory protection page attribute register 18 |
| 0184 AE4C             | L1DMPPA19 | L1D memory protection page attribute register 19 |
| 0184 AE50             | L1DMPPA20 | L1D memory protection page attribute register 20 |
| 0184 AE54             | L1DMPPA21 | L1D memory protection page attribute register 21 |
| 0184 AE58             | L1DMPPA22 | L1D memory protection page attribute register 22 |
| 0184 AE5C             | L1DMPPA23 | L1D memory protection page attribute register 23 |
| 0184 AE60             | L1DMPPA24 | L1D memory protection page attribute register 24 |
| 0184 AE64             | L1DMPPA25 | L1D memory protection page attribute register 25 |
| 0184 AE68             | L1DMPPA26 | L1D memory protection page attribute register 26 |
| 0184 AE6C             | L1DMPPA27 | L1D memory protection page attribute register 27 |
| 0184 AE70             | L1DMPPA28 | L1D memory protection page attribute register 28 |
| 0184 AE74             | L1DMPPA29 | L1D memory protection page attribute register 29 |
| 0184 AE78             | L1DMPPA30 | L1D memory protection page attribute register 30 |
| 0184 AE7C             | L1DMPPA31 | L1D memory protection page attribute register 31 |
| 0184 AE80 - 0185 FFFF | -         | Reserved                                         |

**End of Table 5-12**

- 1 These addresses correspond to the L2 memory protection page attribute registers 32-63 (L2MPPA32 - L2MPPA63) of the C64x+ Megamodule. These registers are not supported for the C6457 device.
- 2 These addresses correspond to the L1P memory protection page attribute registers 0-15 (L1PMPPA0 - L1PMPPA15) of the C64x+ Megamodule. These registers are not supported for the C6457 device.
- 3 These addresses correspond to the L1D memory protection page attribute registers 0-15 (L1DMPPA0 - L1DMPPA15) of the C64x+ Megamodule. These registers are not supported for the C6457 device.

**Table 5-13 CPU Megamodule Bandwidth Management Registers**

| Hex Address Range     | Acronym     | Register Name                                   |
|-----------------------|-------------|-------------------------------------------------|
| 0182 0200             | EMCCPUARBE  | EMC CPU Arbitration Control Register            |
| 0182 0204             | EMCIDMAARBE | EMC IDMA Arbitration Control Register           |
| 0182 0208             | EMCSDMAARBE | EMC Slave DMA Arbitration Control Register      |
| 0182 020C             | EMCMDMAARBE | EMC Master DMA Arbitration Control Register     |
| 0182 0210 - 0182 02FF | -           | Reserved                                        |
| 0184 1000             | L2DCPUARBU  | L2D CPU Arbitration Control Register            |
| 0184 1004             | L2DIDMAARBU | L2D IDMA Arbitration Control Register           |
| 0184 1008             | L2DSDMAARBU | L2D Slave DMA Arbitration Control Register      |
| 0184 100C             | L2DUCARBU   | L2D User Coherence Arbitration Control Register |
| 0184 1010 - 0184 103F | -           | Reserved                                        |
| 0184 1040             | L1DCPUARBD  | L1D CPU Arbitration Control Register            |
| 0184 1044             | L1DIDMAARBD | L1D IDMA Arbitration Control Register           |
| 0184 1048             | L1DSDMAARBD | L1D Slave DMA Arbitration Control Register      |
| 0184 104C             | L1DUCARBD   | L1D User Coherence Arbitration Control Register |

**End of Table 5-13**

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## 6 Device Operating Conditions

Based on JESD22-C101C (Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components), the TMS320C6457 device's charged-device model (CDM) sensitivity classification is Class II (200 V to < 500 V). Specifically, DDR memory interface and SerDes pins conform to  $\pm 200$ -V level. All other pins conform to  $\pm 500$  V.

### 6.1 Absolute Maximum Ratings

**Table 6-1 Absolute Maximum Ratings<sup>(1)</sup>**  
**Over Operating Case Temperature Range (Unless Otherwise Noted)**

|                                                    |                                                             |                                      |                                                        |
|----------------------------------------------------|-------------------------------------------------------------|--------------------------------------|--------------------------------------------------------|
| Supply voltage range <sup>(2)</sup> :              | CV <sub>DD</sub>                                            |                                      | -0.3 V to 1.35 V                                       |
|                                                    | DV <sub>DD18</sub>                                          |                                      | -0.3 V to 2.45 V                                       |
|                                                    | DV <sub>DD33</sub>                                          |                                      | -0.3 V to 3.60V                                        |
|                                                    | V <sub>REFSSTL</sub>                                        |                                      | 0.49 × DV <sub>DD18</sub> to 0.51 × DV <sub>DD18</sub> |
|                                                    | V <sub>DD11</sub> , V <sub>DDD11</sub> , V <sub>DDT11</sub> |                                      | -0.3 V to 1.35 V                                       |
|                                                    | V <sub>DDR18</sub>                                          |                                      | -0.3 V to 2.45 V                                       |
|                                                    | AV <sub>DD118</sub> , AV <sub>DD218</sub>                   |                                      | -0.3 V to 2.45 V                                       |
|                                                    | V <sub>SS</sub> Ground                                      |                                      | 0 V                                                    |
|                                                    | Input voltage (V <sub>I</sub> ) range:                      | LVCMOS (1.8V)                        |                                                        |
| LVCMOS (3.3V)                                      |                                                             | -0.3 V to DV <sub>DD33</sub> + 0.3 V |                                                        |
| DDR2                                               |                                                             | -0.3 V to 2.45 V                     |                                                        |
| I <sup>2</sup> C                                   |                                                             | -0.3 V to 2.45 V                     |                                                        |
| LVDS                                               |                                                             | -0.3 V to D <sub>VDD18</sub> + 0.3 V |                                                        |
| LJCB                                               |                                                             | -0.3 V to 1.35 V                     |                                                        |
| SerDes                                             |                                                             | -0.3 V to D <sub>VDD11</sub> + 0.3 V |                                                        |
| Output voltage (V <sub>O</sub> ) range:            | LVCMOS (1.8V)                                               |                                      | -0.3 V to DV <sub>DD18</sub> + 0.3 V                   |
|                                                    | LVCMOS (3.3V)                                               |                                      | -0.3 V to DV <sub>DD33</sub> + 0.3 V                   |
|                                                    | DDR2                                                        |                                      | -0.3 V to 2.45 V                                       |
|                                                    | I <sup>2</sup> C                                            |                                      | -0.3 V to 2.45 V                                       |
|                                                    | SerDes                                                      |                                      | -0.3 V to DV <sub>DD11</sub> + 0.3 V                   |
| Operating case temperature range, T <sub>C</sub> : | Commercial                                                  | 850 MHz CPU                          | 0°C to 100°C                                           |
|                                                    |                                                             | 1-GHz CPU                            | 0°C to 100°C                                           |
|                                                    |                                                             | 1.2-GHz CPU                          | 0°C to 95°C                                            |
|                                                    | Extended                                                    | 1-GHz CPU                            | -40°C to 100°C                                         |
|                                                    |                                                             | 1.2-GHz CPU                          | -40°C to 95°C                                          |
| Overshoot/undershoot <sup>(3)</sup>                | LVCMOS (1.8V)                                               |                                      | 20% Overshoot/Undershoot for 20% of Signal Duty Cycle  |
|                                                    | LVCMOS (3.3V)                                               |                                      |                                                        |
|                                                    | DDR2                                                        |                                      |                                                        |
|                                                    | I <sup>2</sup> C                                            |                                      |                                                        |
| Storage temperature range, T <sub>stg</sub> :      |                                                             |                                      | -65°C to 150°C                                         |

**End of Table 6-1**

1 Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2 All voltage values are with respect to V<sub>SS</sub>.

3 Overshoot/Undershoot percentage relative to I/O operating values - for example the maximum overshoot value for 1.8-V LVCMOS signals is DV<sub>DD18</sub> + 0.20 × DV<sub>DD18</sub> and maximum undershoot value would be V<sub>SS</sub> - 0.20 × DV<sub>DD18</sub>

## 6.2 Recommended Operating Conditions

**Table 6-2 Recommended Operating Conditions** <sup>(1) (2)</sup>

|                      |                                      |                  | Min                       | Nom                          | Max                       | Unit                       |   |
|----------------------|--------------------------------------|------------------|---------------------------|------------------------------|---------------------------|----------------------------|---|
| CV <sub>DD</sub>     | Supply core voltage                  | 850-MHz CPU      | 1.067                     | 1.1                          | 1.133                     | V                          |   |
|                      |                                      | 1-GHz CPU        | 1.067                     | 1.1                          | 1.133                     |                            |   |
|                      |                                      | 1.2-GHz CPU      | 1.164                     | 1.2                          | 1.236                     |                            |   |
| DV <sub>DD18</sub>   | 1.8-V supply I/O voltage             |                  | 1.71                      | 1.8                          | 1.89                      | V                          |   |
| DV <sub>DD33</sub>   | 3.3-V supply I/O voltage             |                  | 3.135                     | 3.3                          | 3.465                     | V                          |   |
| V <sub>REFSSTL</sub> | DDR2 reference voltage               |                  | 0.49 × DV <sub>DD18</sub> | 0.5 × DV <sub>DD18</sub>     | 0.51 × DV <sub>DD18</sub> | V                          |   |
| V <sub>DDR18</sub>   | SRIO/SGMII SerDes regulator supply   |                  | 1.71                      | 1.8                          | 1.89                      | V                          |   |
| V <sub>DDA11</sub>   | SRIO/SGMII SerDes analog supply      |                  | 1.045                     | 1.1                          | 1.155                     | V                          |   |
| V <sub>DDD11</sub>   | SRIO/SGMII SerDes digital supply     |                  | 1.045                     | 1.1                          | 1.155                     | V                          |   |
| V <sub>DDT11</sub>   | SRIO/SGMII SerDes termination supply |                  | 1.045                     | 1.1                          | 1.155                     | V                          |   |
| PLL <sub>V1</sub>    | PLL1 analog supply                   |                  | 1.71                      | 1.8                          | 1.89                      | V                          |   |
| PLL <sub>V2</sub>    | PLL2 analog supply                   |                  | 1.71                      | 1.8                          | 1.89                      | V                          |   |
| V <sub>SS</sub>      | Ground                               |                  | 0                         | 0                            | 0                         | V                          |   |
| V <sub>IH</sub>      | High-level input voltage             | LVCMOS (1.8 V)   |                           | 0.65 × DV <sub>DD18</sub>    |                           | V                          |   |
|                      |                                      | LVCMOS (3.3 V)   |                           | 2.0                          |                           | V                          |   |
|                      |                                      | I <sup>2</sup> C |                           | 0.7 × DV <sub>DD18</sub>     |                           | V                          |   |
|                      |                                      | DDR2 EMIF        |                           | V <sub>REFSSTL</sub> + 0.125 |                           | DV <sub>DD18</sub> + 0.3   | V |
| V <sub>IL</sub>      | Low-level input voltage              | LVCMOS (1.8 V)   |                           | 0.35 × DV <sub>DD18</sub>    |                           | V                          |   |
|                      |                                      | LVCMOS (3.3 V)   |                           | 0.8                          |                           | V                          |   |
|                      |                                      | DDR2 EMIF        |                           | -0.3                         |                           | V <sub>REFSSTL</sub> - 0.1 | V |
|                      |                                      | I <sup>2</sup> C |                           | 0.3 × DV <sub>DD18</sub>     |                           | V                          |   |
| T <sub>C</sub>       | Operating case temperature           | Commercial       | 850 MHz CPU               | 0                            | 100                       | °C                         |   |
|                      |                                      |                  | 1-GHz CPU                 | 0                            | 100                       |                            |   |
|                      |                                      |                  | 1.2-GHz CPU               | 0                            | 95                        |                            |   |
|                      | Extended                             | 1-GHz CPU        | -40                       | 100                          | °C                        |                            |   |
|                      |                                      | 1.2-GHz CPU      | -40                       | 95                           |                           |                            |   |

**End of Table 6-2**

1 All differential clock inputs comply with the LVDS Electrical Specification, IEEE 1596.3-1996 and all SerDes I/Os comply with the XAUI Electrical Specification, IEEE 802.3ae-2002.

2 All SerDes I/Os comply with the XAUI Electrical Specification, IEEE 802.3ae-2002.



## 6.3 Electrical Characteristics

**Table 6-3 Electrical Characteristics**  
**Over Recommended Ranges of Supply Voltage and Operating Case Temperature (Unless Otherwise Noted)**

| Parameter                                                    |                                                                                       | Test Conditions <sup>(1)</sup>                                           | Min                       | Typ  | Max  | Unit |
|--------------------------------------------------------------|---------------------------------------------------------------------------------------|--------------------------------------------------------------------------|---------------------------|------|------|------|
| V <sub>OH</sub> High-level output voltage                    | LVC MOS (1.8 V)                                                                       | I <sub>O</sub> = I <sub>OH</sub>                                         | DV <sub>DD18</sub> - 0.45 |      |      | V    |
|                                                              | LVC MOS (3.3 V)                                                                       | I <sub>O</sub> = -2 mA                                                   | 2.4                       |      |      |      |
|                                                              | DDR2                                                                                  |                                                                          | 1.4                       |      |      |      |
|                                                              | I <sup>2</sup> C                                                                      |                                                                          | 0.1 × DV <sub>DD18</sub>  |      |      |      |
| V <sub>OL</sub> Low-level output voltage                     | LVC MOS (1.8 V)                                                                       | I <sub>O</sub> = I <sub>OL</sub>                                         |                           |      | 0.45 | V    |
|                                                              | LVC MOS (3.3 V)                                                                       | I <sub>O</sub> = 2 mA                                                    |                           |      | 0.4  |      |
|                                                              | DDR2                                                                                  |                                                                          |                           |      | 0.4  |      |
|                                                              | I <sup>2</sup> C                                                                      | I <sub>O</sub> = 3 mA, pulled up to 1.8 V                                |                           |      | 0.4  |      |
| I <sub>I</sub> <sup>(2)</sup> Input current [DC]             | LVC MOS (1.8 V)                                                                       | No IPD/IPU                                                               | -5                        |      | 5    | μA   |
|                                                              |                                                                                       | Internal pullup                                                          | 50                        | 100  | 170  |      |
|                                                              |                                                                                       | Internal pulldown                                                        | -170                      | -100 | -50  |      |
|                                                              | LVC MOS (3.3 V)                                                                       | No IPD/IPU                                                               | -1                        |      | 1    | μA   |
|                                                              |                                                                                       | Internal pullup                                                          | 70                        | 150  | 270  |      |
|                                                              |                                                                                       | Internal pulldown                                                        | -270                      | -150 | -70  |      |
|                                                              | I <sup>2</sup> C                                                                      | 0.1 × DV <sub>DD18</sub> V < V <sub>I</sub> < 0.9 × DV <sub>DD18</sub> V | -20                       |      | 20   | μA   |
| I <sub>OH</sub> High-level output current [DC]               | EMU[18:00], GPIO[15:0], TIMO[1:0]                                                     |                                                                          |                           |      | -8   | mA   |
|                                                              | SYCLKOUT, TDO, CLKR0, CLKX0, DX0, FSR0, FSX0, CLKR1, CLKX1, DX1, FSR1, FSX1, AECLKOUT |                                                                          |                           |      | -6   |      |
|                                                              | RESETSTAT, MDIO, MDCLK                                                                |                                                                          |                           |      | -4   |      |
|                                                              | DDR2                                                                                  |                                                                          |                           |      | 4    |      |
|                                                              | LVC MOS (3.3 V), except AECLKOUT                                                      |                                                                          |                           |      | -4   |      |
| I <sub>OL</sub> Low-level output current [DC]                | EMU[18:00], GPIO[15:0], TIM[1:0]                                                      |                                                                          |                           |      | 8    | mA   |
|                                                              | SYCLKOUT, TDO, CLKR0, CLKX0, DX0, FSR0, FSX0, CLKR1, CLKX1, DX1, FSR1, FSX1, AECLKOUT |                                                                          |                           |      | 6    |      |
|                                                              | RESETSTAT, MDIO, MDCLK                                                                |                                                                          |                           |      | 4    |      |
|                                                              | DDR2                                                                                  |                                                                          |                           |      | -4   |      |
|                                                              | LVC MOS (3.3 V), except AECLKOUT                                                      |                                                                          |                           |      | 4    |      |
| I <sub>OZ</sub> <sup>(3)</sup> Off-state output current [DC] | LVC MOS (1.8 V)                                                                       |                                                                          | -20                       |      | 20   | μA   |
|                                                              | LVC MOS (3.3 V)                                                                       |                                                                          | -20                       |      | 20   |      |

**End of Table 6-3**

1 For test conditions shown as MIN, MAX, or TYP, use the appropriate value specified in the recommended operating conditions table.

2 I<sub>I</sub> applies to input-only pins and bi-directional pins. For input-only pins, I<sub>I</sub> indicates the input leakage current. For bi-directional pins, I<sub>I</sub> includes input leakage current and off-state (Hi-Z) output leakage current.

3 I<sub>OZ</sub> applies to output-only pins, indicating off-state (Hi-Z) output leakage current.

**Table 6-4 Power Supply to Peripheral I/O Mapping<sup>(1) (2)</sup>**  
**Over Recommended Ranges of Supply Voltage and Operating Case Temperature (Unless Otherwise Noted)<sup>2</sup>**

| Power Supply                                       | I/O Buffer Type    | Associated Peripheral                            |
|----------------------------------------------------|--------------------|--------------------------------------------------|
| CV <sub>DD</sub> Supply core voltage               | LJCB               | CORECLK(P N) PLL input buffers                   |
|                                                    |                    | DDRREFCLK(N P) PLL input buffers                 |
|                                                    |                    | RIOSGMII CLK(N P) SerDes PLL input buffers       |
| DV <sub>DD18</sub> 1.8-V supply I/O voltage        | LVCMOS (1.8 V)     | ALTCORECLK PLL input buffer                      |
|                                                    |                    | ALTDDRCLK PLL input buffer                       |
|                                                    |                    | POR/RESET input buffers                          |
|                                                    |                    | All GPIO peripheral I/O buffer                   |
|                                                    |                    | All McBSP0/McBSP1 peripheral I/O buffer          |
|                                                    |                    | All MDIO peripheral I/O buffer                   |
|                                                    |                    | All Timer0/Timer1 peripheral I/O buffer          |
|                                                    | DDR2 (1.8V)        | All DDR2 memory controller peripheral I/O buffer |
|                                                    | Open-drain (1.8 V) | All I <sup>2</sup> C peripheral I/O buffer       |
| DV <sub>DD33</sub> 3.3-V supply I/O voltage        | LVCMOS (3.3 V)     | All EMIFA peripheral I/O buffer                  |
|                                                    |                    | ALL HPI peripheral I/O buffer                    |
|                                                    |                    | ALL UTOPIA peripheral I/O buffer                 |
| V <sub>DDA11</sub> SRIO/SGMII SerDes analog supply | CML                | SRIO/SGMII SerDes CML I/O buffer                 |
| <b>End of Table 6-4</b>                            |                    |                                                  |

- 1 Please note that this table does not attempt to describe all functions of all power supply terminals but only those whose purpose it is to power peripheral I/O buffers and clock input buffers.
- 2 Please see the *TMS320TCL6484 and TMS320C6457 DSPs Hardware Design Guide* ([SPRAAV7](#)) for more information about individual peripheral I/O.

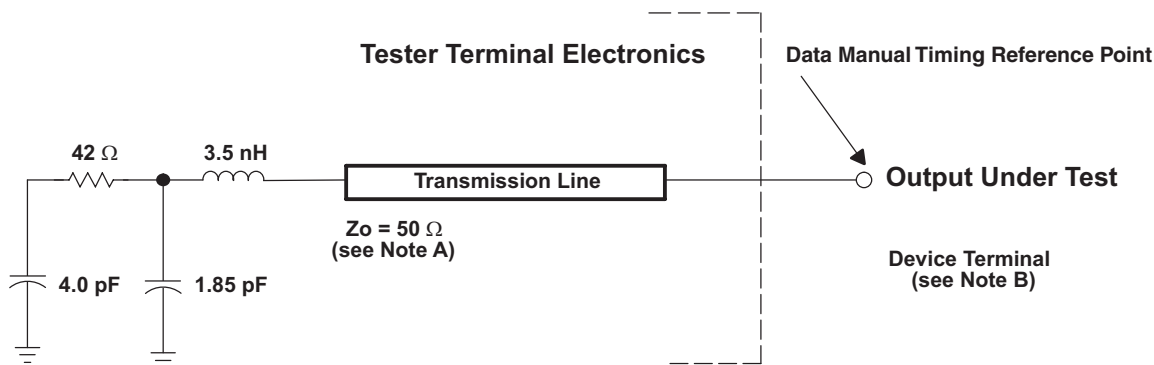
## 7 C64x+ Peripheral Information and Electrical Specifications

This chapter describes the various peripherals on the TMS320C6457 DSP. Peripheral specific information, timing diagrams, electrical specifications and register memory maps are described in this chapter.

### 7.1 Parameter Information

This section describes the conditions used to capture the electrical data seen in this chapter.

**Figure 7-1 Test Load Circuit for AC Timing Measurements**



(A) The data manual provides timing at the device terminal. For output timing analysis, the tester terminal electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns) from the data sheet timings.

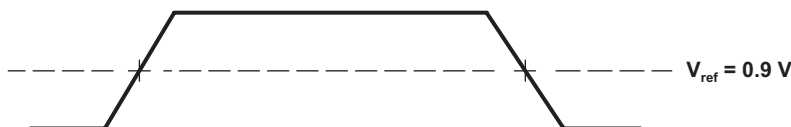
(B) Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device terminal.

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

#### 7.1.1 1.8-V Signal Transition Levels

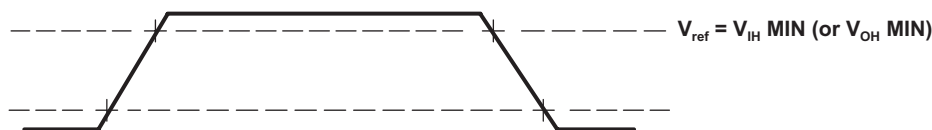
All input and output timing parameters are referenced to 0.9 V for both 0 and 1 logic levels.

**Figure 7-2 Input and Output Voltage Reference Levels for 1.8-V AC Timing Measurements**



All rise and fall transition timing parameters are reference to  $V_{IL}$  MAX and  $V_{IH}$  MIN for input clocks.

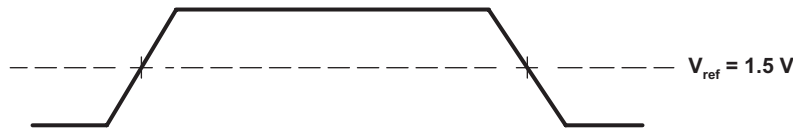
**Figure 7-3 Rise and Fall Transition Time Voltage Reference Levels**



### 7.1.2 3.3-V Signal Transition Levels

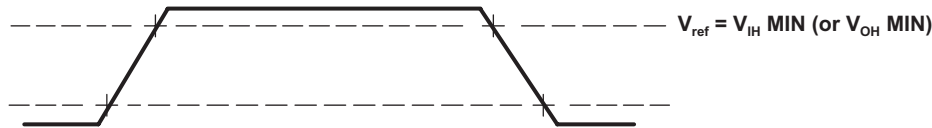
All input and output timing parameters are referenced to 1.5 V for both 0 and 1 logic levels.

**Figure 7-4 Input and Output Voltage Reference Levels for 3.3-V AC Timing Measurements**



All rise and fall transition timing parameters are referenced to  $V_{IL\ MAX}$  and  $V_{IH\ MIN}$  for input clocks,  $V_{OL\ MAX}$  and  $V_{OH\ MIN}$  for output clocks.

**Figure 7-5 Rise and Fall Transition Time Voltage Reference Levels**



### 7.1.3 3.3-V Signal Transition Rates

All timings are tested with an input edge rate of 4 volts per nanosecond (4 V/ns).

### 7.1.4 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data sheet do not include delays by board routings. As a good board design practice, such delays must always be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends using the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number [SPRA839](#)). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

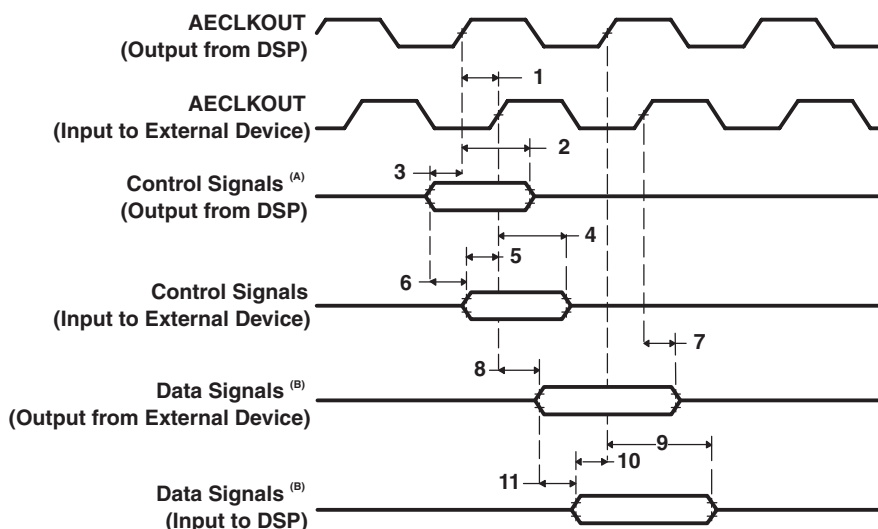
For inputs, timing is most impacted by the round-trip propagation delay from the DSP to the external device and from the external device to the DSP. This round-trip delay tends to negatively impact the input setup time margin, but also tends to improve the input hold time margins (see [Table 7-1](#) and [Figure 7-6](#)).

**Table 7-1 Board-Level Timing Example**  
 (see [Figure 7-6](#))

| No.              | Description                            |
|------------------|----------------------------------------|
| 1                | Clock route delay                      |
| 2                | Minimum DSP hold time                  |
| 3                | Minimum DSP setup time                 |
| 4                | External device hold time requirement  |
| 5                | External device setup time requirement |
| 6                | Control signal route delay             |
| 7                | External device hold time              |
| 8                | External device access time            |
| 9                | DSP hold time requirement              |
| 10               | DSP setup time requirement             |
| 11               | Data route delay                       |
| End of Table 7-1 |                                        |

Figure 7-6 shows a general transfer between the DSP and an external device. The figure also shows board route delays and how they are perceived by the DSP and the external device

Figure 7-6 Board-Level Input/Output Timings



(A) Control signals include data for writes.

(B) Data signals are generated during reads from an external device.

## 7.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals **must** transition between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.

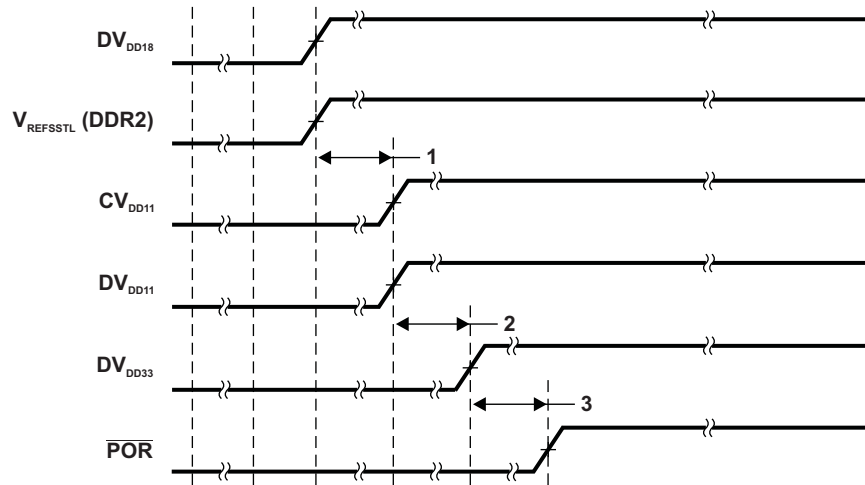
## 7.3 Power Supplies

The following sections describe the proper power-supply sequencing and timing needed to properly power on the C6457 DSP. This section also describes proper power-supply decoupling methods.

### 7.3.1 Power-Supply Sequencing

TI recommends the power-supply sequence shown in Figure 7-7 and described in Table 7-2. The figure shows that the 1.8-V I/O supply should be ramped first. This is followed by the scaled core supply and the fixed 1.1-V supplies which must ramp within 5 ms of each other. The 3.3-V I/O supply should ramp up last. Some TI power-supply devices include features that facilitate power sequencing; for example, Auto-Track or Slow-Start/Enable features. For more information, visit [www.ti.com/dsppower](http://www.ti.com/dsppower). See the *TMS320TCI6468 and TMS329C6457 DSPs Hardware Design Guide (SPRAAV7)* for further details on proper power-supply sequencing.

**Figure 7-7 Power-Supply Sequence**



**Table 7-2 Timing Requirements for Power-Supply Sequence**

| No. |                                                                                                                                            | Min | Max | Unit    |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|---------|
| 1   | $t_{su}(DV_{DD18}-DV_{DD11})$ Setup Time, $DV_{DD18}$ and $V_{REFSSTL}$ supplies stable before $DV_{DD11}$ and $CV_{DD11}$ supplies stable | 0.5 | 200 | ms      |
| 2   | $t_{su}(DV_{DD11}-DV_{DD33})$ Setup Time, $DV_{DD11}$ and $CV_{DD11}$ supplies stable before $DV_{DD33}$ supply stable                     | 0.5 | 200 | ms      |
| 3   | $t_h(DV_{DD33}-POR)$ Hold time, $POR$ low after $DV_{DD33}$ supplies stable                                                                | 100 |     | $\mu s$ |

End of Table 7-2

### 7.3.2 Power-Supply Decoupling

In order to properly decouple the supply planes from system noise, place as many capacitors (caps) as possible close to the DSP. These caps need to be close to the DSP, no more than 1.25 cm maximum distance to be effective. Physically smaller caps are better, such as 0402, but need to be evaluated from a yield/manufacturing point-of-view. Parasitic inductance limits the effectiveness of the decoupling capacitors, therefore physically smaller capacitors should be used while maintaining the largest available capacitance value. As with the selection of any component, verification of capacitor availability over the product's production lifetime should be considered.

### 7.3.3 Power-Down Operation

One of the power goals for the C6457 is to reduce power dissipation due to unused peripherals. There are different ways to power down peripherals on the device.

After device reset, all peripherals on the C6457 device are in a disabled state and must be enabled by software before being used. It is possible to enable only the peripherals needed by the application while keeping the rest disabled. Note that peripherals in a disabled state are held in reset with their clocks gated. For more information on how to enable peripherals, see Section 3.2 “Peripheral Selection After Device Reset” on page 60

Peripherals used for booting, like I<sup>2</sup>C and HPI, are automatically enabled after device reset. It is possible to disable peripherals used for booting after the boot process is complete. This, too, results in gating of the clock(s) to the powered-down peripheral. Once a peripheral is powered-down, it must remain powered down until the next device reset.

The C64x+ Megamodule also allows for software-driven power-down management for all of the C64x+ megamodule components through its Power-Down Controller (PDC). The CPU can power-down part or the entire C64x+ megamodule through the power-down controller based on its own execution thread or in response to an external stimulus from a host or global controller. More information on the power-down features of the C64x+ Megamodule can be found in the *TMS320C64x+ Megamodule Reference Guide* (literature number [SPRU871](#)).

## 7.4 Enhanced Direct Memory Access (EDMA3) Controller

The primary purpose of the EDMA3 is to service user-programmed data transfers between two memory-mapped slave endpoints on the device. The EDMA3 services software-driven paging transfers (e.g., data movement between external memory and internal memory), performs sorting or subframe extraction of various data structures, services event-driven peripherals such as a McBSP or the UTOPIA port, and offloads data transfers from the device CPU.

The EDMA3 includes the following features:

- Fully orthogonal transfer description
  - 3 transfer dimensions:
    - › Array (multiple bytes)
    - › Frame (multiple arrays)
    - › Block (multiple frames)
  - Single event can trigger transfer of array, frame, or entire block
  - Independent indexes on source and destination
- Flexible transfer definition:
  - Increment or FIFO transfer addressing modes
  - Linking mechanism allows for ping-pong buffering, circular buffering, and repetitive/continuous transfers, all with no CPU intervention
  - Chaining allows multiple transfers to execute with one event
- 256 PaRAM entries
  - Used to define transfer context for channels
  - Each PaRAM entry can be used as a DMA entry, QDMA entry, or link entry
- 64 DMA channels
  - Manually triggered (CPU writes to channel controller register), external event triggered, and chain triggered (completion of one transfer triggers another)
- 8 Quick DMA (QDMA) channels
  - Used for software-driven transfers
  - Triggered upon writing to a single PaRAM set entry
- 6 transfer controllers and 6 event queues with programmable system-level priority
- Interrupt generation for transfer completion and error conditions
- Debug visibility
  - Queue watermarking/threshold allows detection of maximum usage of event queues
  - Error and status recording to facilitate debug

Each of the transfer controllers has a direct connection to the switched central resource (SCR). Table 4-1 “[SCR Connection Matrix](#)” on page 67 lists the peripherals that can be accessed by the transfer controllers.

## 7.4.1 EDMA3 Device-Specific Information

The EDMA supports two addressing modes: constant addressing and increment addressing mode. Constant addressing mode is applicable to a very limited set of use cases; for most applications increment mode can be used. On the C6457 DSP, the EDMA can use constant addressing mode only with the Enhanced Viterbi-Decoder Coprocessor (VCP2) and the Enhanced Turbo Decoder Coprocessor (TCP2). Constant addressing mode is not supported by any other peripheral or internal memory in the C6457 DSP. Note that increment mode is supported by all C6457 peripherals, including VCP2 and TCP2. For more information on these two addressing modes, see the *TMS320C6457 DSP Enhanced DMA (EDMA3) Controller User's Guide* (literature number [SPRUGK6](#)).

A DSP interrupt must be generated at the end of an HPI boot operation to begin execution of the loaded application. Because the DSP interrupt generated by the HPI is mapped to the EDMA event DSP\_EVT (DMA channel 0), it will get recorded in bit 0 of the EDMA Event Register (ER). This event must be cleared by software before triggering transfers on DMA channel 0. The EDMA3 on the C6457 DSP supports active memory protection, but it does not support proxied memory protection.

## 7.4.2 EDMA3 Channel Synchronization Events

The EDMA3 supports up to 64 DMA channels that can be used to service system peripherals and to move data between system memories. DMA channels can be triggered by synchronization events generated by system peripherals. [Table 7-3](#) lists the source of the synchronization event associated with each of the DMA channels. On the C6457, the association of each synchronization event and DMA channel is fixed and cannot be reprogrammed.

For more detailed information on the EDMA3 module and how EDMA3 events are enabled, captured, processed, prioritized, linked, chained, and cleared, etc., see the *TMS320C6457 DSP Enhanced DMA (EDMA3) Controller User's Guide* (literature number [SPRUGK6](#)).

**Table 7-3 C6457 EDMA3 Channel Synchronization Events<sup>(1)</sup> (Part 1 of 2)**

| EDMA Channel     | Event Name  | Event Description                                   |
|------------------|-------------|-----------------------------------------------------|
| 0 <sup>(2)</sup> | DSP_EVT     | HPI-to-DSP event                                    |
| 1                | TEVTLO0     | Timer 0 Lower Counter Event                         |
| 2                | TEVTHI0     | Timer 0 High Counter Event                          |
| 3 - 8            | -           | None                                                |
| 9                | ETBHFULLINT | Embedded Trace Buffer (ETB) is half full            |
| 10               | ETBFULLINT  | Embedded Trace Buffer (ETB) is full                 |
| 11               | ETBACQINT   | Embedded Trace Buffer (ETB) acquisition is complete |
| 12               | XEVT0       | McBSP0 Transmit Event                               |
| 13               | REVT0       | McBSP0 Receive Event                                |
| 14               | XEVT1       | McBSP1 Transmit Event                               |
| 15               | REVT1       | McBSP1 Receive Event                                |
| 16               | TEVTLO1     | Timer 1 Lower Counter Event                         |
| 17               | TEVTHI1     | Timer 1 High Counter Event                          |
| 18               | -           | None                                                |
| 19               | INTDST0     | RapidIO Interrupt 0                                 |
| 20               | INTDST1     | RapidIO Interrupt 1                                 |
| 21               | INTDST2     | RapidIO Interrupt 2                                 |
| 22               | INTDST3     | RapidIO Interrupt 3                                 |
| 23               | INTDST4     | RapidIO Interrupt 4                                 |
| 24               | INTDST5     | RapidIO Interrupt 5                                 |
| 25               | INTDST6     | RapidIO Interrupt 6                                 |
| 26 - 27          | -           | None                                                |



**Table 7-3 C6457 EDMA3 Channel Synchronization Events<sup>(1)</sup> (Part 2 of 2)**

| EDMA Channel | Event Name | Event Description               |
|--------------|------------|---------------------------------|
| 28           | VCP2REVT   | VCP2 Receive Event              |
| 29           | VCP2XEVT   | VCP2 Transmit Event             |
| 30           | TCP2AREVT  | TCP2_A Receive Event            |
| 31           | TCP2AXEVT  | TCP2_A Transmit Event           |
| 32           | UREVT      | UTOPIA Receive Event            |
| 33           | TCP2BREVT  | TCP2_B Receive Event            |
| 34           | TCP2BXEVT  | TCP2_B Transmit Event           |
| 35 - 39      | -          | None                            |
| 40           | UXEVT      | UTOPIA Transmit Event           |
| 41 - 43      | -          | None                            |
| 44           | ICREVT     | I <sup>2</sup> C Receive Event  |
| 45           | ICXEVT     | I <sup>2</sup> C Transmit Event |
| 46 - 47      | -          | None                            |
| 48           | GPINT0     | GPIO event 0                    |
| 49           | GPINT1     | GPIO event 1                    |
| 50           | GPINT2     | GPIO event 2                    |
| 51           | GPINT3     | GPIO event 3                    |
| 52           | GPINT4     | GPIO event 4                    |
| 53           | GPINT5     | GPIO event 5                    |
| 54           | GPINT6     | GPIO event 6                    |
| 55           | GPINT7     | GPIO event 7                    |
| 56           | GPINT8     | GPIO event 8                    |
| 57           | GPINT9     | GPIO event 9                    |
| 58           | GPINT10    | GPIO event 10                   |
| 59           | GPINT11    | GPIO event 11                   |
| 60           | GPINT12    | GPIO event 12                   |
| 61           | GPINT13    | GPIO event 13                   |
| 62           | GPINT14    | GPIO event 14                   |
| 63           | GPINT15    | GPIO event 15                   |

**End of Table 7-3**

- In addition to the events shown in this table, each of the 64 channels can also be synchronized with the transfer completion or alternate transfer completion events. For more detailed information on EDMA event-transfer chaining, see the *TMS320C6457 DSP Enhanced DMA (EDMA3) Controller User's Guide* (literature number [SPRUGK6](#)).
- HPI boot is terminated using a DSP interrupt. The DSP interrupt is registered in bit 0 (channel 0) of the EDMA Event Register (ER). This event must be cleared by software before triggering transfers on DMA channel 0.

### 7.4.3 EDMA3 Peripheral Register Description(s)

**Table 7-4 EDMA3 Registers (Part 1 of 15)**

| Hex Address           | Acronym | Register Name                  |
|-----------------------|---------|--------------------------------|
| 02A0 0000             | PID     | Peripheral ID Register         |
| 02A0 0004             | CCCFG   | EDMA3CC Configuration Register |
| 02A0 0008 - 02A0 00FC | -       | Reserved                       |
| 02A0 0100             | DCHMAP0 | DMA Channel 0 Mapping Register |
| 02A0 0104             | DCHMAP1 | DMA Channel 1 Mapping Register |
| 02A0 0108             | DCHMAP2 | DMA Channel 2 Mapping Register |

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**Table 7-4 EDMA3 Registers (Part 2 of 15)**

| Hex Address | Acronym  | Register Name                   |
|-------------|----------|---------------------------------|
| 02A0 010C   | DCHMAP3  | DMA Channel 3 Mapping Register  |
| 02A0 0110   | DCHMAP4  | DMA Channel 4 Mapping Register  |
| 02A0 0114   | DCHMAP5  | DMA Channel 5 Mapping Register  |
| 02A0 0118   | DCHMAP6  | DMA Channel 6 Mapping Register  |
| 02A0 011C   | DCHMAP7  | DMA Channel 7 Mapping Register  |
| 02A0 0120   | DCHMAP8  | DMA Channel 8 Mapping Register  |
| 02A0 0124   | DCHMAP9  | DMA Channel 9 Mapping Register  |
| 02A0 0128   | DCHMAP10 | DMA Channel 10 Mapping Register |
| 02A0 012C   | DCHMAP11 | DMA Channel 11 Mapping Register |
| 02A0 0130   | DCHMAP12 | DMA Channel 12 Mapping Register |
| 02A0 0134   | DCHMAP13 | DMA Channel 13 Mapping Register |
| 02A0 0138   | DCHMAP14 | DMA Channel 14 Mapping Register |
| 02A0 013C   | DCHMAP15 | DMA Channel 15 Mapping Register |
| 02A0 0140   | DCHMAP16 | DMA Channel 16 Mapping Register |
| 02A0 0144   | DCHMAP17 | DMA Channel 17 Mapping Register |
| 02A0 0148   | DCHMAP18 | DMA Channel 18 Mapping Register |
| 02A0 014C   | DCHMAP19 | DMA Channel 19 Mapping Register |
| 02A0 0150   | DCHMAP20 | DMA Channel 20 Mapping Register |
| 02A0 0154   | DCHMAP21 | DMA Channel 21 Mapping Register |
| 02A0 0158   | DCHMAP22 | DMA Channel 22 Mapping Register |
| 02A0 015C   | DCHMAP23 | DMA Channel 23 Mapping Register |
| 02A0 0160   | DCHMAP24 | DMA Channel 24 Mapping Register |
| 02A0 0164   | DCHMAP25 | DMA Channel 25 Mapping Register |
| 02A0 0168   | DCHMAP26 | DMA Channel 26 Mapping Register |
| 02A0 016C   | DCHMAP27 | DMA Channel 27 Mapping Register |
| 02A0 0170   | DCHMAP28 | DMA Channel 28 Mapping Register |
| 02A0 0174   | DCHMAP29 | DMA Channel 29 Mapping Register |
| 02A0 0178   | DCHMAP30 | DMA Channel 30 Mapping Register |
| 02A0 017C   | DCHMAP31 | DMA Channel 31 Mapping Register |
| 02A0 0180   | DCHMAP32 | DMA Channel 32 Mapping Register |
| 02A0 0184   | DCHMAP33 | DMA Channel 33 Mapping Register |
| 02A0 0188   | DCHMAP34 | DMA Channel 34 Mapping Register |
| 02A0 018C   | DCHMAP35 | DMA Channel 35 Mapping Register |
| 02A0 0190   | DCHMAP36 | DMA Channel 36 Mapping Register |
| 02A0 0194   | DCHMAP37 | DMA Channel 37 Mapping Register |
| 02A0 0198   | DCHMAP38 | DMA Channel 38 Mapping Register |
| 02A0 019C   | DCHMAP39 | DMA Channel 39 Mapping Register |
| 02A0 01A0   | DCHMAP40 | DMA Channel 40 Mapping Register |
| 02A0 01A4   | DCHMAP41 | DMA Channel 41 Mapping Register |
| 02A0 01A8   | DCHMAP42 | DMA Channel 42 Mapping Register |
| 02A0 01AC   | DCHMAP43 | DMA Channel 43 Mapping Register |
| 02A0 01B0   | DCHMAP44 | DMA Channel 44 Mapping Register |
| 02A0 01B4   | DCHMAP45 | DMA Channel 45 Mapping Register |
| 02A0 01B8   | DCHMAP46 | DMA Channel 46 Mapping Register |

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**Table 7-4 EDMA3 Registers (Part 3 of 15)**

| Hex Address           | Acronym  | Register Name                    |
|-----------------------|----------|----------------------------------|
| 02A0 01BC             | DCHMAP47 | DMA Channel 47 Mapping Register  |
| 02A0 01C0             | DCHMAP48 | DMA Channel 48 Mapping Register  |
| 02A0 01C4             | DCHMAP49 | DMA Channel 49 Mapping Register  |
| 02A0 01C8             | DCHMAP50 | DMA Channel 50 Mapping Register  |
| 02A0 01CC             | DCHMAP51 | DMA Channel 51 Mapping Register  |
| 02A0 01D0             | DCHMAP52 | DMA Channel 52 Mapping Register  |
| 02A0 01D4             | DCHMAP53 | DMA Channel 53 Mapping Register  |
| 02A0 01D8             | DCHMAP54 | DMA Channel 54 Mapping Register  |
| 02A0 01DC             | DCHMAP55 | DMA Channel 55 Mapping Register  |
| 02A0 01E0             | DCHMAP56 | DMA Channel 56 Mapping Register  |
| 02A0 01E4             | DCHMAP57 | DMA Channel 57 Mapping Register  |
| 02A0 01E8             | DCHMAP58 | DMA Channel 58 Mapping Register  |
| 02A0 01EC             | DCHMAP59 | DMA Channel 59 Mapping Register  |
| 02A0 01F0             | DCHMAP60 | DMA Channel 60 Mapping Register  |
| 02A0 01F4             | DCHMAP61 | DMA Channel 61 Mapping Register  |
| 02A0 01F8             | DCHMAP62 | DMA Channel 62 Mapping Register  |
| 02A0 01FC             | DCHMAP63 | DMA Channel 63 Mapping Register  |
| 02A0 0200             | QCHMAP0  | QDMA Channel 0 Mapping Register  |
| 02A0 0204             | QCHMAP1  | QDMA Channel 1 Mapping Register  |
| 02A0 0208             | QCHMAP2  | QDMA Channel 2 Mapping Register  |
| 02A0 020C             | QCHMAP3  | QDMA Channel 3 Mapping Register  |
| 02A0 0210             | QCHMAP4  | QDMA Channel 4 Mapping Register  |
| 02A0 0214             | QCHMAP5  | QDMA Channel 5 Mapping Register  |
| 02A0 0218             | QCHMAP6  | QDMA Channel 6 Mapping Register  |
| 02A0 021C             | QCHMAP7  | QDMA Channel 7 Mapping Register  |
| 02A0 0220 - 02A0 023C | -        | Reserved                         |
| 02A0 0240             | DMAQNUM0 | DMA Queue Number Register 0      |
| 02A0 0244             | DMAQNUM1 | DMA Queue Number Register 1      |
| 02A0 0248             | DMAQNUM2 | DMA Queue Number Register 2      |
| 02A0 024C             | DMAQNUM3 | DMA Queue Number Register 3      |
| 02A0 0250             | DMAQNUM4 | DMA Queue Number Register 4      |
| 02A0 0254             | DMAQNUM5 | DMA Queue Number Register 5      |
| 02A0 0258             | DMAQNUM6 | DMA Queue Number Register 6      |
| 02A0 025C             | DMAQNUM7 | DMA Queue Number Register 7      |
| 02A0 0260             | QDMAQNUM | QDMA Queue Number Register       |
| 02A0 0264 - 02A0 027C | -        | Reserved                         |
| 02A0 0280             | QUETCMAP | Queue to TC Mapping Register     |
| 02A0 0284             | QUEPRI   | Queue Priority Register          |
| 02A0 0288 - 02A0 02FC | -        | Reserved                         |
| 02A0 0300             | EMR      | Event Missed Register            |
| 02A0 0304             | EMRH     | Event Missed Register High       |
| 02A0 0308             | EMCR     | Event Missed Clear Register      |
| 02A0 030C             | EMCRH    | Event Missed Clear Register High |
| 02A0 0310             | QEMR     | QDMA Event Missed Register       |

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**Table 7-4 EDMA3 Registers (Part 4 of 15)**

| Hex Address           | Acronym  | Register Name                                       |
|-----------------------|----------|-----------------------------------------------------|
| 02A0 0314             | QEMCR    | QDMA Event Missed Clear Register                    |
| 02A0 0318             | CCERR    | EDMA3CC Error Register                              |
| 02A0 031C             | CCERRCLR | EDMA3CC Error Clear Register                        |
| 02A0 0320             | EEVAL    | Error Evaluate Register                             |
| 02A0 0324 - 02A0 033C | -        | Reserved                                            |
| 02A0 0340             | DRAE0    | DMA Region Access Enable Register for Region 0      |
| 02A0 0344             | DRAEH0   | DMA Region Access Enable Register High for Region 0 |
| 02A0 0348             | DRAE1    | DMA Region Access Enable Register for Region 1      |
| 02A0 034C             | DRAEH1   | DMA Region Access Enable Register High for Region 1 |
| 02A0 0350             | DRAE2    | DMA Region Access Enable Register for Region 2      |
| 02A0 0354             | DRAEH2   | DMA Region Access Enable Register High for Region 2 |
| 02A0 0358             | DRAE3    | DMA Region Access Enable Register for Region 3      |
| 02A0 035C             | DRAEH3   | DMA Region Access Enable Register High for Region 3 |
| 02A0 0360             | DRAE4    | DMA Region Access Enable Register for Region 4      |
| 02A0 0364             | DRAEH4   | DMA Region Access Enable Register High for Region 4 |
| 02A0 0368             | DRAE5    | DMA Region Access Enable Register for Region 5      |
| 02A0 036C             | DRAEH5   | DMA Region Access Enable Register High for Region 5 |
| 02A0 0370             | DRAE6    | DMA Region Access Enable Register for Region 6      |
| 02A0 0374             | DRAEH6   | DMA Region Access Enable Register High for Region 6 |
| 02A0 0378             | DRAE7    | DMA Region Access Enable Register for Region 7      |
| 02A0 037C             | DRAEH7   | DMA Region Access Enable Register High for Region 7 |
| 02A0 0380             | QRAE0    | QDMA Region Access Enable Register for Region 0     |
| 02A0 0384             | QRAE1    | QDMA Region Access Enable Register for Region 1     |
| 02A0 0388             | QRAE2    | QDMA Region Access Enable Register for Region 2     |
| 02A0 038C             | QRAE3    | QDMA Region Access Enable Register for Region 3     |
| 02A0 0390             | QRAE4    | QDMA Region Access Enable Register for Region 4     |
| 02A0 0394             | QRAE5    | QDMA Region Access Enable Register for Region 5     |
| 02A0 0398             | QRAE6    | QDMA Region Access Enable Register for Region 6     |
| 02A0 039C             | QRAE7    | QDMA Region Access Enable Register for Region 7     |
| 02A0 0400             | Q0E0     | Event Queue 0 Entry Register 0                      |
| 02A0 0404             | Q0E1     | Event Queue 0 Entry Register 1                      |
| 02A0 0408             | Q0E2     | Event Queue 0 Entry Register 2                      |
| 02A0 040C             | Q0E3     | Event Queue 0 Entry Register 3                      |
| 02A0 0410             | Q0E4     | Event Queue 0 Entry Register 4                      |
| 02A0 0414             | Q0E5     | Event Queue 0 Entry Register 5                      |
| 02A0 0418             | Q0E6     | Event Queue 0 Entry Register 6                      |
| 02A0 041C             | Q0E7     | Event Queue 0 Entry Register 7                      |
| 02A0 0420             | Q0E8     | Event Queue 0 Entry Register 8                      |
| 02A0 0424             | Q0E9     | Event Queue 0 Entry Register 9                      |
| 02A0 0428             | Q0E10    | Event Queue 0 Entry Register 10                     |
| 02A0 042C             | Q0E11    | Event Queue 0 Entry Register 11                     |
| 02A0 0430             | Q0E12    | Event Queue 0 Entry Register 12                     |
| 02A0 0434             | Q0E13    | Event Queue 0 Entry Register 13                     |
| 02A0 0438             | Q0E14    | Event Queue 0 Entry Register 14                     |

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**Table 7-4 EDMA3 Registers (Part 5 of 15)**

| Hex Address | Acronym | Register Name                   |
|-------------|---------|---------------------------------|
| 02A0 043C   | Q0E15   | Event Queue 0 Entry Register 15 |
| 02A0 0440   | Q1E0    | Event Queue 1 Entry Register 0  |
| 02A0 0444   | Q1E1    | Event Queue 1 Entry Register 1  |
| 02A0 0448   | Q1E2    | Event Queue 1 Entry Register 2  |
| 02A0 044C   | Q1E3    | Event Queue 1 Entry Register 3  |
| 02A0 0450   | Q1E4    | Event Queue 1 Entry Register 4  |
| 02A0 0454   | Q1E5    | Event Queue 1 Entry Register 5  |
| 02A0 0458   | Q1E6    | Event Queue 1 Entry Register 6  |
| 02A0 045C   | Q1E7    | Event Queue 1 Entry Register 7  |
| 02A0 0460   | Q1E8    | Event Queue 1 Entry Register 8  |
| 02A0 0464   | Q1E9    | Event Queue 1 Entry Register 9  |
| 02A0 0468   | Q1E10   | Event Queue 1 Entry Register 10 |
| 02A0 046C   | Q1E11   | Event Queue 1 Entry Register 11 |
| 02A0 0470   | Q1E12   | Event Queue 1 Entry Register 12 |
| 02A0 0474   | Q1E13   | Event Queue 1 Entry Register 13 |
| 02A0 0478   | Q1E14   | Event Queue 1 Entry Register 14 |
| 02A0 047C   | Q1E15   | Event Queue 1 Entry Register 15 |
| 02A0 0480   | Q2E0    | Event Queue 2 Entry Register 0  |
| 02A0 0484   | Q2E1    | Event Queue 2 Entry Register 1  |
| 02A0 0488   | Q2E2    | Event Queue 2 Entry Register 2  |
| 02A0 048C   | Q2E3    | Event Queue 2 Entry Register 3  |
| 02A0 0490   | Q2E4    | Event Queue 2 Entry Register 4  |
| 02A0 0494   | Q2E5    | Event Queue 2 Entry Register 5  |
| 02A0 0498   | Q2E6    | Event Queue 2 Entry Register 6  |
| 02A0 049C   | Q2E7    | Event Queue 2 Entry Register 7  |
| 02A0 04A0   | Q2E8    | Event Queue 2 Entry Register 8  |
| 02A0 04A4   | Q2E9    | Event Queue 2 Entry Register 9  |
| 02A0 04A8   | Q2E10   | Event Queue 2 Entry Register 10 |
| 02A0 04AC   | Q2E11   | Event Queue 2 Entry Register 11 |
| 02A0 04B0   | Q2E12   | Event Queue 2 Entry Register 12 |
| 02A0 04B4   | Q2E13   | Event Queue 2 Entry Register 13 |
| 02A0 04B8   | Q2E14   | Event Queue 2 Entry Register 14 |
| 02A0 04BC   | Q2E15   | Event Queue 2 Entry Register 15 |
| 02A0 04C0   | Q3E0    | Event Queue 3 Entry Register 0  |
| 02A0 04C4   | Q3E1    | Event Queue 3 Entry Register 1  |
| 02A0 04C8   | Q3E2    | Event Queue 3 Entry Register 2  |
| 02A0 04CC   | Q3E3    | Event Queue 3 Entry Register 3  |
| 02A0 04D0   | Q3E4    | Event Queue 3 Entry Register 4  |
| 02A0 04D4   | Q3E5    | Event Queue 3 Entry Register 5  |
| 02A0 04D8   | Q3E6    | Event Queue 3 Entry Register 6  |
| 02A0 04DC   | Q3E7    | Event Queue 3 Entry Register 7  |
| 02A0 04E0   | Q3E8    | Event Queue 3 Entry Register 8  |
| 02A0 04E4   | Q3E9    | Event Queue 3 Entry Register 9  |
| 02A0 04E8   | Q3E10   | Event Queue 3 Entry Register 10 |

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**Table 7-4 EDMA3 Registers (Part 6 of 15)**

| Hex Address           | Acronym | Register Name                               |
|-----------------------|---------|---------------------------------------------|
| 02A0 04EC             | Q3E11   | Event Queue 3 Entry Register 11             |
| 02A0 04F0             | Q3E12   | Event Queue 3 Entry Register 12             |
| 02A0 04F4             | Q3E13   | Event Queue 3 Entry Register 13             |
| 02A0 04F8             | Q3E14   | Event Queue 3 Entry Register 14             |
| 02A0 04FC             | Q3E15   | Event Queue 3 Entry Register 15             |
| 02A0 0500             | Q4E0    | Event Queue 4 Entry Register 0              |
| 02A0 0504             | Q4E1    | Event Queue 4 Entry Register 1              |
| 02A0 0508             | Q4E2    | Event Queue 4 Entry Register 2              |
| 02A0 050C             | Q4E3    | Event Queue 4 Entry Register 3              |
| 02A0 0510             | Q4E4    | Event Queue 4 Entry Register 4              |
| 02A0 0514             | Q4E5    | Event Queue 4 Entry Register 5              |
| 02A0 0518             | Q4E6    | Event Queue 4 Entry Register 6              |
| 02A0 051C             | Q4E7    | Event Queue 4 Entry Register 7              |
| 02A0 0520             | Q4E8    | Event Queue 4 Entry Register 8              |
| 02A0 0524             | Q4E9    | Event Queue 4 Entry Register 9              |
| 02A0 0528             | Q4E10   | Event Queue 4 Entry Register 10             |
| 02A0 052C             | Q4E11   | Event Queue 4 Entry Register 11             |
| 02A0 0530             | Q4E12   | Event Queue 4 Entry Register 12             |
| 02A0 0534             | Q4E13   | Event Queue 4 Entry Register 13             |
| 02A0 0538             | Q4E14   | Event Queue 4 Entry Register 14             |
| 02A0 053C             | Q4E15   | Event Queue 4 Entry Register 15             |
| 02A0 0540 - 02A0 05FC | -       | Reserved                                    |
| 02A0 0600             | QSTAT0  | Queue Status Register 0                     |
| 02A0 0604             | QSTAT1  | Queue Status Register 1                     |
| 02A0 0608             | QSTAT2  | Queue Status Register 2                     |
| 02A0 060C             | QSTAT3  | Queue Status Register 3                     |
| 02A0 0610             | QSTAT4  | Queue Status Register 4                     |
| 02A0 0614             | QSTAT5  | Queue Status Register 5                     |
| 02A0 0618 - 02A0 061C | -       | Reserved                                    |
| 02A0 0620             | QWMTHRA | Queue Watermark Threshold A Register        |
| 02A0 0624             | QWMTHRB | Queue Watermark Threshold B Register        |
| 02A0 0628 - 02A0 063C | -       | Reserved                                    |
| 02A0 0640             | CCSTAT  | EDMA3CC Status Register                     |
| 02A0 0644 - 02A0 06FC | -       | Reserved                                    |
| 02A0 0700 - 02A0 07FC | -       | Reserved                                    |
| 02A0 0800             | MPFAR   | Memory Protection Fault Address Register    |
| 02A0 0804             | MPFSR   | Memory Protection Fault Status Register     |
| 02A0 0808             | MPFCR   | Memory Protection Fault Command Register    |
| 02A0 080C             | MPPAG   | Memory Protection Page Attribute Register G |
| 02A0 0810             | MPPA0   | Memory Protection Page Attribute Register 0 |
| 02A0 0814             | MPPA1   | Memory Protection Page Attribute Register 1 |
| 02A0 0818             | MPPA2   | Memory Protection Page Attribute Register 2 |
| 02A0 081C             | MPPA3   | Memory Protection Page Attribute Register 3 |
| 02A0 0820             | MPPA4   | Memory Protection Page Attribute Register 4 |

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**Table 7-4 EDMA3 Registers (Part 7 of 15)**

| Hex Address                              | Acronym | Register Name                               |
|------------------------------------------|---------|---------------------------------------------|
| 02A0 0824                                | MPPA5   | Memory Protection Page Attribute Register 5 |
| 02A0 0828                                | MPPA6   | Memory Protection Page Attribute Register 6 |
| 02A0 082C                                | MPPA7   | Memory Protection Page Attribute Register 7 |
| 02A0 082C - 02A0 0FFC                    | -       | Reserved                                    |
| 02A0 1000                                | ER      | Event Register                              |
| 02A0 1004                                | ERH     | Event Register High                         |
| 02A0 1008                                | ECR     | Event Clear Register                        |
| 02A0 100C                                | ECRH    | Event Clear Register High                   |
| 02A0 1010                                | ESR     | Event Set Register                          |
| 02A0 1014                                | ESRH    | Event Set Register High                     |
| 02A0 1018                                | CER     | Chained Event Register                      |
| 02A0 101C                                | CERH    | Chained Event Register High                 |
| 02A0 1020                                | EER     | Event Enable Register                       |
| 02A0 1024                                | EERH    | Event Enable Register High                  |
| 02A0 1028                                | ECCR    | Event Enable Clear Register                 |
| 02A0 102C                                | EECRH   | Event Enable Clear Register High            |
| 02A0 1030                                | EESR    | Event Enable Set Register                   |
| 02A0 1034                                | EESRH   | Event Enable Set Register High              |
| 02A0 1038                                | SER     | Secondary Event Register                    |
| 02A0 103C                                | SERH    | Secondary Event Register High               |
| 02A0 1040                                | SECR    | Secondary Event Clear Register              |
| 02A0 1044                                | SECRH   | Secondary Event Clear Register High         |
| 02A0 1048 - 02A0 104C                    | -       | Reserved                                    |
| 02A0 1050                                | IER     | Interrupt Enable Register                   |
| 02A0 1054                                | IERH    | Interrupt Enable High Register              |
| 02A0 1058                                | IECR    | Interrupt Enable Clear Register             |
| 02A0 105C                                | IECRH   | Interrupt Enable Clear High Register        |
| 02A0 1060                                | IESR    | Interrupt Enable Set Register               |
| 02A0 1064                                | IESRH   | Interrupt Enable Set High Register          |
| 02A0 1068                                | IPR     | Interrupt Pending Register                  |
| 02A0 106C                                | IPRH    | Interrupt Pending High Register             |
| 02A0 1070                                | ICR     | Interrupt Clear Register                    |
| 02A0 1074                                | ICRH    | Interrupt Clear High Register               |
| 02A0 1078                                | IEVAL   | Interrupt Evaluate Register                 |
| 02A0 107C                                | -       | Reserved                                    |
| 02A0 1080                                | QER     | QDMA Event Register                         |
| 02A0 1084                                | QEER    | QDMA Event Enable Register                  |
| 02A0 1088                                | QECCR   | QDMA Event Enable Clear Register            |
| 02A0 108C                                | QEESR   | QDMA Event Enable Set Register              |
| 02A0 1090                                | QSER    | QDMA Secondary Event Register               |
| 02A0 1094                                | QSECR   | QDMA Secondary Event Clear Register         |
| 02A0 1098 - 02A0 1FFF                    | -       | Reserved                                    |
| <b>Shadow Region 0 Channel Registers</b> |         |                                             |
| 02A0 2000                                | ER      | Event Register                              |

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**Table 7-4 EDMA3 Registers (Part 8 of 15)**

| Hex Address                              | Acronym | Register Name                        |
|------------------------------------------|---------|--------------------------------------|
| 02A0 2004                                | ERH     | Event Register High                  |
| 02A0 2008                                | ECR     | Event Clear Register                 |
| 02A0 200C                                | ECRH    | Event Clear Register High            |
| 02A0 2010                                | ESR     | Event Set Register                   |
| 02A0 2014                                | ESRH    | Event Set Register High              |
| 02A0 2018                                | CER     | Chained Event Register               |
| 02A0 201C                                | CERH    | Chained Event Register High          |
| 02A0 2020                                | EER     | Event Enable Register                |
| 02A0 2024                                | EERH    | Event Enable Register High           |
| 02A0 2028                                | EECR    | Event Enable Clear Register          |
| 02A0 202C                                | EECRH   | Event Enable Clear Register High     |
| 02A0 2030                                | EESR    | Event Enable Set Register            |
| 02A0 2034                                | EESRH   | Event Enable Set Register High       |
| 02A0 2038                                | SER     | Secondary Event Register             |
| 02A0 203C                                | SERH    | Secondary Event Register High        |
| 02A0 2040                                | SECR    | Secondary Event Clear Register       |
| 02A0 2044                                | SECRH   | Secondary Event Clear Register High  |
| 02A0 2048 - 02A0 204C                    | -       | Reserved                             |
| 02A0 2050                                | IER     | Interrupt Enable Register            |
| 02A0 2054                                | IERH    | Interrupt Enable Register High       |
| 02A0 2058                                | IECR    | Interrupt Enable Clear Register      |
| 02A0 205C                                | IECRH   | Interrupt Enable Clear Register High |
| 02A0 2060                                | IESR    | Interrupt Enable Set Register        |
| 02A0 2064                                | IESRH   | Interrupt Enable Set Register High   |
| 02A0 2068                                | IPR     | Interrupt Pending Register           |
| 02A0 206C                                | IPRH    | Interrupt Pending Register High      |
| 02A0 2070                                | ICR     | Interrupt Clear Register             |
| 02A0 2074                                | ICRH    | Interrupt Clear Register High        |
| 02A0 2078                                | IEVAL   | Interrupt Evaluate Register          |
| 02A0 207C                                | -       | Reserved                             |
| 02A0 2080                                | QER     | QDMA Event Register                  |
| 02A0 2084                                | QEER    | QDMA Event Enable Register           |
| 02A0 2088                                | QEECR   | QDMA Event Enable Clear Register     |
| 02A0 208C                                | QEESR   | QDMA Event Enable Set Register       |
| 02A0 2090                                | QSER    | QDMA Secondary Event Register        |
| 02A0 2094                                | QSECR   | QDMA Secondary Event Clear Register  |
| 02A0 2098 - 02A0 21FF                    | -       | Reserved                             |
| <b>Shadow Region 1 Channel Registers</b> |         |                                      |
| 02A0 2200                                | ER      | Event Register                       |
| 02A0 2204                                | ERH     | Event Register High                  |
| 02A0 2208                                | ECR     | Event Clear Register                 |
| 02A0 220C                                | ECRH    | Event Clear Register High            |
| 02A0 2210                                | ESR     | Event Set Register                   |
| 02A0 2214                                | ESRH    | Event Set Register High              |

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**Table 7-4 EDMA3 Registers (Part 9 of 15)**

| Hex Address                              | Acronym | Register Name                        |
|------------------------------------------|---------|--------------------------------------|
| 02A0 2218                                | CER     | Chained Event Register               |
| 02A0 221C                                | CERH    | Chained Event Register High          |
| 02A0 2220                                | EER     | Event Enable Register                |
| 02A0 2224                                | EERH    | Event Enable Register High           |
| 02A0 2228                                | EECR    | Event Enable Clear Register          |
| 02A0 222C                                | EECRH   | Event Enable Clear Register High     |
| 02A0 2230                                | EESR    | Event Enable Set Register            |
| 02A0 2234                                | EESRH   | Event Enable Set Register High       |
| 02A0 2238                                | SER     | Secondary Event Register             |
| 02A0 223C                                | SERH    | Secondary Event Register High        |
| 02A0 2240                                | SECR    | Secondary Event Clear Register       |
| 02A0 2244                                | SECRH   | Secondary Event Clear Register High  |
| 02A0 2248 - 02A0 224C                    | -       | Reserved                             |
| 02A0 2250                                | IER     | Interrupt Enable Register            |
| 02A0 2254                                | IERH    | Interrupt Enable Register High       |
| 02A0 2258                                | IECR    | Interrupt Enable Clear Register      |
| 02A0 225C                                | IECRH   | Interrupt Enable Clear Register High |
| 02A0 2260                                | IESR    | Interrupt Enable Set Register        |
| 02A0 2264                                | IESRH   | Interrupt Enable Set Register High   |
| 02A0 2268                                | IPR     | Interrupt Pending Register           |
| 02A0 226C                                | IPRH    | Interrupt Pending Register High      |
| 02A0 2270                                | ICR     | Interrupt Clear Register             |
| 02A0 2274                                | ICRH    | Interrupt Clear Register High        |
| 02A0 2278                                | IEVAL   | Interrupt Evaluate Register          |
| 02A0 227C                                | -       | Reserved                             |
| 02A0 2280                                | QER     | QDMA Event Register                  |
| 02A0 2284                                | QEER    | QDMA Event Enable Register           |
| 02A0 2288                                | QEECR   | QDMA Event Enable Clear Register     |
| 02A0 228C                                | QEESR   | QDMA Event Enable Set Register       |
| 02A0 2290                                | QSER    | QDMA Secondary Event Register        |
| 02A0 2294                                | QSECR   | QDMA Secondary Event Clear Register  |
| 02A0 2298 - 02A0 23FF                    | -       | Reserved                             |
| <b>Shadow Region 2 Channel Registers</b> |         |                                      |
| 02A0 2400                                | ER      | Event Register                       |
| 02A0 2404                                | ERH     | Event Register High                  |
| 02A0 2408                                | ECR     | Event Clear Register                 |
| 02A0 240C                                | ECRH    | Event Clear Register High            |
| 02A0 2410                                | ESR     | Event Set Register                   |
| 02A0 2414                                | ESRH    | Event Set Register High              |
| 02A0 2418                                | CER     | Chained Event Register               |
| 02A0 241C                                | CERH    | Chained Event Register High          |
| 02A0 2420                                | EER     | Event Enable Register                |
| 02A0 2424                                | EERH    | Event Enable Register High           |
| 02A0 2428                                | EECR    | Event Enable Clear Register          |

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**Table 7-4 EDMA3 Registers (Part 10 of 15)**

| Hex Address                              | Acronym | Register Name                        |
|------------------------------------------|---------|--------------------------------------|
| 02A0 242C                                | EECRH   | Event Enable Clear Register High     |
| 02A0 2430                                | EESR    | Event Enable Set Register            |
| 02A0 2434                                | EESRH   | Event Enable Set Register High       |
| 02A0 2438                                | SER     | Secondary Event Register             |
| 02A0 243C                                | SERH    | Secondary Event Register High        |
| 02A0 2440                                | SECR    | Secondary Event Clear Register       |
| 02A0 2444                                | SECRH   | Secondary Event Clear Register High  |
| 02A0 2448 - 02A0 244C                    | -       | Reserved                             |
| 02A0 2450                                | IER     | Interrupt Enable Register            |
| 02A0 2454                                | IERH    | Interrupt Enable Register High       |
| 02A0 2458                                | IECR    | Interrupt Enable Clear Register      |
| 02A0 245C                                | IECRH   | Interrupt Enable Clear Register High |
| 02A0 2460                                | IESR    | Interrupt Enable Set Register        |
| 02A0 2464                                | IESRH   | Interrupt Enable Set Register High   |
| 02A0 2468                                | IPR     | Interrupt Pending Register           |
| 02A0 246C                                | IPRH    | Interrupt Pending Register High      |
| 02A0 2470                                | ICR     | Interrupt Clear Register             |
| 02A0 2474                                | ICRH    | Interrupt Clear Register High        |
| 02A0 2478                                | IEVAL   | Interrupt Evaluate Register          |
| 02A0 247C                                | -       | Reserved                             |
| 02A0 2480                                | QER     | QDMA Event Register                  |
| 02A0 2484                                | QEER    | QDMA Event Enable Register           |
| 02A0 2488                                | QEECR   | QDMA Event Enable Clear Register     |
| 02A0 248C                                | QEESR   | QDMA Event Enable Set Register       |
| 02A0 2490                                | QSER    | QDMA Secondary Event Register        |
| 02A0 2494                                | QSECR   | QDMA Secondary Event Clear Register  |
| 02A0 2498 - 02A0 25FF                    | -       | Reserved                             |
| <b>Shadow Region 3 Channel Registers</b> |         |                                      |
| 02A0 2600                                | ER      | Event Register                       |
| 02A0 2604                                | ERH     | Event Register High                  |
| 02A0 2608                                | ECR     | Event Clear Register                 |
| 02A0 260C                                | ECRH    | Event Clear Register High            |
| 02A0 2610                                | ESR     | Event Set Register                   |
| 02A0 2614                                | ESRH    | Event Set Register High              |
| 02A0 2618                                | CER     | Chained Event Register               |
| 02A0 261C                                | CERH    | Chained Event Register High          |
| 02A0 2620                                | EER     | Event Enable Register                |
| 02A0 2624                                | EERH    | Event Enable Register High           |
| 02A0 2628                                | EECR    | Event Enable Clear Register          |
| 02A0 262C                                | EECRH   | Event Enable Clear Register High     |
| 02A0 2630                                | EESR    | Event Enable Set Register            |
| 02A0 2634                                | EESRH   | Event Enable Set Register High       |
| 02A0 2638                                | SER     | Secondary Event Register             |
| 02A0 263C                                | SERH    | Secondary Event Register High        |

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**Table 7-4 EDMA3 Registers (Part 11 of 15)**

| Hex Address                              | Acronym | Register Name                        |
|------------------------------------------|---------|--------------------------------------|
| 02A0 2640                                | SECR    | Secondary Event Clear Register       |
| 02A0 2644                                | SECRH   | Secondary Event Clear Register High  |
| 02A0 2648 - 02A0 264C                    | -       | Reserved                             |
| 02A0 2650                                | IER     | Interrupt Enable Register            |
| 02A0 2654                                | IERH    | Interrupt Enable Register High       |
| 02A0 2658                                | IECR    | Interrupt Enable Clear Register      |
| 02A0 265C                                | IECRH   | Interrupt Enable Clear Register High |
| 02A0 2660                                | IESR    | Interrupt Enable Set Register        |
| 02A0 2664                                | IESRH   | Interrupt Enable Set Register High   |
| 02A0 2668                                | IPR     | Interrupt Pending Register           |
| 02A0 266C                                | IPRH    | Interrupt Pending Register High      |
| 02A0 2670                                | ICR     | Interrupt Clear Register             |
| 02A0 2674                                | ICRH    | Interrupt Clear Register High        |
| 02A0 2678                                | IEVAL   | Interrupt Evaluate Register          |
| 02A0 267C                                | -       | Reserved                             |
| 02A0 2680                                | QER     | QDMA Event Register                  |
| 02A0 2684                                | QEER    | QDMA Event Enable Register           |
| 02A0 2688                                | QEECR   | QDMA Event Enable Clear Register     |
| 02A0 268C                                | QEESR   | QDMA Event Enable Set Register       |
| 02A0 2690                                | QSER    | QDMA Secondary Event Register        |
| 02A0 2694                                | QSECR   | QDMA Secondary Event Clear Register  |
| 02A0 2698 - 02A0 27FF                    | -       | Reserved                             |
| <b>Shadow Region 4 Channel Registers</b> |         |                                      |
| 02A0 2800                                | ER      | Event Register                       |
| 02A0 2804                                | ERH     | Event Register High                  |
| 02A0 2808                                | ECR     | Event Clear Register                 |
| 02A0 280C                                | ECRH    | Event Clear Register High            |
| 02A0 2810                                | ESR     | Event Set Register                   |
| 02A0 2814                                | ESRH    | Event Set Register High              |
| 02A0 2818                                | CER     | Chained Event Register               |
| 02A0 281C                                | CERH    | Chained Event Register High          |
| 02A0 2820                                | EER     | Event Enable Register                |
| 02A0 2824                                | EERH    | Event Enable Register High           |
| 02A0 2828                                | EECR    | Event Enable Clear Register          |
| 02A0 282C                                | EECRH   | Event Enable Clear Register High     |
| 02A0 2830                                | EESR    | Event Enable Set Register            |
| 02A0 2834                                | EESRH   | Event Enable Set Register High       |
| 02A0 2838                                | SER     | Secondary Event Register             |
| 02A0 283C                                | SERH    | Secondary Event Register High        |
| 02A0 2840                                | SECR    | Secondary Event Clear Register       |
| 02A0 2844                                | SECRH   | Secondary Event Clear Register High  |
| 02A0 2848 - 02A0 284C                    | -       | Reserved                             |
| 02A0 2850                                | IER     | Interrupt Enable Register            |
| 02A0 2854                                | IERH    | Interrupt Enable Register High       |

**Table 7-4 EDMA3 Registers (Part 12 of 15)**

| Hex Address                              | Acronym | Register Name                        |
|------------------------------------------|---------|--------------------------------------|
| 02A0 2858                                | IECR    | Interrupt Enable Clear Register      |
| 02A0 285C                                | IECRH   | Interrupt Enable Clear Register High |
| 02A0 2860                                | IESR    | Interrupt Enable Set Register        |
| 02A0 2864                                | IESRH   | Interrupt Enable Set Register High   |
| 02A0 2868                                | IPR     | Interrupt Pending Register           |
| 02A0 286C                                | IPRH    | Interrupt Pending Register High      |
| 02A0 2870                                | ICR     | Interrupt Clear Register             |
| 02A0 2874                                | ICRH    | Interrupt Clear Register High        |
| 02A0 2878                                | IEVAL   | Interrupt Evaluate Register          |
| 02A0 287C                                | -       | Reserved                             |
| 02A0 2880                                | QER     | QDMA Event Register                  |
| 02A0 2884                                | QEER    | QDMA Event Enable Register           |
| 02A0 2888                                | QEECR   | QDMA Event Enable Clear Register     |
| 02A0 288C                                | QEESR   | QDMA Event Enable Set Register       |
| 02A0 2890                                | QSER    | QDMA Secondary Event Register        |
| 02A0 2894                                | QSECR   | QDMA Secondary Event Clear Register  |
| 02A0 2898 - 02A0 29FF                    | -       | Reserved                             |
| <b>Shadow Region 5 Channel Registers</b> |         |                                      |
| 02A0 2A00                                | ER      | Event Register                       |
| 02A0 2A04                                | ERH     | Event Register High                  |
| 02A0 2A08                                | ECR     | Event Clear Register                 |
| 02A0 2A0C                                | ECRH    | Event Clear Register High            |
| 02A0 2A10                                | ESR     | Event Set Register                   |
| 02A0 2A14                                | ESRH    | Event Set Register High              |
| 02A0 2A18                                | CER     | Chained Event Register               |
| 02A0 2A1C                                | CERH    | Chained Event Register High          |
| 02A0 2A20                                | EER     | Event Enable Register                |
| 02A0 2A24                                | EERH    | Event Enable Register High           |
| 02A0 2A28                                | EECR    | Event Enable Clear Register          |
| 02A0 2A2C                                | EECRH   | Event Enable Clear Register High     |
| 02A0 2A30                                | EESR    | Event Enable Set Register            |
| 02A0 2A34                                | EESRH   | Event Enable Set Register High       |
| 02A0 2A38                                | SER     | Secondary Event Register             |
| 02A0 2A3C                                | SERH    | Secondary Event Register High        |
| 02A0 2A40                                | SECR    | Secondary Event Clear Register       |
| 02A0 2A44                                | SECRH   | Secondary Event Clear Register High  |
| 02A0 2A48 - 02A0 2A4C                    | -       | Reserved                             |
| 02A0 2A50                                | IER     | Interrupt Enable Register            |
| 02A0 2A54                                | IERH    | Interrupt Enable Register High       |
| 02A0 2A58                                | IECR    | Interrupt Enable Clear Register      |
| 02A0 2A5C                                | IECRH   | Interrupt Enable Clear Register High |
| 02A0 2A60                                | IESR    | Interrupt Enable Set Register        |
| 02A0 2A64                                | IESRH   | Interrupt Enable Set Register High   |
| 02A0 2A68                                | IPR     | Interrupt Pending Register           |

**Table 7-4 EDMA3 Registers (Part 13 of 15)**

| Hex Address                              | Acronym | Register Name                        |
|------------------------------------------|---------|--------------------------------------|
| 02A0 2A6C                                | IPRH    | Interrupt Pending Register High      |
| 02A0 2A70                                | ICR     | Interrupt Clear Register             |
| 02A0 2A74                                | ICRH    | Interrupt Clear Register High        |
| 02A0 2A78                                | IEVAL   | Interrupt Evaluate Register          |
| 02A0 2A7C                                | -       | Reserved                             |
| 02A0 2A80                                | QER     | QDMA Event Register                  |
| 02A0 2A84                                | QEER    | QDMA Event Enable Register           |
| 02A0 2A88                                | QEECR   | QDMA Event Enable Clear Register     |
| 02A0 2A8C                                | QEESR   | QDMA Event Enable Set Register       |
| 02A0 2A90                                | QSER    | QDMA Secondary Event Register        |
| 02A0 2A94                                | QSECR   | QDMA Secondary Event Clear Register  |
| 02A0 2A98 - 02A0 2BFF                    | -       | Reserved                             |
| <b>Shadow Region 6 Channel Registers</b> |         |                                      |
| 02A0 2C00                                | ER      | Event Register                       |
| 02A0 2C04                                | ERH     | Event Register High                  |
| 02A0 2C08                                | ECR     | Event Clear Register                 |
| 02A0 2C0C                                | ECRH    | Event Clear Register High            |
| 02A0 2C10                                | ESR     | Event Set Register                   |
| 02A0 2C14                                | ESRH    | Event Set Register High              |
| 02A0 2C18                                | CER     | Chained Event Register               |
| 02A0 2C1C                                | CERH    | Chained Event Register High          |
| 02A0 2C20                                | EER     | Event Enable Register                |
| 02A0 2C24                                | EERH    | Event Enable Register High           |
| 02A0 2C28                                | EECR    | Event Enable Clear Register          |
| 02A0 2C2C                                | EECRH   | Event Enable Clear Register High     |
| 02A0 2C30                                | EESR    | Event Enable Set Register            |
| 02A0 2C34                                | EESRH   | Event Enable Set Register High       |
| 02A0 2C38                                | SER     | Secondary Event Register             |
| 02A0 2C3C                                | SERH    | Secondary Event Register High        |
| 02A0 2C40                                | SECR    | Secondary Event Clear Register       |
| 02A0 2C44                                | SECRH   | Secondary Event Clear Register High  |
| 02A0 2C48 - 02A0 2C4C                    | -       | Reserved                             |
| 02A0 2C50                                | IER     | Interrupt Enable Register            |
| 02A0 2C54                                | IERH    | Interrupt Enable Register High       |
| 02A0 2C58                                | IECR    | Interrupt Enable Clear Register      |
| 02A0 2C5C                                | IECRH   | Interrupt Enable Clear Register High |
| 02A0 2C60                                | IESR    | Interrupt Enable Set Register        |
| 02A0 2C64                                | IESRH   | Interrupt Enable Set Register High   |
| 02A0 2C68                                | IPR     | Interrupt Pending Register           |
| 02A0 2C6C                                | IPRH    | Interrupt Pending Register High      |
| 02A0 2C70                                | ICR     | Interrupt Clear Register             |
| 02A0 2C74                                | ICRH    | Interrupt Clear Register High        |
| 02A0 2C78                                | IEVAL   | Interrupt Evaluate Register          |
| 02A0 2C7C                                | -       | Reserved                             |

**Table 7-4 EDMA3 Registers (Part 14 of 15)**

| Hex Address                              | Acronym | Register Name                        |
|------------------------------------------|---------|--------------------------------------|
| 02A0 2C80                                | QER     | QDMA Event Register                  |
| 02A0 2C84                                | QEER    | QDMA Event Enable Register           |
| 02A0 2C88                                | QEECR   | QDMA Event Enable Clear Register     |
| 02A0 2C8C                                | QEESR   | QDMA Event Enable Set Register       |
| 02A0 2C90                                | QSER    | QDMA Secondary Event Register        |
| 02A0 2C94                                | QSECR   | QDMA Secondary Event Clear Register  |
| 02A0 2C98 - 02A0 2DFF                    | -       | Reserved                             |
| <b>Shadow Region 7 Channel Registers</b> |         |                                      |
| 02A0 2E00                                | ER      | Event Register                       |
| 02A0 2E04                                | ERH     | Event Register High                  |
| 02A0 2E08                                | ECR     | Event Clear Register                 |
| 02A0 2E0C                                | ECRH    | Event Clear Register High            |
| 02A0 2E10                                | ESR     | Event Set Register                   |
| 02A0 2E14                                | ESRH    | Event Set Register High              |
| 02A0 2E18                                | CER     | Chained Event Register               |
| 02A0 2E1C                                | CERH    | Chained Event Register High          |
| 02A0 2E20                                | EER     | Event Enable Register                |
| 02A0 2E24                                | EERH    | Event Enable Register High           |
| 02A0 2E28                                | EECR    | Event Enable Clear Register          |
| 02A0 2E2C                                | EECRH   | Event Enable Clear Register High     |
| 02A0 2E30                                | EESR    | Event Enable Set Register            |
| 02A0 2E34                                | EESRH   | Event Enable Set Register High       |
| 02A0 2E38                                | SER     | Secondary Event Register             |
| 02A0 2E3C                                | SERH    | Secondary Event Register High        |
| 02A0 2E40                                | SECR    | Secondary Event Clear Register       |
| 02A0 2E44                                | SECRH   | Secondary Event Clear Register High  |
| 02A0 2E48 - 02A0 2E4C                    | -       | Reserved                             |
| 02A0 2E50                                | IER     | Interrupt Enable Register            |
| 02A0 2E54                                | IERH    | Interrupt Enable Register High       |
| 02A0 2E58                                | IECR    | Interrupt Enable Clear Register      |
| 02A0 2E5C                                | IECRH   | Interrupt Enable Clear Register High |
| 02A0 2E60                                | IESR    | Interrupt Enable Set Register        |
| 02A0 2E64                                | IESRH   | Interrupt Enable Set Register High   |
| 02A0 2E68                                | IPR     | Interrupt Pending Register           |
| 02A0 2E6C                                | IPRH    | Interrupt Pending Register High      |
| 02A0 2E70                                | ICR     | Interrupt Clear Register             |
| 02A0 2E74                                | ICRH    | Interrupt Clear Register High        |
| 02A0 2E78                                | IEVAL   | Interrupt Evaluate Register          |
| 02A0 2E7C                                | -       | Reserved                             |
| 02A0 2E80                                | QER     | QDMA Event Register                  |
| 02A0 2E84                                | QEER    | QDMA Event Enable Register           |
| 02A0 2E88                                | QEECR   | QDMA Event Enable Clear Register     |
| 02A0 2E8C                                | QEESR   | QDMA Event Enable Set Register       |
| 02A0 2E90                                | QSER    | QDMA Secondary Event Register        |

**Table 7-4      EDMA3 Registers (Part 15 of 15)**

| Hex Address             | Acronym | Register Name                       |
|-------------------------|---------|-------------------------------------|
| 02A0 2E94               | QSECR   | QDMA Secondary Event Clear Register |
| 02A0 2E98 - 02A0 2FFF   | -       | Reserved                            |
| <b>End of Table 7-4</b> |         |                                     |

**Table 7-5      EDMA3 Parameter RAM**

| Hex Address Range       | Acronym | Register Name     |
|-------------------------|---------|-------------------|
| 02A0 4000 - 02A0 401F   | -       | Parameter Set 0   |
| 02A0 4020 - 02A0 403F   | -       | Parameter Set 1   |
| 02A0 4040 - 02A0 405F   | -       | Parameter Set 2   |
| 02A0 4060 - 02A0 407F   | -       | Parameter Set 3   |
| 02A0 4080 - 02A0 409F   | -       | Parameter Set 4   |
| 02A0 40A0 - 02A0 40BF   | -       | Parameter Set 5   |
| 02A0 40C0 - 02A0 40DF   | -       | Parameter Set 6   |
| 02A0 40E0 - 02A0 40FF   | -       | Parameter Set 7   |
| 02A0 4100 - 02A0 411F   | -       | Parameter Set 8   |
| 02A0 4120 - 02A0 413F   | -       | Parameter Set 9   |
| ...                     |         | ...               |
| 02A0 47E0 - 02A0 47FF   | -       | Parameter Set 63  |
| 02A0 4800 - 02A0 481F   | -       | Parameter Set 64  |
| 02A0 4820 - 02A0 483F   | -       | Parameter Set 65  |
| ...                     |         | ...               |
| 02A0 5FC0 - 02A0 5FDF   | -       | Parameter Set 254 |
| 02A0 5FE0 - 02A0 5FFF   | -       | Parameter Set 255 |
| <b>End of Table 7-5</b> |         |                   |

**Table 7-6      EDMA3 Transfer Controller 0 Registers (Part 1 of 2)**

| Hex Address Range     | Acronym | Register Name                         |
|-----------------------|---------|---------------------------------------|
| 02A2 0000             | PID     | Peripheral Identification Register    |
| 02A2 0004             | TCCFG   | EDMA3TC Configuration Register        |
| 02A2 0008 - 02A2 00FC | -       | Reserved                              |
| 02A2 0100             | TCSTAT  | EDMA3TC Channel Status Register       |
| 02A2 0104 - 02A2 011C | -       | Reserved                              |
| 02A2 0120             | ERRSTAT | Error Register                        |
| 02A2 0124             | ERREN   | Error Enable Register                 |
| 02A2 0128             | ERRCLR  | Error Clear Register                  |
| 02A2 012C             | ERRDET  | Error Details Register                |
| 02A2 0130             | ERRCMD  | Error Interrupt Command Register      |
| 02A2 0134 - 02A2 013C | -       | Reserved                              |
| 02A2 0140             | RDRATE  | Read Rate Register                    |
| 02A2 0144 - 02A2 023C | -       | Reserved                              |
| 02A2 0240             | SAOPT   | Source Active Options Register        |
| 02A2 0244             | SASRC   | Source Active Source Address Register |
| 02A2 0248             | SACNT   | Source Active Count Register          |

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**Table 7-6 EDMA3 Transfer Controller 0 Registers (Part 2 of 2)**

| Hex Address Range       | Acronym   | Register Name                                                 |
|-------------------------|-----------|---------------------------------------------------------------|
| 02A2 024C               | SADST     | Source Active Destination Address Register                    |
| 02A2 0250               | SABIDX    | Source Active Source B-Index Register                         |
| 02A2 0254               | SAMPPRXY  | Source Active Memory Protection Proxy Register                |
| 02A2 0258               | SACNTRLD  | Source Active Count Reload Register                           |
| 02A2 025C               | SASRCBREF | Source Active Source Address B-Reference Register             |
| 02A2 0260               | SADSTBREF | Source Active Destination Address B-Reference Register        |
| 02A2 0264 - 02A2 027C   | -         | Reserved                                                      |
| 02A2 0280               | DFCNTRLD  | Destination FIFO Set Count Reload                             |
| 02A2 0284               | DFSRCBREF | Destination FIFO Set Destination Address B Reference Register |
| 02A2 0288               | DFDSTBREF | Destination FIFO Set Destination Address B Reference Register |
| 02A2 028C - 02A2 02FC   | -         | Reserved                                                      |
| 02A2 0300               | DFOPT0    | Destination FIFO Options Register 0                           |
| 02A2 0304               | DFSRC0    | Destination FIFO Source Address Register 0                    |
| 02A2 0308               | DFCNT0    | Destination FIFO Count Register 0                             |
| 02A2 030C               | DFDST0    | Destination FIFO Destination Address Register 0               |
| 02A2 0310               | DFBIDX0   | Destination FIFO BIDX Register 0                              |
| 02A2 0314               | DFMPPRXY0 | Destination FIFO Memory Protection Proxy Register 0           |
| 02A2 0318 - 02A2 033C   | -         | Reserved                                                      |
| 02A2 0340               | DFOPT1    | Destination FIFO Options Register 1                           |
| 02A2 0344               | DFSRC1    | Destination FIFO Source Address Register 1                    |
| 02A2 0348               | DFCNT1    | Destination FIFO Count Register 1                             |
| 02A2 034C               | DFDST1    | Destination FIFO Destination Address Register 1               |
| 02A2 0350               | DFBIDX1   | Destination FIFO BIDX Register 1                              |
| 02A2 0354               | DFMPPRXY1 | Destination FIFO Memory Protection Proxy Register 1           |
| 02A2 0358 - 02A2 037C   | -         | Reserved                                                      |
| 02A2 0380               | DFOPT2    | Destination FIFO Options Register 2                           |
| 02A2 0384               | DFSRC2    | Destination FIFO Source Address Register 2                    |
| 02A2 0388               | DFCNT2    | Destination FIFO Count Register 2                             |
| 02A2 038C               | DFDST2    | Destination FIFO Destination Address Register 2               |
| 02A2 0390               | DFBIDX2   | Destination FIFO BIDX Register 2                              |
| 02A2 0394               | DFMPPRXY2 | Destination FIFO Memory Protection Proxy Register 2           |
| 02A2 0398 - 02A2 03BC   | -         | Reserved                                                      |
| 02A2 03C0               | DFOPT3    | Destination FIFO Options Register 3                           |
| 02A2 03C4               | DFSRC3    | Destination FIFO Source Address Register 3                    |
| 02A2 03C8               | DFCNT3    | Destination FIFO Count Register 3                             |
| 02A2 03CC               | DFDST3    | Destination FIFO Destination Address Register 3               |
| 02A2 03D0               | DFBIDX3   | Destination FIFO BIDX Register 3                              |
| 02A2 03D4               | DFMPPRXY3 | Destination FIFO Memory Protection Proxy Register 3           |
| 02A2 03D8 - 02A2 7FFC   | -         | Reserved                                                      |
| <b>End of Table 7-6</b> |           |                                                               |

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**Table 7-7      EDMA3 Transfer Controller 1 Registers (Part 1 of 2)**

| Hex Address Range     | Acronym   | Register Name                                                 |
|-----------------------|-----------|---------------------------------------------------------------|
| 02A2 8000             | PID       | Peripheral Identification Register                            |
| 02A2 8004             | TCCFG     | EDMA3TC Configuration Register                                |
| 02A2 8008 - 02A2 80FC | -         | Reserved                                                      |
| 02A2 8100             | TCSTAT    | EDMA3TC Channel Status Register                               |
| 02A2 8104 - 02A2 811C | -         | Reserved                                                      |
| 02A2 8120             | ERRSTAT   | Error Register                                                |
| 02A2 8124             | ERREN     | Error Enable Register                                         |
| 02A2 8128             | ERRCLR    | Error Clear Register                                          |
| 02A2 812C             | ERRDET    | Error Details Register                                        |
| 02A2 8130             | ERRCMD    | Error Interrupt Command Register                              |
| 02A2 8134 - 02A2 813C | -         | Reserved                                                      |
| 02A2 8140             | RDRATE    | Read Rate Register                                            |
| 02A2 8144 - 02A2 823C | -         | Reserved                                                      |
| 02A2 8240             | SAOPT     | Source Active Options Register                                |
| 02A2 8244             | SASRC     | Source Active Source Address Register                         |
| 02A2 8248             | SACNT     | Source Active Count Register                                  |
| 02A2 824C             | SADST     | Source Active Destination Address Register                    |
| 02A2 8250             | SABIDX    | Source Active Source B-Index Register                         |
| 02A2 8254             | SAMPPRXY  | Source Active Memory Protection Proxy Register                |
| 02A2 8258             | SACNTRLD  | Source Active Count Reload Register                           |
| 02A2 825C             | SASRCBREF | Source Active Source Address B-Reference Register             |
| 02A2 8260             | SADSTBREF | Source Active Destination Address B-Reference Register        |
| 02A2 8264 - 02A2 827C | -         | Reserved                                                      |
| 02A2 8280             | DFCNTRLD  | Destination FIFO Set Count Reload                             |
| 02A2 8284             | DFSRCBREF | Destination FIFO Set Destination Address B Reference Register |
| 02A2 8288             | DFDSTBREF | Destination FIFO Set Destination Address B Reference Register |
| 02A2 828C - 02A2 82FC | -         | Reserved                                                      |
| 02A2 8300             | DFOPT0    | Destination FIFO Options Register 0                           |
| 02A2 8304             | DFSRC0    | Destination FIFO Source Address Register 0                    |
| 02A2 8308             | DFCNT0    | Destination FIFO Count Register 0                             |
| 02A2 830C             | DFDST0    | Destination FIFO Destination Address Register 0               |
| 02A2 8310             | DFBIDX0   | Destination FIFO BIDX Register 0                              |
| 02A2 8314             | DFMPPRXY0 | Destination FIFO Memory Protection Proxy Register 0           |
| 02A2 8318 - 02A2 833C | -         | Reserved                                                      |
| 02A2 8340             | DFOPT1    | Destination FIFO Options Register 1                           |
| 02A2 8344             | DFSRC1    | Destination FIFO Source Address Register 1                    |
| 02A2 8348             | DFCNT1    | Destination FIFO Count Register 1                             |
| 02A2 834C             | DFDST1    | Destination FIFO Destination Address Register 1               |
| 02A2 8350             | DFBIDX1   | Destination FIFO BIDX Register 1                              |
| 02A2 8354             | DFMPPRXY1 | Destination FIFO Memory Protection Proxy Register 1           |
| 02A2 8358 - 02A2 837C | -         | Reserved                                                      |
| 02A2 8380             | DFOPT2    | Destination FIFO Options Register 2                           |
| 02A2 8384             | DFSRC2    | Destination FIFO Source Address Register 2                    |
| 02A2 8388             | DFCNT2    | Destination FIFO Count Register 2                             |

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**Table 7-7 EDMA3 Transfer Controller 1 Registers (Part 2 of 2)**

| Hex Address Range       | Acronym   | Register Name                                       |
|-------------------------|-----------|-----------------------------------------------------|
| 02A2 838C               | DFDST2    | Destination FIFO Destination Address Register 2     |
| 02A2 8390               | DFBIDX2   | Destination FIFO BIDX Register 2                    |
| 02A2 8394               | DFMPPRXY2 | Destination FIFO Memory Protection Proxy Register 2 |
| 02A2 8398 - 02A2 83BC   | -         | Reserved                                            |
| 02A2 83C0               | DFOPT3    | Destination FIFO Options Register 3                 |
| 02A2 83C4               | DFSRC3    | Destination FIFO Source Address Register 3          |
| 02A2 83C8               | DFCNT3    | Destination FIFO Count Register 3                   |
| 02A2 83CC               | DFDST3    | Destination FIFO Destination Address Register 3     |
| 02A2 83D0               | DFBIDX3   | Destination FIFO BIDX Register 3                    |
| 02A2 83D4               | DFMPPRXY3 | Destination FIFO Memory Protection Proxy Register 3 |
| 02A2 83D8 - 02A2 FFFC   | -         | Reserved                                            |
| <b>End of Table 7-7</b> |           |                                                     |

**Table 7-8 EDMA3 Transfer Controller 2 Registers (Part 1 of 2)**

| Hex Address Range     | Acronym   | Register Name                                                 |
|-----------------------|-----------|---------------------------------------------------------------|
| 02A3 0000             | PID       | Peripheral Identification Register                            |
| 02A3 0004             | TCCFG     | EDMA3TC Configuration Register                                |
| 02A3 0008 - 02A3 00FC | -         | Reserved                                                      |
| 02A3 0100             | TCSTAT    | EDMA3TC Channel Status Register                               |
| 02A3 0104 - 02A3 011C | -         | Reserved                                                      |
| 02A3 0120             | ERRSTAT   | Error Register                                                |
| 02A3 0124             | ERREN     | Error Enable Register                                         |
| 02A3 0128             | ERRCLR    | Error Clear Register                                          |
| 02A3 012C             | ERRDET    | Error Details Register                                        |
| 02A3 0130             | ERRCMD    | Error Interrupt Command Register                              |
| 02A3 0134 - 02A3 013C | -         | Reserved                                                      |
| 02A3 0140             | RDRATE    | Read Rate Register                                            |
| 02A3 0144 - 02A3 023C | -         | Reserved                                                      |
| 02A3 0240             | SAOPT     | Source Active Options Register                                |
| 02A3 0244             | SASRC     | Source Active Source Address Register                         |
| 02A3 0248             | SACNT     | Source Active Count Register                                  |
| 02A3 024C             | SADST     | Source Active Destination Address Register                    |
| 02A3 0250             | SABIDX    | Source Active Source B-Index Register                         |
| 02A3 0254             | SAMPPRXY  | Source Active Memory Protection Proxy Register                |
| 02A3 0258             | SACNTRLD  | Source Active Count Reload Register                           |
| 02A3 025C             | SASRCBREF | Source Active Source Address B-Reference Register             |
| 02A3 0260             | SADSTBREF | Source Active Destination Address B-Reference Register        |
| 02A3 0264 - 02A3 027C | -         | Reserved                                                      |
| 02A3 0280             | DFCNTRLD  | Destination FIFO Set Count Reload                             |
| 02A3 0284             | DFSRCBREF | Destination FIFO Set Destination Address B Reference Register |
| 02A3 0288             | DFDSTBREF | Destination FIFO Set Destination Address B Reference Register |
| 02A3 028C - 02A3 02FC | -         | Reserved                                                      |
| 02A3 0300             | DFOPT0    | Destination FIFO Options Register 0                           |

**Table 7-8      EDMA3 Transfer Controller 2 Registers (Part 2 of 2)**

| Hex Address Range       | Acronym   | Register Name                                       |
|-------------------------|-----------|-----------------------------------------------------|
| 02A3 0304               | DFSRC0    | Destination FIFO Source Address Register 0          |
| 02A3 0308               | DFCNT0    | Destination FIFO Count Register 0                   |
| 02A3 030C               | DFDST0    | Destination FIFO Destination Address Register 0     |
| 02A3 0310               | DFBIDX0   | Destination FIFO BIDX Register 0                    |
| 02A3 0314               | DFMPPRXY0 | Destination FIFO Memory Protection Proxy Register 0 |
| 02A3 0318 - 02A3 033C   | -         | Reserved                                            |
| 02A3 0340               | DFOPT1    | Destination FIFO Options Register 1                 |
| 02A3 0344               | DFSRC1    | Destination FIFO Source Address Register 1          |
| 02A3 0348               | DFCNT1    | Destination FIFO Count Register 1                   |
| 02A3 034C               | DFDST1    | Destination FIFO Destination Address Register 1     |
| 02A3 0350               | DFBIDX1   | Destination FIFO BIDX Register 1                    |
| 02A3 0354               | DFMPPRXY1 | Destination FIFO Memory Protection Proxy Register 1 |
| 02A3 0358 - 02A3 037C   | -         | Reserved                                            |
| 02A3 0380               | DFOPT2    | Destination FIFO Options Register 2                 |
| 02A3 0384               | DFSRC2    | Destination FIFO Source Address Register 2          |
| 02A3 0388               | DFCNT2    | Destination FIFO Count Register 2                   |
| 02A3 038C               | DFDST2    | Destination FIFO Destination Address Register 2     |
| 02A3 0390               | DFBIDX2   | Destination FIFO BIDX Register 2                    |
| 02A3 0394               | DFMPPRXY2 | Destination FIFO Memory Protection Proxy Register 2 |
| 02A3 0398 - 02A3 03BC   | -         | Reserved                                            |
| 02A3 03C0               | DFOPT3    | Destination FIFO Options Register 3                 |
| 02A3 03C4               | DFSRC3    | Destination FIFO Source Address Register 3          |
| 02A3 03C8               | DFCNT3    | Destination FIFO Count Register 3                   |
| 02A3 03CC               | DFDST3    | Destination FIFO Destination Address Register 3     |
| 02A3 03D0               | DFBIDX3   | Destination FIFO BIDX Register 3                    |
| 02A3 03D4               | DFMPPRXY3 | Destination FIFO Memory Protection Proxy Register 3 |
| 02A3 03D8 - 02A3 7FFC   | -         | Reserved                                            |
| <b>End of Table 7-8</b> |           |                                                     |

**Table 7-9      EDMA3 Transfer Controller 3 Registers (Part 1 of 3)**

| Hex Address Range     | Acronym | Register Name                      |
|-----------------------|---------|------------------------------------|
| 02A3 8000             | PID     | Peripheral Identification Register |
| 02A3 8004             | TCCFG   | EDMA3TC Configuration Register     |
| 02A3 8008 - 02A3 80FC | -       | Reserved                           |
| 02A3 8100             | TCSTAT  | EDMA3TC Channel Status Register    |
| 02A3 8104 - 02A3 811C | -       | Reserved                           |
| 02A3 8120             | ERRSTAT | Error Register                     |
| 02A3 8124             | ERREN   | Error Enable Register              |
| 02A3 8128             | ERRCLR  | Error Clear Register               |
| 02A3 812C             | ERRDET  | Error Details Register             |
| 02A3 8130             | ERRCMD  | Error Interrupt Command Register   |
| 02A3 8134 - 02A3 813C | -       | Reserved                           |

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**Table 7-9 EDMA3 Transfer Controller 3 Registers (Part 2 of 3)**

| Hex Address Range     | Acronym   | Register Name                                                 |
|-----------------------|-----------|---------------------------------------------------------------|
| 02A3 8140             | RDRATE    | Read Rate Register                                            |
| 02A3 8144 - 02A3 823C | -         | Reserved                                                      |
| 02A3 8240             | SAOPT     | Source Active Options Register                                |
| 02A3 8244             | SASRC     | Source Active Source Address Register                         |
| 02A3 8248             | SACNT     | Source Active Count Register                                  |
| 02A3 824C             | SADST     | Source Active Destination Address Register                    |
| 02A3 8250             | SABIDX    | Source Active Source B-Index Register                         |
| 02A3 8254             | SAMPPRXY  | Source Active Memory Protection Proxy Register                |
| 02A3 8258             | SACNTRLD  | Source Active Count Reload Register                           |
| 02A3 825C             | SASRCBREF | Source Active Source Address B-Reference Register             |
| 02A3 8260             | SADSTBREF | Source Active Destination Address B-Reference Register        |
| 02A3 8264 - 02A3 827C | -         | Reserved                                                      |
| 02A3 8280             | DFCNTRLD  | Destination FIFO Set Count Reload                             |
| 02A3 8284             | DFSRCBREF | Destination FIFO Set Destination Address B Reference Register |
| 02A3 8288             | DFDSTBREF | Destination FIFO Set Destination Address B Reference Register |
| 02A3 828C - 02A3 82FC | -         | Reserved                                                      |
| 02A3 8300             | DFOPT0    | Destination FIFO Options Register 0                           |
| 02A3 8304             | DFSRC0    | Destination FIFO Source Address Register 0                    |
| 02A3 8308             | DFCNT0    | Destination FIFO Count Register 0                             |
| 02A3 830C             | DFDST0    | Destination FIFO Destination Address Register 0               |
| 02A3 8310             | DFBIDX0   | Destination FIFO BIDX Register 0                              |
| 02A3 8314             | DFMPPRXY0 | Destination FIFO Memory Protection Proxy Register 0           |
| 02A3 8318 - 02A3 833C | -         | Reserved                                                      |
| 02A3 8340             | DFOPT1    | Destination FIFO Options Register 1                           |
| 02A3 8344             | DFSRC1    | Destination FIFO Source Address Register 1                    |
| 02A3 8348             | DFCNT1    | Destination FIFO Count Register 1                             |
| 02A3 834C             | DFDST1    | Destination FIFO Destination Address Register 1               |
| 02A3 8350             | DFBIDX1   | Destination FIFO BIDX Register 1                              |
| 02A3 8354             | DFMPPRXY1 | Destination FIFO Memory Protection Proxy Register 1           |
| 02A3 8358 - 02A3 837C | -         | Reserved                                                      |
| 02A3 8380             | DFOPT2    | Destination FIFO Options Register 2                           |
| 02A3 8384             | DFSRC2    | Destination FIFO Source Address Register 2                    |
| 02A3 8388             | DFCNT2    | Destination FIFO Count Register 2                             |
| 02A3 838C             | DFDST2    | Destination FIFO Destination Address Register 2               |
| 02A3 8390             | DFBIDX2   | Destination FIFO BIDX Register 2                              |
| 02A3 8394             | DFMPPRXY2 | Destination FIFO Memory Protection Proxy Register 2           |
| 02A3 8398 - 02A3 83BC | -         | Reserved                                                      |
| 02A3 83C0             | DFOPT3    | Destination FIFO Options Register 3                           |
| 02A3 83C4             | DFSRC3    | Destination FIFO Source Address Register 3                    |
| 02A3 83C8             | DFCNT3    | Destination FIFO Count Register 3                             |
| 02A3 83CC             | DFDST3    | Destination FIFO Destination Address Register 3               |
| 02A3 83D0             | DFBIDX3   | Destination FIFO BIDX Register 3                              |

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**Table 7-9      EDMA3 Transfer Controller 3 Registers (Part 3 of 3)**

| Hex Address Range       | Acronym   | Register Name                                       |
|-------------------------|-----------|-----------------------------------------------------|
| 02A3 83D4               | DFMPPRXY3 | Destination FIFO Memory Protection Proxy Register 3 |
| 02A3 83D8 - 02A3 FFFC   | -         | Reserved                                            |
| <b>End of Table 7-9</b> |           |                                                     |

**Table 7-10      EDMA3 Transfer Controller 4 Registers (Part 1 of 2)**

| Hex Address Range     | Acronym   | Register Name                                                 |
|-----------------------|-----------|---------------------------------------------------------------|
| 02A4 0000             | PID       | Peripheral Identification Register                            |
| 02A4 0004             | TCCFG     | EDMA3TC Configuration Register                                |
| 02A4 0008 - 02A4 00FC | -         | Reserved                                                      |
| 02A4 0100             | TCSTAT    | EDMA3TC Channel Status Register                               |
| 02A4 0104 - 02A4 011C | -         | Reserved                                                      |
| 02A4 0120             | ERRSTAT   | Error Register                                                |
| 02A4 0124             | ERREN     | Error Enable Register                                         |
| 02A4 0128             | ERRCLR    | Error Clear Register                                          |
| 02A4 012C             | ERRDET    | Error Details Register                                        |
| 02A4 0130             | ERRCMD    | Error Interrupt Command Register                              |
| 02A4 0134 - 02A4 013C | -         | Reserved                                                      |
| 02A4 0140             | RDRATE    | Read Rate Register                                            |
| 02A4 0144 - 02A4 023C | -         | Reserved                                                      |
| 02A4 0240             | SAOPT     | Source Active Options Register                                |
| 02A4 0244             | SASRC     | Source Active Source Address Register                         |
| 02A4 0248             | SACNT     | Source Active Count Register                                  |
| 02A4 024C             | SADST     | Source Active Destination Address Register                    |
| 02A4 0250             | SABIDX    | Source Active Source B-Index Register                         |
| 02A4 0254             | SAMPPRXY  | Source Active Memory Protection Proxy Register                |
| 02A4 0258             | SACNTRLD  | Source Active Count Reload Register                           |
| 02A4 025C             | SASRCBREF | Source Active Source Address B-Reference Register             |
| 02A4 0260             | SADSTBREF | Source Active Destination Address B-Reference Register        |
| 02A4 0264 - 02A4 027C | -         | Reserved                                                      |
| 02A4 0280             | DFCNTRLD  | Destination FIFO Set Count Reload                             |
| 02A4 0284             | DFSRCBREF | Destination FIFO Set Destination Address B Reference Register |
| 02A4 0288             | DFDSTBREF | Destination FIFO Set Destination Address B Reference Register |
| 02A4 028C - 02A4 02FC | -         | Reserved                                                      |
| 02A4 0300             | DFOPT0    | Destination FIFO Options Register 0                           |
| 02A4 0304             | DFSRC0    | Destination FIFO Source Address Register 0                    |
| 02A4 0308             | DFCNT0    | Destination FIFO Count Register 0                             |
| 02A4 030C             | DFDST0    | Destination FIFO Destination Address Register 0               |
| 02A4 0310             | DFBIDX0   | Destination FIFO BIDX Register 0                              |
| 02A4 0314             | DFMPPRXY0 | Destination FIFO Memory Protection Proxy Register 0           |
| 02A4 0318 - 02A4 033C | -         | Reserved                                                      |
| 02A4 0340             | DFOPT1    | Destination FIFO Options Register 1                           |
| 02A4 0344             | DFSRC1    | Destination FIFO Source Address Register 1                    |
| 02A4 0348             | DFCNT1    | Destination FIFO Count Register 1                             |

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**Table 7-10 EDMA3 Transfer Controller 4 Registers (Part 2 of 2)**

| Hex Address Range        | Acronym   | Register Name                                       |
|--------------------------|-----------|-----------------------------------------------------|
| 02A4 034C                | DFDST1    | Destination FIFO Destination Address Register 1     |
| 02A4 0350                | DFBIDX1   | Destination FIFO BIDX Register 1                    |
| 02A4 0354                | DFMPPRXY1 | Destination FIFO Memory Protection Proxy Register 1 |
| 02A4 0358 - 02A4 037C    | -         | Reserved                                            |
| 02A4 0380                | DFOPT2    | Destination FIFO Options Register 2                 |
| 02A4 0384                | DFSRC2    | Destination FIFO Source Address Register 2          |
| 02A4 0388                | DFCNT2    | Destination FIFO Count Register 2                   |
| 02A4 038C                | DFDST2    | Destination FIFO Destination Address Register 2     |
| 02A4 0390                | DFBIDX2   | Destination FIFO BIDX Register 2                    |
| 02A4 0394                | DFMPPRXY2 | Destination FIFO Memory Protection Proxy Register 2 |
| 02A4 0398 - 02A4 03BC    | -         | Reserved                                            |
| 02A4 03C0                | DFOPT3    | Destination FIFO Options Register 3                 |
| 02A4 03C4                | DFSRC3    | Destination FIFO Source Address Register 3          |
| 02A4 03C8                | DFCNT3    | Destination FIFO Count Register 3                   |
| 02A4 03CC                | DFDST3    | Destination FIFO Destination Address Register 3     |
| 02A4 03D0                | DFBIDX3   | Destination FIFO BIDX Register 3                    |
| 02A4 03D4                | DFMPPRXY3 | Destination FIFO Memory Protection Proxy Register 3 |
| 02A4 03D8 - 02A4 7FFC    | -         | Reserved                                            |
| <b>End of Table 7-10</b> |           |                                                     |

**Table 7-11 EDMA3 Transfer Controller 5 Registers (Part 1 of 2)**

| Hex Address Range     | Acronym   | Register Name                                     |
|-----------------------|-----------|---------------------------------------------------|
| 02A4 8000             | PID       | Peripheral Identification Register                |
| 02A4 8004             | TCCFG     | EDMA3TC Configuration Register                    |
| 02A4 8008 - 02A4 80FC | -         | Reserved                                          |
| 02A4 8100             | TCSTAT    | EDMA3TC Channel Status Register                   |
| 02A4 8104 - 02A4 811C | -         | Reserved                                          |
| 02A4 8120             | ERRSTAT   | Error Register                                    |
| 02A4 8124             | ERREN     | Error Enable Register                             |
| 02A4 8128             | ERRCLR    | Error Clear Register                              |
| 02A4 812C             | ERRDET    | Error Details Register                            |
| 02A4 8130             | ERRCMD    | Error Interrupt Command Register                  |
| 02A4 8134 - 02A4 813C | -         | Reserved                                          |
| 02A4 8140             | RDRATE    | Read Rate Register                                |
| 02A4 8144 - 02A4 823C | -         | Reserved                                          |
| 02A4 8240             | SAOPT     | Source Active Options Register                    |
| 02A4 8244             | SASRC     | Source Active Source Address Register             |
| 02A4 8248             | SACNT     | Source Active Count Register                      |
| 02A4 824C             | SADST     | Source Active Destination Address Register        |
| 02A4 8250             | SABIDX    | Source Active Source B-Index Register             |
| 02A4 8254             | SAMPPrXY  | Source Active Memory Protection Proxy Register    |
| 02A4 8258             | SACNTRLD  | Source Active Count Reload Register               |
| 02A4 825C             | SASRCBREF | Source Active Source Address B-Reference Register |

**Table 7-11 EDMA3 Transfer Controller 5 Registers (Part 2 of 2)**

| Hex Address Range        | Acronym   | Register Name                                                 |
|--------------------------|-----------|---------------------------------------------------------------|
| 02A4 8260                | SADSTBREF | Source Active Destination Address B-Reference Register        |
| 02A4 8264 - 02A4 827C    | -         | Reserved                                                      |
| 02A4 8280                | DFCNTRLD  | Destination FIFO Set Count Reload                             |
| 02A4 8284                | DFSRCBREF | Destination FIFO Set Destination Address B Reference Register |
| 02A4 8288                | DFDSTBREF | Destination FIFO Set Destination Address B Reference Register |
| 02A4 828C - 02A4 82FC    | -         | Reserved                                                      |
| 02A4 8300                | DFOPT0    | Destination FIFO Options Register 0                           |
| 02A4 8304                | DFSRC0    | Destination FIFO Source Address Register 0                    |
| 02A4 8308                | DFCNT0    | Destination FIFO Count Register 0                             |
| 02A4 830C                | DFDST0    | Destination FIFO Destination Address Register 0               |
| 02A4 8310                | DFBIDX0   | Destination FIFO BIDX Register 0                              |
| 02A4 8314                | DFMPPRXY0 | Destination FIFO Memory Protection Proxy Register 0           |
| 02A4 8318 - 02A4 833C    | -         | Reserved                                                      |
| 02A4 8340                | DFOPT1    | Destination FIFO Options Register 1                           |
| 02A4 8344                | DFSRC1    | Destination FIFO Source Address Register 1                    |
| 02A4 8348                | DFCNT1    | Destination FIFO Count Register 1                             |
| 02A4 834C                | DFDST1    | Destination FIFO Destination Address Register 1               |
| 02A4 8350                | DFBIDX1   | Destination FIFO BIDX Register 1                              |
| 02A4 8354                | DFMPPRXY1 | Destination FIFO Memory Protection Proxy Register 1           |
| 02A4 8358 - 02A4 837C    | -         | Reserved                                                      |
| 02A4 8380                | DFOPT2    | Destination FIFO Options Register 2                           |
| 02A4 8384                | DFSRC2    | Destination FIFO Source Address Register 2                    |
| 02A4 8388                | DFCNT2    | Destination FIFO Count Register 2                             |
| 02A4 838C                | DFDST2    | Destination FIFO Destination Address Register 2               |
| 02A4 8390                | DFBIDX2   | Destination FIFO BIDX Register 2                              |
| 02A4 8394                | DFMPPRXY2 | Destination FIFO Memory Protection Proxy Register 2           |
| 02A4 8398 - 02A4 83BC    | -         | Reserved                                                      |
| 02A4 83C0                | DFOPT3    | Destination FIFO Options Register 3                           |
| 02A4 83C4                | DFSRC3    | Destination FIFO Source Address Register 3                    |
| 02A4 83C8                | DFCNT3    | Destination FIFO Count Register 3                             |
| 02A4 83CC                | DFDST3    | Destination FIFO Destination Address Register 3               |
| 02A4 83D0                | DFBIDX3   | Destination FIFO BIDX Register 3                              |
| 02A4 83D4                | DFMPPRXY3 | Destination FIFO Memory Protection Proxy Register 3           |
| 02A4 83D8 - 02A4 FFFC    | -         | Reserved                                                      |
| <b>End of Table 7-11</b> |           |                                                               |

## 7.5 Interrupts

### 7.5.1 Interrupt Sources and Interrupt Controller

The CPU interrupts on the C6457 device are configured through the C64x+ Megamodule Interrupt Controller. The interrupt controller allows for up to 128 system events to be programmed to any of the twelve CPU interrupt inputs (CPUINT4 - CPUINT15), the CPU exception input (EXCEP), or the advanced emulation logic. The 128 system events consist of both internally-generated events (within the megamodule) and chip-level events. [Table 7-12](#) shows the mapping of system events. For more information on the Interrupt Controller, see the *TMS320C64x+ Megamodule Reference Guide* (literature number [SPRU871](#)).

**Table 7-12 TMS320C6457 System Event Mapping (Part 1 of 3)**

| Event Number      | Interrupt Event | Description                                                                                                                                         |
|-------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 <sup>(1)</sup>  | EVT0            | Output of event combiner 0 in interrupt controller, for events 1 - 31.                                                                              |
| 1 <sup>(1)</sup>  | EVT1            | Output of event combiner 1 in interrupt controller, for events 32 - 63.                                                                             |
| 2 <sup>(1)</sup>  | EVT2            | Output of event combiner 2 in interrupt controller, for events 64 - 95.                                                                             |
| 3 <sup>(1)</sup>  | EVT3            | Output of event combiner 3 in interrupt controller, for events 96 - 127.                                                                            |
| 4 - 8             | Reserved        | Reserved. These system events are not connected and, therefore, not used.                                                                           |
| 9 <sup>(1)</sup>  | EMU_DTDMA       | EMU interrupt for: <ul style="list-style-type: none"> <li>• Host scan access</li> <li>• DTDMA transfer complete</li> <li>• AET interrupt</li> </ul> |
| 10                | None            | This system event is not connected and, therefore, not used.                                                                                        |
| 11 <sup>(1)</sup> | EMU_RTDXRX      | EMU real-time data exchange (RTDX) receive complete                                                                                                 |
| 12 <sup>(1)</sup> | EMU_RTDXTX      | EMU RTDX transmit complete                                                                                                                          |
| 13 <sup>(1)</sup> | IDMA0           | IDMA channel 0 interrupt                                                                                                                            |
| 14 <sup>(1)</sup> | IDMA1           | IDMA channel 1 interrupt                                                                                                                            |
| 15                | DSPINT          | HPI-to-DSP interrupt                                                                                                                                |
| 16                | I2CINT          | I <sup>2</sup> C interrupt                                                                                                                          |
| 17                | MACINT          | Ethernet MAC interrupt                                                                                                                              |
| 18                | AEASYNCERR      | EMIFA error interrupt                                                                                                                               |
| 19                | Reserved        | Reserved. This system event is not connected and, therefore, not used.                                                                              |
| 20                | INTDST0         | RapidIO interrupt 0                                                                                                                                 |
| 21                | INTDST1         | RapidIO interrupt 1                                                                                                                                 |
| 22                | INTDST2         | RapidIO interrupt 2                                                                                                                                 |
| 23                | INTDST3         | RapidIO interrupt 3                                                                                                                                 |
| 24                | EDMA3CC_GINT    | EDMA3 channel global completion interrupt                                                                                                           |
| 25                | MACRXINT        | Ethernet MAC receive interrupt                                                                                                                      |
| 26                | MACTXINT        | Ethernet MAC transmit interrupt                                                                                                                     |
| 27                | MACTHRESH       | Ethernet MAC receive threshold interrupt                                                                                                            |
| 28                | INTDST4         | RapidIO interrupt 4                                                                                                                                 |
| 29                | INTDST5         | RapidIO interrupt 5                                                                                                                                 |
| 30                | INTDST6         | RapidIO interrupt 6                                                                                                                                 |
| 31                | Reserved        | Reserved. These system events are not connected and, therefore, not used.                                                                           |
| 32                | VCP2_INT        | VCP2 error interrupt                                                                                                                                |
| 33                | TCP2A_INT       | TCP2_A error interrupt                                                                                                                              |
| 34                | TCP2B_INT       | TCP2_B error interrupt                                                                                                                              |
| 35                | Reserved        | Reserved. These system events are not connected and, therefore, not used.                                                                           |
| 36                | UINT            | UTOPIA interrupt                                                                                                                                    |



**Table 7-12 TMS320C6457 System Event Mapping (Part 2 of 3)**

| Event Number | Interrupt Event | Description                                                               |
|--------------|-----------------|---------------------------------------------------------------------------|
| 37 - 39      | Reserved        | Reserved. These system events are not connected and, therefore, not used. |
| 40           | RINT0           | McBSP0 receive interrupt                                                  |
| 41           | XINT0           | McBSP0 transmit interrupt                                                 |
| 42           | RINT1           | McBSP1 receive interrupt                                                  |
| 43           | XINT1           | McBSP1 transmit interrupt                                                 |
| 44 - 50      | Reserved        | Reserved. Do not use.                                                     |
| 51           | GPINT0          | GPIO interrupt                                                            |
| 52           | GPINT1          | GPIO interrupt                                                            |
| 53           | GPINT2          | GPIO interrupt                                                            |
| 54           | GPINT3          | GPIO interrupt                                                            |
| 55           | GPINT4          | GPIO interrupt                                                            |
| 56           | GPINT5          | GPIO interrupt                                                            |
| 57           | GPINT6          | GPIO interrupt                                                            |
| 58           | GPINT7          | GPIO interrupt                                                            |
| 59           | GPINT8          | GPIO interrupt                                                            |
| 60           | GPINT9          | GPIO interrupt                                                            |
| 61           | GPINT10         | GPIO interrupt                                                            |
| 62           | GPINT11         | GPIO interrupt                                                            |
| 63           | GPINT12         | GPIO interrupt                                                            |
| 64           | GPINT13         | GPIO interrupt                                                            |
| 65           | GPINT14         | GPIO interrupt                                                            |
| 66           | GPINT15         | GPIO interrupt                                                            |
| 67           | TINTLO0         | Timer 0 lower counter interrupt                                           |
| 68           | TINTHI0         | Timer 0 higher counter interrupt                                          |
| 69           | TINTLO1         | Timer 1 lower counter interrupt                                           |
| 70           | TINTHI1         | Timer 1 higher counter interrupt                                          |
| 71           | EDMA3CC_INT0    | EDMA3CC completion interrupt - Mask0                                      |
| 72           | EDMA3CC_INT1    | EDMA3CC completion interrupt - Mask1                                      |
| 73           | EDMA3CC_INT2    | EDMA3CC completion interrupt - Mask2                                      |
| 74           | EDMA3CC_INT3    | EDMA3CC completion interrupt - Mask3                                      |
| 75           | EDMA3CC_INT4    | EDMA3CC completion interrupt - Mask4                                      |
| 76           | EDMA3CC_INT5    | EDMA3CC completion interrupt - Mask5                                      |
| 77           | EDMA3CC_INT6    | EDMA3CC completion interrupt - Mask6                                      |
| 78           | EDMA3CC_INT7    | EDMA3CC completion interrupt - Mask7                                      |
| 79           | EDMA3CC_ERRINT  | EDMA3CC error interrupt                                                   |
| 80           | Reserved        | Reserved. This system event is not connected and, therefore, not used.    |
| 81           | EDMA3TC0_ERRINT | EDMA3TC0 error interrupt                                                  |
| 82           | EDMA3TC1_ERRINT | EDMA3TC1 error interrupt                                                  |
| 83           | EDMA3TC2_ERRINT | EDMA3TC2 error interrupt                                                  |
| 84           | EDMA3TC3_ERRINT | EDMA3TC3 error interrupt                                                  |
| 85           | EDMA3CC_AET     | EDMA3CC AET Event                                                         |
| 86           | EDMA3TC4_ERRINT | EDMA3TC4 error interrupt                                                  |
| 87           | EDMA3TC5_ERRINT | EDMA3TC5 error interrupt                                                  |
| 88 - 93      | Reserved        | Reserved. These system events are not connected and, therefore, not used. |

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**Table 7-12 TMS320C6457 System Event Mapping (Part 3 of 3)**

| Event Number             | Interrupt Event | Description                                                               |
|--------------------------|-----------------|---------------------------------------------------------------------------|
| 94                       | ETBOVFLINT      | Overflow condition occurred in ETB                                        |
| 95                       | ETBUNFLINT      | Underflow condition occurred in ETB                                       |
| 96 <sup>(1)</sup>        | INTERR          | Interrupt Controller dropped CPU interrupt event                          |
| 97 <sup>(1)</sup>        | EMC_IDMAERR     | EMC invalid IDMA parameters                                               |
| 98 - 99                  | Reserved        | Reserved. These system events are not connected and, therefore, not used. |
| 100 <sup>(1)</sup>       | EFIINTA         | EFI interrupt from side A                                                 |
| 101 <sup>(1)</sup>       | EFIINTB         | EFI interrupt from side B                                                 |
| 102 - 112                | Reserved        | Reserved. These system events are not connected and, therefore, not used. |
| 113 <sup>(1)</sup>       | L1P_ED1         | L1P single bit error detected during DMA read                             |
| 114 - 115                | Reserved        | Reserved. These system events are not connected and, therefore, not used. |
| 116 <sup>(1)</sup>       | L2_ED1          | L2 single bit error detected                                              |
| 117 <sup>(1)</sup>       | L2_ED2          | L2 two bit error detected                                                 |
| 118 <sup>(1)</sup>       | PDC_INT         | Powerdown sleep interrupt                                                 |
| 119 <sup>(1)</sup>       | SYS_CMPA        | CPU memory protection fault                                               |
| 120 <sup>(1)</sup>       | L1P_CMPA        | L1P CPU memory protection fault                                           |
| 121 <sup>(1)</sup>       | L1P_DMPA        | L1P DMA memory protection fault                                           |
| 122 <sup>(1)</sup>       | L1D_CMPA        | L1D CPU memory protection fault                                           |
| 123 <sup>(1)</sup>       | L1D_DMPA        | L1D DMA memory protection fault                                           |
| 124 <sup>(1)</sup>       | L2_CMPA         | L2 CPU memory protection fault                                            |
| 125 <sup>(1)</sup>       | L2_DMPA         | L2 DMA memory protection fault                                            |
| 126 <sup>(1)</sup>       | IDMA_CMPA       | IDMA CPU memory protection fault                                          |
| 127 <sup>(1)</sup>       | IDMA_BUSERR     | IDMA bus error interrupt                                                  |
| <b>End of Table 7-12</b> |                 |                                                                           |

<sup>1</sup> This system event is generated from within the C64x+ megamodule.

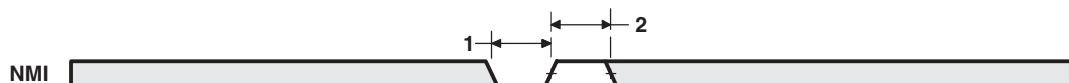
## 7.5.2 External Interrupts Electrical Data/Timing

**Table 7-13 Timing Requirements for External Interrupts<sup>(1)</sup>**  
(see Figure 7-8)

| No.                      |                                                     | Min | Max | Unit |
|--------------------------|-----------------------------------------------------|-----|-----|------|
| 1                        | $t_{w(NMIL)}$ Width of the NMI interrupt pulse low  | 6P  |     | ns   |
| 2                        | $t_{w(NMIH)}$ Width of the NMI interrupt pulse high | 6P  |     | ns   |
| <b>End of Table 7-13</b> |                                                     |     |     |      |

<sup>1</sup> P = 1/CPU clock frequency in ns. For example, when running parts at 1000 MHz, use P = 1 ns.

**Figure 7-8 NMI Interrupt Timing**



## 7.6 Reset Controller

The reset controller detects the different type of resets supported on the TMS320C6457 device and manages the distribution of those resets throughout the device.

The C6457 device has several types of resets:

- Power-on reset
- Warm reset
- System reset
- CPU reset

Table 7-14 explains further the types of reset, the reset initiator, and the effects of each reset on the device. For more information on the effects of each reset on the PLL controllers and their clocks, see Section 7.6.7 “Reset Electrical Data/Timing” on page 128.

**Table 7-14 Reset Types**

| Type            | Initiator                                           | Effect(s)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----------------|-----------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Power-on Reset  | $\overline{\text{POR}}$ pin                         | Resets the entire chip including the test and emulation logic. The device configuration pins are latched only during POR.                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Warm Reset      | $\overline{\text{RESET}}$ pin                       | Resets everything except for the test and emulation logic and PLL2. The emulator stays alive during warm reset. The device configuration pins are not re-latched. DDR2 memory contents will be preserved if the user places the DDR2 SDRAM in “Self-Refresh” mode before starting a Warm Reset sequence.                                                                                                                                                                                                                                                                             |
| System Reset    | Emulator<br>Serial RapidIO<br>PLLCTL <sup>(1)</sup> | System reset, by default, behaves as hard reset, but can be configured as soft reset if initiated by Serial RapidIO or PLLCTL. Emulator-initiated reset is always a hard reset.<br>• Hard reset effects are the same as those of a warm reset.<br>• Soft reset means external memory contents can be maintained, it does not affect the clock logic, or the power control logic of the peripherals. See 7.6.3 “System Reset” on page 124 for more details.<br>A system reset does not reset the test and emulation circuitry. The device configuration pins are also not re-latched. |
| CPU Local Reset | Watchdog Timer                                      | CPU local reset.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

**End of Table 7-14**

<sup>1</sup> All masters in the device have access to the PLLCTL registers.

### 7.6.1 Power-on Reset ( $\overline{\text{POR}}$ Pin)

Power-on reset is initiated by the  $\overline{\text{POR}}$  pin and is used to reset the entire device, including the test and emulation logic. Power-on reset is also referred to as a cold reset because the device usually goes through a power-up cycle. During power-up, the  $\overline{\text{POR}}$  pin must be asserted (driven low) until the power supplies have reached their normal operating conditions. Note that a device power-up cycle is not required to initiate a power-on reset. For power-on reset, the main PLL controller comes up in bypass mode and the PLL is not enabled. Other resets do not affect the state of the PLL or the dividers in the PLL controller. For the secondary PLL, the PLL is enabled and always clocking when  $\overline{\text{POR}}$  is not asserted.

The following sequence must be followed during a power-on reset:

1. Wait for all power supplies to reach normal operating conditions while keeping the  $\overline{\text{POR}}$  pin asserted (driven low). While  $\overline{\text{POR}}$  is asserted, all pins except  $\overline{\text{RESETSTAT}}$  will be set to high-impedance. After the  $\overline{\text{POR}}$  pin is de-asserted (driven high), all Z group pins, low group pins, and high group pins are set to their reset state and will remain at their reset state until otherwise configured by their respective peripheral. All peripherals that are power managed, are disabled after a Power-on Reset and must be enabled through the Device State Control registers (for more details, see Section 3.2 “Peripheral Selection After Device Reset” on page 60).
2. Clocks are reset, and they are propagated throughout the chip to reset any logic that was using reset synchronously. All logic is now reset and  $\overline{\text{RESETSTAT}}$  will be driven low indicating that the device is in reset.
3.  $\overline{\text{POR}}$  must be held active until all supplies on the board are stable then for at least an additional 100  $\mu\text{s}$  + 2000 CLKIN2 cycles.

4. The  $\overline{\text{POR}}$  pin can now be de-asserted. Reset sampled pin values are latched at this point. PLL2 is taken out of reset and begins its locking sequence, and all power-on device initialization also begins.
5. After device initialization is complete, the  $\overline{\text{RESETSTAT}}$  pin is de-asserted (driven high). By this time, PLL2 has already completed its locking sequence and is outputting a valid clock. The system clocks of both PLL controllers are allowed to finish their current cycles and then paused for 10 cycles of their respective system reference clocks. After the pause, the system clocks are restarted at their default divide by settings.
6. The device is now out of reset and device execution begins as dictated by the selected boot mode.



**Note**—To most of the device, reset is de-asserted only when the  $\overline{\text{POR}}$  and  $\overline{\text{RESET}}$  pins are both de-asserted (driven high). Therefore, in the sequence described above, if the  $\overline{\text{RESET}}$  pin is held low past the low period of the  $\overline{\text{POR}}$  pin, most of the device will remain in reset. The  $\overline{\text{RESET}}$  pin should not be tied together with the  $\overline{\text{POR}}$  pin.

## 7.6.2 Warm Reset (RESET Pin)

A warm reset will reset everything on the device except the PLLs, PLL controller, test, and emulation logic.  $\overline{\text{POR}}$  should also remain de-asserted during this time.

The following sequence must be followed during a warm reset:

1. The  $\overline{\text{RESET}}$  pin is pulled active low for a minimum of 24 CLKIN1 cycles. During this time the  $\overline{\text{RESET}}$  signal is able to propagate to all modules (except those specifically mentioned above). All I/O are Hi-Z for modules affected by  $\overline{\text{RESET}}$ , to prevent off-chip contention during the warm reset.
2. Once all logic is reset,  $\overline{\text{RESETSTAT}}$  is driven active to denote that the device is in reset.
3. The  $\overline{\text{RESET}}$  pin can now be released. A minimal device initialization begins to occur. Note that configuration pins are not re-latched and clocking is unaffected within the device.
4. After device initialization is complete, the  $\overline{\text{RESETSTAT}}$  pin is de-asserted (driven high).



**Note**—The  $\overline{\text{POR}}$  pin should be held inactive (high) throughout the warm reset sequence. Otherwise, if  $\overline{\text{POR}}$  is activated (brought low), the minimum  $\overline{\text{POR}}$  pulse width must be met. The  $\overline{\text{RESET}}$  pin should not be tied together with the  $\overline{\text{POR}}$  pin.



**Note**—The DDR2 SDRAM contents will also be preserved if the user places the SDRAM into *Self-Refresh* mode before starting a Warm Reset sequence. Please see the *TMS320C6457 DSP DDR2 Memory Controller User's Guide* (literature number [SPRUGK5](#)).

## 7.6.3 System Reset

In a System Reset, test and emulation logic are unaffected. The device configuration pins are also not re-latched. System reset can be initiated by the emulator or Serial RapidIO or by the PLLCTL:

- **Emulator Initiated System Reset:** The emulator initiated System Reset is always a Hard Reset. The effects of a Hard Reset are the same as a Warm Reset (defined in section 7.6.2 “[Warm Reset \(RESET Pin\)](#)” on page 124).
- **Serial RapidIO Initiated System Reset:** The Serial Rapid IO initiated System Reset can be configured by the RSTCFG register (section 7.6.6.3 “[Reset Configuration Register](#)” on page 127) as a Soft Reset or Hard Reset. For more information on the Serial RapidIO initiated system reset, see Section 4.2 of the *TMS320C6457 DSP Serial RapidIO (SRIO) User's Guide* (literature number [SPRUGK4](#)).
- **PLLCTL Initiated System Reset:** The PLLCTL module can initiate a System Reset using the RSTCTRL register; see section 7.6.6.2 “[Software Reset Control Register](#)” on page 127. The PLLCTL initiated System Reset can be configured by the RSTCFG register (section 7.6.6.3 “[Reset Configuration Register](#)” on page 127) as a Soft Reset or Hard Reset.

In the case of a Soft Reset, the clock logic or the power control logic of the peripherals are not affected, and, therefore, the enabled/disabled state of the peripherals is not affected. The following external memory contents are maintained during a soft reset:

- **DDR2 Memory Controller:** The DDR2 Memory Controller registers are *not* reset. In addition, the DDR2 SDRAM memory content is retained if the user places the DDR2 SDRAM in self-refresh mode before invoking the soft reset.
- **EMIFA:** The contents of the memory connected to the EMIFA are retained. The EMIFA registers are *not* reset.

During a soft reset, the following happens:

1. The  $\overline{\text{RESETSTAT}}$  pin goes low to indicate an internal reset is being generated. The reset is allowed to propagate through the system. Internal system clocks are not affected. PLLs also remain locked.
2. After device initialization is complete, the  $\overline{\text{RESETSTAT}}$  pin is deasserted (driven high). In addition, the PLL controllers pause their system clocks for about 10 cycles.

At this point:

- › The state of the peripherals before the soft reset is not changed. For example, if McBSP0 was in the enabled state before soft reset, it will remain in the enabled state after soft reset.
- › The I/O pins are controlled as dictated by the DEVSTAT register.
- › The DDR2 Memory Controller and EMIFA registers retain their previous values. Only the DDR2 Memory Controller and EMIFA state machines are reset by the soft reset.
- › The PLL controllers are operating in the mode prior to soft reset. System clocks are unaffected.

The boot sequence is started after the system clocks are restarted. Since the configuration pins (including the BOOTMODE[3:0] pins) are not latched with a System Reset, the previous values, as shown in the DEVSTAT register, are used to select the boot mode.

#### 7.6.4 CPU Reset

Timer1 can provide a local CPU reset if it is set up in watchdog mode.

#### 7.6.5 Reset Priority

If any of the above reset sources occur simultaneously, the PLLCTL processes only the highest priority reset request. The reset request priorities are as follows (high to low):

- Power-on reset
- Warm reset and system reset

#### 7.6.6 Reset Controller Register

There are three reset controller registers: Reset Type Status (RSTYPE) register (029A 00E4), Software Reset Control (RSTCTRL) register (029A 00E8), and Reset Configuration (RSTCFG) register (029A 00EC). All three registers fall in the same memory range as the PLL1 Controller registers [029A 0000 - 029A 0170] (see Table 7-26 “[PLL1 Controller Registers \(Including Reset Controller\)](#)” on page 133).

### 7.6.6.1 Reset Type Status Register

The reset type status (RSTYPE) register latches the cause of the last reset. If multiple reset sources occur simultaneously, this register latches the highest priority reset source. The Reset Type Status register is shown in Table 7-15 and described in Table 7-16.

**Table 7-15 Reset Type Status Register (RSTYPE)**

| Address - 029A 00E4h |          |    |    |         |          |    |    |         |          |    |    |    |    |            |      |     |
|----------------------|----------|----|----|---------|----------|----|----|---------|----------|----|----|----|----|------------|------|-----|
| Bit                  | 31       | 30 | 29 | 28      | 27       | 26 | 25 | 24      | 23       | 22 | 21 | 20 | 19 | 18         | 17   | 16  |
| Acronym              | Reserved |    |    | EMU-RST | Reserved |    |    |         |          |    |    |    |    |            |      |     |
| Reset <sup>(1)</sup> | R-0      |    |    | R-0     | R-0      |    |    |         |          |    |    |    |    |            |      |     |
| Bit                  | 15       | 14 | 13 | 12      | 11       | 10 | 9  | 8       | 7        | 6  | 5  | 4  | 3  | 2          | 1    | 0   |
| Acronym              | Reserved |    |    |         |          |    |    | SRIORST | Reserved |    |    |    |    | PLLCTRLRST | WRST | POR |
| Reset <sup>(1)</sup> | R-0      |    |    |         |          |    |    | R-0     | R-0      |    |    |    |    | R-0        | R-0  | R-0 |

<sup>1</sup> R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-16 Reset Type Status Register (RSTYPE) Field Descriptions**

| Bit   | Acronym   | Description                                                                                                               |
|-------|-----------|---------------------------------------------------------------------------------------------------------------------------|
| 31:29 | Reserved  | Reserved. Read only. Always reads as 0. Writes have no effect.                                                            |
| 28    | EMU-RST   | System reset initiated by emulator.<br>0 = Not the last reset to occur.<br>1 = The last reset to occur.                   |
| 27:9  | Reserved  | Reserved. Read only. Always reads as 0. Writes have no effect.                                                            |
| 8     | SRIORST   | System reset initiated by SRIO.<br>0 = Not the last reset to occur.<br>1 = The last reset to occur.                       |
| 7:3   | Reserved  | Reserved. Read only. Always reads as 0. Writes have no effect.                                                            |
| 2     | PLLCTRLST | System reset initiated by PLLCTL.<br>0 = Not the last reset to occur.<br>1 = The last reset to occur.                     |
| 1     | WRST      | Warm reset.<br>0 = Warm reset was not the last reset to occur.<br>1 = Warm reset was the last reset to occur.             |
| 0     | POR       | Power-on reset.<br>0 = Power-on reset was not the last reset to occur.<br>1 = Power-on reset was the last reset to occur. |

**End of Table 7-16**

### 7.6.6.2 Software Reset Control Register

This register contains a key that enables writes to the MSB of this register and the RSTCFG register. The key value is 0x5A69. A valid key will be stored as 0x000C, any other key value is invalid. When the RSTCTRL or the RSTCFG is written, the key is invalidated. Every write must be set up with a valid key. The Software Reset Control register (RSTCTRL) is shown in [Table 7-17](#) and described in [Table 7-18](#).

**Table 7-17 Software Reset Control Register (RSTCTRL)**

| Hex Address - 029A 00E8h |            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                       |
|--------------------------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------------------|
| Bit                      | 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| Acronym                  | Reserved   |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SWRST                 |
| Reset <sup>(1)</sup>     | R-0x0000   |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R/W-0x <sup>(2)</sup> |
| Bit                      | 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| Acronym                  | KEY        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                       |
| Reset <sup>(1)</sup>     | R/W-0x0003 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                       |

1 R/W = Read/Write; R = Read only; -n = value after reset

2 Writes are conditional based on valid key.

**Table 7-18 Software Reset Control Register Field Descriptions**

| Bit               | Acronym  | Description                                      |
|-------------------|----------|--------------------------------------------------|
| 31:17             | Reserved | Reserved.                                        |
| 16                | SWRST    | Software reset<br>0 = Reset<br>1 = Not reset     |
| 15:0              | KEY      | Key used to enable writes to RSTCTRL and RSTCFG. |
| End of Table 7-18 |          |                                                  |

### 7.6.6.3 Reset Configuration Register

This register is used to configure the type of system resets initiated by the SRIO module or a PLL controller; i.e., a hard reset or a soft reset. By default, both the system resets will be hard resets. The Reset Configuration register (RSTCFG) is shown in [Table 7-19](#) and described in [Table 7-20](#).

**Table 7-19 Reset Configuration Register (RSTCFG)**

| Address - 029A 00ECh |          |    |                      |  |          |    |    |    |    |    |    |    |    |    |    |    |                        |  |
|----------------------|----------|----|----------------------|--|----------|----|----|----|----|----|----|----|----|----|----|----|------------------------|--|
| Bit                  | 31       | 30 | 29                   |  | 28       | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16                     |  |
| Acronym              | Reserved |    |                      |  |          |    |    |    |    |    |    |    |    |    |    |    |                        |  |
| Reset <sup>(1)</sup> | R-0x2000 |    |                      |  |          |    |    |    |    |    |    |    |    |    |    |    |                        |  |
| Bit                  | 15       | 14 | 13                   |  | 12       | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0                      |  |
| Acronym              | Reserved |    | PLLCTLRSTTYPE        |  | Reserved |    |    |    |    |    |    |    |    |    |    |    | SRIORSTTYPE            |  |
| Reset <sup>(1)</sup> | R-0x000  |    | R/W-0 <sup>(2)</sup> |  | R-0x000  |    |    |    |    |    |    |    |    |    |    |    | R/W-0x0 <sup>(2)</sup> |  |

1 R/W = Read/Write; R = Read only; -n = value after reset

2 Writes are conditional based on valid key. For details, see Section 7.6.6.2 “Software Reset Control Register”.

**Table 7-20 Reset Configuration Register (RSTCFG) Field Descriptions (Part 1 of 2)**

| Bit   | Acronym       | Description                                                                                             |
|-------|---------------|---------------------------------------------------------------------------------------------------------|
| 31:14 | Reserved      | Reserved.                                                                                               |
| 13    | PLLCTLRSTTYPE | PLL controller initiates a software driven reset of type:<br>0 = Hard reset (default)<br>1 = Soft reset |

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**Table 7-20 Reset Configuration Register (RSTCFG) Field Descriptions (Part 2 of 2)**

| Bit               | Acronym     | Description                                                                          |
|-------------------|-------------|--------------------------------------------------------------------------------------|
| 12:1              | Reserved    | Reserved.                                                                            |
| 0                 | SRIORSTTYPE | SRIO module initiates a reset of type:<br>0 = Hard Reset (default)<br>1 = Soft Reset |
| End of Table 7-20 |             |                                                                                      |

### 7.6.7 Reset Electrical Data/Timing

**Table 7-21 Reset Timing Requirements** <sup>(1) (2)</sup>  
(see Figure 7-9 and Figure 7-10)

| No.               |                                                                                                                     | Min  | Max | Unit |
|-------------------|---------------------------------------------------------------------------------------------------------------------|------|-----|------|
| 1                 | $t_{H(SUPPLY-POR)}$ Hold Time, $\overline{POR}$ low after supplies stable and input clocks valid                    | 1000 |     | ns   |
| 2                 | $t_{SU(RESETH-PORH)}$ Setup Time, $\overline{RESET}$ high to $\overline{POR}$ high                                  | 1000 |     | ns   |
| 4                 | $t_{W(RESET)}$ Pulse Duration, $\overline{RESET}$ low                                                               | 24C  |     | ns   |
| 7                 | $t_{S(BOOT)}$ Setup time, boot mode and configuration pins valid before $\overline{POR}$ or $\overline{RESET}$ high | 12C  |     | ns   |
| 8                 | $t_{H(BOOT)}$ Hold time, bootmode and configuration pins valid after $\overline{POR}$ or $\overline{RESET}$ high    | 12C  |     | ns   |
| End of Table 7-21 |                                                                                                                     |      |     |      |

1 If CORECLKSEL = 0, C = 1 ÷ CORECLK(N|P) frequency in ns.

2 If CORECLKSEL = 1, C = 1 ÷ ALT CORECLK frequency in ns.

**Table 7-22 Reset Switching Characteristics Over Recommended Operating Conditions**  
(see Figure 7-9 and Figure 7-10)

| No.               | Parameter                                                                                 | Min | Max | Unit |
|-------------------|-------------------------------------------------------------------------------------------|-----|-----|------|
| 3                 | $t_{d(PORH-RSTATH)}$ Delay Time, $\overline{POR}$ high to $\overline{RESETSTAT}$ high     |     | 200 | μs   |
| 5                 | $t_{d(RESETH-RSTATH)}$ Delay Time, $\overline{RESET}$ high to $\overline{RESETSTAT}$ high |     | 5   | μs   |
| End of Table 7-22 |                                                                                           |     |     |      |

**Table 7-23 Warm Reset Switching Characteristics Over Recommended Operating Conditions**  
(see Figure 7-10 and Figure 7-11)

| No.               | Parameter                                                                         | Min  | Max | Unit |
|-------------------|-----------------------------------------------------------------------------------|------|-----|------|
| 9                 | $t_{SU(PORH-RESETH)}$ Setup time, $\overline{POR}$ high to $\overline{RESET}$ low | 1.34 |     | ns   |
| End of Table 7-23 |                                                                                   |      |     |      |

PRODUCT PREVIEW



Figure 7-9 Power-On Reset Timing

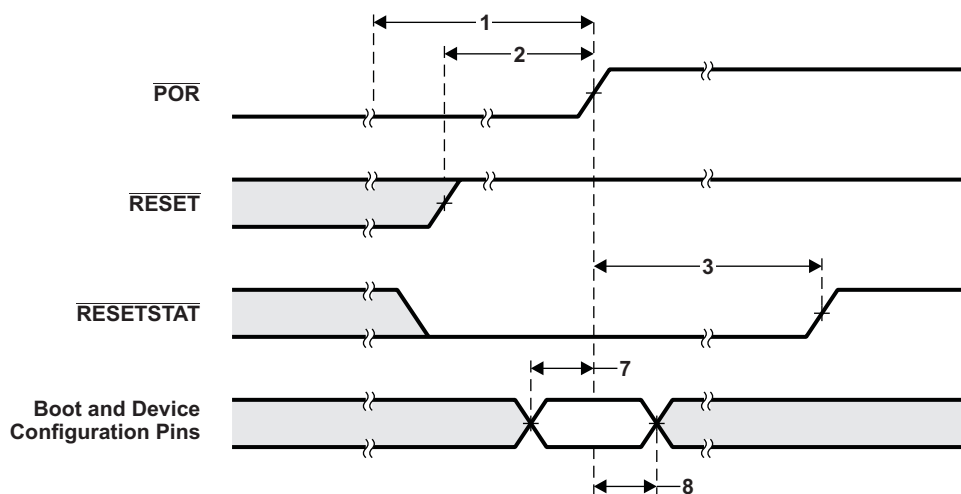


Figure 7-10 Warm Reset Timing —  $\overline{\text{RESETSTAT}}$  Relative to  $\overline{\text{RESET}}$

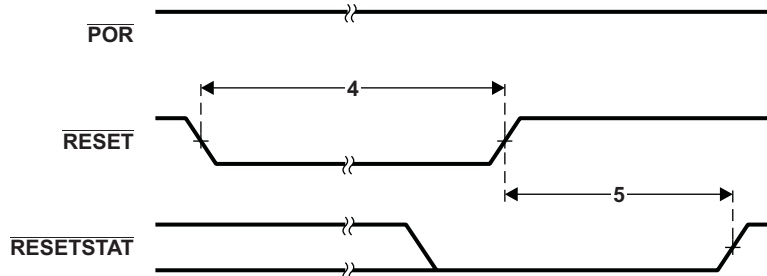
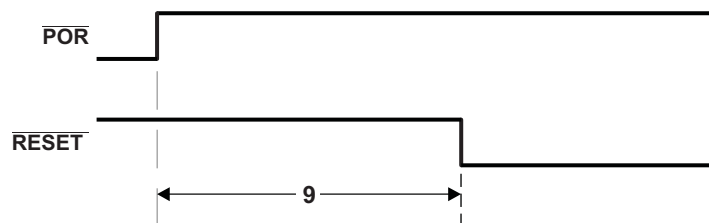


Figure 7-11 Warm Reset Timing — Setup Time Between  $\overline{\text{POR}}$  De-Asserted and  $\overline{\text{RESET}}$  Asserted



## 7.7 PLL1 and PLL1 Controller

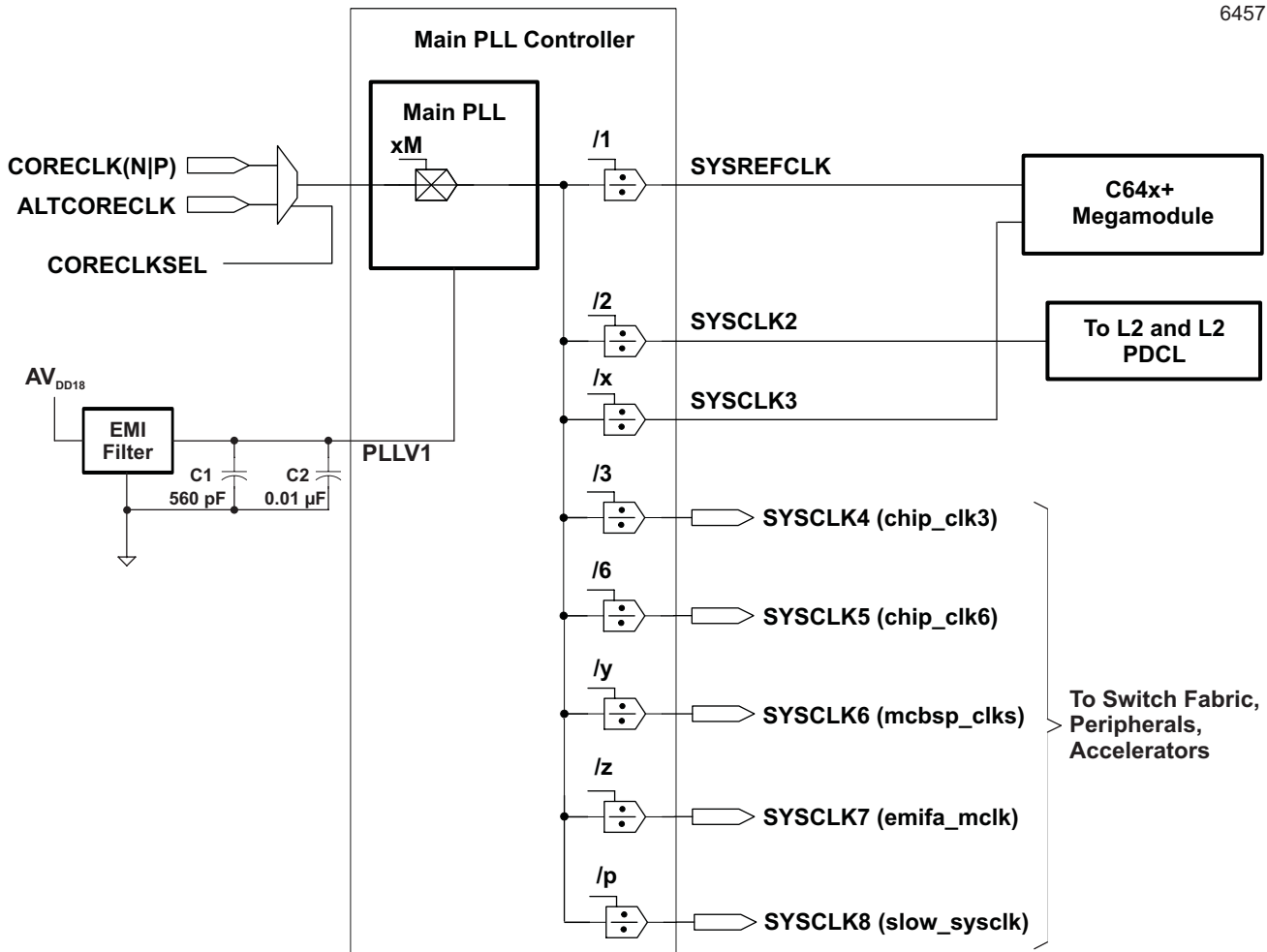
This section provides a description of the PLL1 controller. For details on the operation of the PLL controller module, see the *TMS320C6457 DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (literature number [SPRUGL3](#)).



**Note**—The PLL1 controller registers can be accessed by any master in the device.

The main PLL is controlled by the standard PLL controller. The PLL controller manages the clock ratios, alignment, and gating for the system clocks to the device. [Figure 7-12](#) shows a block diagram of the PLL controller. The following paragraphs define the clocks and PLL controller parameters.

**Figure 7-12 PLL1 and PLL1 Controller**



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The inputs, multiply factor within the PLL, and post-division for each of the chip-level clocks from the PLL output. The PLL controller also controls reset propagation through the chip, clock alignment, and test points. The PLL controller monitors the PLL status and provides an output signal indicating when the PLL is locked.

PLL1 power is supplied externally via the PLL1 power-supply pin (PLLV1). An external EMI filter circuit must be added to PLLV1, as shown in [Figure 7-12](#). The 1.8-V supply of the EMI filter must be from the same 1.8-V power plane supplying the I/O power-supply pin, DV<sub>DD18</sub>. TI requires EMI filter manufacturer Murata, part number NFM18CC222R1C3 or NFM18CC223R1C3.

All PLL external components (C1, C2, and the EMI Filter) must be placed as close to the C64x+ DSP device as possible. For the best performance, TI recommends that all the PLL external components be on a single side of the board without jumpers, switches, or components other than those shown. For reduced PLL jitter, maximize the spacing between switching signal traces and the PLL external components (C1, C2, and the EMI Filter).

The minimum CORECLK rise and fall times should also be observed. For the input clock timing requirements, see Section 7.7.4 “PLL1 Controller Input and Output Electrical Data/Timing”.



**CAUTION**—The PLL controller module as described in the *TMS320C6457 DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (literature number [SPRUGL3](#)) includes a superset of features, some of which are not supported on the TMS320C6457TMS320C6457 DSP. The following sections describe the registers that are supported; it should be assumed that any registers not included in these sections is not supported by the C6457 DSP. Furthermore, only the bits within the registers described here are supported. Avoid writing to any reserved memory location or changing the value of reserved bits.

## 7.7.1 PLL1 Controller Device-Specific Information

### 7.7.1.1 Internal Clocks and Maximum Operating Frequencies

The main PLL, used to drive the core, the switch fabric, and a majority of the peripheral clocks (all but the DDR2 clock) requires a PLL controller to manage the various clock divisions, gating, and synchronization. The main PLL controller has several SYSCLK outputs that are listed below, along with the clock description. Each SYSCLK has a corresponding divider that divides down the output clock of the PLL. Note that dividers are not programmable unless explicitly mentioned in the description below.

- **SYSREFCLK:** Full-rate clock (GEM\_CLK1) for C64x+ megamodule.
- **SYSCLK2:** 1/2-rate clock (GEM\_L2\_CLK) used to clock the L2 and L2 powerdown controller.
- **SYSCLK3:** 1/x-rate clock (GEM\_TRACE\_CLK) for emulation and trace logic of the DSP. The default rate for this clock is 1/3. This is programmable from /1 to /32, where this clock does not violate the maximum clock rate of 333 MHz. The data rate on the trace pins are 1/2 of this clock.
- **SYSCLK4:** 1/3-rate clock (CHIP\_CLK3) for the switched central resources (SCRs), EDMA3, VCP2, TCP2\_A, TCP2\_B, SRIO, as well as the data bus interfaces of the EMIFA and DDR2 memory controller.
- **SYSCLK5:** 1/6-rate clock (CHIP\_CLK6) for other peripherals (PLL controller, PSC, L3 ROM, McBSPs, Timer64s, EMAC, HPI, UTOPIA, I<sup>2</sup>C, and GPIO).
- **SYSCLK6:** 1/y-rate clock (CHIP\_CLKS) for an optional McBSP CLKS module input to drive the clock generator. The default for this clock is 1/10. This is programmable from /6 to /32, where this clock does not violate the maximum clock rate of 100 MHz. This clock is also output to the SYSCLKOUT pin.
- **SYSCLK7:** 1/z-rate clock (EMIF\_MCLK) for an optional internal clock for EMIFA. The default for this clock is 1/10. This is programmable from /6 to /32, where this clock does not violate the maximum clock rate of 166 MHz. The data rate at the pins must not violate 100 MHz.
- **SYSCLK8:** 1/p-rate clock (SLOW\_SYSCLK). The default for this clock is 1/10. This is programmable from /10 to /32.



**Note**—In case any of the other programmable SYSCLKs are set slower than 1/10 rate, then SYSCLK8 (SLOW\_SYSCLK) needs to be programmed to either match, or be slower than, the slowest SYSCLK in the system.

Note that there is a minimum and maximum operating frequency for CORECLK(N|P), ALTCORECLK, SYSREFCLK, SYSCLK3, SYSCLK6, and SYSCLK7. The PLL1 controller must not be configured to exceed any of these constraints (certain combinations of external core clock input, internal dividers, and PLL multiply ratios might not be supported). For the PLL clocks input and output frequency ranges, see [Table 7-24](#).

**Table 7-24 Timing Requirements for Reset**

| Clock Signal             | Min | Max   | Unit |
|--------------------------|-----|-------|------|
| CORECLK(N P)             | 50  | 61.44 | MHz  |
| ALTCORECLK               | 50  | 61.44 | MHz  |
| SYSREFCLK                | 400 | 1200  | MHz  |
| SYSCLK3                  |     | 333   | MHz  |
| SYSCLK6                  |     | 100   | MHz  |
| SYSCLK7                  |     | 166   | MHz  |
| <b>End of Table 7-24</b> |     |       |      |

### 7.7.1.2 PLL1 Controller Operating Modes

The PLL1 controller has two modes of operation: bypass mode and PLL mode. The mode of operation is determined by the PLEN bit of the PLL control register (PLLCTL). In PLL mode, SYSREFCLK is generated from the device input clock CORECLK(N|P) using the divider POSTDIV and the PLL multiplier PLLM. In bypass mode, CORECLK(N|P) is fed directly to SYSREFCLK.

All hosts (HPI, etc.) must hold off accesses to the DSP while the frequency of its internal clocks is changing. A mechanism must be in place such that the DSP notifies the host when the PLL configuration has completed.

### 7.7.1.3 PLL1 Stabilization, Lock, and Reset Times

The PLL stabilization time is the amount of time that must be allotted for the internal PLL regulators to become stable after device powerup. The PLL should not be operated until this stabilization time has expired.

The PLL reset time is the amount of wait time needed when resetting the PLL (writing PLLRST = 1), in order for the PLL to properly reset, before bringing the PLL out of reset (writing PLLRST = 0). For the PLL1 reset time value, see [Table 7-25](#).

The PLL lock time is the amount of time needed from when the PLL is taken out of reset (PLLRST = 1 with PLEN = 0) to when the PLL controller can be switched to PLL mode (PLEN = 1). The PLL1 lock time is given in [Table 7-25](#).

**Table 7-25 PLL1 Stabilization, Lock, and Reset Times**

|                          | Min  | Typ                     | Max | Unit |
|--------------------------|------|-------------------------|-----|------|
| PLL stabilization time   | 100  |                         |     | μs   |
| PLL lock time            |      | 2000 × C <sup>(1)</sup> |     |      |
| PLL reset time           | 1000 |                         |     | ns   |
| <b>End of Table 7-25</b> |      |                         |     |      |

<sup>1</sup> C = CORECLK(N|P) cycle time in ns.

## 7.7.2 PLL1 Controller Memory Map

The memory map of the PLL1 controller is shown in [Table 7-26](#). Note that only registers documented here are accessible on the TMS320C6457. Other addresses in the PLL1 controller memory map should not be modified.

**Table 7-26 PLL1 Controller Registers (Including Reset Controller)**

| Hex Address Range        | Acronym | Register Name                                 |
|--------------------------|---------|-----------------------------------------------|
| 029A 0000 - 029A 00E3    | -       | Reserved                                      |
| 029A 00E4                | RSTYPE  | Reset Type Status Register (Reset Controller) |
| 029A 00E8                | RSTCTRL | Software Reset Control Register               |
| 029A 00EC                | RSTCFG  | Reset Configuration Register                  |
| 029A 00F0 - 029A 00FF    | -       | Reserved                                      |
| 029A 0100                | PLLCTL  | PLL Control Register                          |
| 029A 0104                | -       | Reserved                                      |
| 029A 0108                | -       | Reserved                                      |
| 029A 010C                | -       | Reserved                                      |
| 029A 0110                | PLLM    | PLL Multiplier Control Register               |
| 029A 0114                | -       | Reserved                                      |
| 029A 0118                | -       | Reserved                                      |
| 029A 011C                | -       | Reserved                                      |
| 029A 0120                | PLLDIV3 | PLL Controller Divider 3 Register             |
| 029A 0124                | -       | Reserved                                      |
| 029A 0128                | POSTDIV | PLL Post-Divider Register                     |
| 029A 012C                | -       | Reserved                                      |
| 029A 0130                | -       | Reserved                                      |
| 029A 0134                | -       | Reserved                                      |
| 029A 0138                | PLLCMD  | PLL Controller Command Register               |
| 029A 013C                | PLLSTAT | PLL Controller Status Register                |
| 029A 0140                | ALNCTL  | PLL Controller Clock Align Control Register   |
| 029A 0144                | DCHANGE | PLLDIV Ratio Change Status Register           |
| 029A 0148                | -       | Reserved                                      |
| 029A 014C                | -       | Reserved                                      |
| 029A 0150                | SYSTAT  | SYSClk Status Register                        |
| 029A 0154                | -       | Reserved                                      |
| 029A 0158                | -       | Reserved                                      |
| 029A 015C                | -       | Reserved                                      |
| 029A 0160 - 029A 0164    | -       | Reserved                                      |
| 029A 0168                | PLLDIV6 | PLL Controller Divider 6 Register             |
| 029A 016C                | PLLDIV7 | PLL Controller Divider 7 Register             |
| 029A 0170                | PLLDIV8 | PLL Controller Divider 8 Register             |
| 029A 0174 - 029B FFFF    | -       | Reserved                                      |
| <b>End of Table 7-26</b> |         |                                               |

### 7.7.3 PLL1 Controller Registers

This section provides a description of the PLL1 controller registers. For details on the operation of the PLL controller module, see the *TMS320C6457 DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (literature number [SPRUGL3](#)).



**Note**—The PLL1 controller registers can be accessed by any master in the device.



**CAUTION**—Not all of the registers documented in the *TMS320C6457 DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (literature number [SPRUGL3](#)) are supported on the TMS320C6457. Only those registers documented in this section are supported. Furthermore, only the bits within the registers described here are supported. Avoid writing to any reserved memory location or changing the value of reserved bits.

#### 7.7.3.1 PLL1 Control Register

The PLL1 control register (PLLCTL) is shown in [Table 7-27](#) and described in [Table 7-28](#).

**Table 7-27 PLL1 Control Register (PLLCTL)**

| Address - 029A 0100h |          |    |    |    |    |    |    |    |          |          |          |    |         |          |           |       |
|----------------------|----------|----|----|----|----|----|----|----|----------|----------|----------|----|---------|----------|-----------|-------|
| Bit                  | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23       | 22       | 21       | 20 | 19      | 18       | 17        | 16    |
| Acronym              | Reserved |    |    |    |    |    |    |    |          |          |          |    |         |          |           |       |
| Reset <sup>(1)</sup> | R-0      |    |    |    |    |    |    |    |          |          |          |    |         |          |           |       |
| Bit                  | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7        | 6        | 5        | 4  | 3       | 2        | 1         | 0     |
| Acronym              | Reserved |    |    |    |    |    |    |    | Reserved | Reserved | Reserved |    | PLL RST | Reserved | PLL PWRDN | PLLEN |
| Reset <sup>(1)</sup> | R-0      |    |    |    |    |    |    |    | R/W-0    | R-1      | R/W-0    |    | R/W-1   | R-0      | R/W-0     | R/W-0 |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-28 PLL1 Control Register (PLLCTL) Field Descriptions**

| Bit               | Acronym   | Description                                                                                                                                                                                                                                                                                                             |
|-------------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8              | Reserved  | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                                                                                          |
| 7                 | Reserved  | Reserved. Writes to this register must keep this bit as 0.                                                                                                                                                                                                                                                              |
| 6                 | Reserved  | Reserved. Read only. Always reads as 1. Writes have no effect.                                                                                                                                                                                                                                                          |
| 5:4               | Reserved  | Reserved. Writes to this register must keep this bit as 0.                                                                                                                                                                                                                                                              |
| 3                 | PLL RST   | PLL reset bit<br>0 = PLL reset is released<br>1 = PLL reset is asserted                                                                                                                                                                                                                                                 |
| 2                 | Reserved  | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                                                                                          |
| 1                 | PLL PWRDN | PLL power-down mode select bit<br>0 = PLL is operational<br>1 = PLL is placed in power-down state, i.e., all analog circuitry in the PLL is turned-off                                                                                                                                                                  |
| 0                 | PLLEN     | PLL enable bit<br>0 = Bypass mode. Divider POSTDIV and PLL are bypassed. All the system clocks (SYSCLKn) are divided down directly from input reference clock.<br>1 = PLL mode. Divider POSTDIV and PLL are not bypassed. PLL output path is enabled. All the system clocks (SYSCLKn) are divided down from PLL output. |
| End of Table 7-28 |           |                                                                                                                                                                                                                                                                                                                         |

### 7.7.3.2 PLL Multiplier Control Register

The PLL multiplier control register (PLLM) is shown in [Table 7-29](#) and described in [Table 7-30](#). The PLLM register defines the input reference clock frequency multiplier in conjunction with the PLL divider ratio bits (RATIO) in the PLL controller post-divider register (POSTDIV).

**Table 7-29 PLL Multiplier Control Register (PLLM)**

|                             |          |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |
|-----------------------------|----------|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|----|
| <b>Address - 029A 0110h</b> |          |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |
| <b>Bit</b>                  | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20    | 19 | 18 | 17 | 16 |
| <b>Acronym</b>              | Reserved |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |
| <b>Reset <sup>(1)</sup></b> | R-0      |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |
| <b>Bit</b>                  | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4     | 3  | 2  | 1  | 0  |
| <b>Acronym</b>              | Reserved |    |    |    |    |    |    |    |    |    |    | PLLM  |    |    |    |    |
| <b>Reset <sup>(1)</sup></b> | R-0      |    |    |    |    |    |    |    |    |    |    | R/W-0 |    |    |    |    |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-30 PLL Multiplier Control Register (PLLM) Field Descriptions**

| Bit             | Acronym         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
|-----------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 31:5            | Reserved        | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| 4:0             | PLLM            | <div>PLL multiplier bits. Defines the frequency multiplier of the input reference clock in conjunction with the PLL divider ratio bits (RATIO) in POSTDIV.</div> <table><tr><td>• 000000 = × 1</td><td>• 010000 = × 17</td><td>• 100000 = × 33</td><td>• 110000 = × 49</td></tr><tr><td>• 000001 = × 2</td><td>• 010001 = × 18</td><td>• 100001 = × 34</td><td>• 110001 = × 50</td></tr><tr><td>• 000010 = × 3</td><td>• 010010 = × 19</td><td>• 100010 = × 35</td><td>• 110010 = × 51</td></tr><tr><td>• 000011 = × 4</td><td>• 010011 = × 20</td><td>• 100011 = × 36</td><td>• 110011 = × 52</td></tr><tr><td>• 000100 = × 5</td><td>• 010100 = × 21</td><td>• 100100 = × 37</td><td>• 110100 = × 53</td></tr><tr><td>• 000101 = × 6</td><td>• 010101 = × 22</td><td>• 100101 = × 38</td><td>• 110101 = × 54</td></tr><tr><td>• 000110 = × 7</td><td>• 010110 = × 23</td><td>• 100110 = × 39</td><td>• 110110 = × 55</td></tr><tr><td>• 000111 = × 8</td><td>• 010111 = × 24</td><td>• 100111 = × 40</td><td>• 110111 = × 56</td></tr><tr><td>• 001000 = × 9</td><td>• 011000 = × 25</td><td>• 101000 = × 41</td><td>• 111000 = × 57</td></tr><tr><td>• 001001 = × 10</td><td>• 011001 = × 26</td><td>• 101001 = × 42</td><td>• 111001 = × 58</td></tr><tr><td>• 001010 = × 11</td><td>• 011010 = × 27</td><td>• 101010 = × 43</td><td>• 111010 = × 59</td></tr><tr><td>• 001011 = × 12</td><td>• 011011 = × 28</td><td>• 101011 = × 44</td><td>• 111011 = × 60</td></tr><tr><td>• 001100 = × 13</td><td>• 011100 = × 29</td><td>• 101100 = × 45</td><td>• 111100 = × 61</td></tr><tr><td>• 001101 = × 14</td><td>• 011101 = × 30</td><td>• 101101 = × 46</td><td>• 111101 = × 62</td></tr><tr><td>• 001110 = × 15</td><td>• 011110 = × 31</td><td>• 101110 = × 47</td><td>• 111110 = × 63</td></tr><tr><td>• 001111 = × 16</td><td>• 011111 = × 32</td><td>• 101111 = × 48</td><td>• 111111 = × 64</td></tr></table> | • 000000 = × 1  | • 010000 = × 17 | • 100000 = × 33 | • 110000 = × 49 | • 000001 = × 2 | • 010001 = × 18 | • 100001 = × 34 | • 110001 = × 50 | • 000010 = × 3 | • 010010 = × 19 | • 100010 = × 35 | • 110010 = × 51 | • 000011 = × 4 | • 010011 = × 20 | • 100011 = × 36 | • 110011 = × 52 | • 000100 = × 5 | • 010100 = × 21 | • 100100 = × 37 | • 110100 = × 53 | • 000101 = × 6 | • 010101 = × 22 | • 100101 = × 38 | • 110101 = × 54 | • 000110 = × 7 | • 010110 = × 23 | • 100110 = × 39 | • 110110 = × 55 | • 000111 = × 8 | • 010111 = × 24 | • 100111 = × 40 | • 110111 = × 56 | • 001000 = × 9 | • 011000 = × 25 | • 101000 = × 41 | • 111000 = × 57 | • 001001 = × 10 | • 011001 = × 26 | • 101001 = × 42 | • 111001 = × 58 | • 001010 = × 11 | • 011010 = × 27 | • 101010 = × 43 | • 111010 = × 59 | • 001011 = × 12 | • 011011 = × 28 | • 101011 = × 44 | • 111011 = × 60 | • 001100 = × 13 | • 011100 = × 29 | • 101100 = × 45 | • 111100 = × 61 | • 001101 = × 14 | • 011101 = × 30 | • 101101 = × 46 | • 111101 = × 62 | • 001110 = × 15 | • 011110 = × 31 | • 101110 = × 47 | • 111110 = × 63 | • 001111 = × 16 | • 011111 = × 32 | • 101111 = × 48 | • 111111 = × 64 |
| • 000000 = × 1  | • 010000 = × 17 | • 100000 = × 33                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 110000 = × 49 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 000001 = × 2  | • 010001 = × 18 | • 100001 = × 34                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 110001 = × 50 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 000010 = × 3  | • 010010 = × 19 | • 100010 = × 35                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 110010 = × 51 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 000011 = × 4  | • 010011 = × 20 | • 100011 = × 36                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 110011 = × 52 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 000100 = × 5  | • 010100 = × 21 | • 100100 = × 37                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 110100 = × 53 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 000101 = × 6  | • 010101 = × 22 | • 100101 = × 38                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 110101 = × 54 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 000110 = × 7  | • 010110 = × 23 | • 100110 = × 39                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 110110 = × 55 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 000111 = × 8  | • 010111 = × 24 | • 100111 = × 40                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 110111 = × 56 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 001000 = × 9  | • 011000 = × 25 | • 101000 = × 41                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 111000 = × 57 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 001001 = × 10 | • 011001 = × 26 | • 101001 = × 42                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 111001 = × 58 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 001010 = × 11 | • 011010 = × 27 | • 101010 = × 43                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 111010 = × 59 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 001011 = × 12 | • 011011 = × 28 | • 101011 = × 44                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 111011 = × 60 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 001100 = × 13 | • 011100 = × 29 | • 101100 = × 45                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 111100 = × 61 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 001101 = × 14 | • 011101 = × 30 | • 101101 = × 46                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 111101 = × 62 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 001110 = × 15 | • 011110 = × 31 | • 101110 = × 47                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 111110 = × 63 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |
| • 001111 = × 16 | • 011111 = × 32 | • 101111 = × 48                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | • 111111 = × 64 |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |

End of Table 7-30

### 7.7.3.3 PLL Post-Divider Control Register

The PLL post-divider control register (POSTDIV) is shown in [Table 7-31](#) and described in [Table 7-32](#).

**Table 7-31 PLL Post-Divider Control Register (POSTDIV)**

|                             |          |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
|-----------------------------|----------|----------|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|
| <b>Address - 029A 0128</b>  |          |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
| <b>Bit</b>                  | 31       | 30       | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20     | 19 | 18 | 17 | 16 |
| <b>Acronym</b>              | Reserved |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
| <b>Reset <sup>(1)</sup></b> | R-0      |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
| <b>Bit</b>                  | 15       | 14       | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4      | 3  | 2  | 1  | 0  |
| <b>Acronym</b>              | POSTDEN  | Reserved |    |    |    |    |    |    |    |    |    | RATIO  |    |    |    |    |
| <b>Reset <sup>(1)</sup></b> | R/W-1    | R-0      |    |    |    |    |    |    |    |    |    | R/W-2h |    |    |    |    |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-32 PLL Post-Divider Control Register (POSTDIV) Field Descriptions**

| Bit                      | Acronym  | Description                                                                                                                                                                                        |
|--------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16                    | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                     |
| 15                       | POSTDEN  | Post-divider enable bit.<br>0 = Post-divider is disabled. No clock output.<br>1 = Post-divider is enabled.                                                                                         |
| 14:5                     | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                     |
| 4:0                      | RATIO    | 0 through 1Fh are divider ratio bits:<br>» 0 = ÷ 1. Divide frequency by 1.<br>» 1h = ÷ 2. Divide frequency by 2.<br>» 2h = ÷ 3. Divide frequency by 3.<br>» 3h through 1Fh = Reserved, do not use. |
| <b>End of Table 7-32</b> |          |                                                                                                                                                                                                    |

### 7.7.3.4 PLL Controller Divider 3 Register

The PLL controller divider 3 register (PLLDIV3) is shown in [Table 7-33](#) and described in [Table 7-34](#).

**Table 7-33 PLL Controller Divider 3 Register (PLLDIV3)**

| <b>Address - 029A 015Ch</b> |          |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
|-----------------------------|----------|----------|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|
| Bit                         | 31       | 30       | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20     | 19 | 18 | 17 | 16 |
| <b>Acronym</b>              | Reserved |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
| <b>Reset <sup>(1)</sup></b> | R-0      |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
| Bit                         | 15       | 14       | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4      | 3  | 2  | 1  | 0  |
| <b>Acronym</b>              | D3EN     | Reserved |    |    |    |    |    |    |    |    |    | RATIO  |    |    |    |    |
| <b>Reset <sup>(1)</sup></b> | R/W-1    | R-0      |    |    |    |    |    |    |    |    |    | R/W-2h |    |    |    |    |

<sup>1</sup> R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-34 PLL Controller Divider 3 Register (PLLDIV3) Field Descriptions**

| Bit                      | Acronym  | Description                                                                                                                                                                                                                                                                      |
|--------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16                    | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                                                   |
| 15                       | D3EN     | Divider 3 enable bit.<br>0 = Divider 3 is disabled. No clock output.<br>1 = Divider 3 is enabled.                                                                                                                                                                                |
| 14:5                     | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                                                   |
| 4:0                      | RATIO    | 0 through 1Fh are divider ratio bits:<br>» 0 = ÷ 1. Divide frequency by 1.<br>» 1h = ÷ 2. Divide frequency by 2.<br>» 2h = ÷ 3. Divide frequency by 3.<br>» 3h = ÷ 4. Divide frequency by 4.<br>» 4h through 1Fh = ÷ 5 to ÷ 32. Divide frequency by 5 to divide frequency by 32. |
| <b>End of Table 7-34</b> |          |                                                                                                                                                                                                                                                                                  |



### 7.7.3.5 PLL Controller Divider 6 Register

The PLL controller divider 6 register (PLLDIV6) is shown in [Table 7-35](#) and described in [Table 7-36](#).

**Table 7-35 PLL Controller Divider 6 Register (PLLDIV6)**

|                             |          |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
|-----------------------------|----------|----------|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|
| <b>Address - 029A 0168</b>  |          |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
| <b>Bit</b>                  | 31       | 30       | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20     | 19 | 18 | 17 | 16 |
| <b>Acronym</b>              | Reserved |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
| <b>Reset <sup>(1)</sup></b> | R-0      |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
| <b>Bit</b>                  | 15       | 14       | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4      | 3  | 2  | 1  | 0  |
| <b>Acronym</b>              | D6EN     | Reserved |    |    |    |    |    |    |    |    |    | RATIO  |    |    |    |    |
| <b>Reset <sup>(1)</sup></b> | R/W-1    | R-0      |    |    |    |    |    |    |    |    |    | R/W-9h |    |    |    |    |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-36 PLL Controller Divider 6 Register (PLLDIV6) Field Descriptions**

| Bit                      | Acronym  | Description                                                                                                                                                                                                                                                                      |
|--------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16                    | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                                                   |
| 15                       | D6EN     | Divider 6 enable bit.<br>0 = Divider 6 is disabled. No clock output.<br>1 = Divider 6 is enabled.                                                                                                                                                                                |
| 14:5                     | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                                                   |
| 4:0                      | RATIO    | 0 through 1Fh are divider ratio bits:<br>» 0 = ÷ 1. Divide frequency by 1.<br>» 1h = ÷ 2. Divide frequency by 2.<br>» 2h = ÷ 3. Divide frequency by 3.<br>» 3h = ÷ 4. Divide frequency by 4.<br>» 4h through 1Fh = ÷ 5 to ÷ 32. Divide frequency by 5 to divide frequency by 32. |
| <b>End of Table 7-36</b> |          |                                                                                                                                                                                                                                                                                  |

### 7.7.3.6 PLL Controller Divider 7 Register

The PLL controller divider 7 register (PLLDIV7) is shown in [Table 7-37](#) and described in [Table 7-38](#).

**Table 7-37 PLL Controller Divider 7 Register (PLLDIV7)**

|                             |          |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
|-----------------------------|----------|----------|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|
| <b>Address - 029A 016Ch</b> |          |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
| <b>Bit</b>                  | 31       | 30       | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20     | 19 | 18 | 17 | 16 |
| <b>Acronym</b>              | Reserved |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
| <b>Reset <sup>(1)</sup></b> | R-0      |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
| <b>Bit</b>                  | 15       | 14       | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4      | 3  | 2  | 1  | 0  |
| <b>Acronym</b>              | D7EN     | Reserved |    |    |    |    |    |    |    |    |    | RATIO  |    |    |    |    |
| <b>Reset <sup>(1)</sup></b> | R/W-1    | R-0      |    |    |    |    |    |    |    |    |    | R/W-9h |    |    |    |    |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-38 PLL Controller Divider 7 Register (PLLDIV7) Field Descriptions (Part 1 of 2)**

| Bit   | Acronym  | Description                                                                                       |
|-------|----------|---------------------------------------------------------------------------------------------------|
| 31:16 | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                    |
| 15    | D7EN     | Divider 7 enable bit.<br>0 = Divider 6 is disabled. No clock output.<br>1 = Divider 6 is enabled. |

**Table 7-38 PLL Controller Divider 7 Register (PLLDIV7) Field Descriptions (Part 2 of 2)**

| Bit                      | Acronym  | Description                                                                                                                                                                                                                                                                      |
|--------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14:5                     | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                                                   |
| 4:0                      | RATIO    | 0 through 1Fh are divider ratio bits:<br>» 0 = ÷ 1. Divide frequency by 1.<br>» 1h = ÷ 2. Divide frequency by 2.<br>» 2h = ÷ 3. Divide frequency by 3.<br>» 3h = ÷ 4. Divide frequency by 4.<br>» 4h through 1Fh = ÷ 5 to ÷ 32. Divide frequency by 5 to divide frequency by 32. |
| <b>End of Table 7-38</b> |          |                                                                                                                                                                                                                                                                                  |

### 7.7.3.7 PLL Controller Divider 8 Register

The PLL controller divider 8 register (PLLDIV7) is shown in [Table 7-39](#) and described in [Table 7-40](#).

**Table 7-39 PLL Controller Divider 8 Register (PLLDIV8)**

| Address - 029A 0170  |          |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
|----------------------|----------|----------|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|
| Bit                  | 31       | 30       | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20     | 19 | 18 | 17 | 16 |
| Acronym              | Reserved |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
| Reset <sup>(1)</sup> | R-0      |          |    |    |    |    |    |    |    |    |    |        |    |    |    |    |
| Bit                  | 15       | 14       | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4      | 3  | 2  | 1  | 0  |
| Acronym              | D8EN     | Reserved |    |    |    |    |    |    |    |    |    | RATIO  |    |    |    |    |
| Reset <sup>(1)</sup> | R/W-1    | R-0      |    |    |    |    |    |    |    |    |    | R/W-9h |    |    |    |    |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-40 PLL Controller Divider 8 Register (PLLDIV8) Field Descriptions**

| Bit                      | Acronym  | Description                                                                                                                                                                                                                                                                      |
|--------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16                    | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                                                   |
| 15                       | D8EN     | Divider 8 enable bit.<br>0 = Divider 6 is disabled. No clock output.<br>1 = Divider 6 is enabled.                                                                                                                                                                                |
| 14:5                     | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                                                   |
| 4:0                      | RATIO    | 0 through 1Fh are divider ratio bits:<br>» 0 = ÷ 1. Divide frequency by 1.<br>» 1h = ÷ 2. Divide frequency by 2.<br>» 2h = ÷ 3. Divide frequency by 3.<br>» 3h = ÷ 4. Divide frequency by 4.<br>» 4h through 1Fh = ÷ 5 to ÷ 32. Divide frequency by 5 to divide frequency by 32. |
| <b>End of Table 7-40</b> |          |                                                                                                                                                                                                                                                                                  |

### 7.7.3.8 PLL Controller Command Register

The PLL controller command register (PLLCMD) contains the command bit for GO operation. PLLCMD is shown in [Table 7-41](#) and described in [Table 7-42](#).

**Table 7-41 PLL Controller Command Register (PLLCMD)**

| Address - 029A 0138h |          |    |    |    |    |    |    |    |    |    |    |    |    |    |          |       |
|----------------------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|-------|
| Bit                  | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17       | 16    |
| Acronym              | Reserved |    |    |    |    |    |    |    |    |    |    |    |    |    |          |       |
| Reset <sup>(1)</sup> | R-0      |    |    |    |    |    |    |    |    |    |    |    |    |    |          |       |
| Bit                  | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1        | 0     |
| Acronym              | Reserved |    |    |    |    |    |    |    |    |    |    |    |    |    | Reserved | GOSET |
| Reset <sup>(1)</sup> | R-0      |    |    |    |    |    |    |    |    |    |    |    |    |    | R/W-0    | R/W-0 |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-42 PLL Controller Command Register (PLLCMD) Field Descriptions**

| Bit               | Acronym  | Description                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2              | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                                                                                                                                                                                                 |
| 1                 | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                                                                                                                                                                                                 |
| 0                 | GOSET    | GO operation command for SYSCLK rate change and phase alignment. Before setting this bit to 1 to initiate a GO operation, check the GOSTAT bit in the PLLSTAT register to ensure all previous GO operations have completed.<br>0 = No effect. Write of 0 clears bit to 0.<br>1 = Initiates GO operation. Write of 1 initiates GO operation. Once set, GOSET remains set but further writes of 1 can initiate the GO operation. |
| End of Table 7-42 |          |                                                                                                                                                                                                                                                                                                                                                                                                                                |

### 7.7.3.9 PLL Controller Status Register

The PLL controller status register (PLLSTAT) shows the PLL controller status. PLLSTAT is shown in [Table 7-43](#) and described in [Table 7-44](#).

**Table 7-43 PLL Controller Status Register (PLLSTAT)**

| Address - 029A 013C  |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |
|----------------------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|
| Bit                  | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16     |
| Acronym              | Reserved |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |
| Reset <sup>(1)</sup> | R-0      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |
| Bit                  | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0      |
| Acronym              | Reserved |    |    |    |    |    |    |    |    |    |    |    |    |    |    | GOSTAT |
| Reset <sup>(1)</sup> | R-0      |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R-0    |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-44 PLL Controller Status Register (PLLSTAT) Field Descriptions**

| Bit               | Acronym  | Description                                                                                                                                                                          |
|-------------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1              | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                       |
| 0                 | GOSTAT   | GO operation status.<br>0 = GO operation is not in progress. SYSCLK divide ratios are not being changed.<br>1 = GO operation is in progress. SYSCLK divide ratios are being changed. |
| End of Table 7-44 |          |                                                                                                                                                                                      |

### 7.7.3.10 PLL Controller Clock Align Control Register

The PLL controller clock align control register (ALNCTL) is shown in [Table 7-45](#) and described in [Table 7-46](#).

**Table 7-45 PLL Controller Clock Align Control Register (ALNCTL)**

| Address - 029A 0140  |          |    |    |    |    |    |    |    |    |    |    |      |      |          |    |    |
|----------------------|----------|----|----|----|----|----|----|----|----|----|----|------|------|----------|----|----|
| Bit                  | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20   | 19   | 18       | 17 | 16 |
| Acronym              | Reserved |    |    |    |    |    |    |    |    |    |    |      |      |          |    |    |
| Reset <sup>(1)</sup> | R-0      |    |    |    |    |    |    |    |    |    |    |      |      |          |    |    |
| Bit                  | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4    | 3    | 2        | 1  | 0  |
| Acronym              | Reserved |    |    |    |    |    |    |    |    |    |    | ALN5 | ALN4 | Reserved |    |    |
| Reset <sup>(1)</sup> | R-0      |    |    |    |    |    |    |    |    |    |    | R-1  | R-1  | R-1      |    |    |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-46 PLL Controller Clock Align Control Register (ALNCTL) Field Descriptions**

| Bit                      | Acronym  | Description                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------------------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5                     | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                                                                                                                                                                                                        |
| 4:3                      | ALNn     | SYSClKn alignment. Do not change the default values of these fields.<br>0 = Do not align SYSClKn to other SYSClKs during GO operation. If SYSn in DCHANGE is set to 1, SYSClKn switches to the new ratio immediately after the GOSET bit in PLLCMD is set.<br>1 = Align SYSClKn to other SYSClKs selected in ALNCTL when the GOSET bit in PLLCMD is set. The SYSClKn ratio is set to the ratio programmed in the RATIO bit in PLLDIVn |
| 2:0                      | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                                                                                                                                                                                                        |
| <b>End of Table 7-46</b> |          |                                                                                                                                                                                                                                                                                                                                                                                                                                       |

### 7.7.3.11 PLLDIV Ratio Change Status Register

Whenever a different ratio is written to the PLLDIVn registers, the PLLCTL flags the change in the PLLDIV ratio change status registers (DCHANGE). During the GO operation, the PLL controller will change the divide ratio of only the SYSClKs with the bit set in DCHANGE. Note that changed clocks will be automatically aligned to other clocks. The PLLDIV divider ratio change status register is shown in [Table 7-47](#) and described in [Table 7-48](#).

**Table 7-47 PLLDIV Divider Ratio Change Status Register (DCHANGE)**

| Address - 029A 0144  |          |    |    |    |    |    |    |    |    |    |    |      |      |          |    |    |
|----------------------|----------|----|----|----|----|----|----|----|----|----|----|------|------|----------|----|----|
| Bit                  | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20   | 19   | 18       | 17 | 16 |
| Acronym              | Reserved |    |    |    |    |    |    |    |    |    |    |      |      |          |    |    |
| Reset <sup>(1)</sup> | R-0      |    |    |    |    |    |    |    |    |    |    |      |      |          |    |    |
| Bit                  | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4    | 3    | 2        | 1  | 0  |
| Acronym              | Reserved |    |    |    |    |    |    |    |    |    |    | SYS5 | SYS4 | Reserved |    |    |
| Reset <sup>(1)</sup> | R-0      |    |    |    |    |    |    |    |    |    |    | R-0  | R-0  | R-0      |    |    |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-48 PLLDIV Divider Ratio Change Status Register (DCHANGE) Field Descriptions (Part 1 of 2)**

| Bit  | Acronym  | Description                                                                                                                                                                                                                                               |
|------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                            |
| 4    | SYS5     | Identifies when the SYSClK5 divide ratio has been modified.<br>0 = SYSClK5 ratio has not been modified. When GOSET is set, SYSClK5 will not be affected.<br>1 = SYSClK5 ratio has been modified. When GOSET is set, SYSClK5 will change to the new ratio. |

**Table 7-48 PLLDIV Divider Ratio Change Status Register (DCHANGE) Field Descriptions (Part 2 of 2)**

| Bit                      | Acronym  | Description                                                                                                                                                                                                                                               |
|--------------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3                        | SYS4     | Identifies when the SYSCLK4 divide ratio has been modified.<br>0 = SYSCLK4 ratio has not been modified. When GOSET is set, SYSCLK4 will not be affected.<br>1 = SYSCLK4 ratio has been modified. When GOSET is set, SYSCLK4 will change to the new ratio. |
| 2:0                      | Reserved | Reserved. Read only. Always reads as 0. Writes have no effect.                                                                                                                                                                                            |
| <b>End of Table 7-48</b> |          |                                                                                                                                                                                                                                                           |

### 7.7.3.12 SYSCLK Status Register

The SYSCLK status register (SYSTAT) shows the status of the system clocks (SYSCLK<sub>n</sub>). SYSTAT is shown in [Table 7-49](#) and described in [Table 7-50](#).

**Table 7-49 SYSCLK Status Register (SYSTAT)**

| Address - 029A 0150  |          |    |    |    |    |    |    |    |    |    |    |        |        |        |        |          |
|----------------------|----------|----|----|----|----|----|----|----|----|----|----|--------|--------|--------|--------|----------|
| Bit                  | 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20     | 19     | 18     | 17     | 16       |
| Acronym              | Reserved |    |    |    |    |    |    |    |    |    |    |        |        |        |        |          |
| Reset <sup>(1)</sup> | R-0      |    |    |    |    |    |    |    |    |    |    |        |        |        |        |          |
| Bit                  | 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4      | 3      | 2      | 1      | 0        |
| Acronym              | Reserved |    |    |    |    |    |    |    |    |    |    | SYS5ON | SYS4ON | SYS3ON | SYS2ON | Reserved |
| Reset <sup>(1)</sup> | R-0      |    |    |    |    |    |    |    |    |    |    | R-1    | R-1    | R-1    | R-1    | R-1      |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-50 SYSCLK Status Register (SYSTAT) Field Descriptions**

| Bit                      | Acronym             | Description                                                                                           |
|--------------------------|---------------------|-------------------------------------------------------------------------------------------------------|
| 31:4                     | Reserved            | Reserved. Read only. Always reads as 0. Writes have no effect.                                        |
| 4:1                      | SYS <sub>n</sub> ON | SYSCLK <sub>n</sub> on status.<br>0 = SYSCLK <sub>n</sub> is gated.<br>1 = SYSCLK <sub>n</sub> is on. |
| 0:                       | Reserved            | Reserved. Read only. Always reads as 1. Writes have no effect.                                        |
| <b>End of Table 7-50</b> |                     |                                                                                                       |

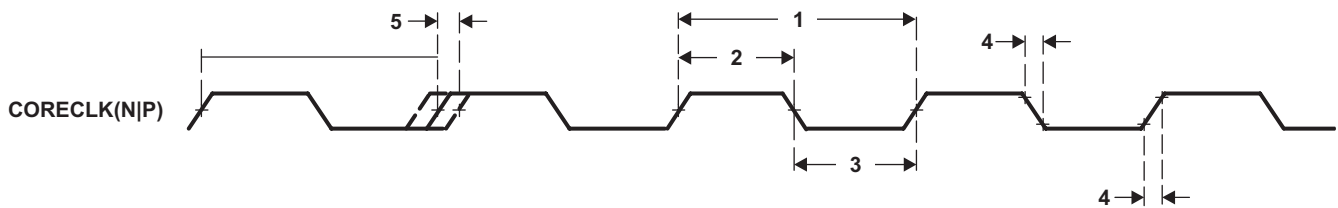
### 7.7.4 PLL1 Controller Input and Output Electrical Data/Timing

**Table 7-51 CORECLK(N|P) and ALT CORECLK Timing Requirements <sup>(1)</sup>**

| No.                          |                          |                                                           | Min                      | Max                       | Unit |
|------------------------------|--------------------------|-----------------------------------------------------------|--------------------------|---------------------------|------|
| CORECLK(N P) and ALT CORECLK |                          |                                                           |                          |                           |      |
| 1                            | t <sub>c</sub> (SYSCLK)  | Cycle time, CORECLK(N P) or ALT CORECLK                   | 16.27                    | 20.00                     | ns   |
| 2                            | t <sub>w</sub> (SYSCLKH) | Pulse duration, CORECLK(N P) or ALT CORECLK high          | 0.45 x C <sub>1</sub>    |                           | ns   |
| 3                            | t <sub>w</sub> (SYSCLKL) | Pulse duration, CORECLK(N P) or ALT CORECLK low           | 0.45 x C <sub>1</sub>    |                           | ns   |
| 4                            | t <sub>t</sub> (SYSCLK)  | Transition time, CORECLK(N P) or ALT CORECLK              | 50                       | 1300                      | ps   |
| 5                            | t <sub>j</sub> (SYSCLK)  | Period Jitter (peak-to-peak), CORECLK(N P) or ALT CORECLK |                          | 100                       | ps   |
| SYSCLKOUT                    |                          |                                                           |                          |                           |      |
| 1                            | t <sub>c</sub> (CKO)     | Cycle time, SYSCLKOUT                                     | 10 x C <sub>1</sub>      | 32 x C <sub>1</sub>       | ns   |
| 2                            | t <sub>w</sub> (CKOH)    | Pulse duration, SYSCLKOUT high                            | 4 x C <sub>1</sub> - 0.7 | 32 x C <sub>1</sub> + 0.7 | ns   |
| 3                            | t <sub>w</sub> (CKOL)    | Pulse duration, SYSCLKOUT low                             | 4 x C <sub>1</sub> - 0.7 | 32 x C <sub>1</sub> + 0.7 | ns   |
| 4                            | t <sub>t</sub> (CKO)     | Transition time, SYSCLKOUT                                |                          | 1.0                       | ns   |
| End of Table 7-51            |                          |                                                           |                          |                           |      |

1 If CORECLKSEL = 0, C<sub>1</sub> = CORECLK(N|P) cycle time in ns. If CORECLKSEL = 1, C<sub>1</sub> = ALT CORECLK cycle time in ns.

**Figure 7-13 CORECLK(N|P) and ALT CORECLK Timing**



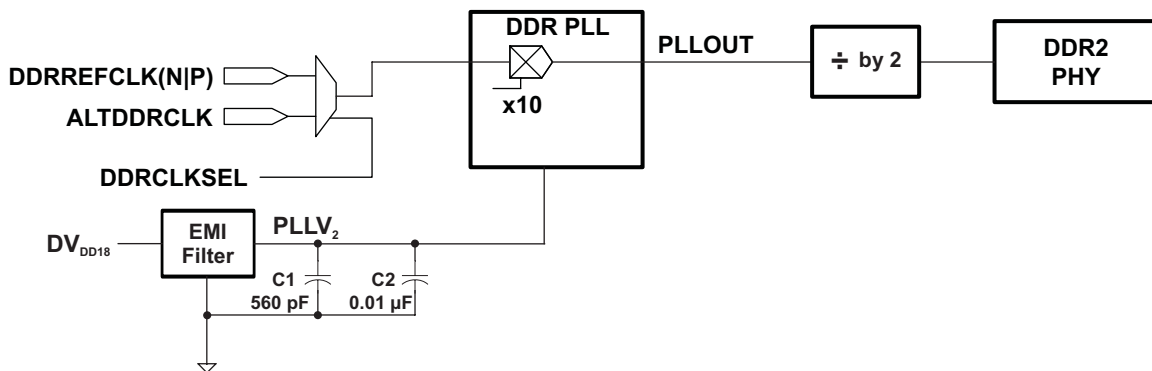
## 7.8 PLL2

The secondary PLL generates interface clocks for the DDR2 memory controller. Using the DDRCLKSEL pin the user can select the input source of PLL2 as either the DDRREFCLK or the ALTDDRCLK clock reference sources.

When coming out of power-on reset, PLL2 is enabled and initialized.

As shown in [Figure 7-14](#), the PLL2 multiplier is fixed at a  $\times 10$  multiplier rate followed by a fixed  $/2$  divider resulting in an effective  $\times 5$  multiplier going to the DDR2PHY and attached DDR2 memory.

**Figure 7-14 PLL2 Block Diagram**



PLL2 power is supplied externally via the PLL2 power supply (PLLV<sub>2</sub>). An external PLL filter circuit must be added to PLLV<sub>2</sub> as shown in [Figure 7-14](#). The 1.8-V supply for the EMI filter must be from the same 1.8-V power plane supplying the I/O power-supply pin, DV<sub>DD18</sub>. TI requires EMI filter manufacturer Murata NFM18CC222R1C3 or NFM18CC223R1C3. For more information on the external PLL filter or the EMI filter, see the *TMS320TCI6484 and TMS320C6457 DSPs Hardware Design Guide* (literature number [SPRAAV7](#)).

All PLL external components (capacitors and the EMI filter) should be placed as close to the C64x+ DSP device as possible. For the best performance, TI requires that all the PLL external components be on a single side of the board without jumpers, switches, or components other than the ones shown. For reduced PLL jitter, maximize the spacing between switching signal traces and the PLL external components (capacitors and the EMI filter). The minimum CLKIN2 rise and fall times should also be observed.

### 7.8.1 PLL2 Device-Specific Information

#### 7.8.1.1 Internal Clocks and Maximum Operating Frequencies

As shown in [Figure 7-14](#), the output of PLL2, PLLOUT, is divided by 2 and directly fed to the DDR2 memory controller. This clock is used by the DDR2 memory controller to generate DDR2CLKOUT(N|P)0 and DDR2CLKOUT(N|P)1. Note that, internally, the data bus interface of the DDR2 memory controller is clocked by SYSCLK4 and PLL1 controller.

Note that there is a minimum and maximum operating frequency for DDRREFCLK and associated DDR2CLKOUT(N|P)0 and DDR2CLKOUT(N|P)1. For the PLL clocks input and output frequency ranges, see [Table 7-52](#).

**Table 7-52 PLL2 Clock Frequency Ranges**

| Signal                                | Min | Max   | Unit |
|---------------------------------------|-----|-------|------|
| DDRREFCLK (PLLEN = 1)                 | 40  | 66.67 | MHz  |
| DDR2CLKOUT0(P N) and DDR2CLKOUT1(P N) | 200 | 333   | MHz  |
| End of Table 7-52                     |     |       |      |

### 7.8.1.2 PLL2 Operating Modes

Unlike the PLL1 which can operate in by-pass and PLL mode, the PLL2 only operates in PLL mode. In PLL mode, DDR2CLKOUT0(P|N) and DDR2CLKOUT1(P|N) are generated by an effective x5 multiplier consisting of the PLL2 fixed x10 multiplier followed by a /2 divider.

The PLL2 is affected by power-on reset. During power-on resets, the internal clocks of the PLL2 are affected as described in Section 7.6 “Reset Controller” on page 123.

PLL2 is unlocked only during the power-up sequence (see Section 7.6 “Reset Controller” on page 123) and is locked by the time the RESETSTAT pin goes high. It does not lose lock during any of the other reset

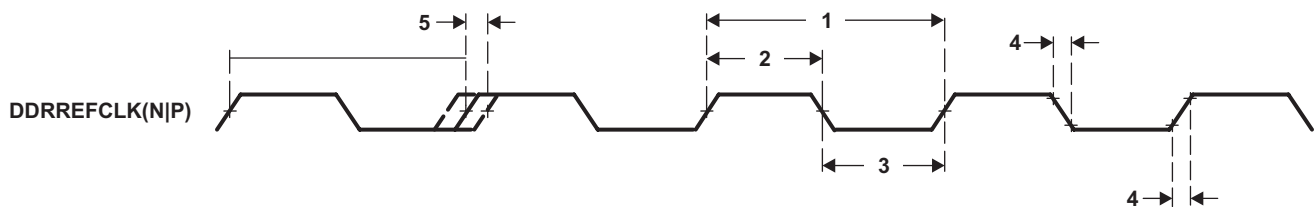
### 7.8.2 PLL2 Input Clock Electrical Data/Timing

**Table 7-53 Timing Requirements for DDRREFCLK(N|P) and ALTDDRCLK<sup>(1)</sup>**  
(see [Figure 7-15](#))

| No.               |                         |                                                           | Min                           | Max                   | Unit |
|-------------------|-------------------------|-----------------------------------------------------------|-------------------------------|-----------------------|------|
| 1                 | t <sub>c(CLKIN2)</sub>  | Cycle time, DDRREFCLK(N P) or ALTDDRCLK                   | 15.00                         | 25.00                 | ns   |
| 2                 | t <sub>w(CLKIN2H)</sub> | Pulse duration, DDRREFCLK(N P) or ALTDDRCLK high          | 0.45 × C <sub>2</sub>         | 0.55 × C <sub>2</sub> | ns   |
| 3                 | t <sub>w(CLKIN2L)</sub> | Pulse duration, DDRREFCLK(N P) or ALTDDRCLK low           | 0.45 × C <sub>2</sub>         | 0.55 × C <sub>2</sub> | ns   |
| 4                 | t <sub>t(CLKIN2)</sub>  | Transition time, DDRREFCLK(N P) or ALTDDRCLK              | 50                            | 1300                  | ps   |
| 5                 | t <sub>j(CLKIN2)</sub>  | Period jitter (peak-to-peak), DDRREFCLK(N P) or ALTDDRCLK | 0.02 × t <sub>c(CLKIN2)</sub> |                       |      |
| End of Table 7-53 |                         |                                                           |                               |                       |      |

<sup>1</sup> If DDRCLKSEL = 0,  $C_2$  = DDRREFCLK(N|P) cycle time in ns. If DDRCLKSEL = 1,  $C_2$  = ALTDDRCLK cycle time in ns.

**Figure 7-15 DDRREFCLK(N|P) Timing**



## 7.9 DDR2 Memory Controller

The 32-bit DDR2 Memory Controller bus of the TMS320C6457 is used to interface to JESD79-2B standard-compliant DDR2 SDRAM devices. The DDR2 external bus interfaces only to DDR2 SDRAM devices; it does not share the bus with any other types of peripherals. The decoupling of DDR2 memories from other devices both simplifies board design and provides I/O concurrency from a second external memory interface, EMIFA.

The internal data bus clock frequency and DDR2 bus clock frequency directly affect the maximum throughput of the DDR2 bus. The clock frequency of the DDR2 bus is equal to the CLKIN2 frequency multiplied by 10. The internal data bus clock frequency of the DDR2 Memory Controller is fixed at a divide-by-three ratio of the CPU frequency. The maximum DDR2 throughput is determined by the smaller of the two bus frequencies. The DDR2 bus is designed to sustain a throughput of up to 2.67 Gbyte/sec at a 667-MHz data rate (333-MHz clock rate) as long as data requests are pending in the DDR2 Memory Controller.

### 7.9.1 DDR2 Memory Controller Device-Specific Information

The approach to specifying interface timing for the DDR2 memory bus is different than on other interfaces such as EMIF, McBSP, and HPI. For these other interfaces, the device timing was specified in terms of data manual specifications and I/O buffer information specification (IBIS) models.

For the C6457 DDR2 memory bus, the approach is to specify compatible DDR2 devices and provide the printed circuit board (PCB) solution and guidelines directly to the user. Texas Instruments (TI) has performed the simulation and system characterization to ensure all DDR2 interface timings in this solution are met. The complete DDR2 system solution is documented in the *TMS320C6457 DDR2 Implementation Guidelines* application report (literature number [SPRAB21](#)).

TI supports only designs that follow the board design guidelines outlined in the application report.

The DDR2 memory controller on the C6457 device supports the following memory topologies:

- A 32-bit wide configuration interfacing to two 16-bit wide DDR2 SDRAM devices.
- A 16-bit wide configuration interfacing to a single 16-bit wide DDR2 SDRAM device.

A race condition may exist when certain masters write data to the DDR2 memory controller. For example, if master A passes a software message via a buffer in external memory and does not wait for indication that the write completes, when master B attempts to read the software message, then the master B read may bypass the master A write and, thus, master B may read stale data and, therefore, receive an incorrect message.

Some master peripherals (e.g., EDMA3 transfer controllers) will always wait for the write to complete before signaling an interrupt to the system, thus avoiding this race condition. For masters that do not have a hardware specification of write-read ordering, it may be necessary to specify data ordering via software.

If master A does not wait for indication that a write is complete, it must perform the following workaround:

1. Perform the required write.
2. Perform a dummy write to the DDR2 memory controller module ID and revision register.
3. Perform a dummy read to the DDR2 memory controller module ID and revision register.
4. Indicate to master B that the data is ready to be read after completion of the read in step 3. The completion of the read in step 3 ensures that the previous write was done.



## 7.9.2 DDR2 Memory Controller Peripheral Register Description(s)

**Table 7-54 DDR2 Memory Controller Registers**

| Hex Address Range        | Acronym | Register Name                                         |
|--------------------------|---------|-------------------------------------------------------|
| 7800 0000                | MIDR    | DDR2 Memory Controller Module and Revision Register   |
| 7800 0004                | DMCSTAT | DDR2 Memory Controller Status Register                |
| 7800 0008                | SDCFG   | DDR2 Memory Controller SDRAM Configuration Register   |
| 7800 000C                | SDRFC   | DDR2 Memory Controller SDRAM Refresh Control Register |
| 7800 0010                | SDTIM1  | DDR2 Memory Controller SDRAM Timing 1 Register        |
| 7800 0014                | SDTIM2  | DDR2 Memory Controller SDRAM Timing 2 Register        |
| 7800 0018                | -       | Reserved                                              |
| 7800 0020                | BPRI0   | DDR2 Memory Controller Burst Priority Register        |
| 7800 0024 - 7800 004C    | -       | Reserved                                              |
| 7800 0050 - 7800 0078    | -       | Reserved                                              |
| 7800 007C - 7800 00BC    | -       | Reserved                                              |
| 7800 00C0 - 7800 00E0    | -       | Reserved                                              |
| 7800 00E4                | DMCCTL  | DDR2 Memory Controller Control Register               |
| 7800 00E8 - 7FFF FFFF    | -       | Reserved                                              |
| <b>End of Table 7-54</b> |         |                                                       |

## 7.9.3 DDR2 Memory Controller Electrical Data/Timing

The *TMS320C6457 DDR2 Implementation Guidelines* application report (literature number [SPRAB21](#)) specifies a complete DDR2 interface solution for the C6457 as well as a list of compatible DDR2 devices. TI has performed the simulation and system characterization to ensure all DDR2 interface timings in this solution are met; therefore, no electrical data/timing information is supplied here for this interface.



**Note**—TI supports *only* designs that follow the board design guidelines outlined in the application report.

## 7.10 External Memory Interface A (EMIFA)

The EMIFA can interface to a variety of external devices or ASICs, including:

- Pipelined and flow-through synchronous-burst SRAM (SBSRAM)
- ZBT (zero bus turnaround) SRAM and late write SRAM
- Synchronous FIFOs
- Asynchronous memory, including SRAM, ROM, and Flash

For more information about the EMIF peripheral, see the *TMS320C6457 DSP External Memory Interface (EMIF) User's Guide* (literature number [SPRUGK2](#)).

### 7.10.1 EMIFA Device-Specific Information

Timing analysis must be done to verify all AC timings are met. TI recommends using I/O buffer information specification (IBIS) to analyze all AC timings.

To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number [SPRA839](#)).

To maintain signal integrity, serial termination resistors should be inserted into all EMIF output signal lines (for the EMIF output signals, see Table 2-6 “[Terminal Functions](#)” on page 33).

A race condition may exist when certain masters write data to the EMIFA. For example, if master A passes a software message via a buffer in external memory and does not wait for indication that the write completes, when master B attempts to read the software message, then the master B read may bypass the master A write and, thus, master B may read stale data and, therefore, receive an incorrect message.

Some master peripherals (e.g., EDMA3 transfer controllers) will always wait for the write to complete before signaling an interrupt to the system, thus avoiding this race condition. For masters that do not have a hardware specification of write-read ordering, it may be necessary to specify data ordering via software.

If master A does not wait for indication that a write is complete, it must perform the following workaround:

1. Perform the required write.
2. Perform a dummy write to the EMIFA module ID and revision register.
3. Perform a dummy read to the EMIFA module ID and revision register.
4. Indicate to master B that the data is ready to be read after completion of the read in step 3. The completion of the read in step 3 ensures that the previous write was done.

### 7.10.2 EMIFA Peripheral Register Description(s)

**Table 7-55 EMIFA Registers**

| Hex Address Range        | Acronym    | Register Name                                 |
|--------------------------|------------|-----------------------------------------------|
| 7000 0000                | MIDR       | Module ID and Revision Register               |
| 7000 0004                | STAT       | Status Register                               |
| 7000 0008                | -          | Reserved                                      |
| 7000 000C - 7000 001C    | -          | Reserved                                      |
| 7000 0020                | BURST_Prio | Burst Priority Register                       |
| 7000 0024 - 7000 004C    | -          | Reserved                                      |
| 7000 0050 - 7000 007C    | -          | Reserved                                      |
| 7000 0080                | CE2CFG     | EMIFA CE2 Configuration Register              |
| 7000 0084                | CE3CFG     | EMIFA CE3 Configuration Register              |
| 7000 0088                | CE4CFG     | EMIFA CE4 Configuration Register              |
| 7000 008C                | CE5CFG     | EMIFA CE5 Configuration Register              |
| 7000 0090 - 7000 009C    | -          | Reserved                                      |
| 7000 00A0                | AWCC       | EMIFA Async Wait Cycle Configuration Register |
| 7000 00A4 - 7000 00BC    | -          | Reserved                                      |
| 7000 00C0                | INTRAW     | EMIFA Interrupt RAW Register                  |
| 7000 00C4                | INTMSK     | EMIFA Interrupt Masked Register               |
| 7000 00C8                | INTMSKSET  | EMIFA Interrupt Mask Set Register             |
| 7000 00CC                | INTMSKCLR  | EMIFA Interrupt Mask Clear Register           |
| 7000 00D0 - 7000 00DC    | -          | Reserved                                      |
| 7000 00E0 - 77FF FFFF    | -          | Reserved                                      |
| <b>End of Table 7-55</b> |            |                                               |

### 7.10.3 EMIFA Electrical Data/Timing

This section describes the electrical timing for the EMIFA peripheral.

#### 7.10.3.1 AECLKIN and AECLKOUT Timing

**Table 7-56** EMIFA AECLKIN Timing Requirements <sup>(1) (2)</sup>  
(see Figure 7-16)

| No. |                                            | Min               | Max                  | Unit |
|-----|--------------------------------------------|-------------------|----------------------|------|
| 1   | $t_{c(EKI)}$ Cycle time, AECLKIN           | 10 <sup>(3)</sup> | 40                   | ns   |
| 2   | $t_{w(EKIH)}$ Pulse duration, AECLKIN high | 2.7               |                      | ns   |
| 3   | $t_{w(EKIL)}$ Pulse duration, AECLKIN low  | 2.7               |                      | ns   |
| 4   | $t_{t(EKI)}$ Transition time, AECLKIN      |                   | 2                    | ns   |
| 5   | $t_{j(EKI)}$ Period Jitter, AECLKIN        |                   | 0.02E <sup>(4)</sup> | ns   |

**End of Table 7-56**

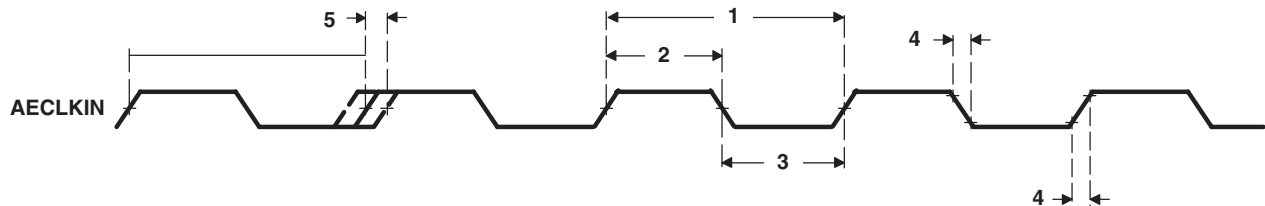
1 The reference points for the rise and fall transitions are measured at  $V_{IL}$  MAX and  $V_{IH}$  MIN.

2 E = the EMIF input clock (AECLKIN or SYSCLK7) period in ns for EMIFA.

3 Minimum AECLKIN cycle times must be met, even when AECLKIN is generated by an internal clock source. Minimum AECLKIN times are based on internal logic speed; the maximum usable speed of the EMIF may be lower due to AC timing requirements.

4 This timing applies only when AECLKIN is used for EMIFA.

**Figure 7-16** EMIFA AECLKIN Timing



**Table 7-57** EMIFA AECLKOUT Switching Characteristics <sup>(1) (2) (3) (4)</sup>  
(see Figure 7-17)

| No. | Parameter                                                    | Min      | Max      | Unit |
|-----|--------------------------------------------------------------|----------|----------|------|
| 1   | $t_{c(EKO)}$ Cycle time, AECLKOUT                            | E - 0.7  | E + 0.7  | ns   |
| 2   | $t_{w(EKOH)}$ Pulse duration, AECLKOUT high                  | EH - 0.7 | EH + 0.7 | ns   |
| 3   | $t_{w(EKOL)}$ Pulse duration, AECLKOUT low                   | EL - 0.7 | EL + 0.7 | ns   |
| 4   | $t_{t(EKO)}$ Transition time, AECLKOUT                       |          | 1        | ns   |
| 5   | $t_{d(EKIH-EKOH)}$ Delay time, AECLKIN high to AECLKOUT high | 1        | 8        | ns   |
| 6   | $t_{d(EKIL-EKOL)}$ Delay time, AECLKIN low to AECLKOUT low   | 1        | 8        | ns   |

**End of Table 7-57**

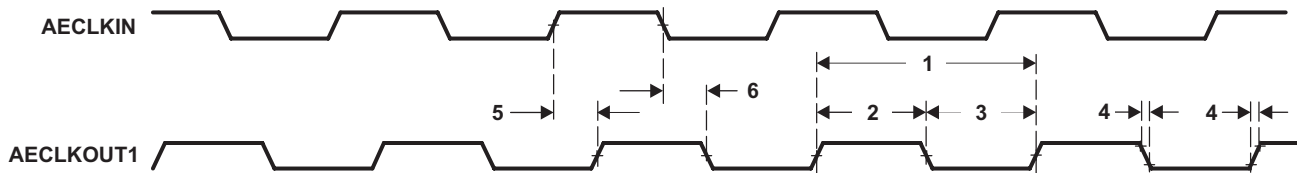
1 Over Recommended Operating Conditions.

2 E = the EMIF input clock (AECLKIN or SYSCLK7) period in ns for EMIFA.

3 The reference points for the rise and fall transitions are measured at  $V_{OL}$  MAX and  $V_{OH}$  MIN.

4 EH is the high period of E (EMIF input clock period) in ns and EL is the low period of E (EMIF input clock period) in ns for EMIFA.

**Figure 7-17** EMIFA AECLKOUT Timing



### 7.10.3.2 Asynchronous Memory Timing

This section describes the asynchronous EMIFA Read, Write, EM\_WAIT Read and EM\_WAIT Write timing requirements and switching characteristics.

**Table 7-58 EMIFA Asynchronous Memory Read Switching Characteristics** <sup>(1) (2)</sup>  
(see Figure 7-18)

| No.               | Parameter             |                                                                                                                           | Min                                | Max                                | Unit                   |    |
|-------------------|-----------------------|---------------------------------------------------------------------------------------------------------------------------|------------------------------------|------------------------------------|------------------------|----|
| 3                 | $t_{c(ACEL-read)}$    | EMIF read cycle time when ew = 0. Meaning not in extended wait mode                                                       | $(RS + RST + RH + 3) \times E - 1$ | $(RS + RST + RH + 3) \times E + 1$ | ns                     |    |
|                   |                       | EMIF read cycle time when ew = 1. Meaning extended wait mode enabled                                                      | $(RS + RST + RH + 3) \times E - 1$ | $(RS + RST + RH + 3) \times E + 1$ | ns                     |    |
| 4                 | $t_{osu(ACEL-AAOEL)}$ | Output setup time from $\overline{ACEn}$ low to $\overline{AAOE}/\overline{ASOE}$ low. SS = 0, not in select strobe mode  | $(RS+1) \times E-1.5$              |                                    | ns                     |    |
|                   |                       | Output setup time from $\overline{ACEn}$ low to $\overline{AAOE}/\overline{ASOE}$ low. SS = 1, in select strobe mode      |                                    |                                    |                        |    |
| 5                 | $t_{oh(AAOEH-ACEH)}$  | Output hold time from $\overline{AAOE}/\overline{ASOE}$ high to $\overline{ACEn}$ high. SS = 0, not in select strobe mode | $(RS+1) \times E-1.9$              |                                    | ns                     |    |
|                   |                       | Output hold time from $\overline{AAOE}/\overline{ASOE}$ high to $\overline{ACEn}$ high. SS = 1, in select strobe mode     |                                    |                                    |                        |    |
| 6                 | $t_{osu(ABAV-AAOEL)}$ | Output setup time from ABA valid to $\overline{AAOE}/\overline{ASOE}$ low                                                 | $(RS+1) \times E-1.5$              |                                    | ns                     |    |
| 7                 | $t_{oh(AAOEH-ABAV)}$  | Output hold time from $\overline{AAOE}/\overline{ASOE}$ high to BA invalid                                                | $(RS+1) \times E-1.9$              |                                    | ns                     |    |
| 8                 | $t_{osu(AEAV-OEL)}$   | Output setup time from AEA valid to $\overline{AAOE}/\overline{ASOE}$ low                                                 | $(RS+1) \times E-1.5$              |                                    | ns                     |    |
| 9                 | $t_{oh(AAOEH-AEAV)}$  | Output hold time from $\overline{AAOE}/\overline{ASOE}$ high to AEA invalid                                               | $(RS+1) \times E-1.9$              |                                    | ns                     |    |
| 10                | $t_{w(AAOEL)}$        | $\overline{AAOE}/\overline{ASOE}$ active time low, when ew = 0, extended wait mode is disabled                            | $(RST+1) \times E - 6$             |                                    | $(RST+1) \times E + 6$ | ns |
|                   |                       | $\overline{AAOE}/\overline{ASOE}$ active time low, when ew = 1, extended wait mode is enabled                             |                                    |                                    |                        |    |
| End of Table 7-58 |                       |                                                                                                                           |                                    |                                    |                        |    |

1 E = the EMIF input clock (AECLKIN or SYSCLK7) period in ns for EMIFA.

2 RS, RST, RH, WS, WST, WH, and TA are all based on the memory mapped register values. This means that the actual value listed here is the value in EMIF cycles - 1.  
Example: For read setup of 1 EMIF cycle, RS = 0.

**Table 7-59 EMIFA Asynchronous Memory Read Timing Requirements**  
(see Figure 7-18)

| No.                      | Parameter                                                                                      | Min | Max | Unit |
|--------------------------|------------------------------------------------------------------------------------------------|-----|-----|------|
| 12                       | $t_{su(AEDV-AAOEH)}$ Input setup time from AED valid to $\overline{AAOE}/\overline{ASOE}$ high | 6.5 |     | ns   |
| 13                       | $t_{h(AAOEH-AEDV)}$ Input hold time from $\overline{AAOE}/\overline{ASOE}$ high to AED invalid | 0   |     | ns   |
| <b>End of Table 7-59</b> |                                                                                                |     |     |      |

Figure 7-18 EMIFA Asynchronous Memory Read Timing

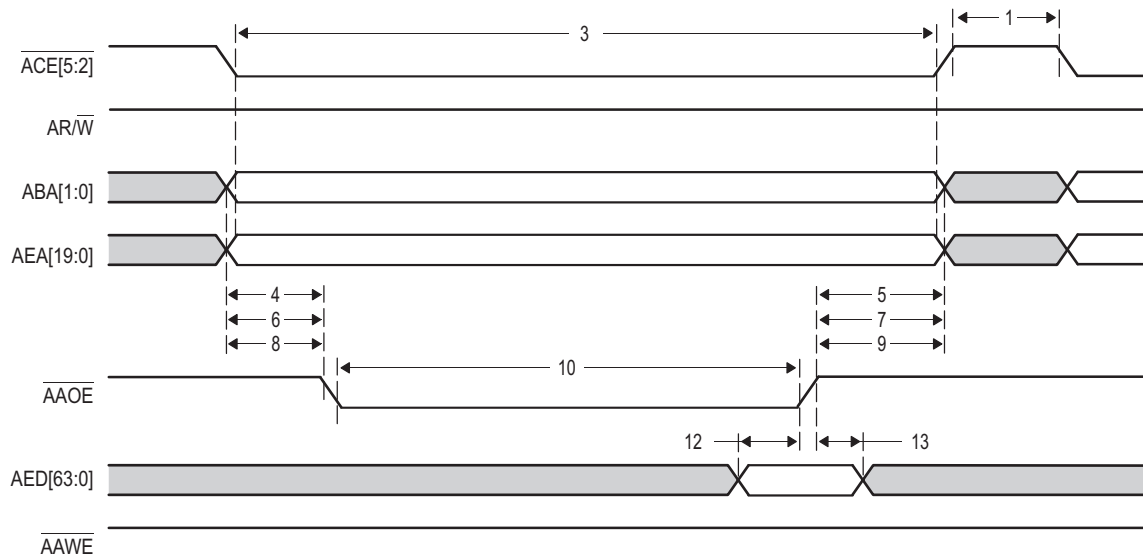


Table 7-60 EMIFA Asynchronous Memory Write Timing Requirements <sup>(1)</sup> <sup>(2)</sup>  
(see Figure 7-19)

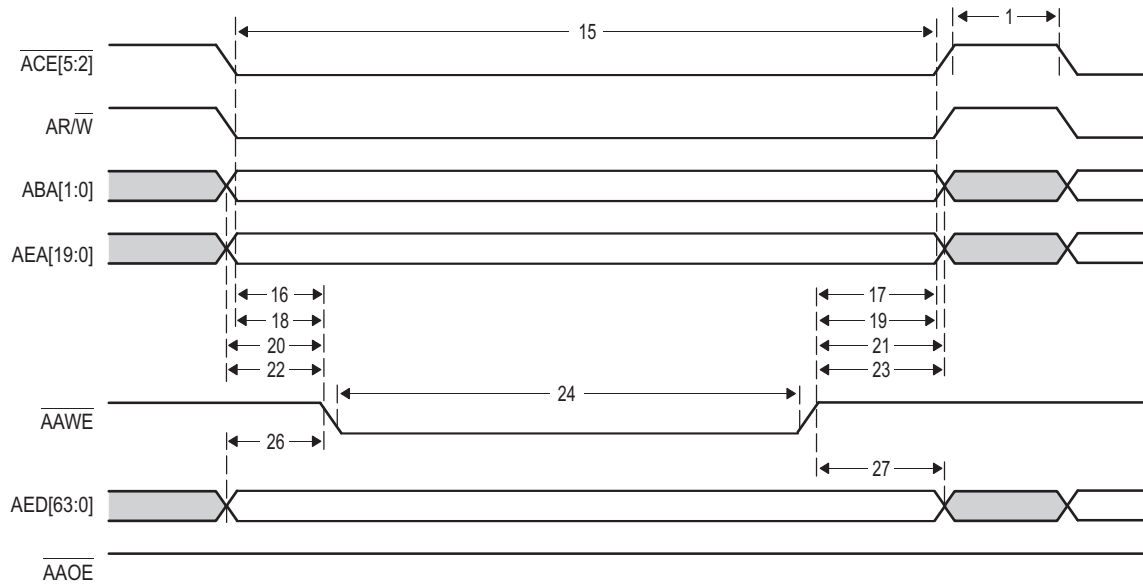
| No.               |                                                                                                                       | Min                                                                                                                       | Max | Unit |
|-------------------|-----------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|-----|------|
| 15                | $t_{c(ACEL-write)}$                                                                                                   | EMIF write cycle time when ew = 0, extended wait mode                                                                     |     | ns   |
|                   | EMIF write cycle time when ew = 1, extended wait mode is enabled.                                                     |                                                                                                                           |     |      |
| 16                | $t_{osu(ACEL-AAWEL)}$                                                                                                 | Output setup time from $\overline{ACEN}$ low to $\overline{ASWE}/\overline{AAWE}$ low. SS = 0, not in select strobe mode  |     | ns   |
|                   | Output setup time from $\overline{ACEN}$ low to $\overline{ASWE}/\overline{AAWE}$ low. SS = 1, in select strobe mode  |                                                                                                                           |     |      |
| 17                | $t_{oh(AAWEH-ACEH)}$                                                                                                  | Output hold time from $\overline{ASWE}/\overline{AAWE}$ high to $\overline{ACEN}$ high. SS = 0, not in select strobe mode |     | ns   |
|                   | Output hold time from $\overline{ASWE}/\overline{AAWE}$ high to $\overline{ACEN}$ high. SS = 1, in select strobe mode |                                                                                                                           |     |      |
| 18                | $t_{osu(WV-AAWEL)}$                                                                                                   | Output setup time from $AR/\overline{W}$ valid to $\overline{ASWE}/\overline{AAWE}$ low                                   |     | ns   |
| 19                | $t_{oh(AAWEH-WIV)}$                                                                                                   | Output hold time from $\overline{ASWE}/\overline{AAWE}$ high to $AR/\overline{W}$ invalid                                 |     | ns   |
| 20                | $t_{osu(ABAV-AAWEL)}$                                                                                                 | Output setup time from BA valid to $\overline{ASWE}/\overline{AAWE}$ low                                                  |     | ns   |
| 21                | $t_{oh(AAWEH-ABAV)}$                                                                                                  | Output hold time from $\overline{ASWE}/\overline{AAWE}$ high to ABA invalid                                               |     | ns   |
| 22                | $t_{osu(AEAV-AAWEL)}$                                                                                                 | Output setup time from $\overline{AEA}$ valid to $\overline{ASWE}/\overline{AAWE}$ low                                    |     | ns   |
| 23                | $t_{oh(AAWEH-AEAV)}$                                                                                                  | Output hold time from $\overline{ASWE}/\overline{AAWE}$ high to $\overline{AEA}$ invalid                                  |     | ns   |
| 24                | $t_{w(AAWEL)}$                                                                                                        | $\overline{ASWE}/\overline{AAWE}$ active time low, when ew = 0. Extended wait mode is disabled.                           |     | ns   |
|                   | $\overline{ASWE}/\overline{AAWE}$ active time low, when ew = 1. Extended wait mode is enabled.                        |                                                                                                                           |     |      |
| 26                | $t_{osu(AEDV-AAWEL)}$                                                                                                 | Output setup time from AED valid to $\overline{ASWE}/\overline{AAWE}$ low                                                 |     | ns   |
| 27                | $t_{oh(AAWEH-AEDIV)}$                                                                                                 | Output hold time from $\overline{ASWE}/\overline{AAWE}$ high to AED invalid                                               |     | ns   |
| End of Table 7-60 |                                                                                                                       |                                                                                                                           |     |      |

End of Table 7-60

<sup>1</sup> E = the EMIF input clock (AECLKIN or SYSCLK7) period in ns for EMIFA.

<sup>2</sup> RS, RST, RH, WS, WST, WH, and TA are all based on the memory mapped register values. This means that the actual value listed here is the value in EMIF cycles - 1.  
Example: For read setup of 1 EMIF cycle, RS = 0.

**Figure 7-19 EMIFA Asynchronous Memory Write Timing**



**Table 7-61 EMIFA EM\_Wait Read Timing Requirements <sup>(1)</sup>**  
(see Figure 7-20)

| No. | Parameter                                                                   | Min | Max    | Unit |
|-----|-----------------------------------------------------------------------------|-----|--------|------|
| 2   | $t_{w(AARDY)}$ Pulse duration, AARDY assertion and deassertion minimum time |     | 2E     |      |
| 14  | $t_{d(AARDY-AAOE)}$ Setup time, AARDY asserted before AAOE high             |     | 4E + 6 |      |

**End of Table 7-61**

<sup>1</sup> E = the EMIF input clock (AECLKIN or SYSCLK7) period in ns for EMIFA.

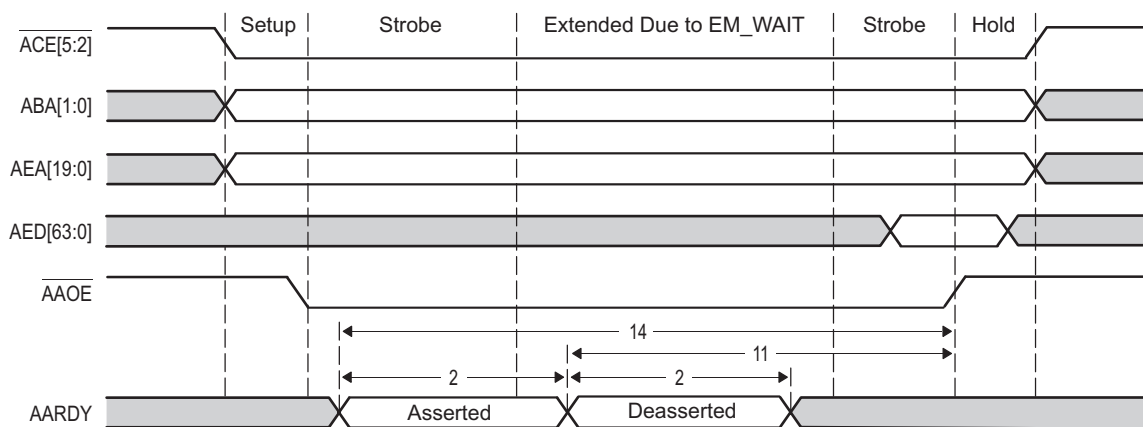
**Table 7-62 EMIFA EM\_Wait Read Switching Characteristics <sup>(1)</sup>**  
(see Figure 7-20)

| No. | Parameter                                                               | Min | Max    | Unit |
|-----|-------------------------------------------------------------------------|-----|--------|------|
| 11  | $t_{d(AARDYH-AAOE)}$ Delay time from AARDY deasserted to AAOE/ASOE high |     | 4E + 6 |      |

**End of Table 7-62**

<sup>1</sup> E = the EMIF input clock (AECLKIN or SYSCLK7) period in ns for EMIFA.

**Figure 7-20 EMIFA EM\_Wait Read Timing**



**Table 7-63 EMIFA EM\_Wait Write Timing Requirements**  
(see Figure 7-21)

| No.                      |                                                                                       | Min | Nom      | Max | Unit |
|--------------------------|---------------------------------------------------------------------------------------|-----|----------|-----|------|
| 2                        | $t_{w(AARDY)}$ Pulse duration, AARDY assertion and deassertion minimum time           |     |          | 2E  |      |
| 25                       | $t_{d(AARDYH-AAWEH)}$ Delay time from AARDY deasserted to $\overline{ASWE}/AAWE$ high |     | 4E + 6.0 |     |      |
| 28                       | $t_{su(AARDY-AAWEH)}$ Setup time, AARDY asserted before $\overline{ASWE}/AAWE$ high   |     | 4E + 6.0 |     |      |
| <b>End of Table 7-63</b> |                                                                                       |     |          |     |      |

**Figure 7-21 EMIFA EM\_Wait Write Timing**



### 7.10.3.3 Programmable Synchronous Interface Timing

This section describes the synchronous EMIFA Read and Write timing requirements.

The following parameters are programmable via the EMIFA CE Configuration registers (CEnCFG) (see Table 7-65) and via the EMIFA Chip Select *n* Configuration Register (CESECn):

- **Read latency (R\_LTNCY):** 1-, 2-, or 3-cycle read latency
- **Write latency (W\_LTNCY):** 0-, 1-, 2-, or 3-cycle write latency
- **ACEx assertion length (CE\_EXT):** For standard SBSRAM or ZBT SRAM interface,  $\overline{ACEx}$  goes inactive after the final command has been issued ( $CE\_EXT = 0$ ). For synchronous FIFO interface, ACEx is active when ASOE is active ( $CE\_EXT = 1$ ).
- **Function of  $\overline{ASADS}/\overline{ASRE}$  (R\_ENABLE):** For standard SBSRAM or ZBT SRAM interface,  $\overline{ASADS}/\overline{ASRE}$  acts as  $\overline{ASADS}$  with deselect cycles ( $R\_ENABLE = 0$ ). For FIFO interface,  $\overline{ASADS}/\overline{ASRE}$  acts as  $\overline{SRE}$  with NO deselect cycles ( $R\_ENABLE = 1$ ).

Figure 7-22, Figure 7-23, and Figure 7-24 are given as examples diagrams depicting some of the programmable options.

- In Figure 7-22,  $R\_LTNCY = 2$ ,  $CE\_EXT = 0$ ,  $R\_ENABLE = 0$ , and  $SSEL = 1$ .
- In Figure 7-23,  $W\_LTNCY = 0$ ,  $CE\_EXT = 0$ ,  $R\_ENABLE = 0$ , and  $SSEL = 1$ .
- In Figure 7-24,  $W\_LTNCY = 1$ ,  $CE\_EXT = 0$ ,  $R\_ENABLE = 0$ , and  $SSEL = 1$ .

**Table 7-64 Timing Requirements for Programmable Synchronous Interface Cycles for EMIFA Module**  
(see Figure 7-22)

| No.                      |                                                                     | Min | Max | Unit |
|--------------------------|---------------------------------------------------------------------|-----|-----|------|
| 6                        | $t_{su(EDV-EKOH)}$ Setup time, read AEDx valid before AECLKOUT high | 2   |     | ns   |
| 7                        | $t_{h(EKOH-EDV)}$ Hold time, read AEDx valid after AECLKOUT high    | 1.5 |     | ns   |
| <b>End of Table 7-64</b> |                                                                     |     |     |      |

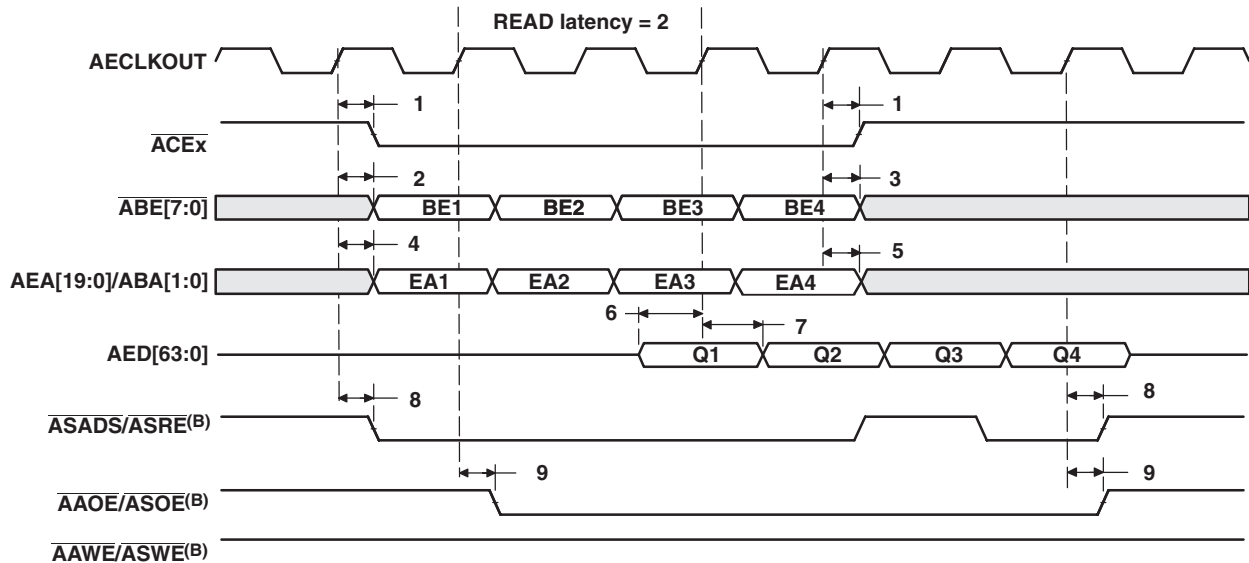
**Table 7-65 Switching Characteristics for Programmable Synchronous Interface Cycles for EMIFA Module<sup>(1)</sup>**  
(see Figure 7-22, Figure 7-23, and Figure 7-24)

| No. | Parameter                                                                                | Min | Max | Unit |
|-----|------------------------------------------------------------------------------------------|-----|-----|------|
| 1   | $t_{d(EKOH-CEV)}$ Delay time, AECLKOUT high to $\overline{ACEx}$ valid                   | 1.3 | 4.9 | ns   |
| 2   | $t_{d(EKOH-BEV)}$ Delay time, AECLKOUT high to $\overline{ABEx}$ valid                   |     | 4.9 | ns   |
| 3   | $t_{d(EKOH-BEIV)}$ Delay time, AECLKOUT high to $\overline{ABEx}$ invalid                | 1.3 |     | ns   |
| 4   | $t_{d(EKOH-EAV)}$ Delay time, AECLKOUT high to AEAx valid                                |     | 4.9 | ns   |
| 5   | $t_{d(EKOH-EAIV)}$ Delay time, AECLKOUT high to AEAx invalid                             | 1.3 |     | ns   |
| 8   | $t_{d(EKOH-ADSV)}$ Delay time, AECLKOUT high to $\overline{ASADS}/\overline{ASRE}$ valid | 1.3 | 4.9 | ns   |
| 9   | $t_{d(EKOH-OEV)}$ Delay time, AECLKOUT high to $\overline{ASOE}$ valid                   | 1.3 | 4.9 | ns   |
| 10  | $t_{d(EKOH-EDV)}$ Delay time, AECLKOUT high to AEDx valid                                |     | 5.2 | ns   |
| 11  | $t_{d(EKOH-EDIV)}$ Delay time, AECLKOUT high to AEDx invalid                             | 1.3 |     | ns   |
| 12  | $t_{d(EKOH-WEV)}$ Delay time, AECLKOUT high to $\overline{ASWE}$ valid                   | 1.3 | 4.9 | ns   |

**End of Table 7-65**

<sup>1</sup> Over recommended operating conditions.

**Figure 7-22 EMIFA Programmable Synchronous Interface Read Timing (With Read Latency = 2)<sup>(A)</sup>**

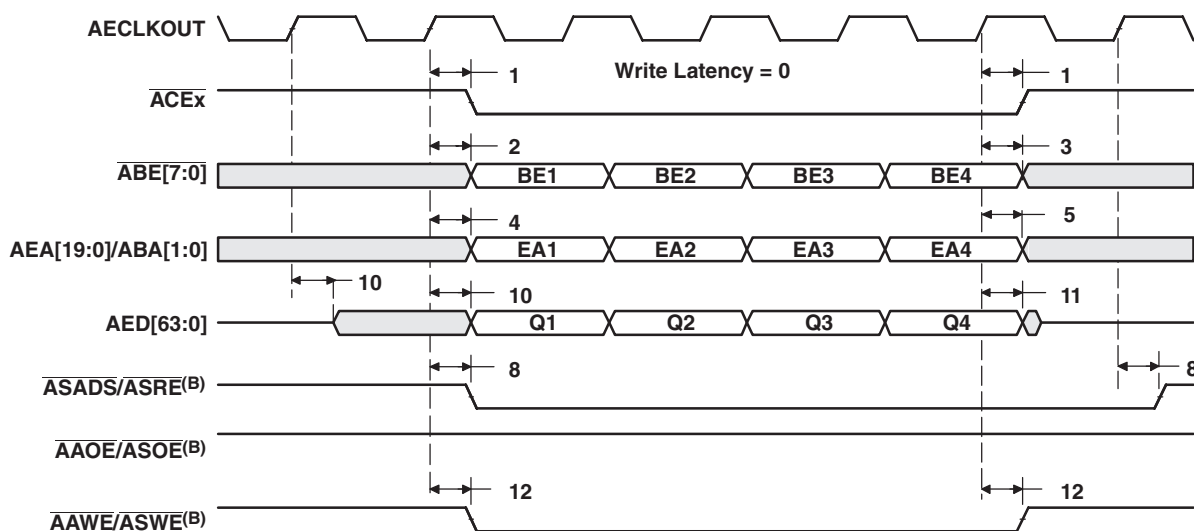


(A) In this figure R\_LTNKY = 2, CE\_EXT = 0, R\_ENABLE = 0, and SSEL = 1.

(B) AAOE/ASOE, and AAW/ASWE operate as ASOE, and ASWE, respectively, during programmable synchronous interface accesses.



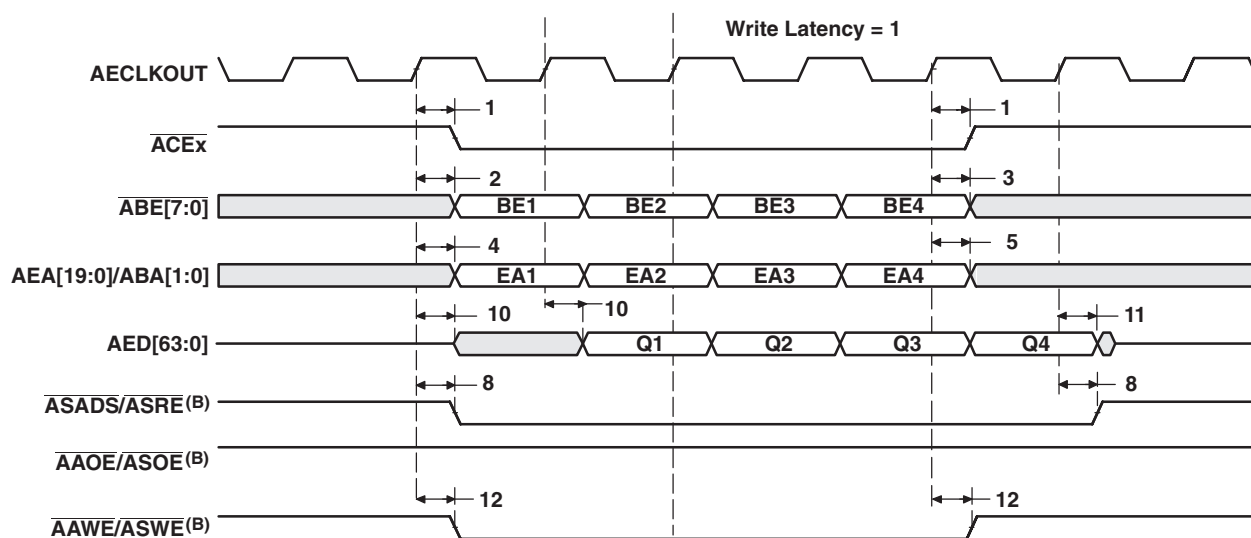
Figure 7-23 EMIFA Programmable Synchronous Interface Write Timing (With Write Latency = 0)<sup>(A)</sup>



(A) In this figure W\_LTNCY = 0, CE\_EXT = 0, R\_ENABLE = 0, and SSEL = 1.

(B) AAOE/ASOE, and AAWE/ASWE operate as ASOE, and ASWE, respectively, during programmable synchronous interface accesses.

Figure 7-24 EMIFA Programmable Synchronous Interface Write Timing (With Write Latency = 1)<sup>(A)</sup>



(A) In this figure W\_LTNCY = 1, CE\_EXT = 0, R\_ENABLE = 0, and SSEL = 1.

(B) AAOE/ASOE, and AAWE/ASWE operate as ASOE, and ASWE, respectively, during programmable synchronous interface accesses.

## 7.11 I<sup>2</sup>C Peripheral

The inter-integrated circuit (I<sup>2</sup>C) module provides an interface between a C64x+ DSP and other devices compliant with Philips Semiconductors Inter-IC bus (I<sup>2</sup>C bus) specification version 2.1 and connected by way of an I<sup>2</sup>C bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the DSP through the I<sup>2</sup>C module.

### 7.11.1 I<sup>2</sup>C Device-Specific Information

The TMS320C6457 device includes an I<sup>2</sup>C peripheral module. NOTE: when using the I<sup>2</sup>C module, ensure there are external pullup resistors on the SDA and SCL pins.

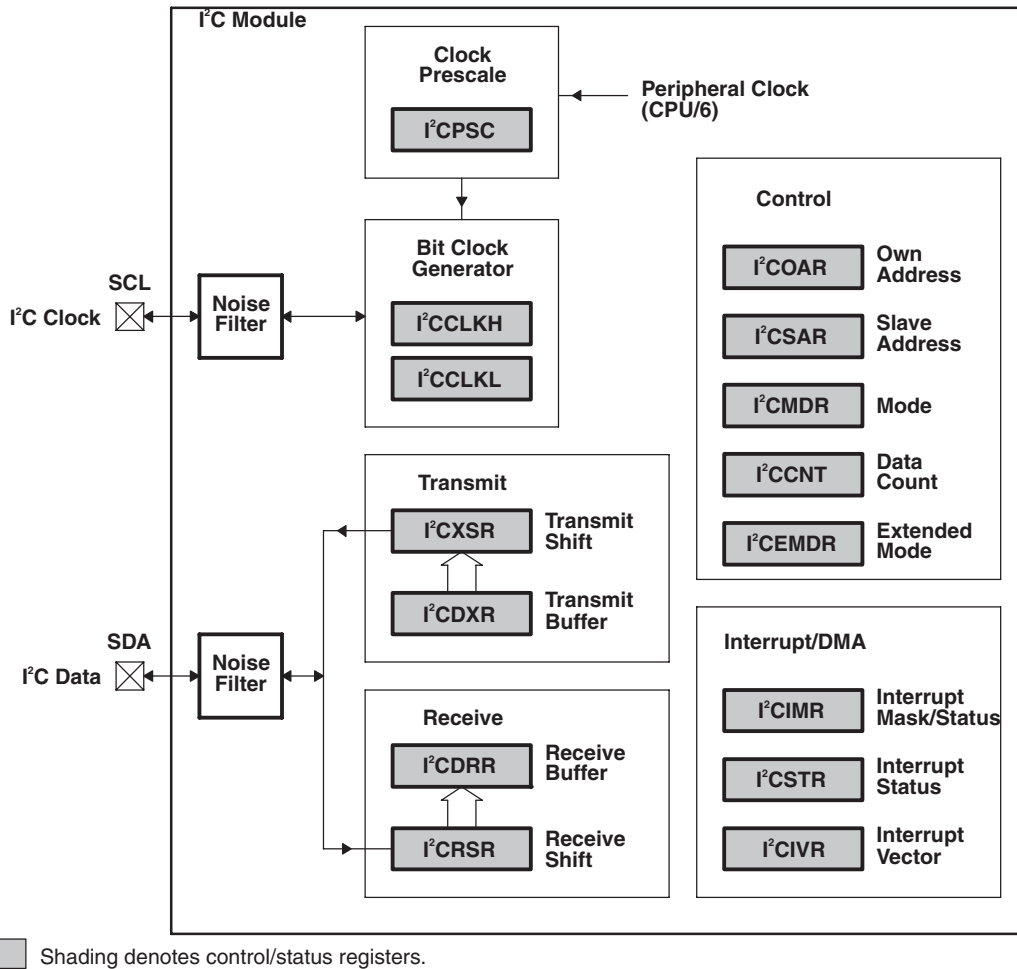
The I<sup>2</sup>C modules on the C6457 may be used by the DSP to control local peripheral ICs (DACs, ADCs, etc.) or may be used to communicate with other controllers in a system or to implement a user interface.

The I<sup>2</sup>C port supports:

- Compatible with Philips I<sup>2</sup>C specification revision 2.1 (January 2000)
- Fast mode up to 400 Kbps (no fail-safe I/O buffers)
- Noise filter to remove noise 50 ns or less
- 7-bit and 10-bit device addressing modes
- Multi-master (transmit/receive) and slave (transmit/receive) functionality
- Events: DMA, interrupt, or polling
- Slew-rate limited open-drain output buffers

Figure 7-25 shows a block diagram of the I<sup>2</sup>C module.

Figure 7-25 I<sup>2</sup>C Module Block Diagram



### 7.11.2 I<sup>2</sup>C Peripheral Register Description(s)

Table 7-66 I<sup>2</sup>C Registers (Part 1 of 2)

| Hex Address Range | Acronym | Register Name                                     |
|-------------------|---------|---------------------------------------------------|
| 02B0 4000         | ICOAR   | I <sup>2</sup> C own address register             |
| 02B0 4004         | ICIMR   | I <sup>2</sup> C interrupt mask/status register   |
| 02B0 4008         | ICSTR   | I <sup>2</sup> C interrupt status register        |
| 02B0 400C         | ICCLKL  | I <sup>2</sup> C clock low-time divider register  |
| 02B0 4010         | ICCLKH  | I <sup>2</sup> C clock high-time divider register |
| 02B0 4014         | ICCNT   | I <sup>2</sup> C data count register              |
| 02B0 4018         | ICDRR   | I <sup>2</sup> C data receive register            |
| 02B0 401C         | ICSAR   | I <sup>2</sup> C slave address register           |
| 02B0 4020         | ICDXR   | I <sup>2</sup> C data transmit register           |
| 02B0 4024         | ICMDR   | I <sup>2</sup> C mode register                    |
| 02B0 4028         | ICIVR   | I <sup>2</sup> C interrupt vector register        |
| 02B0 402C         | ICEMDR  | I <sup>2</sup> C extended mode register           |
| 02B0 4030         | ICPSC   | I <sup>2</sup> C prescaler register               |

**Table 7-66** I<sup>2</sup>C Registers (Part 2 of 2)

| Hex Address Range        | Acronym | Register Name                                                              |
|--------------------------|---------|----------------------------------------------------------------------------|
| 02B0 4034                | ICPID1  | I <sup>2</sup> C peripheral identification register 1 [Value: 0x0000 0105] |
| 02B0 4038                | ICPID2  | I <sup>2</sup> C peripheral identification register 2 [Value: 0x0000 0005] |
| 02B0 403C - 02B0 405C    | -       | Reserved                                                                   |
| 02B0 4060 - 02B3 407F    | -       | Reserved                                                                   |
| 02B0 4080 - 02B3 FFFF    | -       | Reserved                                                                   |
| <b>End of Table 7-66</b> |         |                                                                            |

### 7.11.3 I<sup>2</sup>C Electrical Data/Timing

#### 7.11.3.1 Inter-Integrated Circuits (I<sup>2</sup>C) Timing

**Table 7-67** I<sup>2</sup>C Timing Requirements <sup>(1)</sup>  
(see Figure 7-26)

| No.                      |                               |                                                                               | Standard Mode    |      | Fast Mode                             |                    | Units |
|--------------------------|-------------------------------|-------------------------------------------------------------------------------|------------------|------|---------------------------------------|--------------------|-------|
|                          |                               |                                                                               | Min              | Max  | Min                                   | Max                |       |
| 1                        | t <sub>c(SCL)</sub>           | Cycle time, SCL                                                               | 10               |      | 2.5                                   |                    | us    |
| 2                        | t <sub>su(SCLH-SDAL)</sub>    | Setup time, SCL high before SDA low (for a repeated START condition)          | 4.7              |      | 0.6                                   |                    | us    |
| 3                        | t <sub>h(SDAL-SCLL)</sub>     | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4                |      | 0.6                                   |                    | us    |
| 4                        | t <sub>w(SCLL)</sub>          | Pulse duration, SCL low                                                       | 4.7              |      | 1.3                                   |                    | us    |
| 5                        | t <sub>w(SCLH)</sub>          | Pulse duration, SCL high                                                      | 4                |      | 0.6                                   |                    | us    |
| 6                        | t <sub>su(SDAV-SCLH)</sub>    | Setup time, SDA valid before SCL high                                         | 250              |      | 100 <sup>(2)</sup>                    |                    | ns    |
| 7                        | t <sub>h(SCLL-SDAV)</sub>     | Hold time, SDA valid after SCL low (For I <sup>2</sup> C bus devices)         | 0 <sup>(3)</sup> | 3.45 | 0 <sup>(3)</sup>                      | 0.9 <sup>(4)</sup> | us    |
| 8                        | t <sub>w(SDAH)</sub>          | Pulse duration, SDA high between STOP and START conditions                    | 4.7              |      | 1.3                                   |                    | us    |
| 9                        | t <sub>r(SDA)</sub>           | Rise time, SDA                                                                |                  | 1000 | 20 + 0.1C <sub>b</sub> <sup>(5)</sup> | 300                | ns    |
| 10                       | t <sub>r(SCL)</sub>           | Rise time, SCL                                                                |                  | 1000 | 20 + 0.1C <sub>b</sub> <sup>(5)</sup> | 300                | ns    |
| 11                       | t <sub>f(SDA)</sub>           | Fall time, SDA                                                                |                  | 300  | 20 + 0.1C <sub>b</sub> <sup>(5)</sup> | 300                | ns    |
| 12                       | t <sub>f(SCL)</sub>           | Fall time, SCL                                                                |                  | 300  | 20 + 0.1C <sub>b</sub> <sup>(5)</sup> | 300                | ns    |
| 13                       | t <sub>su(SCLH-SDAH)</sub>    | Setup time, SCL high before SDA high (for STOP condition)                     | 4                |      | 0.6                                   |                    | us    |
| 14                       | t <sub>w(SP)</sub>            | Pulse duration, spike (must be suppressed)                                    |                  |      | 0                                     | 50                 | ns    |
| 15                       | C <sub>b</sub> <sup>(5)</sup> | Capacitive load for each bus line                                             |                  | 400  |                                       | 400                | pF    |
| <b>End of Table 7-67</b> |                               |                                                                               |                  |      |                                       |                    |       |

1 The I<sup>2</sup>C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down

2 A Fast-mode I<sup>2</sup>C-bus™ device can be used in a Standard-mode I<sup>2</sup>C-bus™ system, but the requirement t<sub>su(SDA-SCLH)</sub> ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t<sub>r</sub> max + t<sub>su(SDA-SCLH)</sub> = 1000 + 250 = 1250 ns (according to the Standard-mode I<sup>2</sup>C-Bus Specification) before the SCL line is released.

3 A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IHmin</sub> of the SCL signal) to bridge the undefined region of the falling edge of SCL.

4 The maximum t<sub>h(SDAL-SCLL)</sub> has only to be met if the device does not stretch the low period [t<sub>w(SCLL)</sub>] of the SCL signal.

5 C<sub>b</sub> = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

Figure 7-26 I<sup>2</sup>C Receive Timing

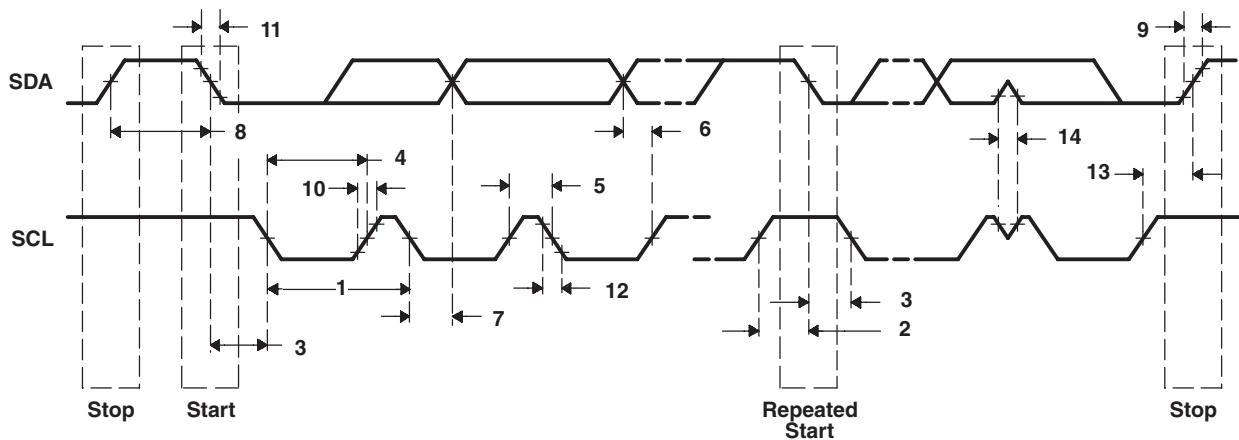


Table 7-68 I<sup>2</sup>C Switching Characteristics <sup>(1)</sup>  
(see Figure 7-27)

| No. | Parameter                                                                                        | Standard Mode |      | Fast Mode           |     | Unit |
|-----|--------------------------------------------------------------------------------------------------|---------------|------|---------------------|-----|------|
|     |                                                                                                  | Min           | Max  | Min                 | Max |      |
| 16  | $t_{c(SCL)}$ Cycle time, SCL                                                                     | 10            |      | 2.5                 |     | ms   |
| 17  | $t_{su(SCLH-SDAL)}$ Setup time, SCL high to SDA low (for a repeated START condition)             | 4.7           |      | 0.6                 |     | ms   |
| 18  | $t_{h(SDAL-SCLL)}$ Hold time, SDA low after SCL low (for a START and a repeated START condition) | 4             |      | 0.6                 |     | ms   |
| 19  | $t_{w(SCLL)}$ Pulse duration, SCL low                                                            | 4.7           |      | 1.3                 |     | ms   |
| 20  | $t_{w(SCLH)}$ Pulse duration, SCL high                                                           | 4             |      | 0.6                 |     | ms   |
| 21  | $t_{d(SDAV-SDLH)}$ Delay time, SDA valid to SCL high                                             | 250           |      | 100                 |     | ns   |
| 22  | $t_{v(SDLL-SDAV)}$ Valid time, SDA valid after SCL low (For I <sup>2</sup> C bus devices)        | 0             |      | 0                   | 0.9 | ms   |
| 23  | $t_{w(SDAH)}$ Pulse duration, SDA high between STOP and START conditions                         | 4.7           |      | 1.3                 |     | ms   |
| 24  | $t_r(SDA)$ Rise time, SDA                                                                        |               | 1000 | $20 + 0.1C_b^{(1)}$ | 300 | ns   |
| 25  | $t_r(SCL)$ Rise time, SCL                                                                        |               | 1000 | $20 + 0.1C_b^{(1)}$ | 300 | ns   |
| 26  | $t_f(SDA)$ Fall time, SDA                                                                        |               | 300  | $20 + 0.1C_b^{(1)}$ | 300 | ns   |
| 27  | $t_f(SCL)$ Fall time, SCL                                                                        |               | 300  | $20 + 0.1C_b^{(1)}$ | 300 | ns   |
| 28  | $t_{d(SCLH-SDAH)}$ Delay time, SCL high to SDA high (for STOP condition)                         | 4             |      | 0.6                 |     | ms   |
| 29  | $C_p$ Capacitance for each I <sup>2</sup> C pin                                                  |               | 10   |                     | 10  | pF   |

End of Table 7-68

<sup>1</sup>  $C_b$  = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

# TMS320C6457

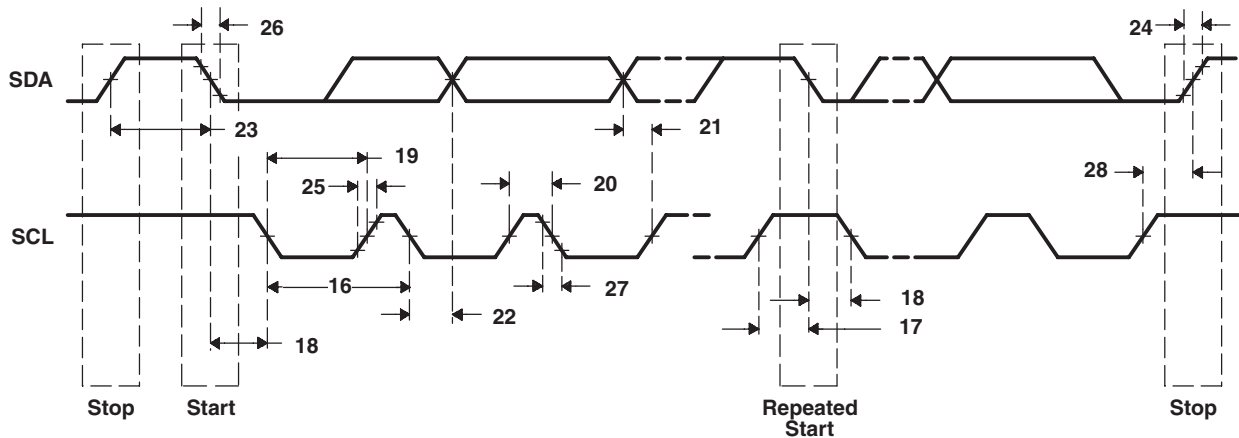
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**Figure 7-27 I<sup>2</sup>C Transmit Timing**



## 7.12 Host-Port Interface (HPI) Peripheral

### 7.12.1 HPI Device-Specific Information

The TMS320C6457 device includes a user-configurable 16-bit or 32-bit Host-port interface (HPI16/HPI32). The HPIWIDTH pin allows the user configuration of the HPI as a 16-bit or 32-bit peripheral.

**Table 7-69 HPIWIDTH Selection**

| Configuration Pin Setting | Peripheral Function Selected |                |
|---------------------------|------------------------------|----------------|
| HPIWIDTH                  | HPI Data Lower               | HPI Data Upper |
| 0 (default is HPI16 mode) | Enabled                      | Hi-Z           |
| 1 (HPI32 mode)            | Enabled                      | Enabled        |

End of Table 7-69

Software handshaking via the HRDY bit of the Host Port Control Register (HPIC) is not supported on the C6457.

An HPI boot is terminated using a DSP interrupt. The DSP interrupt is registered in bit 0 (channel 0) of the EDMA Event Register (ER). This event must be cleared by software before triggering transfers on DMA channel 0.

### 7.12.2 HPI Peripheral Register Description(s)

**Table 7-70 HPI Control Registers (Part 1 of 2)**

| Hex Address Range     | Acronym                     | Register Name                               | Comments                                                                                                       |
|-----------------------|-----------------------------|---------------------------------------------|----------------------------------------------------------------------------------------------------------------|
| 0288 0000             | -                           | Reserved                                    |                                                                                                                |
| 0288 0004             | PWREMU_MGMT                 | HPI power and emulation management register | The CPU has read/write access to the PWREMU_MGMT register; the Host does not have any access to this register. |
| 0288 0008 - 0288 0024 | -                           | Reserved                                    |                                                                                                                |
| 0288 0028             | -                           | Reserved                                    |                                                                                                                |
| 0288 002C             | -                           | Reserved                                    |                                                                                                                |
| 0288 0030             | HPIC                        | HPI control register                        | The Host and the CPU have read/write access to the HPIC register. <sup>(1)</sup>                               |
| 0288 0034             | HPIA (HPIAW) <sup>(2)</sup> | HPI address register (Write)                | The Host has read/write access to the HPIA registers. The CPU has only read access to the HPIA registers.      |
| 0288 0038             | HPIA (HPIAR) <sup>(2)</sup> | HPI address register (Read)                 |                                                                                                                |

**Table 7-70 HPI Control Registers (Part 2 of 2)**

| Hex Address Range     | Acronym | Register Name | Comments |
|-----------------------|---------|---------------|----------|
| 0288 000C - 028B 007F | -       | Reserved      |          |
| 0288 0080 - 028B FFFF | -       | Reserved      |          |

**End of Table 7-70**

- The CPU can write 1 to the HINT bit to generate an interrupt to the host and it can write 1 to the DSPINT bit to clear/acknowledge an interrupt from the host.
- There are two 32-bit HPIA registers: HPIAR for read operations and HPIAW for write operations. The HPI can be configured such that HPIAR and HPIAW act as a single 32-bit HPIA (single-HPIA mode) or as two separate 32-bit HPIAs (dual-HPIA mode) from the perspective of the host. The CPU can access HPIAW and HPIAR independently. For details about the HPIA registers and their modes, see the *TMS320C6457 DSP Host Port Interface (HPI) User's Guide* (literature number [SPRUGK7](#)).

### 7.12.3 HPI Electrical Data/Timing

**Table 7-71 Host-Port Interface Timing Requirements <sup>(1) (2)</sup>**

(see [Table 7-72](#) and see [Figure 7-28](#), [Figure 7-29](#), [Figure 7-30](#), [Figure 7-31](#), [Figure 7-32](#), [Figure 7-33](#), [Figure 7-34](#), and [Figure 7-35](#))

| No. |                                                                                                                                                                                                                               | Min | Max | Unit |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|
| 9   | $t_{su}(HASL-HSTBL)$ Setup time, $\overline{HAS}$ low before $\overline{HSTROBE}$ low                                                                                                                                         | 5   |     | ns   |
| 10  | $t_h(HSTBL-HASL)$ Hold time, $\overline{HAS}$ low after $\overline{HSTROBE}$ low                                                                                                                                              | 2   |     | ns   |
| 11  | $t_{su}(SELV-HASL)$ Setup time, select signals <sup>(3)</sup> valid before $\overline{HAS}$ low                                                                                                                               | 5   |     | ns   |
| 12  | $t_h(HASL-SELV)$ Hold time, select signals <sup>(3)</sup> valid after $\overline{HAS}$ low                                                                                                                                    | 5   |     | ns   |
| 13  | $t_w(HSTBL)$ Pulse duration, $\overline{HSTROBE}$ low                                                                                                                                                                         | 15  |     | ns   |
| 14  | $t_w(HSTBH)$ Pulse duration, $\overline{HSTROBE}$ high between consecutive accesses                                                                                                                                           | 2M  |     | ns   |
| 15  | $t_{su}(SELV-HSTBL)$ Setup time, select signals <sup>(3)</sup> valid before $\overline{HSTROBE}$ low                                                                                                                          | 5   |     | ns   |
| 16  | $t_h(HSTBL-SELV)$ Hold time, select signals <sup>(3)</sup> valid after $\overline{HSTROBE}$ low                                                                                                                               | 5   |     | ns   |
| 17  | $t_{su}(HDV-HSTBH)$ Setup time, host data valid before $\overline{HSTROBE}$ high                                                                                                                                              | 5   |     | ns   |
| 18  | $t_h(HSTBH-HDV)$ Hold time, host data valid after $\overline{HSTROBE}$ high                                                                                                                                                   | 1   |     | ns   |
| 37  | $t_{su}(HCSL-HSTBL)$ Setup time, $\overline{HCS}$ low before $\overline{HSTROBE}$ low                                                                                                                                         | 0   |     | ns   |
| 38  | $t_h(HRDYL-HSTBL)$ Hold time, $\overline{HSTROBE}$ low after $\overline{HRDY}$ low. $\overline{HSTROBE}$ should not be inactivated until $\overline{HRDY}$ is active (low); otherwise, HPI writes will not complete properly. | 1.1 |     | ns   |

**End of Table 7-71**

<sup>1</sup>  $\overline{HSTROBE}$  refers to the following logical operation on  $\overline{HCS}$ ,  $\overline{HDS1}$ , and  $\overline{HDS2}$ :  $[\text{NOT}(\overline{HDS1} \text{ XOR } \overline{HDS2})] \text{ OR } \overline{HCS}$ .

<sup>2</sup>  $M = \text{SYSCLK5 period} = 6 \div \text{CPU clock frequency in ns}$ . For example, when running parts at 1000 MHz, use  $M = 6 \text{ ns}$ .

<sup>3</sup> Select signals include:  $\overline{HCNTL}[1:0]$  and  $\overline{HR}/\overline{W}$ . For HPI16 mode only, select signals also include  $\overline{HHWIL}$ .

**Table 7-72 Host-Port Interface Switching Characteristics <sup>(1) (2)</sup> (Part 1 of 2)**

(see [Table 7-71](#) and see [Figure 7-28](#), [Figure 7-29](#), [Figure 7-30](#), [Figure 7-31](#), [Figure 7-32](#), [Figure 7-33](#), [Figure 7-34](#), and [Figure 7-35](#))

| No. | Parameter                                                                           | Min                                                                                     | Max                | Unit |
|-----|-------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|--------------------|------|
| 1   | $t_d(HSTBL-HDV)$ Delay time, $\overline{HSTROBE}$ low to DSP data valid             | Case 1. HPIC or HPIA read                                                               | 1                  | 15   |
|     |                                                                                     | Case 2. HPID read with no auto-increment <sup>(3)</sup>                                 | $9 \times M + 20$  |      |
|     |                                                                                     | Case 3. HPID read with auto-increment and read FIFO initially empty <sup>(3)</sup>      | $9 \times M + 20$  |      |
|     |                                                                                     | Case 4. HPID read with auto-increment and data previously prefetched into the read FIFO | 1                  | 15   |
| 2   | $t_{dis}(HSTBH-HDV)$ Disable time, HD high-impedance from $\overline{HSTROBE}$ high | 1                                                                                       | 4                  | ns   |
| 3   | $t_{en}(HSTBL-HD)$ Enable time, HD driven from $\overline{HSTROBE}$ low             | 3                                                                                       | 15                 | ns   |
| 4   | $t_d(HSTBL-HRDYH)$ Delay time, $\overline{HSTROBE}$ low to $\overline{HRDY}$ high   |                                                                                         | 12                 | ns   |
| 5   | $t_d(HSTBH-HRDYH)$ Delay time, $\overline{HSTROBE}$ high to $\overline{HRDY}$ high  |                                                                                         | 12                 | ns   |
| 6   | $t_d(HSTBL-HRDYL)$ Delay time, $\overline{HSTROBE}$ low to $\overline{HRDY}$ low    | Case 1. HPID read with no auto-increment <sup>(3)</sup>                                 | $10 \times M + 20$ |      |
|     |                                                                                     | Case 2. HPID read with auto-increment and read FIFO initially empty <sup>(3)</sup>      | $10 \times M + 20$ |      |
| 7   | $t_d(HDV-HRDYL)$ Delay time, HD valid to $\overline{HRDY}$ low                      | 0                                                                                       |                    | ns   |

**Table 7-72 Host-Port Interface Switching Characteristics<sup>(1) (2)</sup> (Part 2 of 2)**

(see Table 7-71 and see Figure 7-28, Figure 7-29, Figure 7-30, Figure 7-31, Figure 7-32, Figure 7-33, Figure 7-34, and Figure 7-35)

| No. | Parameter                                                                                                                           | Min                                                      | Max                | Unit |
|-----|-------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|--------------------|------|
| 34  | $t_{d(HSTBH-HRDYL)}$ Delay time, $\overline{HSTROBE}$ high to $\overline{HRDY}$ low                                                 | Case 1. HPIA write <sup>(3)</sup>                        | $5 \times M + 20$  | ns   |
|     |                                                                                                                                     | Case 2. HPID write with no auto-increment <sup>(3)</sup> | $5 \times M + 20$  |      |
| 35  | $t_{d(HSTBL-HRDYL)}$ Delay time, $\overline{HSTROBE}$ low to $\overline{HRDY}$ low for HPIA write and FIFO not empty <sup>(3)</sup> |                                                          | $40 \times M + 20$ | ns   |
| 36  | $t_{d(HASL-HRDYH)}$ Delay time, $\overline{HAS}$ low to $\overline{HRDY}$ high                                                      |                                                          | 12                 | ns   |

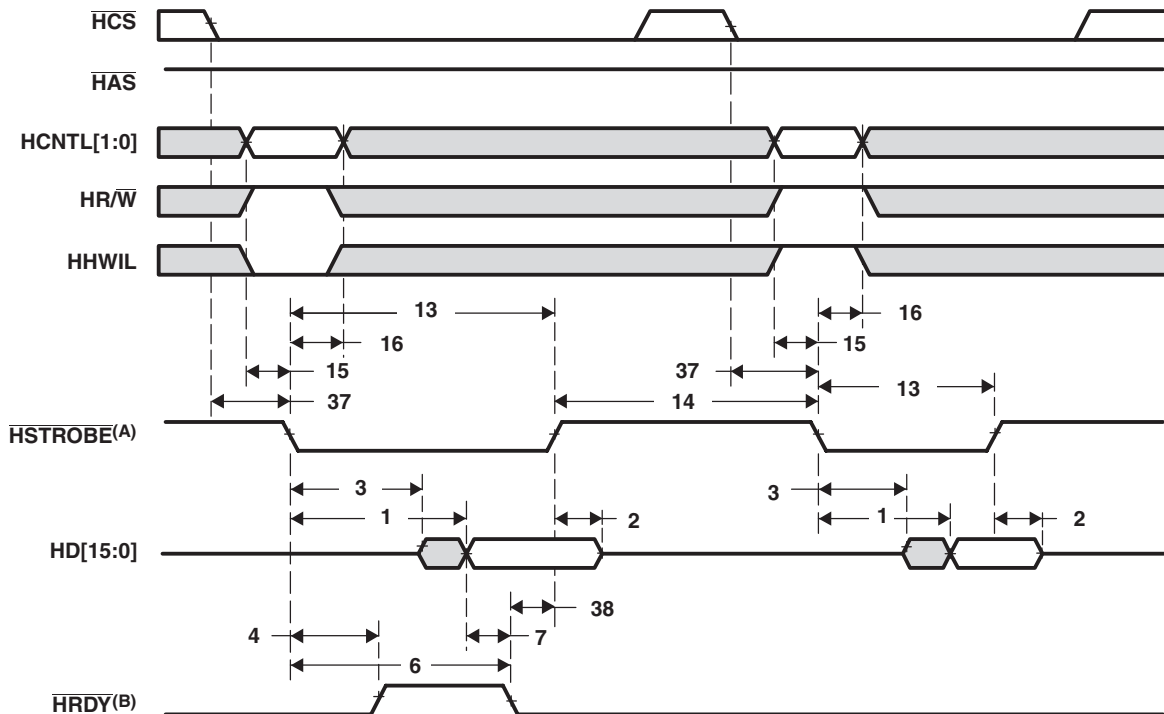
**End of Table 7-72**

1  $M = \text{SYSCLK5 period} = 6 \div \text{CPU clock frequency in ns}$ . For example, when running parts at 1000 MHz, use  $M = 6$  ns.

2  $\overline{HSTROBE}$  refers to the following logical operation on  $\overline{HCS}$ ,  $\overline{HDS1}$ , and  $\overline{HDS2}$ :  $[\text{NOT}(\overline{HDS1} \text{ XOR } \overline{HDS2})] \text{ OR } \overline{HCS}$ .

3 Assumes the HPI is accessing L2/L1 memory and no other master is accessing the same memory location.

**Figure 7-28 HPI16 Read Timing ( $\overline{HAS}$  Not Used, Tied High)**

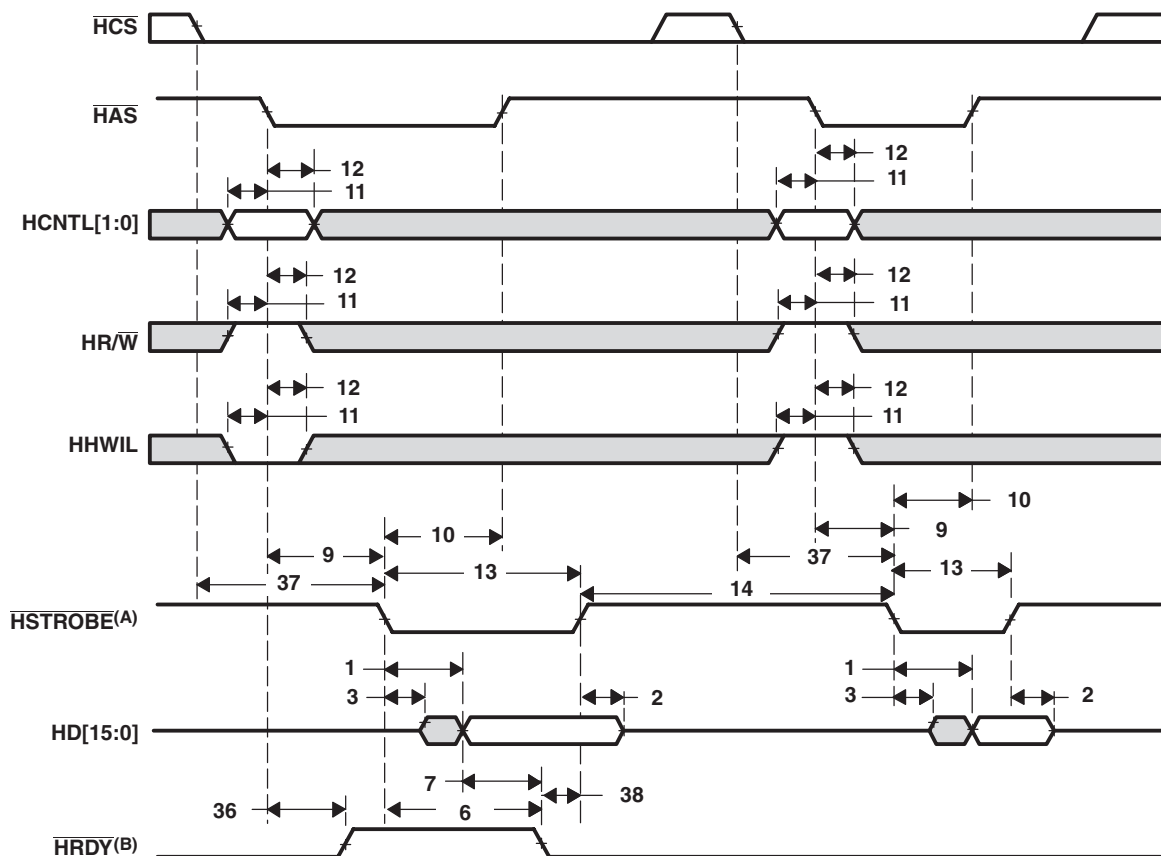


(A)  $\overline{HSTROBE}$  refers to the following logical operation on  $\overline{HCS}$ ,  $\overline{HDS1}$ , and  $\overline{HDS2}$ :  $[\text{NOT}(\overline{HDS1} \text{ XOR } \overline{HDS2})] \text{ OR } \overline{HCS}$ .

(B) Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on  $\overline{HRDY}$  may or may not occur. For more detailed information on the HPI peripheral, see the *TMS320C6457 DSP Host Port Interface (HPI) User's Guide* (literature number [SPRUGK7](#)).



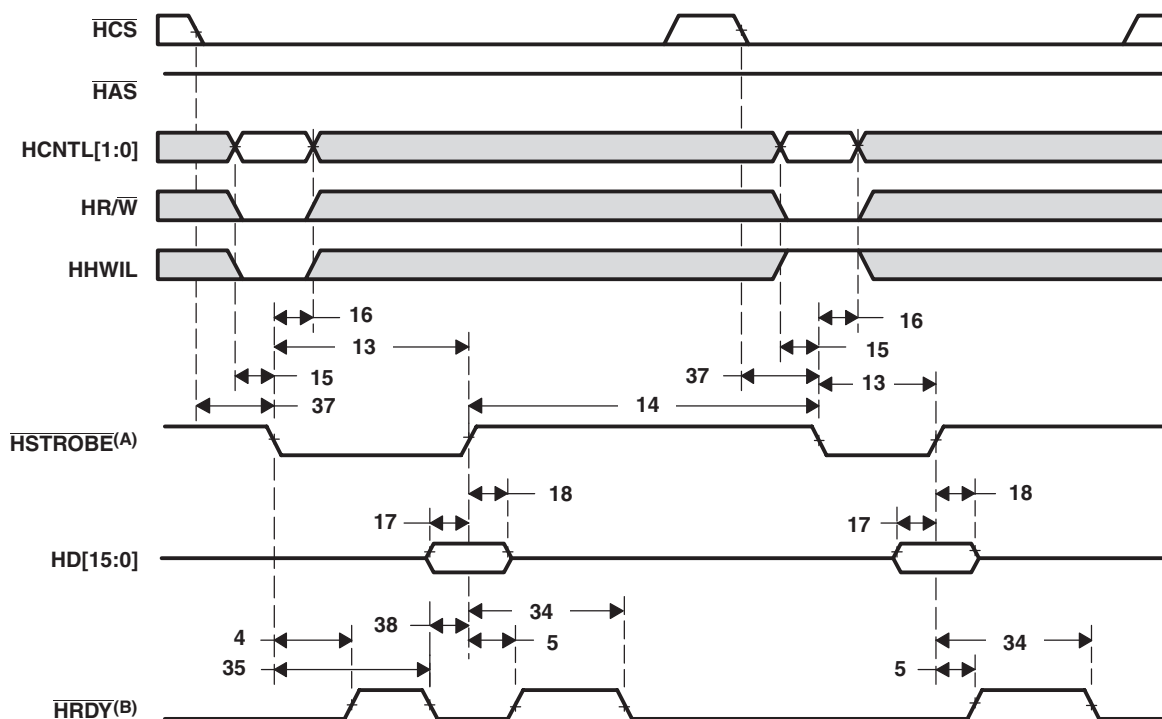
Figure 7-29 HPI16 Read Timing (HAS Used)



(A)  $\overline{\text{HSTROBE}}$  refers to the following logical operation on  $\overline{\text{HCS}}$ ,  $\overline{\text{HDS1}}$ , and  $\overline{\text{HDS2}}$ :  $[\text{NOT}(\text{HDS1 XOR HDS2})] \text{ OR } \overline{\text{HCS}}$ .

(B) Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on  $\overline{\text{HRDY}}$  may or may not occur. For more detailed information on the HPI peripheral, see the *TMS320C6457 DSP Host Port Interface (HPI) User's Guide* (literature number [SPRUGK7](#)).

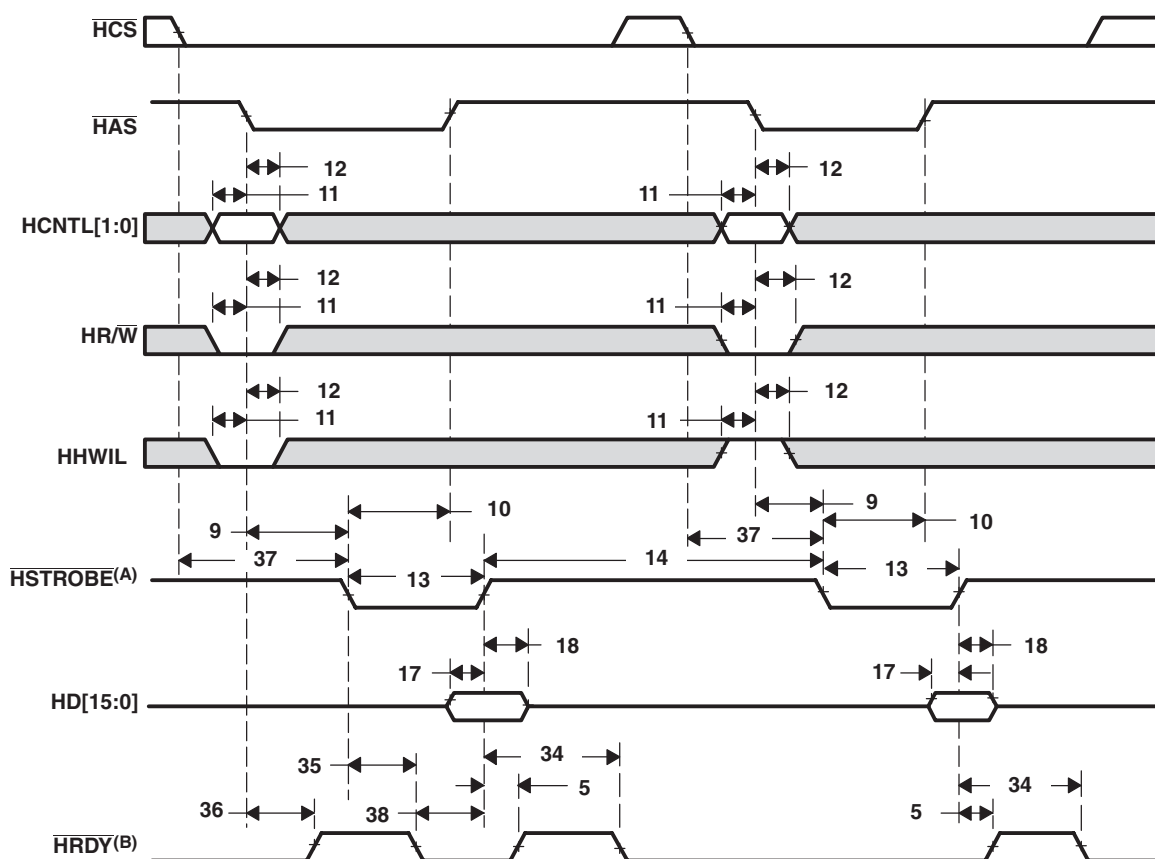
**Figure 7-30 HPI16 Write Timing (HAS Not Used, Tied High)**



(A)  $\overline{\text{HSTROBE}}$  refers to the following logical operation on  $\overline{\text{HCS}}$ ,  $\overline{\text{HDS1}}$ , and  $\overline{\text{HDS2}}$ :  $[\text{NOT}(\overline{\text{HDS1}} \text{ XOR } \overline{\text{HDS2}})] \text{ OR } \overline{\text{HCS}}$ .

(B) Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on  $\overline{\text{HRDY}}$  may or may not occur. For more detailed information on the HPI peripheral, see the *TMS320C6457 DSP Host Port Interface (HPI) User's Guide* (literature number [SPRUGK7](#)).

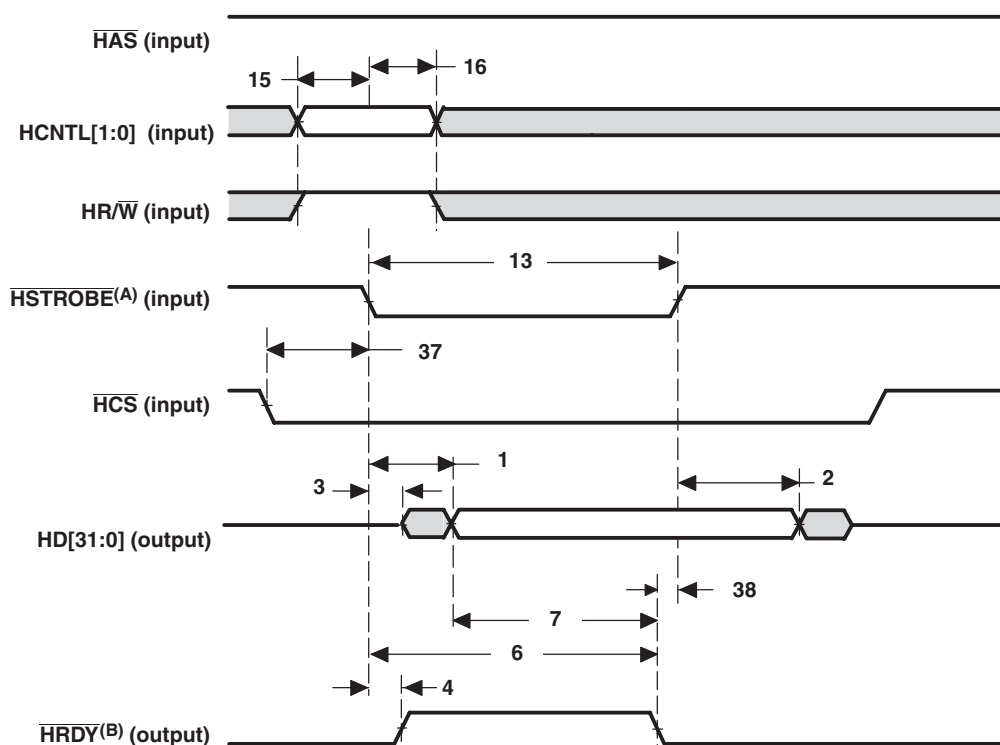
Figure 7-31 HPI16 Write Timing (HAS Used)



(A)  $\overline{\text{HSTROBE}}$  refers to the following logical operation on  $\overline{\text{HCS}}$ ,  $\overline{\text{HDS1}}$ , and  $\overline{\text{HDS2}}$ :  $[\text{NOT}(\text{HDS1 XOR HDS2})] \text{ OR } \overline{\text{HCS}}$ .

(B) Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on  $\overline{\text{HRDY}}$  may or may not occur. For more detailed information on the HPI peripheral, see the *TMS320C6457 DSP Host Port Interface (HPI) User's Guide* (literature number [SPRUGK7](#)).

**Figure 7-32 HPI32 Read Timing (H<sub>AS</sub> Not Used, Tied High)**

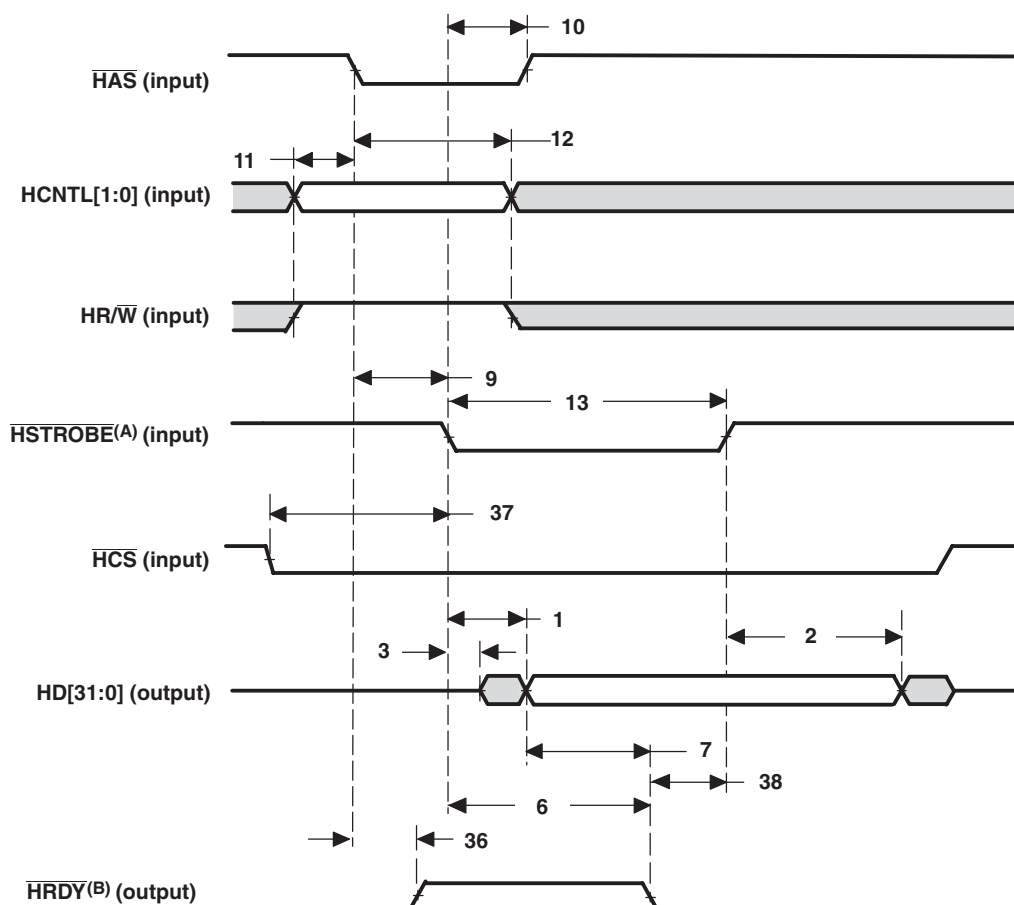


(A)  $\overline{\text{HSTROBE}}$  refers to the following logical operation on  $\overline{\text{HCS}}$ ,  $\overline{\text{HDS1}}$ , and  $\overline{\text{HDS2}}$ :  $[\text{NOT}(\overline{\text{HDS1}} \text{ XOR } \overline{\text{HDS2}})] \text{ OR } \overline{\text{HCS}}$ .

(B) Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on  $\overline{\text{HRDY}}$  may or may not occur. For more detailed information on the HPI peripheral, see the *TMS320C6457 DSP Host Port Interface (HPI) User's Guide* (literature number [SPRUGK7](#)).

(C) The timing  $t_{w(\text{HSTBH})}$   $\overline{\text{HSTROBE}}$  high pulse duration, must be met between consecutive HPI accesses in HPI32 mode.

Figure 7-33 HPI32 Read Timing (HAS Used)

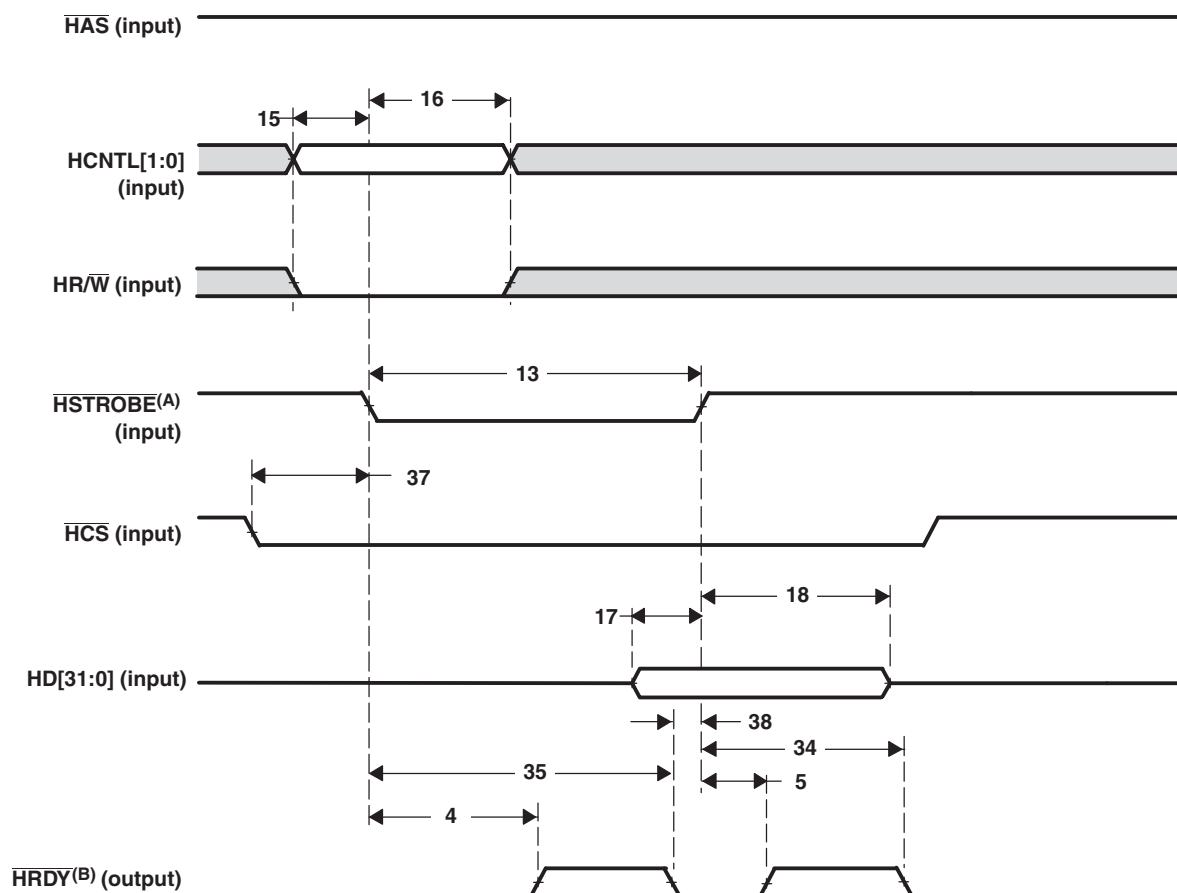


(A)  $\text{HSTROBE}$  refers to the following logical operation on  $\overline{\text{HCS}}$ ,  $\text{HDS1}$ , and  $\text{HDS2}$ :  $[\text{NOT}(\text{HDS1} \text{ XOR } \text{HDS2})] \text{ OR } \overline{\text{HCS}}$ .

(B) Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on  $\text{HRDY}$  may or may not occur. For more detailed information on the HPI peripheral, see the *TMS320C6457 DSP Host Port Interface (HPI) User's Guide* (literature number [SPRUGK7](#)).

(C) The timing  $t_{\text{w}(\text{HSTBH})}$ ,  $\text{HSTROBE}$  high pulse duration, must be met between consecutive HPI accesses in HPI32 mode.

**Figure 7-34 HPI32 Write Timing (HAS Not Used, Tied High)**

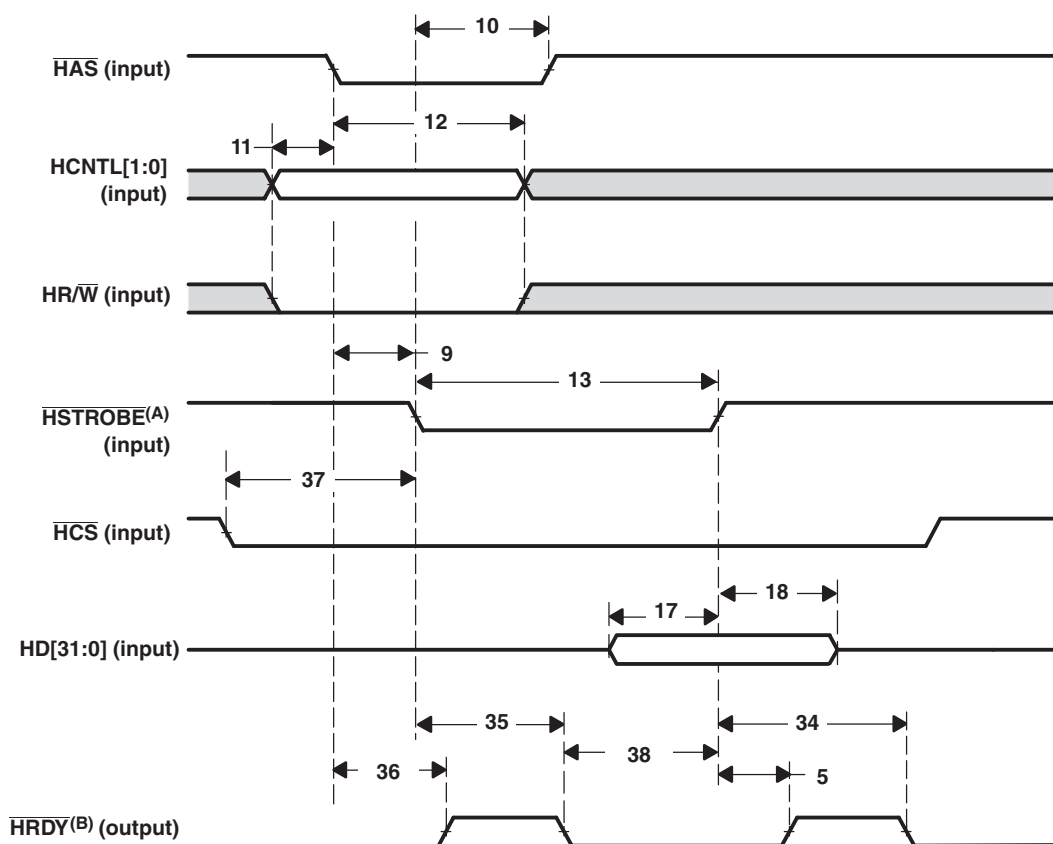


(A)  $\overline{\text{HSTROBE}}$  refers to the following logical operation on  $\overline{\text{HCS}}$ ,  $\overline{\text{HDS1}}$ , and  $\overline{\text{HDS2}}$ :  $[\text{NOT}(\overline{\text{HDS1}} \text{ XOR } \overline{\text{HDS2}})] \text{ OR } \overline{\text{HCS}}$ .

(B) Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on  $\overline{\text{HRDY}}$  may or may not occur. For more detailed information on the HPI peripheral, see the *TMS320C6457 DSP Host Port Interface (HPI) User's Guide* (literature number [SPRUGK7](#)).

(C) The timing  $t_{w(\overline{\text{HSTROBE}})}$ ,  $\overline{\text{HSTROBE}}$  high pulse duration, must be met between consecutive HPI accesses in HPI32 mode.

Figure 7-35 HPI32 Write Timing (HAS Used)



(A)  $\overline{\text{HSTROBE}}$  refers to the following logical operation on  $\overline{\text{HCS}}$ ,  $\overline{\text{HDS1}}$ , and  $\overline{\text{HDS2}}$ :  $[\text{NOT}(\overline{\text{HDS1}} \text{ XOR } \overline{\text{HDS2}})] \text{ OR } \overline{\text{HCS}}$ .

(B) Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on  $\overline{\text{HRDY}}$  may or may not occur. For more detailed information on the HPI peripheral, see the *TMS320C6457 DSP Host Port Interface (HPI) User's Guide* (literature number [SPRUGK7](#)).

(C) The timing  $t_{w(\overline{\text{HSTROBE}})}$ ,  $\overline{\text{HSTROBE}}$  high pulse duration, must be met between consecutive HPI accesses in HPI32 mode.

## 7.13 Multichannel Buffered Serial Port (McBSP)

The McBSP provides these functions:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- External shift clock or an internal, programmable frequency shift clock for data transfer

For more detailed information on the McBSP peripheral, see the *TMS320C6457 DSP Multichannel Buffered Serial Port (McBSP) Reference Guide* (literature number [SPRUGK8](#)).

### 7.13.1 McBSP Device-Specific Information

The CLKS signal for MCBSP0 and MCBSP1 can be sourced from an external pin or by the PLL1 controller; for details, see Section 7.7 “[PLL1 and PLL1 Controller](#)” on page 130. If the clock from the PLL1 controller is used, the clock is shared between the two McBSPs.

#### 7.13.1.1 McBSP Peripheral Register Description(s)

**Table 7-73 McBSP 0 Registers**

| Hex Address Range     | Acronym | Register Name                                                     |
|-----------------------|---------|-------------------------------------------------------------------|
| 028C 0000             | DRR0    | McBSP0 Data Receive Register via Configuration Bus <sup>(1)</sup> |
| 3000 0000             | DRR0    | McBSP0 Data Receive Register via EDMA3 Bus                        |
| 028C 0004             | DXR0    | McBSP0 Data Transmit Register via Configuration Bus               |
| 3000 0010             | DXR0    | McBSP0 Data Transmit Register via EDMA Bus                        |
| 028C 0008             | SPCR0   | McBSP0 Serial Port Control Register                               |
| 028C 000C             | RCR0    | McBSP0 Receive Control Register                                   |
| 028C 0010             | XCR0    | McBSP0 Transmit Control Register                                  |
| 028C 0014             | SRGR0   | McBSP0 Sample Rate Generator register                             |
| 028C 0018             | MCR0    | McBSP0 Multichannel Control Register                              |
| 028C 001C             | RCERE00 | McBSP0 Enhanced Receive Channel Enable Register 0 Partition A/B   |
| 028C 0020             | XCERE00 | McBSP0 Enhanced Transmit Channel Enable Register 0 Partition A/B  |
| 028C 0024             | PCR0    | McBSP0 Pin Control Register                                       |
| 028C 0028             | RCERE10 | McBSP0 Enhanced Receive Channel Enable Register 1 Partition C/D   |
| 028C 002C             | XCERE10 | McBSP0 Enhanced Transmit Channel Enable Register 1 Partition C/D  |
| 028C 0030             | RCERE20 | McBSP0 Enhanced Receive Channel Enable Register 2 Partition E/F   |
| 028C 0034             | XCERE20 | McBSP0 Enhanced Transmit Channel Enable Register 2 Partition E/F  |
| 028C 0038             | RCERE30 | McBSP0 Enhanced Receive Channel Enable Register 3 Partition G/H   |
| 028C 003C             | XCERE30 | McBSP0 Enhanced Transmit Channel Enable Register 3 Partition G/H  |
| 028C 0040 - 028F FFFF | -       | Reserved                                                          |

**End of Table 7-73**

<sup>1</sup> The CPU and EDMA3 controller can only read the register, they cannot write to it.



**Table 7-74      McBSP 1 Registers**

| Hex Address Range        | Acronym | Register Name                                                    |
|--------------------------|---------|------------------------------------------------------------------|
| 0290 0000                | DRR1    | McBSP1 Data Receive Register via Configuration Bus(1)            |
| 3400 0000                | DRR1    | McBSP1 Data Receive Register via EDMA bus                        |
| 0290 0004                | DXR1    | McBSP1 Data Transmit Register via configuration bus              |
| 3400 0010                | DXR1    | McBSP1 Data Transmit Register via EDMA bus                       |
| 0290 0008                | SPCR1   | McBSP1 serial port control register                              |
| 0290 000C                | RCR1    | McBSP1 Receive Control Register                                  |
| 0290 0010                | XCR1    | McBSP1 Transmit Control Register                                 |
| 0290 0014                | SRGR1   | McBSP1 sample rate generator register                            |
| 0290 0018                | MCR1    | McBSP1 multichannel control register                             |
| 0290 001C                | RCERE01 | McBSP1 Enhanced Receive Channel Enable Register 0 Partition A/B  |
| 0290 0020                | XCERE01 | McBSP1 Enhanced Transmit Channel Enable Register 0 Partition A/B |
| 0290 0024                | PCR1    | McBSP1 Pin Control Register                                      |
| 0290 0028                | RCERE11 | McBSP1 Enhanced Receive Channel Enable Register 1 Partition C/D  |
| 0290 002C                | XCERE11 | McBSP1 Enhanced Transmit Channel Enable Register 1 Partition C/D |
| 0290 0030                | RCERE21 | McBSP1 Enhanced Receive Channel Enable Register 2 Partition E/F  |
| 0290 0034                | XCERE21 | McBSP1 Enhanced Transmit Channel Enable Register 2 Partition E/F |
| 0290 0038                | RCERE31 | McBSP1 Enhanced Receive Channel Enable Register 3 Partition G/H  |
| 0290 003C                | XCERE31 | McBSP1 Enhanced Transmit Channel Enable Register 3 Partition G/H |
| 0290 0040 - 0293 FFFF    | -       | Reserved                                                         |
| <b>End of Table 7-74</b> |         |                                                                  |

### 7.13.2 McBSP Electrical Data/Timing

**Table 7-75      McBSP Timing Requirements <sup>(1)</sup>**  
(see Figure 7-36)

| No.               |                            |                                               |            | Min                                         | Max | Unit |
|-------------------|----------------------------|-----------------------------------------------|------------|---------------------------------------------|-----|------|
| 2                 | t <sub>c</sub> (CKRX)      | Cycle time, CLKR/X                            | CLKR/X ext | 10P <sup>(2)</sup>                          |     | ns   |
| 3                 | t <sub>w</sub> (CKRX)      | Pulse duration, CLKR/X high or CLKR/X low     | CLKR/X ext | 0.5t <sub>c</sub> (CKRX) - 1 <sup>(2)</sup> |     | ns   |
| 5                 | t <sub>su</sub> (FRH-CKRL) | Setup time, external FSR high before CLKR low | CLKR int   | 9                                           |     | ns   |
|                   |                            |                                               | CLKR ext   | 1.3                                         |     |      |
| 6                 | t <sub>h</sub> (CKRL-FRH)  | Hold time, external FSR high after CLKR low   | CLKR int   | 6                                           |     | ns   |
|                   |                            |                                               | CLKR ext   | 3                                           |     |      |
| 7                 | t <sub>su</sub> (DRV-CKRL) | Setup time, DR valid before CLKR low          | CLKR int   | 8                                           |     | ns   |
|                   |                            |                                               | CLKR ext   | 0.9                                         |     |      |
| 8                 | t <sub>h</sub> (CKRL-DRV)  | Hold time, DR valid after CLKR low            | CLKR int   | 3                                           |     | ns   |
|                   |                            |                                               | CLKR ext   | 3.1                                         |     |      |
| 10                | t <sub>su</sub> (FXH-CKXL) | Setup time, external FSX high before CLKX low | CLKR int   | 9                                           |     | ns   |
|                   |                            |                                               | CLKR ext   | 1.3                                         |     |      |
| 11                | t <sub>h</sub> (CKXL-FXH)  | Hold time, external FSX high after CLKX low   | CLKR int   | 6                                           |     | ns   |
|                   |                            |                                               | CLKR ext   | 3                                           |     |      |
| End of Table 7-75 |                            |                                               |            |                                             |     |      |

1 P = 1/SYSREFCLK frequency in ns. For example, when running parts at 1000 MHz, use P = 1 ns.

2 This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

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**Table 7-76 Switching Characteristics for McBSP<sup>(1) (2) (3)</sup>**  
(see Figure 7-36)

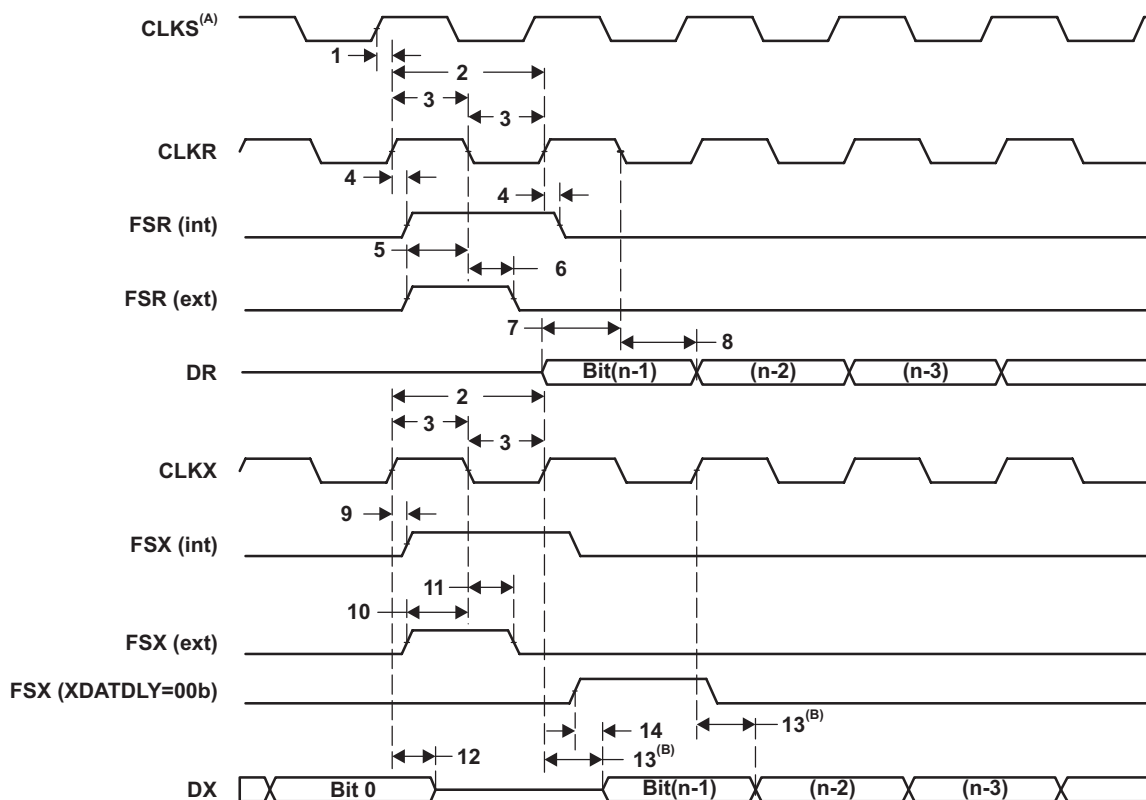
| No. | Parameter                                                                                                              | Min                        | Max                      | Unit                    |
|-----|------------------------------------------------------------------------------------------------------------------------|----------------------------|--------------------------|-------------------------|
| 1   | $t_{d(CKSH-CKRXH)}$ Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input. <sup>(4)</sup> | 1.4                        | 10                       | ns                      |
| 2   | $t_{c(CKRX)}$ Cycle time, CLKR/X                                                                                       | 10P <sup>(5) (6) (7)</sup> |                          | ns                      |
| 3   | $t_{w(CKRX)}$ Pulse duration, CLKR/X high or CLKR/X low                                                                | $0.5t_{c(CKRX)} - 1$       |                          | ns                      |
| 4   | $t_{d(CKRH-FRV)}$ Delay time, CLKR high to internal FSR valid                                                          | -2.1                       | 3                        | ns                      |
| 9   | $t_{d(CKXH-FXV)}$ Delay time, CLKX high to internal FSX valid                                                          | CLKX int                   | -1.7                     | 3                       |
|     |                                                                                                                        | CLKX ext                   | 1.7                      | 9                       |
| 12  | $t_{dis(CKXH-DXHZ)}$ Disable time, DX Hi-Z following last data bit from CLKX high                                      | CLKX int                   | -3.9                     | 4                       |
|     |                                                                                                                        | CLKX ext                   | 2                        | 9                       |
| 13  | $t_{d(CKXH-DXV)}$ Delay time, CLKX high to DX valid                                                                    | CLKX int                   | -3.9                     | 4                       |
| 14  | $t_{d(FXH-DXV)}$ Delay time, FSX high to DX valid applies ONLY when in data delay 0 (XDATDLY = 00b) mode               | CLKX ext                   | 2                        | 9                       |
|     |                                                                                                                        | FSX int                    | -2.3 + D1 <sup>(8)</sup> | 5.6 + D2 <sup>(8)</sup> |
|     |                                                                                                                        | FSX ext                    | 1.9 + D1 <sup>(8)</sup>  | 9 + D2 <sup>(8)</sup>   |

End of Table 7-76

- Over recommended operating conditions.
- CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
- Minimum delay times also represent minimum output hold times.
- The CLKS signal is shared by both McBSP0 and McBSP1 on this device.
- Minimum CLKR ÷ X cycle times must be met, even when CLKR ÷ X is generated by an internal clock source. Minimum CLKR ÷ X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements
- P = 1/SYSREFCLK frequency in ns. For example, when running parts at 1000 MHz, use P = 1 ns.
- Use whichever value is greater
- Extra delay from FSX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.  
if DXENA = 0, then D1 = D2 = 0  
if DXENA = 1, then D1 = 4P, D2 = 8P

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Figure 7-36 McBSP Timing



(A) The CLKs signal is shared by both McBSP0 and McBSP1 on this device.

(B) Parameter No. 13 applies to the first data bit *only* when XDATDLY  $\neq$  0.

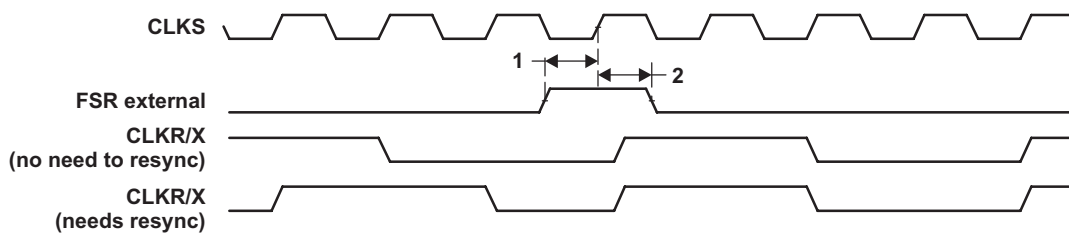
Table 7-77 Timing Requirements for FSR When GSYNC = 1

(see Figure 7-37)

| No. |                                                          | Min | Max | Unit |
|-----|----------------------------------------------------------|-----|-----|------|
| 1   | $t_{su}(FRH-CKSH)$ Setup time, FSR high before CLKs high | 4   |     | ns   |
| 2   | $t_h(CKSH-FRH)$ Hold time, FSR high after CLKs high      | 4   |     | ns   |

End of Table 7-77

Figure 7-37 FSR Timing When GSYNC = 1



**Table 7-78 SPI Timing Requirements as Master or Slave: CLKSTP = 10b, CLKXP = 0<sup>(1) (2)</sup>**  
(see Figure 7-38)

| No. |                    |                                      | Master |     | Slave |     | Unit |
|-----|--------------------|--------------------------------------|--------|-----|-------|-----|------|
|     |                    |                                      | Min    | Max | Min   | Max |      |
| 4   | $t_{su(DRV-CKXL)}$ | Setup time, DR valid before CLKX low | 12     |     | 2-12P |     | ns   |
| 5   | $t_{h(CKXL-DRV)}$  | Hold time, DR valid after CLKX low   | 4      |     | 5+24P |     | ns   |

End of Table 7-78

- For all SPI Slave modes, CLKG is programmed as 1/6 of the CPU clock by setting CLKSM = CLKGDV = 1.
- P = 1/SYSREFCLK frequency in ns. For example, when running parts at 1000 MHz, use P = 1 ns.

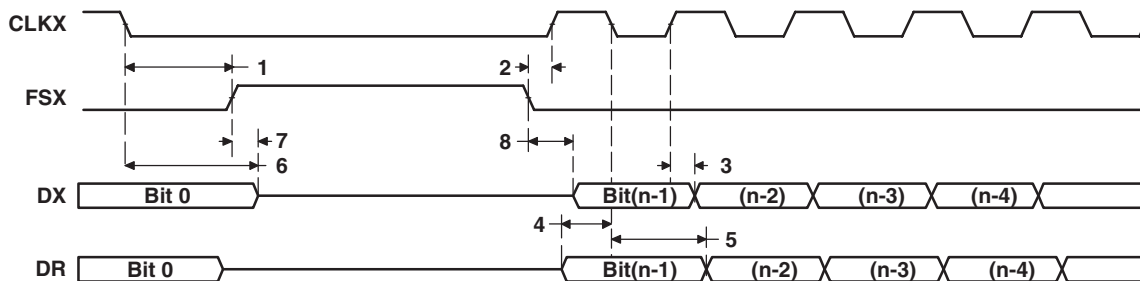
**Table 7-79 SPI Switching Characteristics as Master or Slave: CLKSTP = 10b, CLKXP = 0<sup>(1) (2) (3) (4) (5)</sup>**  
(see Figure 7-38)

| No. | Parameters           | Master |     | Slave   |        | Unit |
|-----|----------------------|--------|-----|---------|--------|------|
|     |                      | Min    | Max | Min     | Max    |      |
| 1   | $t_{d(CKXL-FXH)}$    | T-2    | T+3 |         |        | ns   |
| 2   | $t_{d(FXL-CKXH)}$    | L-3    | L+3 |         |        | ns   |
| 3   | $t_{d(CKXH-DXV)}$    | -2     | 4   | 12P+2.8 | 24P+17 | ns   |
| 6   | $t_{dis(CKXL-DXHZ)}$ | L-2    | L+3 |         |        | ns   |
| 7   | $t_{dis(FXH-DXHZ)}$  |        |     | 4P+3    | 12P+17 | ns   |
| 8   | $t_{d(FXL-DXV)}$     |        |     | 8P+1.8  | 18P+17 | ns   |

End of Table 7-79

- P = 1/SYSREFCLK frequency in ns. For example, when running parts at 1000 MHz, use P = 1 ns.
- For all SPI Slave modes, CLKG is programmed as 1/6 of the CPU clock by setting CLKSM = CLKGDV = 1.
- S = Sample rate generator input clock = 6P if CLKSM = 1  
S = Sample rate generator input clock = P\_clks if CLKSM = 0 (P\_clks = CLKS period)  
T = CLKX period = (1 + CLKGDV) \* S  
H = CLKX high pulse width = (CLKGDV/2 + 1) \* S if CLKGDV is even  
H = (CLKGDV + 1)/2 \* S if CLKGDV is odd  
L = CLKX low pulse width = (CLKGDV/2) \* S if CLKGDV is even  
L = (CLKGDV + 1)/2 \* S if CLKGDV is odd
- FSRP = FSXP = 1. As a SPI Master, FSX is inverted to provide active-low slave-enable output. As a Slave, the active-low signal input on FSX and FSR is inverted before being used internally.  
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for Master McBSP  
CLKXM = CLKRM = FSXM = FSRM = 0 for Slave McBSP
- FSX should be low before the rising edge of clock to enable Slave devices and then begin a SPI transfer at the rising edge of the Master clock (CLKX).

**Figure 7-38 SPI Timing as Master or Slave: CLKSTP = 10b, CLKXP = 0**



**Table 7-80 SPI Timing Requirements as Master or Slave: CLKSTP = 10b, CLKXP = 1<sup>(1)</sup> (2)**  
(see Figure 7-39)

| No. |                    |                                       | Master |     | Slave |     | Unit |
|-----|--------------------|---------------------------------------|--------|-----|-------|-----|------|
|     |                    |                                       | Min    | Max | Min   | Max |      |
| 4   | $t_{su(DRV-CKXH)}$ | Setup time, DR valid before CLKX high | 12     |     | 2-12P |     | ns   |
| 5   | $t_{h(CKXH-DRV)}$  | Hold time, DR valid after CLKX high   | 4      |     | 5+24P |     | ns   |

End of Table 7-80

- 1 P = 1/SYSREFCLK frequency in ns. For example, when running parts at 1000 MHz, use P = 1 ns.  
2 For all SPI Slave modes, CLKG is programmed as 1/6 of the CPU clock by setting CLKSM = CLKGDV = 1.

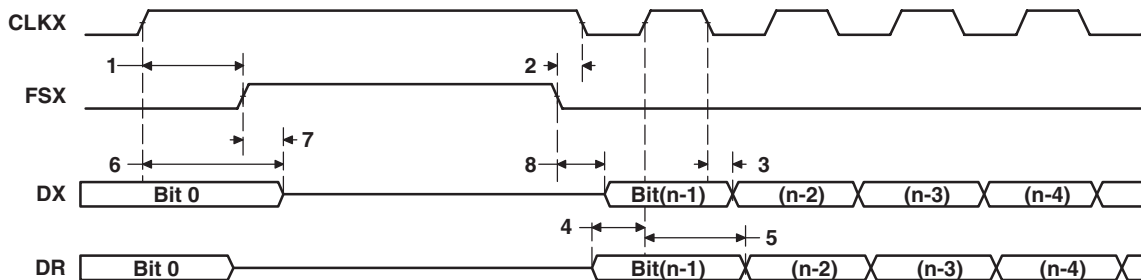
**Table 7-81 SPI Switching Characteristics as Master or Slave: CLKSTP = 10b, CLKXP = 1<sup>(1)</sup> (2) (3) (4) (5)**  
(see Figure 7-39)

| No. | Parameter            |                                                                        | Master |     | Slave     |          | Unit |
|-----|----------------------|------------------------------------------------------------------------|--------|-----|-----------|----------|------|
|     |                      |                                                                        | Min    | Max | Min       | Max      |      |
| 1   | $t_{d(CKXH-FXH)}$    | Delay time, FSX high after CLKX high                                   | T-2    | T+3 |           |          | ns   |
| 2   | $t_{d(FXL-CKXL)}$    | Delay time, CLKX low after FSX low                                     | H-3    | H+3 |           |          | ns   |
| 3   | $t_{d(CKXL-DXV)}$    | Delay time, CLKX low to DX valid                                       | -2     | 4   | 12P + 2.8 | 24P + 17 | ns   |
| 6   | $t_{dis(CKXH-DXHZ)}$ | Disable time, DX high impedance following last data bit from CLKX high | H-2    | H+3 |           |          | ns   |
| 7   | $t_{dis(FXH-DXHZ)}$  | Disable time, DX high impedance following last data bit from FSX high  |        |     | 4P+3      | 12P+17   | ns   |
| 8   | $t_{d(FXL-DXV)}$     | Delay time, FSX low to DX valid                                        |        |     | 8P+2      | 18P+17   | ns   |

End of Table 7-81

- 1 P = 1/SYSREFCLK frequency in ns. For example, when running parts at 1000 MHz, use P = 1 ns.  
2 For all SPI Slave modes, CLKG is programmed as 1/6 of the CPU clock by setting CLKSM = CLKGDV = 1.  
3 S = Sample rate generator input clock = 6P if CLKSM = 1  
S = Sample rate generator input clock = P\_clks if CLKSM = 0 (P\_clks = CLKS period)  
T = CLKX period = (1 + CLKGDV) \* S  
H = CLKX high pulse width = (CLKGDV/2 + 1) \* S if CLKGDV is even  
H = (CLKGDV + 1)/2 \* S if CLKGDV is odd  
L = CLKX low pulse width = (CLKGDV/2) \* S if CLKGDV is even  
L = (CLKGDV + 1)/2 \* S if CLKGDV is odd  
4 FSRP = FSXP = 1. As a SPI Master, FSX is inverted to provide active-low slave-enable output. As a Slave, the active-low signal input on FSX and FSR is inverted before being used internally.  
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for Master McBSP  
CLKXM = CLKRM = FSXM = FSRM = 0 for Slave McBSP  
5 FSX should be low before the rising edge of clock to enable Slave devices and then begin a SPI transfer at the rising edge of the Master clock (CLKX).

**Figure 7-39 SPI Timing as Master or Slave: CLKSTP = 10b, CLKXP = 1**



**Table 7-82 SPI Timing Requirements as Master or Slave: CLKSTP = 11b, CLKXP = 0<sup>(1) (2)</sup>**  
(see Figure 7-40)

| No. |                    |                                       | Master |     | Slave |     | Unit |
|-----|--------------------|---------------------------------------|--------|-----|-------|-----|------|
|     |                    |                                       | Min    | Max | Min   | Max |      |
| 4   | $t_{su(DRV-CKXH)}$ | Setup time, DR valid before CLKX high | 12     |     | 2-12P |     | ns   |
| 5   | $t_{h(CKXH-DRV)}$  | Hold time, DR valid after CLKX high   | 4      |     | 5+24P |     | ns   |

**End of Table 7-82**

- 1 P = 1/SYSREFCLK frequency in ns. For example, when running parts at 1000 MHz, use P = 1 ns.  
2 For all SPI Slave modes, CLKG is programmed as 1/6 of the CPU clock by setting CLKSM = CLKGDV = 1.

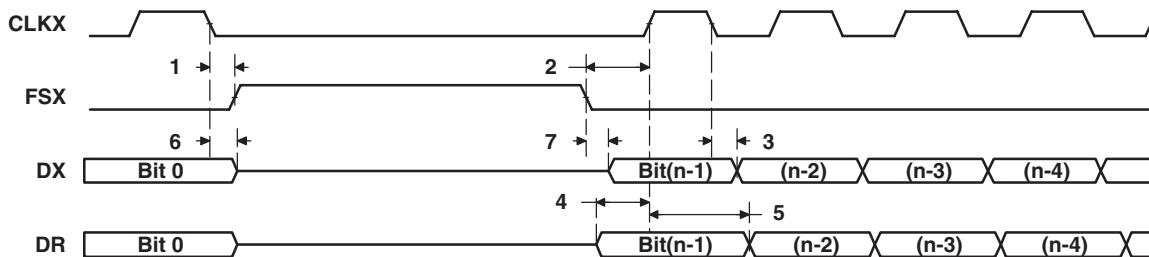
**Table 7-83 SPI Switching Characteristics as Master or Slave: CLKSTP = 11b, CLKXP = 0<sup>(1) (2) (3) (4) (5)</sup>**  
(see Figure 7-40)

| No. | Parameter            |                                                                       | Master |     | Slave   |        | Unit |
|-----|----------------------|-----------------------------------------------------------------------|--------|-----|---------|--------|------|
|     |                      |                                                                       | Min    | Max | Min     | Max    |      |
| 1   | $t_{d(CKXL-FXH)}$    | Delay time, FSX high after CLKX low                                   | L-2    | L+3 |         |        | ns   |
| 2   | $t_{d(FXL-CKXH)}$    | Delay time, CLKX high after FSX low                                   | T-3    | T+3 |         |        | ns   |
| 3   | $t_{d(CKXL-DXV)}$    | Delay time, CLKX low to DX valid                                      | -2     | 4   | 12P+2.8 | 24P+17 | ns   |
| 6   | $t_{dis(CKXL-DXHZ)}$ | Disable time, DX high impedance following last data bit from CLKX low | -2     | 4   | 12P+3   | 20P+17 | ns   |
| 7   | $t_{dis(FXL-DXHZ)}$  | Disable time, DX high impedance following last data bit from FSX low  | H-2    | H+4 | 8P+2    | 18P+17 | ns   |

**End of Table 7-83**

- 1 P = 1/SYSREFCLK frequency in ns. For example, when running parts at 1000 MHz, use P = 1 ns.  
2 For all SPI Slave modes, CLKG is programmed as 1/6 of the CPU clock by setting CLKSM = CLKGDV = 1.  
3 S = Sample rate generator input clock = 6P if CLKSM = 1  
S = Sample rate generator input clock = P\_clks if CLKSM = 0 (P\_clks = CLKS period)  
T = CLKX period = (1 + CLKGDV) \* S  
H = CLKX high pulse width = (CLKGDV/2 + 1) \* S if CLKGDV is even  
H = (CLKGDV + 1)/2 \* S if CLKGDV is odd  
L = CLKX low pulse width = (CLKGDV/2) \* S if CLKGDV is even  
L = (CLKGDV + 1)/2 \* S if CLKGDV is odd  
4 FSRP = FSXP = 1. As a SPI Master, FSX is inverted to provide active-low slave-enable output. As a Slave, the active-low signal input on FSX and FSR is inverted before being used internally.  
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for Master McBSP  
CLKXM = CLKRM = FSXM = FSRM = 0 for Slave McBSP  
5 FSX should be low before the rising edge of clock to enable Slave devices and then begin a SPI transfer at the rising edge of the Master clock (CLKX).

**Figure 7-40 SPI Timing as Master or Slave: CLKSTP = 11b, CLKXP = 0**



**Table 7-84 SPI Timing Requirements as Master or Slave: CLKSTP = 11b, CLKXP = 1<sup>(1) (2)</sup>**  
(see Figure 7-41)

| No. |                    |                                       | Master |     | Slave |     | Unit |
|-----|--------------------|---------------------------------------|--------|-----|-------|-----|------|
|     |                    |                                       | Min    | Max | Min   | Max |      |
| 4   | $t_{su(DRV-CKXH)}$ | Setup time, DR valid before CLKX high | 12     |     | 2-12P |     | ns   |
| 5   | $t_{h(CKXH-DRV)}$  | Hold time, DR valid after CLKX high   | 4      |     | 5+24P |     | ns   |

**End of Table 7-84**

- 1 P = 1/SYSREFCLK frequency in ns. For example, when running parts at 1000 MHz, use P = 1 ns.
- 2 For all SPI Slave modes, CLKG is programmed as 1/6 of the CPU clock by setting CLKSM = CLKGDV = 1.

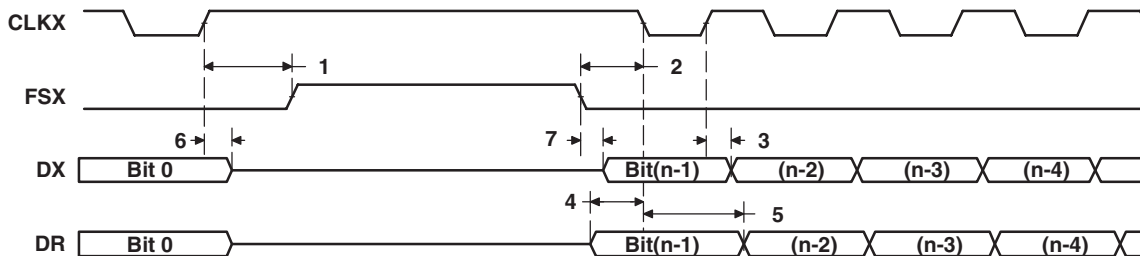
**Table 7-85 SPI Switching Characteristics as Master or Slave: CLKSTP = 11b, CLKXP = 1** <sup>(1) (2) (3) (4) (5)</sup>  
(see Figure 7-41)

| No. | Parameter                                                                                   | Master |     | Slave   |        | Unit |
|-----|---------------------------------------------------------------------------------------------|--------|-----|---------|--------|------|
|     |                                                                                             | Min    | Max | Min     | Max    |      |
| 1   | $t_{d(CKXH-FXL)}$ Delay time, FSX low after CLKX high                                       | H-2    | H+3 |         |        | ns   |
| 2   | $t_{d(FXL-CKXL)}$ Delay time, CLKX low after FSX low                                        | T-3    | T+3 |         |        | ns   |
| 3   | $t_{d(CKXH-DXV)}$ Delay time, CLKX high to DX valid                                         | -2     | 4   | 12P+2.8 | 24P+17 | ns   |
| 6   | $t_{dis(CKXH-DXHZ)}$ Disable time, DX high impedance following last data bit from CLKX high | -2     | 4   | 12P+3   | 20P+17 | ns   |
| 7   | $t_{dis(FXL-DXHZ)}$ Disable time, DX high impedance following last data bit from FSX low    | L-2    | L+4 | 8P+2    | 18P+17 | ns   |

**End of Table 7-85**

- 1 P = 1/SYSREFCLK frequency in ns. For example, when running parts at 1000 MHz, use P = 1 ns.
- 2 For all SPI Slave modes, CLKG is programmed as 1/6 of the CPU clock by setting CLKSM = CLKGDV = 1.
- 3 S = Sample rate generator input clock = 6P if CLKSM = 1  
S = Sample rate generator input clock = P\_clks if CLKSM = 0 (P\_clks = CLK period)  
T = CLKX period = (1 + CLKGDV) \* S  
H = CLKX high pulse width = (CLKGDV/2 + 1) \* S if CLKGDV is even; H = (CLKGDV + 1)/2 \* S if CLKGDV is odd  
L = CLKX low pulse width = (CLKGDV/2) \* S if CLKGDV is even  
L = (CLKGDV + 1)/2 \* S if CLKGDV is odd
- 4 FSRP = FSXP = 1. As a SPI Master, FSX is inverted to provide active-low slave-enable output. As a Slave, the active-low signal input on FSX and FSR is inverted before being used internally.  
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for Master McBSP  
CLKXM = CLKRM = FSXM = FSRM = 0 for Slave McBSP
- 5 FSX should be low before the rising edge of clock to enable Slave devices and then begin a SPI transfer at the rising edge of the Master clock (CLKX).

**Figure 7-41 SPI Timing as Master or Slave: CLKSTP = 11b, CLKXP = 1**



## 7.14 Ethernet MAC (EMAC)

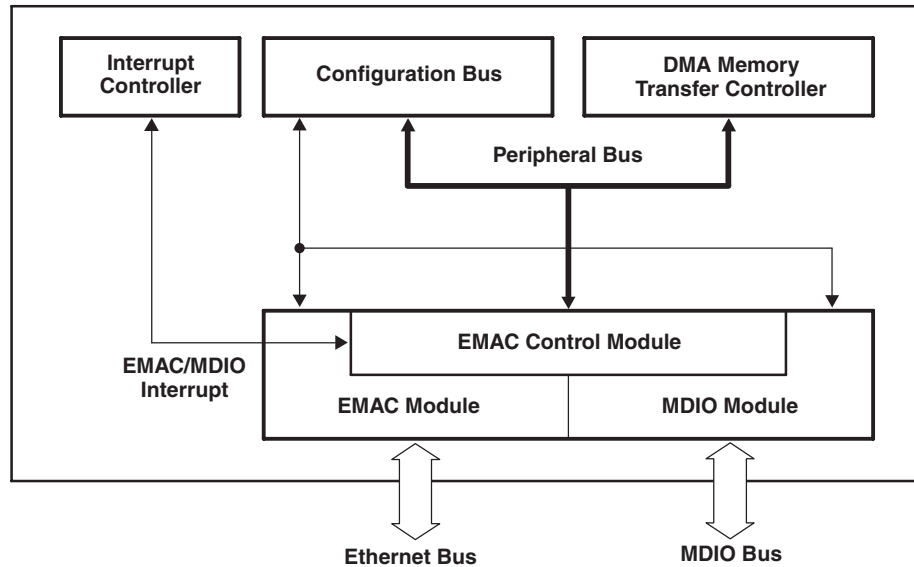
The Ethernet Media Access Controller (EMAC) module provides an efficient interface between the TMS320C6457 DSP core processor and the networked community. The EMAC supports 10Base-T (10 Mb/s), and 100BaseTX (100 Mb/s), in half- or full-duplex mode, and 1000BaseT (1000 Mb/s) in full-duplex mode, with hardware flow control and quality-of-service (QoS) support.

The EMAC module conforms to the IEEE 802.3-2002 standard, describing the *Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer* specifications. The IEEE 802.3 standard has also been adopted by ISO/IEC and re-designated as ISO/IEC 8802-3:2000(E).

Deviation from this standard, the EMAC module does not use the Transmit Coding Error signal MTXER. Instead of driving the error pin when an underflow condition occurs on a transmitted frame, the EMAC will intentionally generate an incorrect checksum by inverting the frame CRC, so that the transmitted frame will be detected as an error by the network.

The EMAC control module is the main interface between the device core processor, the MDIO module, and the EMAC module. The relationship between these three components is shown in Figure 7-42. The EMAC control module contains the necessary components to allow the EMAC to make efficient use of device memory, plus it controls device interrupts. The EMAC control module incorporates 8K-bytes of internal RAM to hold EMAC buffer descriptors.

Figure 7-42 EMAC, MDIO, and EMAC Control Modules



For more detailed information on the EMAC/MDIO, see the *TMS320C6457 DSP EMAC/MDIO Module Reference Guide* (literature number [SPRUGK9](#)).

#### 7.14.1 EMAC Device-Specific Information

The EMAC module on the device supports Serial Gigabit Media Independent Interface (SGMII). The SGMII interface conforms to version 1.8 of the industry standard specification.

#### 7.14.2 EMAC Peripheral Register Description(s)

The memory maps of the EMAC are shown in [Table 7-86](#) through [Table 7-91](#).

Table 7-86 Ethernet MAC (EMAC) Control Registers (Part 1 of 4)

| Hex Address           | Acronym         | Register Name                                 |
|-----------------------|-----------------|-----------------------------------------------|
| 02C8 0000             | TXIDVER         | Transmit Identification and Version Register  |
| 02C8 0004             | TXCONTROL       | Transmit Control Register                     |
| 02C8 0008             | TXTEARDOWN      | Transmit Teardown register                    |
| 02C8 000F             | -               | Reserved                                      |
| 02C8 0010             | RXIDVER         | Receive Identification and Version Register   |
| 02C8 0014             | RXCONTROL       | Receive Control Register                      |
| 02C8 0018             | RXTEARDOWN      | Receive Teardown Register                     |
| 02C8 001C             | -               | Reserved                                      |
| 02C8 0020 - 02C8 007C | -               | Reserved                                      |
| 02C8 0080             | TXINTSTATRAW    | Transmit Interrupt Status (Unmasked) Register |
| 02C8 0084             | TXINTSTATMASKED | Transmit Interrupt Status (Masked) Register   |
| 02C8 0088             | TXINTMASKSET    | Transmit Interrupt Mask Set Register          |



**Table 7-86 Ethernet MAC (EMAC) Control Registers (Part 2 of 4)**

| Hex Address           | Acronym           | Register Name                                                   |
|-----------------------|-------------------|-----------------------------------------------------------------|
| 02C8 008C             | TXINTMASKCLEAR    | Transmit Interrupt Mask Clear Register                          |
| 02C8 0090             | MACINVECTOR       | MAC Input Vector Register                                       |
| 02C8 0094             | MACEOIVECTOR      | MAC End of Interrupt Vector Register                            |
| 02C8 0098 - 02C8 019C | -                 | Reserved                                                        |
| 02C8 00A0             | RXINTSTATRAW      | Receive Interrupt Status (Unmasked) Register                    |
| 02C8 00A4             | RXINTSTATMASKED   | Receive Interrupt Status (Masked) Register                      |
| 02C8 00A8             | RXINTMASKSET      | Receive Interrupt Mask Set Register                             |
| 02C8 00AC             | RXINTMASKCLEAR    | Receive Interrupt Mask Clear Register                           |
| 02C8 00B0             | MACINTSTATRAW     | MAC Interrupt Status (Unmasked) Register                        |
| 02C8 00B4             | MACINTSTATMASKED  | MAC Interrupt Status (Masked) Register                          |
| 02C8 00B8             | MACINTMASKSET     | MAC Interrupt Mask Set Register                                 |
| 02C8 00BC             | MACINTMASKCLEAR   | MAC Interrupt Mask Clear Register                               |
| 02C8 00C0 - 02C8 00FC | -                 | Reserved                                                        |
| 02C8 0100             | RXMBPENABLE       | Receive Multicast/Broadcast/Promiscuous Channel Enable Register |
| 02C8 0104             | RXUNICASTSET      | Receive Unicast Enable Set Register                             |
| 02C8 0108             | RXUNICASTCLEAR    | Receive Unicast Clear Register                                  |
| 02C8 010C             | RXMAXLEN          | Receive Maximum Length Register                                 |
| 02C8 0110             | RXBUFFEROFFSET    | Receive Buffer Offset Register                                  |
| 02C8 0114             | RXFILTERLOWTHRESH | Receive Filter Low Priority Frame Threshold Register            |
| 02C8 0118 - 02C8 011C | -                 | Reserved                                                        |
| 02C8 0120             | RX0FLOWTHRESH     | Receive Channel 0 Flow Control Threshold Register               |
| 02C8 0124             | RX1FLOWTHRESH     | Receive Channel 1 Flow Control Threshold Register               |
| 02C8 0128             | RX2FLOWTHRESH     | Receive Channel 2 Flow Control Threshold Register               |
| 02C8 012C             | RX3FLOWTHRESH     | Receive Channel 3 Flow Control Threshold Register               |
| 02C8 0130             | RX4FLOWTHRESH     | Receive Channel 4 Flow Control Threshold Register               |
| 02C8 0134             | RX5FLOWTHRESH     | Receive Channel 5 Flow Control Threshold Register               |
| 02C8 0138             | RX6FLOWTHRESH     | Receive Channel 6 Flow Control Threshold Register               |
| 02C8 013C             | RX7FLOWTHRESH     | Receive Channel 7 Flow Control Threshold Register               |
| 02C8 0140             | RX0FREEBUFFER     | Receive Channel 0 Free Buffer Count Register                    |
| 02C8 0144             | RX1FREEBUFFER     | Receive Channel 1 Free Buffer Count Register                    |
| 02C8 0148             | RX2FREEBUFFER     | Receive Channel 2 Free Buffer Count Register                    |
| 02C8 014C             | RX3FREEBUFFER     | Receive Channel 3 Free Buffer Count Register                    |
| 02C8 0150             | RX4FREEBUFFER     | Receive Channel 4 Free Buffer Count Register                    |
| 02C8 0154             | RX5FREEBUFFER     | Receive Channel 5 Free Buffer Count Register                    |
| 02C8 0158             | RX6FREEBUFFER     | Receive Channel 6 Free Buffer Count Register                    |
| 02C8 015C             | RX7FREEBUFFER     | Receive Channel 7 Free Buffer Count Register                    |
| 02C8 0160             | MACCONTROL        | MAC Control Register                                            |
| 02C8 0164             | MACSTATUS         | MAC Status Register                                             |
| 02C8 0168             | EMCONTROL         | Emulation Control Register                                      |
| 02C8 016C             | FIFOCONTROL       | FIFO Control Register                                           |
| 02C8 0170             | MACCONFIG         | MAC Configuration Register                                      |
| 02C8 0174             | SOFTRESET         | Soft Reset Register                                             |
| 02C8 01D0             | MACSRCADDRLO      | MAC Source Address Low Bytes Register                           |
| 02C8 01D4             | MACSRCADDRHI      | MAC Source Address High Bytes Register                          |

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**Table 7-86 Ethernet MAC (EMAC) Control Registers (Part 3 of 4)**

| Hex Address           | Acronym   | Register Name                                                          |
|-----------------------|-----------|------------------------------------------------------------------------|
| 02C8 01D8             | MACHASH1  | MAC Hash Address Register 1                                            |
| 02C8 01DC             | MACHASH2  | MAC Hash Address Register 2                                            |
| 02C8 01E0             | BOFFTEST  | Back Off Test Register                                                 |
| 02C8 01E4             | TPACETEST | Transmit Pacing Algorithm Test Register                                |
| 02C8 01E8             | RXPAUSE   | Receive Pause Timer Register                                           |
| 02C8 01EC             | TXPAUSE   | Transmit Pause Timer Register                                          |
| 02C8 0300 - 02C8 03FC | -         | Reserved                                                               |
| 02C8 0400 - 02C8 04FC | -         | Reserved                                                               |
| 02C8 0500             | MACADDRLO | MAC Address Low Bytes Register (used in Receive Address Matching)      |
| 02C8 0504             | MACADDRHI | MAC Address High Bytes Register (used in Receive Address Matching)     |
| 02C8 0508             | MACINDEX  | MAC Index Register                                                     |
| 02C8 050C - 02C8 05FC | -         | Reserved                                                               |
| 02C8 0600             | TX0HDP    | Transmit Channel 0 DMA Head Descriptor Pointer Register                |
| 02C8 0604             | TX1HDP    | Transmit Channel 1 DMA Head Descriptor Pointer Register                |
| 02C8 0608             | TX2HDP    | Transmit Channel 2 DMA Head Descriptor Pointer Register                |
| 02C8 060C             | TX3HDP    | Transmit Channel 3 DMA Head Descriptor Pointer Register                |
| 02C8 0610             | TX4HDP    | Transmit Channel 4 DMA Head Descriptor Pointer Register                |
| 02C8 0614             | TX5HDP    | Transmit Channel 5 DMA Head Descriptor Pointer Register                |
| 02C8 0618             | TX6HDP    | Transmit Channel 6 DMA Head Descriptor Pointer Register                |
| 02C8 061C             | TX7HDP    | Transmit Channel 7 DMA Head Descriptor Pointer Register                |
| 02C8 0620             | RX0HDP    | Receive Channel 0 DMA Head Descriptor Pointer Register                 |
| 02C8 0624             | RX1HDP    | Receive Channel 1 DMA Head Descriptor Pointer Register                 |
| 02C8 0628             | RX2HDP    | Receive Channel 2 DMA Head Descriptor Pointer Register                 |
| 02C8 062C             | RX3HDP    | Receive Channel 3 DMA Head Descriptor Pointer Register                 |
| 02C8 0630             | RX4HDP    | Receive Channel 4 DMA Head Descriptor Pointer Register                 |
| 02C8 0634             | RX5HDP    | Receive Channel 5 DMA Head Descriptor Pointer Register                 |
| 02C8 0638             | RX6HDP    | Receive Channel 6 DMA Head Descriptor Pointer Register                 |
| 02C8 063C             | RX7HDP    | Receive Channel 7 DMA Head Descriptor Pointer Register                 |
| 02C8 0640             | TX0CP     | Transmit Channel 0 Completion Pointer (Interrupt Acknowledge) Register |
| 02C8 0644             | TX1CP     | Transmit Channel 1 Completion Pointer (Interrupt Acknowledge) Register |
| 02C8 0648             | TX2CP     | Transmit Channel 2 Completion Pointer (Interrupt Acknowledge) Register |
| 02C8 064C             | TX3CP     | Transmit Channel 3 Completion Pointer (Interrupt Acknowledge) Register |
| 02C8 0650             | TX4CP     | Transmit Channel 4 Completion Pointer (Interrupt Acknowledge) Register |
| 02C8 0654             | TX5CP     | Transmit Channel 5 Completion Pointer (Interrupt Acknowledge) Register |
| 02C8 0658             | TX6CP     | Transmit Channel 6 Completion Pointer (Interrupt Acknowledge) Register |
| 02C8 065C             | TX7CP     | Transmit Channel 7 Completion Pointer (Interrupt Acknowledge) Register |
| 02C8 0660             | RX0CP     | Receive Channel 0 Completion Pointer (Interrupt Acknowledge) Register  |
| 02C8 0664             | RX1CP     | Receive Channel 1 Completion Pointer (Interrupt Acknowledge) Register  |
| 02C8 0668             | RX2CP     | Receive Channel 2 Completion Pointer (Interrupt Acknowledge) Register  |
| 02C8 066C             | RX3CP     | Receive Channel 3 Completion Pointer (Interrupt Acknowledge) Register  |
| 02C8 0670             | RX4CP     | Receive Channel 4 Completion Pointer (Interrupt Acknowledge) Register  |
| 02C8 0674             | RX5CP     | Receive Channel 5 Completion Pointer (Interrupt Acknowledge) Register  |
| 02C8 0678             | RX6CP     | Receive Channel 6 Completion Pointer (Interrupt Acknowledge) Register  |
| 02C8 067C             | RX7CP     | Receive Channel 7 Completion Pointer (Interrupt Acknowledge) Register  |

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**Table 7-86 Ethernet MAC (EMAC) Control Registers (Part 4 of 4)**

| Hex Address              | Acronym | Register Name |
|--------------------------|---------|---------------|
| 02C8 0680 - 02C8 06FC    | -       | Reserved      |
| 02C8 0700 - 02C8 077C    | -       | Reserved      |
| 02C8 0780 - 02C8 0FFF    | -       | Reserved      |
| <b>End of Table 7-86</b> |         |               |

**Table 7-87 EMAC Statistics Registers (Part 1 of 2)**

| Hex Address | Acronym           | Register Name                                                                                       |
|-------------|-------------------|-----------------------------------------------------------------------------------------------------|
| 02C8 0200   | RXGOODFRAMES      | Good Receive Frames Register                                                                        |
| 02C8 0204   | RXBROADCASTFRAMES | Broadcast Receive Frames Register (Total number of Good Broadcast Frames Receive)                   |
| 02C8 0208   | RXMCASTFRAMES     | Multicast Receive Frames Register (Total number of Good Multicast Frames Received)                  |
| 02C8 020C   | RXPAUSEFRAMES     | Pause Receive Frames Register                                                                       |
| 02C8 0210   | RXCRCERRORS       | Receive CRC Errors Register (Total number of Frames Received with CRC Errors)                       |
| 02C8 0214   | RXALIGNCODEERRORS | Receive Alignment/Code Errors register (Total number of frames received with alignment/code errors) |
| 02C8 0218   | RXOVERSIZED       | Receive Oversized Frames Register (Total number of Oversized Frames Received)                       |
| 02C8 021C   | RXJABBER          | Receive Jabber Frames Register (Total number of Jabber Frames Received)                             |
| 02C8 0220   | RXUNDERSIZED      | Receive Undersized Frames Register (Total number of Undersized Frames Received)                     |
| 02C8 0224   | RXFRAGMENTS       | Receive Frame Fragments Register                                                                    |
| 02C8 0228   | RXFILTERED        | Filtered Receive Frames Register                                                                    |
| 02C8 022C   | RXQOSFILTERED     | Received QOS Filtered Frames Register                                                               |
| 02C8 0230   | RXOCTETS          | Receive Octet Frames Register (Total number of Received Bytes in Good Frames)                       |
| 02C8 0234   | TXGOODFRAMES      | Good Transmit Frames Register (Total number of Good Frames Transmitted)                             |
| 02C8 0238   | TXBROADCASTFRAMES | Broadcast Transmit Frames Register                                                                  |
| 02C8 023C   | TXMCASTFRAMES     | Multicast Transmit Frames Register                                                                  |
| 02C8 0240   | TXPAUSEFRAMES     | Pause Transmit Frames Register                                                                      |
| 02C8 0244   | TXDEFERED         | Deferred Transmit Frames Register                                                                   |
| 02C8 0248   | TXCOLLISION       | Transmit Collision Frames Register                                                                  |
| 02C8 024C   | TXSINGLECOLL      | Transmit Single Collision Frames Register                                                           |
| 02C8 0250   | TXMULTICOLL       | Transmit Multiple Collision Frames Register                                                         |
| 02C8 0254   | TXEXCESSIVECOLL   | Transmit Excessive Collision Frames Register                                                        |
| 02C8 0258   | TXLATECOLL        | Transmit Late Collision Frames Register                                                             |
| 02C8 025C   | TXUNDERRUN        | Transmit Under Run Error Register                                                                   |
| 02C8 0260   | TXCARRIERSENSE    | Transmit Carrier Sense Errors Register                                                              |
| 02C8 0264   | TXOCTETS          | Transmit Octet Frames Register                                                                      |
| 02C8 0268   | FRAME64           | Transmit and Receive 64 Octet Frames Register                                                       |
| 02C8 026C   | FRAME65T127       | Transmit and Receive 65 to 127 Octet Frames Register                                                |
| 02C8 0270   | FRAME128T255      | Transmit and Receive 128 to 255 Octet Frames Register                                               |
| 02C8 0274   | FRAME256T511      | Transmit and Receive 256 to 511 Octet Frames Register                                               |
| 02C8 0278   | FRAME512T1023     | Transmit and Receive 512 to 1023 Octet Frames Register                                              |
| 02C8 027C   | FRAME1024TUP      | Transmit and Receive 1024 to 1518 Octet Frames Register                                             |
| 02C8 0280   | NETOCTETS         | Network Octet Frames Register                                                                       |
| 02C8 0284   | RXSOFOVERRUNS     | Receive FIFO or DMA Start of Frame Overruns Register                                                |
| 02C8 0288   | RXMOFOVERRUNS     | Receive FIFO or DMA Middle of Frame Overruns Register                                               |

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**Table 7-87 EMAC Statistics Registers (Part 2 of 2)**

| Hex Address              | Acronym       | Register Name                                                    |
|--------------------------|---------------|------------------------------------------------------------------|
| 02C8 028C                | RXDMAOVERRUNS | Receive DMA Start of Frame and Middle of Frame Overruns Register |
| 02C8 0290 - 02C8 02FC    | -             | Reserved                                                         |
| <b>End of Table 7-87</b> |               |                                                                  |

**Table 7-88 EMAC Descriptor Memory**

| Hex Address              | Acronym | Register Name          |
|--------------------------|---------|------------------------|
| 02E0 0000 - 02E0 3FFF    | -       | EMAC Descriptor Memory |
| <b>End of Table 7-88</b> |         |                        |

**Table 7-89 SGMII Control Registers**

| Hex Address              | Acronym           | Register Name                            |
|--------------------------|-------------------|------------------------------------------|
| 02C4 0000                | IDVER             | Identification and Version register      |
| 02C4 0004                | SOFT_RESET        | Software Reset Register                  |
| 02C4 0010                | CONTROL           | Control Register                         |
| 02C4 0014                | STATUS            | Status Register                          |
| 02C4 0018                | MR_ADV_ABILITY    | Advertised Ability Register              |
| 02C4 001C                | -                 | Reserved                                 |
| 02C4 0020                | MR_LP_ADV_ABILITY | Link Partner Advertised Ability Register |
| 02C4 0024                | -                 | Reserved                                 |
| 02C4 0030                | TX_CFG            | Transmit Configuration Register          |
| 02C4 0034                | RX_CFG            | Receive Configuration Register           |
| 02C4 0038                | AUX_CFG           | Auxiliary Configuration Register         |
| 02C4 0040 - 02C4 0048    | -                 | Reserved                                 |
| <b>End of Table 7-89</b> |                   |                                          |

**Table 7-90 EMIC Control Registers**

| Hex Address              | Acronym          | Register Name                                       |
|--------------------------|------------------|-----------------------------------------------------|
| 02C8 1000                | IDVER            | Identification and Version register                 |
| 02C8 1004                | SOFT_RESET       | Software Reset Register                             |
| 02C8 1008                | EM_CONTROL       | Emulation Control Register                          |
| 02C8 100C                | INT_CONTROL      | Interrupt Control Register                          |
| 02C8 1010                | C_RX_THRESH_EN   | Receive Threshold Interrupt Enable Register         |
| 02C8 1014                | C_RX_EN          | Receive Interrupt Enable Register                   |
| 02C8 1018                | C_TX_EN          | Transmit Interrupt Enable Register                  |
| 02C8 101C                | C_MISC_EN        | Misc Interrupt Enable Register                      |
| 02C8 1040                | C_RX_THRESH_STAT | Receive Threshold Masked Interrupt Status Register  |
| 02C8 1044                | C_RX_STAT        | Receive Interrupt Masked Interrupt Status Register  |
| 02C8 1048                | C_TX_STAT        | Transmit Interrupt Masked Interrupt Status Register |
| 02C8 104C                | C_MISC_STAT      | Misc Interrupt Masked Interrupt Status Register     |
| 02C8 1070                | C_RX_IMAX        | Receive Interrupts Per Millisecond                  |
| 02C8 1074                | C_TX_IMAX        | Transmit Interrupts Per Millisecond                 |
| <b>End of Table 7-90</b> |                  |                                                     |

### 7.14.3 EMAC Electrical Data/Timing (SGMII)

The *TMS320TCI6484 and TMS320C6457 DSPs Hardware Design Guide* application report (literature number [SPRAAV7](#)) specifies a complete EMAC and SGMII interface solutions for the C6457 as well as a list of compatible EMAC and SGMII devices. TI has performed the simulation and system characterization to ensure all EMAC and SGMII interface timings in this solution are met; therefore, no electrical data/timing information is supplied here for this interface.



**Note**—TI supports *only* designs that follow the board design guidelines outlined in the application report.

## 7.15 Management Data Input/Output (MDIO)

The Management Data Input/Output (MDIO) module implements the 802.3 serial management interface to interrogate and controls up to 32 Ethernet PHY(s) connected to the device, using a shared two-wire bus. Application software uses the MDIO module to configure the auto-negotiation parameters of each PHY attached to the EMAC, retrieve the negotiation results, and configure required parameters in the EMAC module for correct operation. The module is designed to allow almost transparent operation of the MDIO interface, with very little maintenance from the core processor.

The EMAC control module is the main interface between the device core processor, the MDIO module, and the EMAC module. The relationship between these three components is shown in [Figure 7-42](#).

For more detailed information on the EMAC/MDIO, see the *TMS320C6457 DSP EMAC/MDIO Module Reference Guide* (literature number [SPRUGK9](#)).

### 7.15.1 MDIO Peripheral Register Description(s)

The memory map of the MDIO is shown in [Table 7-91](#).

**Table 7-91 MDIO Registers**

| Hex Address           | Acronym          | Register Name                                            |
|-----------------------|------------------|----------------------------------------------------------|
| 02C8 1800             | VERSION          | MDIO Version Register                                    |
| 02C8 1804             | CONTROL          | MDIO Control Register                                    |
| 02C8 1808             | ALIVE            | MDIO PHY Alive Status Register                           |
| 02C8 180C             | LINK             | MDIO PHY Link Status Register                            |
| 02C8 1810             | LINKINTRAW       | MDIO link Status Change Interrupt (unmasked) Register    |
| 02C8 1814             | LINKINTMASKED    | MDIO link Status Change Interrupt (masked) Register      |
| 02C8 1818 - 02C8 181C | -                | Reserved                                                 |
| 02C8 1820             | USERINTRAW       | MDIO User Command Complete Interrupt (Unmasked) Register |
| 02C8 1824             | USERINTMASKED    | MDIO User Command Complete Interrupt (Masked) Register   |
| 02C8 1828             | USERINTMASKSET   | MDIO User Command Complete Interrupt Mask Set Register   |
| 02C8 182C             | USERINTMASKCLEAR | MDIO User Command Complete Interrupt Mask Clear Register |
| 02C8 1830 - 02C8 187C | -                | Reserved                                                 |
| 02C8 1880             | USERACCESS0      | MDIO User Access Register 0                              |
| 02C8 1884             | USERPHYSEL0      | MDIO User PHY Select Register 0                          |
| 02C8 1888             | USERACCESS1      | MDIO User Access Register 1                              |
| 02C8 188C             | USERPHYSEL1      | MDIO User PHY Select Register 1                          |
| 02C8 1890 - 02C8 1FFF | -                | Reserved                                                 |

**End of Table 7-91**

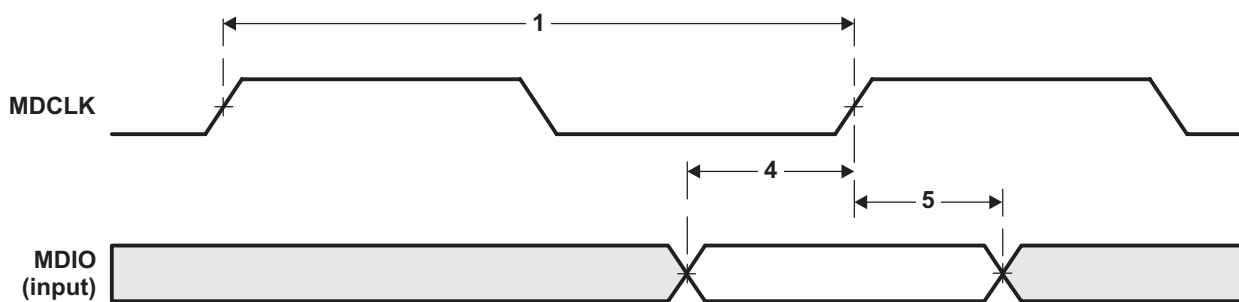
## 7.15.2 MDIO Electrical Data/Timing

**Table 7-92 MDIO Input Timing Requirements**  
(see Figure 7-43)

| No. |                                                                           | Min | Max | Unit |
|-----|---------------------------------------------------------------------------|-----|-----|------|
| 1   | $t_{c(MDCLK)}$ Cycle time, MDCLK                                          | 400 |     | ns   |
| 2a  | $t_{w(MDCLKH)}$ Pulse duration, MDCLK high                                | 180 |     | ns   |
| 2b  | $t_{w(MDCLKL)}$ Pulse duration, MDCLK low                                 | 180 |     | ns   |
| 3   | $t_t(MDCLK)$ Transition time, MDCLK                                       |     | 5   | ns   |
| 4   | $t_{su(MDIO-MDCLKH)}$ Setup time, MDIO data input valid before MDCLK high | 10  |     | ns   |
| 5   | $t_h(MDCLKH-MDIO)$ Hold time, MDIO data input valid after MDCLK high      | 10  |     | ns   |

**End of Table 7-92**

**Figure 7-43 MDIO Input Timing**



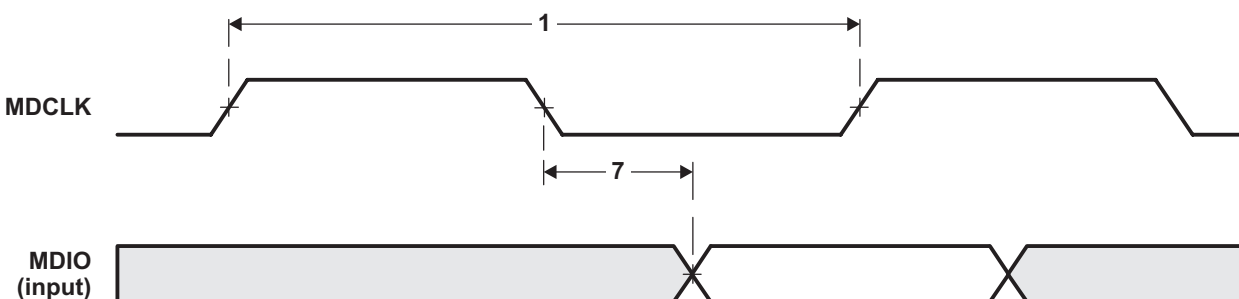
**Table 7-93 MDIO Output Switching Characteristics <sup>(1)</sup>**  
(see Figure 7-44)

| No. | Parameter                                                            | Min | Max | Unit |
|-----|----------------------------------------------------------------------|-----|-----|------|
| 7   | $t_{d(MDCLKL-MDIO)}$ Delay time, MDCLK low to MDIO data output valid | 100 |     | ns   |

**End of Table 7-93**

<sup>1</sup> Over recommended operating conditions.

**Figure 7-44 MDIO Output Timing**



## 7.16 Timers

The timers can be used to: time events, count events, generate pulses, interrupt the CPU, and send synchronization events to the EDMA3 channel controller.

### 7.16.1 Timers Device-Specific Information

The TMS320C6457 device has two general-purpose timers, Timer0 and Timer1, each of which can be configured as a general-purpose timer or as a watchdog timer. When configured as a general-purpose timer, each timer can be programmed as a 64-bit timer or as two separate 32-bit timers.

Each timer is made up of two 32-bit counters: a high counter and a low counter. The timer pins, TINPLx and TOUTLx are connected to the low counter. The high counter does not have any external device pins.

#### 7.16.1.1 Timer Watchdog Select

As mentioned previously, the timers can operate in watchdog mode. When in watchdog mode, the event output from Timer1 can optionally reset the CPU. In order for the event to trigger the reset when this operation is desired, the Timer1 watchdog reset selection register (WDRSTSEL) should be set to 1. The WDRSTSEL register is shown in Table 7-94 and described in Table 7-95.

**Table 7-94 Timer1 Watchdog Reset Selection Register (WDRSTSEL)**

| Address - 0288 0920h |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |
|----------------------|--------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|
| Bit                  | 31                                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
| Acronym              | Reserved                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |
| Reset <sup>(1)</sup> |                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |
| Bit                  | 15                                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| Acronym              | Reserved                             |    |    |    |    |    |    |    |    |    |    |    |    |    |    | WDRSTSEL |
| Reset <sup>(1)</sup> | R- 0000 0000 0000 0000 0000 0000 000 |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R/W-0    |

1 R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-95 Timer1 Watchdog Reset Selection Register (WDRSTSEL) Field Descriptions**

| Bit               | Acronym  | Description                                                                                                                                                  |
|-------------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1              | Reserved | Reserved.                                                                                                                                                    |
| 0                 | WDRSTSEL | Reset Select for Watchdog Timer1<br>0 = TOUT1L does not cause a reset to the C64x+ megamodule (default)<br>1 = TOUT1L causes a reset to the C64x+ megamodule |
| End of Table 7-95 |          |                                                                                                                                                              |

### 7.16.2 Timers Peripheral Register Description(s)

**Table 7-96 Timer 0 Registers (Part 1 of 2)**

| Hex Address Range | Acronym        | Register Name                                     |
|-------------------|----------------|---------------------------------------------------|
| 0294 0000         | -              | Reserved                                          |
| 0294 0004         | EMUMGT_CLKSPD0 | Timer 0 Emulation Management/Clock Speed Register |
| 0294 0008         | -              | Reserved                                          |
| 0294 000C         | -              | Reserved                                          |
| 0294 0010         | CNTLO0         | Timer 0 Counter Register Low                      |
| 0294 0014         | CNTHI0         | Timer 0 Counter Register High                     |
| 0294 0018         | PRDLO0         | Timer 0 Period Register Low                       |
| 0294 001C         | PRDHI0         | Timer 0 Period Register High                      |
| 0294 0020         | TCR0           | Timer 0 Control Register                          |
| 0294 0024         | TGCR0          | Timer 0 Global Control Register                   |
| 0294 0028         | WDTCR0         | Timer 0 Watchdog Timer Control Register           |
| 0294 002C         | -              | Reserved                                          |

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**Table 7-96 Timer 0 Registers (Part 2 of 2)**

| Hex Address Range        | Acronym | Register Name |
|--------------------------|---------|---------------|
| 0294 0030                | -       | Reserved      |
| 0294 0034 - 0297 FFFF    | -       | Reserved      |
| <b>End of Table 7-96</b> |         |               |

**Table 7-97 Timer 1 Registers**

| Hex Address Range        | Acronym        | Register Name                                     |
|--------------------------|----------------|---------------------------------------------------|
| 0298 0000                | -              | Reserved                                          |
| 0298 0004                | EMUMGT_CLKSPD1 | Timer 1 Emulation Management/Clock Speed Register |
| 0298 0008                | -              | Reserved                                          |
| 0298 000C                | -              | Reserved                                          |
| 0298 0010                | CNTLO1         | Timer 1 Counter Register Low                      |
| 0298 0014                | CNTHI1         | Timer 1 Counter Register High                     |
| 0298 0018                | PRDLO1         | Timer 1 Period Register Low                       |
| 0298 001C                | PRDHI1         | Timer 1 Period Register High                      |
| 0298 0020                | TCR1           | Timer 1 Control Register                          |
| 0298 0024                | TGCR1          | Timer 1 Global Control Register                   |
| 0298 0028                | WDTCR1         | Timer 1 Watchdog Timer Control Register           |
| 0298 002C                | -              | Reserved                                          |
| 0298 0030                | -              | Reserved                                          |
| 0298 0034 - 0299 FFFF    | -              | Reserved                                          |
| <b>End of Table 7-97</b> |                |                                                   |

### 7.16.3 Timers Electrical Data/Timing

The below tables and figures describe the timing requirements and switching characteristics of both the Timer0 and Timer1 peripherals.

**Table 7-98 Timer Input Timing Requirements<sup>(1)</sup>**  
(see Figure 7-45)

| No.                      |                                            | Min | Max | Unit |
|--------------------------|--------------------------------------------|-----|-----|------|
| 1                        | $t_{w(TIMI\ H)}$ Pulse duration, TIMI high | 12C |     | ns   |
| 2                        | $t_{w(TIMI\ L)}$ Pulse duration, TIMI low  | 12C |     | ns   |
| <b>End of Table 7-98</b> |                                            |     |     |      |

<sup>1</sup> If CORECLKSEL = 0, C = 1/CORECLK(NIP) frequency in ns. If CORECLKSEL = 1, C = 1/ALTCORECLK frequency in ns.

**Table 7-99 Timer Output Switching Characteristics<sup>(1) (2)</sup>**  
(see Figure 7-45)

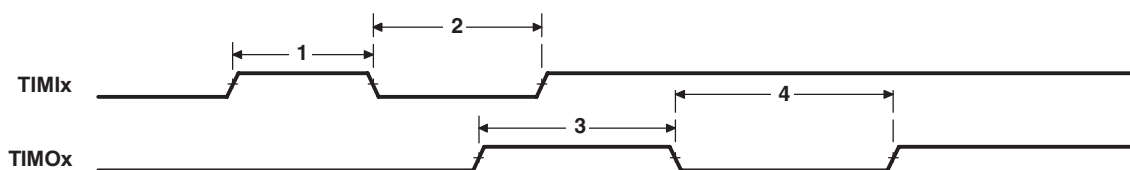
| No.                      | Parameter                                  | Min     | Max | Unit |
|--------------------------|--------------------------------------------|---------|-----|------|
| 3                        | $t_{w(TIMO\ H)}$ Pulse duration, TIMO high | 12C - 3 |     | ns   |
| 4                        | $t_{w(TIMO\ L)}$ Pulse duration, TIMO low  | 12C - 3 |     | ns   |
| <b>End of Table 7-99</b> |                                            |         |     |      |

<sup>1</sup> Over recommended operating conditions.

<sup>2</sup> If CORECLKSEL = 0, C = 1/CORECLK(NIP) frequency in ns. If CORECLKSEL = 1, C = 1/ALTCORECLK frequency in ns.



Figure 7-45 Timer Timing



## 7.17 Enhanced Viterbi-Decoder Coprocessor (VCP2)

### 7.17.1 VCP2 Device-Specific Information

The TMS320C6457 device has a high-performance embedded Viterbi-Decoder Coprocessor (VCP2) that significantly speeds up channel-decoding operations on-chip. The VCP2, operating at CPU clock divided-by-3, can decode more than 694 7.95-Kbps adaptive multi-rate (AMR) [K = 9, R = 1/3] voice channels. The VCP2 supports constraint lengths K = 5, 6, 7, 8, and 9, rates R = 3/4, 1/2, 1/3, 1/4, and 1/5, and flexible polynomials, while generating hard decisions or soft decisions. Communications between the VCP2 and the CPU are carried out through the EDMA3 controller.

The VCP2 supports:

- Unlimited frame sizes
- Code rates 3/4, 1/2, 1/3, 1/4, and 1/5
- Constraint lengths 5, 6, 7, 8, and 9
- Programmable encoder polynomials
- Programmable reliability and convergence lengths
- Hard and soft decoded decisions
- Tail and convergent modes
- Yamamoto logic
- Tail biting logic
- Various input and output FIFO lengths

For more detailed information on the VCP2, see the *TMS320C6457 DSP Viterbi-Decoder Coprocessor 2 (VCP2) Reference Guide* (literature number [SPRUGK0](#)).

### 7.17.2 VCP2 Peripheral Register Description

Table 7-100 VCP2 Registers (Part 1 of 2)

| EDMA Bus Hex Address Range | Configuration Bus Hex Address Range | Acronym | Register Name                           |
|----------------------------|-------------------------------------|---------|-----------------------------------------|
| 5800 0000                  | -                                   | VCPIC0  | VCP2 Input Configuration Register 0     |
| 5800 0004                  | -                                   | VCPIC1  | VCP2 Input Configuration Register 1     |
| 5800 0008                  | -                                   | VCPIC2  | VCP2 Input Configuration Register 2     |
| 5800 000C                  | -                                   | VCPIC3  | VCP2 Input Configuration Register 3     |
| 5800 0010                  | -                                   | VCPIC4  | VCP2 Input Configuration Register 4     |
| 5800 0014                  | -                                   | VCPIC5  | VCP2 Input Configuration Register 5     |
| 5800 0018 - 5800 0044      | -                                   | -       | Reserved                                |
| 5800 0048                  | -                                   | VCPOUT0 | VCP2 Output Register 0                  |
| 5800 004C                  | -                                   | VCPOUT1 | VCP2 Output Register 1                  |
| 5800 0050 - 5800 007C      | -                                   | -       | Reserved                                |
| 5800 0080                  | N/A                                 | VCPWBM  | VCP2 Branch Metrics Write FIFO Register |
| 5800 0084 - 5800 009C      | -                                   | -       | Reserved                                |

**Table 7-100 VCP2 Registers (Part 2 of 2)**

| EDMA Bus Hex Address Range | Configuration Bus Hex Address Range | Acronym  | Register Name                     |
|----------------------------|-------------------------------------|----------|-----------------------------------|
| 5800 00C0                  | N/A                                 | VCPRDECS | VCP2 Decisions Read FIFO Register |
| N/A                        | 02B8 0000                           | VCPPID   | VCP2 Peripheral ID Register       |
| N/A                        | 02B8 0018                           | VCPEXE   | VCP2 Execution Register           |
| N/A                        | 02B8 0020                           | VCPEND   | VCP2 Endian Mode Register         |
| N/A                        | 02B8 0040                           | VCPSTAT0 | VCP2 Status Register 0            |
| N/A                        | 02B8 0044                           | VCPSTAT1 | VCP2 Status Register 1            |
| N/A                        | 02B8 0050                           | VCPEER   | VCP2 Error Register               |
| -                          | -                                   | -        | Reserved                          |
| N/A                        | 02B8 0060                           | VCPEMU   | VCP2 Emulation Control Register   |
| N/A                        | 02B8 0064 - 02B9 FFFF               | -        | Reserved                          |
| 5800 1000                  | -                                   | BM       | Branch Metrics                    |
| 5800 2000                  | -                                   | SM       | State Metric                      |
| 5800 3000                  | -                                   | TBHD     | Traceback Hard Decision           |
| 5800 6000                  | -                                   | TBSD     | Traceback Soft Decision           |
| 5800 F000                  | -                                   | IO       | Decoded Bits                      |
| <b>End of Table 7-100</b>  |                                     |          |                                   |

## 7.18 Enhanced Turbo Decoder Coprocessor (TCP2)

### 7.18.1 TCP2 Device-Specific Information

The C6457 device has two high-performance embedded Turbo-Decoder Coprocessors (TCP2\_A and TCP2\_B) that significantly speed up channel-decoding operations on-chip. Each TCP2, operating at CPU clock divided-by-3, can decode up to fifty 384-Kbps or eight 2-Mbps turbo-encoded channels (assuming 6 iterations). The TCP2 implements the max \* log-map algorithm and is designed to support all polynomials and rates required by Third-Generation Partnership Projects (3GPP and 3GPP2), with fully programmable frame length and turbo interleaver. Decoding parameters such as the number of iterations and stopping criteria are also programmable. Communications between the TCP2 and the CPU are carried out through the EDMA3 controller.

Each TCP2 supports:

- Parallel concatenated convolutional turbo decoding using the MAP algorithm
- All turbo code rates greater than or equal to 1/5
- 3GPP and CDMA2000 turbo encoder trellis
- 3GPP and CDMA2000 block sizes in standalone mode
- Larger block sizes in shared processing mode
- Both max log MAP and log MAP decoding
- Sliding windows algorithm with variable reliability and prolog lengths
- The prolog reduction algorithm
- Execution of a minimum and maximum number of iterations
- The SNR stopping criteria algorithm
- The CRC stopping criteria algorithm

For more detailed information on the TCP2, see the *TMS320C6457 DSP Turbo-Decoder Coprocessor 2 (TCP2) Reference Guide* (literature number [SPRUGK1](#)).

**Table 7-101 TCP2\_A Registers**

| EDMA Bus Hex Address Range | Configuration Bus Hex Address Range | Acronym | Register Name                           |
|----------------------------|-------------------------------------|---------|-----------------------------------------|
| 5000 0000                  | -                                   | TCPIC0  | TCP2 Input Configuration Register 0     |
| 5000 0004                  | -                                   | TCPIC1  | TCP2 Input Configuration Register 1     |
| 5000 0008                  | -                                   | TCPIC2  | TCP2 Input Configuration Register 2     |
| 5000 000C                  | -                                   | TCPIC3  | TCP2 Input Configuration Register 3     |
| 5000 0010                  | -                                   | TCPIC4  | TCP2 Input Configuration Register 4     |
| 5000 0014                  | -                                   | TCPIC5  | TCP2 Input Configuration Register 5     |
| 5000 0018                  | -                                   | TCPIC6  | TCP2 Input Configuration Register 6     |
| 5000 001C                  | -                                   | TCPIC7  | TCP2 Input Configuration Register 7     |
| 5000 0020                  | -                                   | TCPIC8  | TCP2 Input Configuration Register 8     |
| 5000 0024                  | -                                   | TCPIC9  | TCP2 Input Configuration Register 9     |
| 5000 0028                  | -                                   | TCPIC10 | TCP2 Input Configuration Register 10    |
| 5000 002C                  | -                                   | TCPIC11 | TCP2 Input Configuration Register 11    |
| 5000 0030                  | -                                   | TCPIC12 | TCP2 Input Configuration Register 12    |
| 5000 0034                  | -                                   | TCPIC13 | TCP2 Input Configuration Register 13    |
| 5000 0038                  | -                                   | TCPIC14 | TCP2 Input Configuration Register 14    |
| 5000 003C                  | -                                   | TCPIC15 | TCP2 Input Configuration Register 15    |
| 5000 0040                  | -                                   | TCPOUT0 | TCP2 Output Parameters Register 0       |
| 5000 0044                  | -                                   | TCPOUT1 | TCP2 Output Parameters Register 1       |
| 5000 0048                  | -                                   | TCPOUT2 | TCP2 Output Parameters Register 2       |
| 5001 0000                  | N/A                                 | X0      | TCP2 Data/Sys and Parity Memory         |
| 5003 0000                  | N/A                                 | W0      | TCP2 Extrinsic Mem 0                    |
| 5004 0000                  | N/A                                 | W1      | TCP2 Extrinsic Mem 1                    |
| 5005 0000                  | N/A                                 | I0      | TCP2 Interleaver Memory                 |
| 5006 0000                  | N/A                                 | O0      | TCP2 Output/Decision Memory             |
| 5007 0000                  | N/A                                 | S0      | TCP2 Scratch Pad Memory                 |
| 5008 0000                  | N/A                                 | T0      | TCP2 Beta State Memory                  |
| 5009 0000                  | N/A                                 | C0      | TCP2 CRC Memory                         |
| 500A 0000                  | N/A                                 | B0      | TCP2 Beta Prolog Memory                 |
| 500B 0000                  | N/A                                 | A0      | TCP2 Alpha Prolog Memory                |
|                            | 02BA 0000                           | TCPPID  | TCP2 Peripheral Identification Register |
| N/A                        | 02BA 004C                           | TCPEXE  | TCP2 Execute Register                   |
| N/A                        | 02BA 0050                           | TCPEND  | TCP2 Endianness Register                |
| N/A                        | 02BA 0060                           | TCPERR  | TCP2 Error Register                     |
| N/A                        | 02BA 0068                           | TCPSTAT | TCP2 Status Register                    |
| N/A                        | 02BA 0070                           | TCPEMU  | TCP2 Emulation Register                 |
| N/A                        | 02BA 0074 - 02BA 00FF               | -       | Reserved                                |

End of Table 7-101

**Table 7-102 TCP2\_B Registers (Part 1 of 2)**

| EDMA Bus Hex Address Range | Configuration Bus Hex Address Range | Acronym | Register Name                       |
|----------------------------|-------------------------------------|---------|-------------------------------------|
| 5010 0000                  | -                                   | TCPIC0  | TCP2 Input Configuration Register 0 |
| 5010 0004                  | -                                   | TCPIC1  | TCP2 Input Configuration Register 1 |
| 5010 0008                  | -                                   | TCPIC2  | TCP2 Input Configuration Register 2 |

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**Table 7-102 TCP2\_B Registers (Part 2 of 2)**

| EDMA Bus Hex Address Range | Configuration Bus Hex Address Range | Acronym | Register Name                           |
|----------------------------|-------------------------------------|---------|-----------------------------------------|
| 5010 000C                  | -                                   | TCPIC3  | TCP2 Input Configuration Register 3     |
| 5010 0010                  | -                                   | TCPIC4  | TCP2 Input Configuration Register 4     |
| 5010 0014                  | -                                   | TCPIC5  | TCP2 Input Configuration Register 5     |
| 5010 0018                  | -                                   | TCPIC6  | TCP2 Input Configuration Register 6     |
| 5010 001C                  | -                                   | TCPIC7  | TCP2 Input Configuration Register 7     |
| 5010 0020                  | -                                   | TCPIC8  | TCP2 Input Configuration Register 8     |
| 5010 0024                  | -                                   | TCPIC9  | TCP2 Input Configuration Register 9     |
| 5010 0028                  | -                                   | TCPIC10 | TCP2 Input Configuration Register 10    |
| 5010 002C                  | -                                   | TCPIC11 | TCP2 Input Configuration Register 11    |
| 5010 0030                  | -                                   | TCPIC12 | TCP2 Input Configuration Register 12    |
| 5010 0034                  | -                                   | TCPIC13 | TCP2 Input Configuration Register 13    |
| 5010 0038                  | -                                   | TCPIC14 | TCP2 Input Configuration Register 14    |
| 5010 003C                  | -                                   | TCPIC15 | TCP2 Input Configuration Register 15    |
| 5010 0040                  | -                                   | TCPOUT0 | TCP2 Output Parameters Register 0       |
| 5010 0044                  | -                                   | TCPOUT1 | TCP2 Output Parameters Register 1       |
| 5010 0048                  | -                                   | TCPOUT2 | TCP2 Output Parameters Register 2       |
| 5011 0000                  | N/A                                 | X0      | TCP2 Data/Sys and Parity Memory         |
| 5013 0000                  | N/A                                 | W0      | TCP2 Extrinsic Mem 0                    |
| 5014 0000                  | N/A                                 | W1      | TCP2 Extrinsic Mem 1                    |
| 5015 0000                  | N/A                                 | I0      | TCP2 Interleaver Memory                 |
| 5016 0000                  | N/A                                 | O0      | TCP2 Output/Decision Memory             |
| 5017 0000                  | N/A                                 | S0      | TCP2 Scratch Pad Memory                 |
| 5018 0000                  | N/A                                 | T0      | TCP2 Beta State Memory                  |
| 5019 0000                  | N/A                                 | C0      | TCP2 CRC Memory                         |
| 501A 0000                  | N/A                                 | B0      | TCP2 Beta Prolog Memory                 |
| 501B 0000                  | N/A                                 | A0      | TCP2 Alpha Prolog Memory                |
|                            | 02BA 0100                           | TCPPID  | TCP2 Peripheral Identification Register |
| N/A                        | 02BA 014C                           | TCPEXE  | TCP2 Execute Register                   |
| N/A                        | 02BA 0150                           | TCPEND  | TCP2 Endianness Register                |
| N/A                        | 02BA 0160                           | TCPEXR  | TCP2 Error Register                     |
| N/A                        | 02BA 0168                           | TCPSTAT | TCP2 Status Register                    |
| N/A                        | 02BA 0170                           | TCPEMU  | TCP2 Emulation Register                 |
| N/A                        | 02BA 0174 - 02BB FFFF               | -       | Reserved                                |

**End of Table 7-102**

PRODUCT PREVIEW

## 7.19 UTOPIA

### 7.19.1 UTOPIA Device-Specific Information

The Universal Test and Operations PHY Interface for ATM (UTOPIA) peripheral is a 50 MHz, 8-Bit Slave-only interface. The UTOPIA is more simplistic than the Ethernet MAC, in that the UTOPIA is serviced directly by the EDMA3 controller. The UTOPIA peripheral contains two, two-cell FIFOs, one for transmit and one for receive, with which to buffer up data sent/received across the pins. There is a transmit and a receive event to the EDMA3 channel controller to enable servicing.

For more detailed information on the UTOPIA peripheral, see the *TMS320C6457 DSP Universal Test and Operations PHY Interface for ATM 2 (UTOPIA2)* (literature number [SPRUGL1](#)).

### 7.19.2 UTOPIA Peripheral Register Description(s)

**Table 7-103 UTOPIA Registers**

| Hex Address Range         | Acronym | Register Name                    |
|---------------------------|---------|----------------------------------|
| 02B4 0000                 | UCR     | UTOPIA Control Register          |
| 02B4 0004                 | -       | Reserved                         |
| 02B4 0008                 | -       | Reserved                         |
| 02B4 000C                 | -       | Reserved                         |
| 02B4 0010                 | -       | Reserved                         |
| 02B4 0014                 | CDR     | Clock Detect Register            |
| 02B4 0018                 | EIER    | Error Interrupt Enable Register  |
| 02B4 001C                 | EIPR    | Error Interrupt Pending Register |
| 02B4 0020 - 02B4 01FF     | -       | Reserved                         |
| 02B4 0200 - 02B7 FFFF     | -       | Reserved                         |
| <b>End of Table 7-103</b> |         |                                  |

**Table 7-104 UTOPIA Data Queues (Receive and Transmit) Registers**

| Hex Address Range         | Acronym | Register Name                   |
|---------------------------|---------|---------------------------------|
| 3D00 0000 - 3D00 007F     | URQ     | UTOPIA Receive (RX) Data Queue  |
| 3D00 0080 - 3D00 03FF     | -       | Reserved                        |
| 3D00 0400 - 3D00 047F     | UXQ     | UTOPIA Transmit (TX) Data Queue |
| 3D00 0480 - 3D00 07FF     | -       | Reserved                        |
| <b>End of Table 7-104</b> |         |                                 |

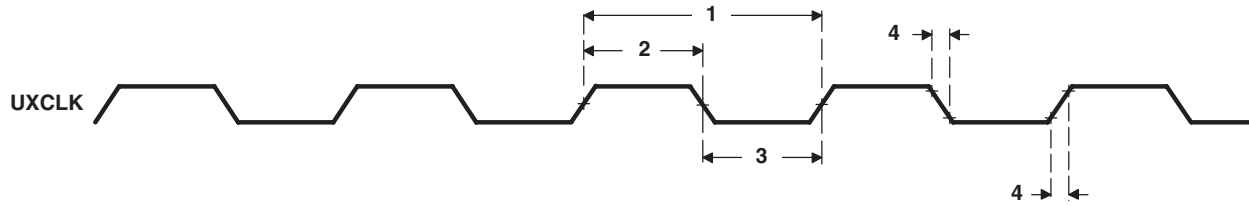
### 7.19.3 UTOPIA Electrical Data/Timing

**Table 7-105 UXCLK Timing Requirements<sup>(1)</sup>**  
(see [Figure 7-46](#))

| No.                       |                                            | Min               | Max               | Unit |
|---------------------------|--------------------------------------------|-------------------|-------------------|------|
| 1                         | $t_{c(UXCLK)}$ Cycle time, UXCLK           | 20                |                   | ns   |
| 2                         | $t_{w(UXCLKH)}$ Pulse duration, UXCLK high | $0.4t_{c(UXCLK)}$ | $0.6t_{c(UXCLK)}$ | ns   |
| 3                         | $t_{w(UXCLKL)}$ Pulse duration, UXCLK low  | $0.4t_{c(UXCLK)}$ | $0.6t_{c(UXCLK)}$ | ns   |
| 4                         | $t_{t(UXCLK)}$ Transition time, UXCLK      |                   | 2                 | ns   |
| <b>End of Table 7-105</b> |                                            |                   |                   |      |

<sup>1</sup> The reference points for the rise and fall transitions are measured at  $V_{IL}$  MAX and  $V_{IH}$  MIN.

**Figure 7-46 UXCLK Timing**



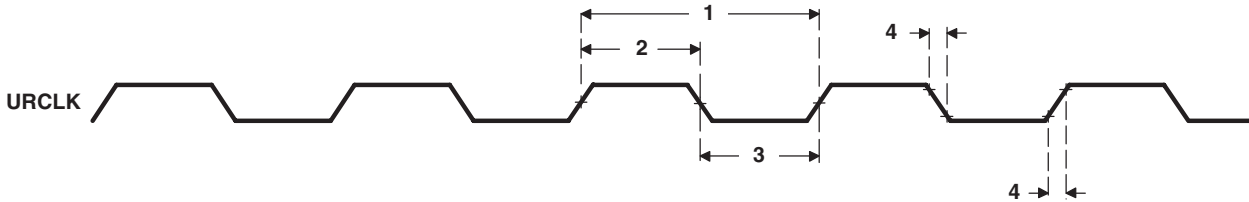
**Table 7-106 URCLK Timing Requirements** <sup>(1)</sup>  
(see Figure 7-47)

| No. |                                           | Min              | Max              | Unit |
|-----|-------------------------------------------|------------------|------------------|------|
| 1   | $t_{c(URCK)}$ Cycle time, URCLK           | 20               |                  | ns   |
| 2   | $t_{w(URCKH)}$ Pulse duration, URCLK high | $0.4t_{c(URCK)}$ | $0.6t_{c(URCK)}$ | ns   |
| 3   | $t_{w(URCKL)}$ Pulse duration, URCLK low  | $0.4t_{c(URCK)}$ | $0.6t_{c(URCK)}$ | ns   |
| 4   | $t_{t(URCK)}$ Transition time, URCLK      |                  | 2                | ns   |

**End of Table 7-106**

<sup>1</sup> The reference points for the rise and fall transitions are measured at  $V_{IL}$  MAX and  $V_{IH}$  MIN.

**Figure 7-47 URCLK Timing**



**Table 7-107 UTOPIA Slave Transmit Timing Requirements**  
(see Figure 7-48)

| No. |                                                                           | Min | Max | Unit |
|-----|---------------------------------------------------------------------------|-----|-----|------|
| 2   | $t_{su(UXAV-UXCH)}$ Setup time, UXADDR valid before UXCLK high            | 4   |     | ns   |
| 3   | $t_{h(UXCH-UXAV)}$ Hold time, UXADDR valid after UXCLK high               | 1   |     | ns   |
| 8   | $t_{su(UXENB-UXCH)}$ Setup time, $\overline{UXENB}$ low before UXCLK high | 4   |     | ns   |
| 9   | $t_{h(UXCH-UXENB)}$ Hold time, $\overline{UXENB}$ low after UXCLK high    | 1   |     | ns   |

**End of Table 7-107**

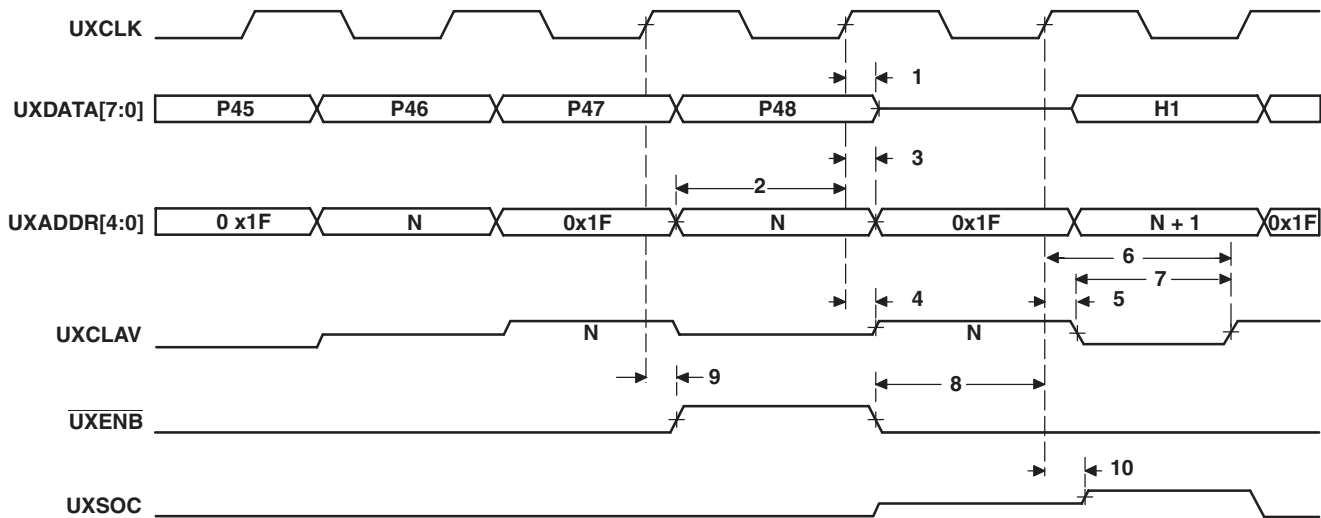
**Table 7-108 UTOPIA Slave Transmit Cycles Switching Characteristics** <sup>(1)</sup>  
(see Figure 7-48)

| No. | Parameter                                                                  | Min | Max  | Unit |
|-----|----------------------------------------------------------------------------|-----|------|------|
| 1   | $t_{d(UXCH-UXDV)}$ Delay time, UXCLK high to UXDATA valid                  | 2   | 12   | ns   |
| 4   | $t_{d(UXCH-UXCLAV)}$ Delay time, UXCLK high to UXCLAV driven active value  | 2   | 12   | ns   |
| 5   | $t_{d(UXCH-UXCLAVL)}$ Delay time, UXCLK high to UXCLAV driven inactive low | 2   | 12   | ns   |
| 6   | $t_{d(UXCH-UXCLAVHZ)}$ Delay time, UXCLK high to UXCLAV going Hi-Z         | 9   | 18.5 | ns   |
| 7   | $t_{w(UXCLAVL-UXCLAVHZ)}$ Pulse duration (low), UXCLAV low to UXCLAV Hi-Z  | 2   |      | ns   |
| 10  | $t_{d(UXCH-UXSV)}$ Delay time, UXCLK high to UXSOC valid                   | 2   | 12   | ns   |

**End of Table 7-108**

<sup>1</sup> Over recommended operating conditions.

**Figure 7-48 UTOPIA Slave Transmit Timing**<sup>(A)</sup>



(A) The UTOPIA slave module has signals that are middle-level signals indicating a high-impedance state (i.e., the UXCLAV and UXSOC signals).

**Table 7-109 UTOPIA Slave Receive Timing Requirements**

(see Figure 7-49)

| No. |                                                                             | Min | Max | Unit |
|-----|-----------------------------------------------------------------------------|-----|-----|------|
| 1   | $t_{su}(URDV-URCH)$ Setup time, URDATA valid before URCLK high              | 4   |     | ns   |
| 2   | $t_h(URCH-URDV)$ Hold time, URDATA valid after URCLK high                   | 1   |     | ns   |
| 3   | $t_{su}(URAV-URCH)$ Setup time, URADDR valid before URCLK high              | 4   |     | ns   |
| 4   | $t_h(URCH-URAV)$ Hold time, URADDR valid after URCLK high                   | 1   |     | ns   |
| 9   | $t_{su}(URENBL-URCH)$ Setup time, $\overline{URENBL}$ low before URCLK high | 4   |     | ns   |
| 10  | $t_h(URCH-URENBL)$ Hold time, $\overline{URENBL}$ low after URCLK high      | 1   |     | ns   |
| 11  | $t_{su}(URSH-URCH)$ Setup time, URSOC high before URCLK high                | 4   |     | ns   |
| 12  | $t_h(URCH-URSH)$ Hold time, URSOC high after URCLK high                     | 1   |     | ns   |

**End of Table 7-109**

**Table 7-110 Switching Characteristics for UTOPIA Slave Receive Cycles**<sup>(1)</sup>

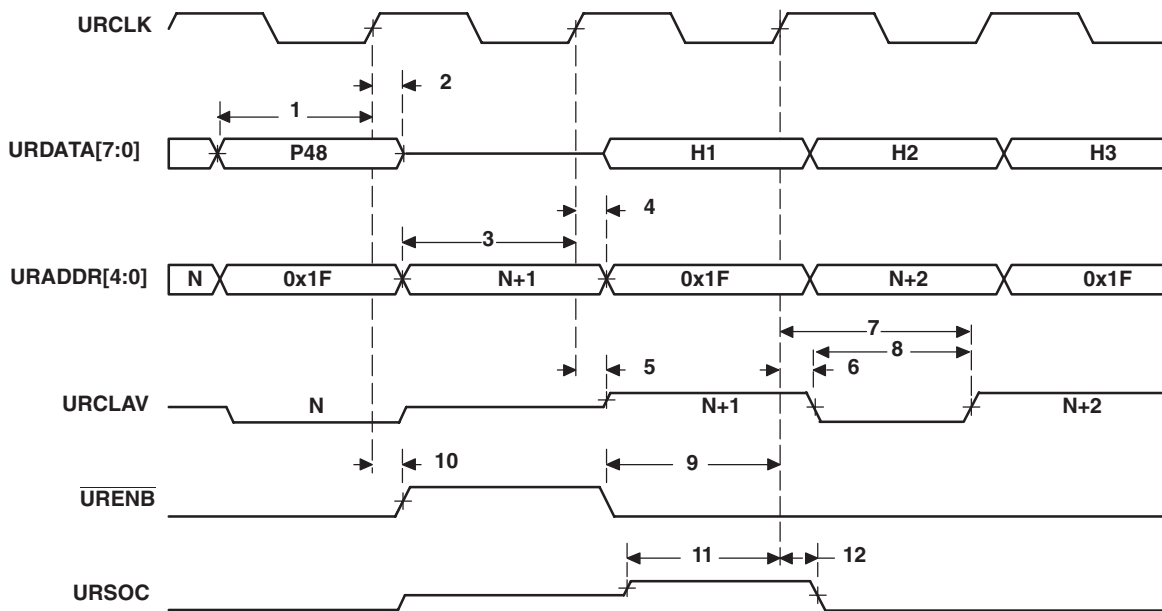
(see Figure 7-49)

| No. | Parameter                                                                | Min | Max  | Unit |
|-----|--------------------------------------------------------------------------|-----|------|------|
| 5   | $t_d(URCH-URCLAV)$ Delay time, URCLK high to URCLAV driven active value  | 3   | 12   | ns   |
| 6   | $t_d(URCH-URCLAVL)$ Delay time, URCLK high to URCLAV driven inactive low | 3   | 12   | ns   |
| 7   | $t_d(URCH-URCLAVHZ)$ Delay time, URCLK high to URCLAV going Hi-Z         | 9   | 18.5 | ns   |
| 8   | $t_w(URCLAVL-URCLAVHZ)$ Pulse duration (low), URCLAV low to URCLAV Hi-Z  | 3   |      | ns   |

**End of Table 7-110**

<sup>1</sup> Over recommended operating conditions.

**Figure 7-49 UTOPIA Slave Receive Timing<sup>(A)</sup>**



(A) The UTOPIA slave module has signals that are middle-level signals indicating a high-impedance state (i.e., the URCLAV and URSOC signals).

## 7.20 Serial RapidIO (SRIO) Port

The SRIO port on the TMS320C6457 device is a high-performance, low pin-count interconnect aimed for embedded markets. The use of the RapidIO interconnect in a baseband board design can create a homogeneous interconnect environment, providing even more connectivity and control among the components. RapidIO is based on the memory and device addressing concepts of processor buses where the transaction processing is managed completely by hardware. This enables the RapidIO interconnect to lower the system cost by providing lower latency, reduced overhead of packet data processing, and higher system bandwidth, all of which are key for wireless interfaces. The RapidIO interconnect offers very low pin-count interfaces with scalable system bandwidth based on 10-Gigabit per second (Gbps) bidirectional links.

The PHY part of the RIO consists of the physical layer and includes the input and output buffers (each serial link consists of a differential pair), the 8-bit/10-bit encoder/decoder, the PLL clock recovery, and the parallel-to-serial/serial-to-parallel converters.

The C6457 device supports four 1× or one 4× Serial RapidIO links. The RapidIO interface should be designed to operate at a data rate of 3.125 Gbps per differential pair. This equals 12.5 raw Gbaud/s for the 4× RapidIO port, or approximately 9 Gbps data throughput rate.

### 7.20.1 Serial RapidIO Device-Specific Information

The approach to specifying interface timing for the SRIO Port is different than on other interfaces such as EMIFA, HPI, and McBSP. For these other interfaces, the device timing was specified in terms of data manual specifications and I/O buffer information specification (IBIS) models.



For the C6457 SRIO Port, Texas Instruments (TI) provides a printed circuit board (PCB) solution showing two DSPs connected via a 4× SRIO link directly to the user. TI has performed the simulation and system characterization to ensure all SRIO interface timings in this solution are met. The complete SRIO system solution is documented in the *TMS320TCI6484 and TMS320C6457 SerDes Implementation Guidelines* application report (literature number [SPRAAY1](#)).



**Note**—TI supports *only* designs that follow the board design guidelines outlined in the application report.

The Serial RapidIO peripheral is a master peripheral in the C6457 DSP. It conforms to the *RapidIO™ Interconnect Specification, Part VI: Physical Layer 1×/4× LP-Serial Specification*, Revision 1.3.

## 7.20.2 Serial RapidIO Peripheral Register Description(s)

**Table 7-111 RapidIO Control Registers (Part 1 of 12)**

| Hex Address Range     | Acronym           | Register Name                                      |
|-----------------------|-------------------|----------------------------------------------------|
| 02D0 0000             | RIO_PID           | Peripheral Identification Register                 |
| 02D0 0004             | RIO_PCR           | Peripheral Control Register                        |
| 02D0 0008 - 02D0 001C | -                 | Reserved                                           |
| 02D0 0020             | RIO_PER_SET_CNTL0 | Peripheral Settings Control Register 0             |
| 02D0 0024             | RIO_PER_SET_CNTL1 | Peripheral Settings Control Register 1             |
| 02D0 0028 - 02D0 002C | -                 | Reserved                                           |
| 02D0 0030             | RIO_GBL_EN        | Peripheral Global Enable Register                  |
| 02D0 0034             | RIO_GBL_EN_STAT   | Peripheral Global Enable Status                    |
| 02D0 0038             | RIO_BLK0_EN       | Block Enable 0                                     |
| 02D0 003C             | RIO_BLK0_EN_STAT  | Block Enable Status 0                              |
| 02D0 0040             | RIO_BLK1_EN       | Block Enable 1                                     |
| 02D0 0044             | RIO_BLK1_EN_STAT  | Block Enable Status 1                              |
| 02D0 0048             | BLK2_EN           | Block Enable 2                                     |
| 02D0 004C             | BLK2_EN_STAT      | Block Enable Status 2                              |
| 02D0 0050             | BLK3_EN           | Block Enable 3                                     |
| 02D0 0054             | BLK3_EN_STAT      | Block Enable Status 3                              |
| 02D0 0058             | BLK4_EN           | Block Enable 4                                     |
| 02D0 005C             | BLK4_EN_STAT      | Block Enable Status 4                              |
| 02D0 0060             | BLK5_EN           | Block Enable 5                                     |
| 02D0 0064             | BLK5_EN_STAT      | Block Enable Status 5                              |
| 02D0 0068             | BLK6_EN           | Block Enable 6                                     |
| 02D0 006C             | BLK6_EN_STAT      | Block Enable Status 6                              |
| 02D0 0070             | BLK7_EN           | Block Enable 7                                     |
| 02D0 0074             | BLK7_EN_STAT      | Block Enable Status 7                              |
| 02D0 0078             | BLK8_EN           | Block Enable 8                                     |
| 02D0 007C             | BLK8_EN_STAT      | Block Enable Status 8                              |
| 02D0 0080             | DEVICEID_REG1     | RapidIO DEVICEID1 Register                         |
| 02D0 0084             | DEVICEID_REG2     | RapidIO DEVICEID2 Register                         |
| 02D0 0088             | DEVICEID_REG3     | RapidIO DEVICEID3 Register                         |
| 02D0 008C             | DEVICEID_REG4     | RapidIO DEVICEID4 Register                         |
| 02D0 0090             | PF_16B_CNTL0      | Packet Forwarding Register 0 for 16-bit Device IDs |
| 02D0 0094             | PF_8B_CNTL0       | Packet Forwarding Register 0 for 8-bit Device IDs  |

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**Table 7-111 RapidIO Control Registers (Part 2 of 12)**

| Hex Address Range     | Acronym            | Register Name                                      |
|-----------------------|--------------------|----------------------------------------------------|
| 02D0 0098             | PF_16B_CNTL1       | Packet Forwarding Register 1 for 16-bit Device IDs |
| 02D0 009C             | PF_8B_CNTL1        | Packet Forwarding Register 1 for 8-bit Device IDs  |
| 02D0 00A0             | PF_16B_CNTL2       | Packet Forwarding Register 2 for 16-bit Device IDs |
| 02D0 00A4             | PF_8B_CNTL2        | Packet Forwarding Register 2 for 8-bit Device IDs  |
| 02D0 00A8             | PF_16B_CNTL3       | Packet Forwarding Register 3 for 16-bit Device IDs |
| 02D0 00AC             | PF_8B_CNTL3        | Packet Forwarding Register 3 for 8-bit Device IDs  |
| 02D0 00B0 - 02D0 00FC | -                  | Reserved                                           |
| 02D0 0100             | SERDES_CFGRX0_CNTL | SerDes Receive Channel Configuration Register 0    |
| 02D0 0104             | SERDES_CFGRX1_CNTL | SerDes Receive Channel Configuration Register 1    |
| 02D0 0108             | SERDES_CFGRX2_CNTL | SerDes Receive Channel Configuration Register 2    |
| 02D0 010C             | SERDES_CFGRX3_CNTL | SerDes Receive Channel Configuration Register 3    |
| 02D0 0110             | SERDES_CFGTX0_CNTL | SerDes Transmit Channel Configuration Register 0   |
| 02D0 0114             | SERDES_CFGTX1_CNTL | SerDes Transmit Channel Configuration Register 1   |
| 02D0 0118             | SERDES_CFGTX2_CNTL | SerDes Transmit Channel Configuration Register 2   |
| 02D0 011C             | SERDES_CFGTX3_CNTL | SerDes Transmit Channel Configuration Register 3   |
| 02D0 0120             | SERDES_CFG0_CNTL   | SerDes Macro Configuration Register 0              |
| 02D0 0124             | SERDES_CFG1_CNTL   | SerDes Macro Configuration Register 1              |
| 02D0 0128             | SERDES_CFG2_CNTL   | SerDes Macro Configuration Register 2              |
| 02D0 012C             | SERDES_CFG3_CNTL   | SerDes Macro Configuration Register 3              |
| 02D0 0130 - 02D0 01FC | -                  | Reserved                                           |
| 02D0 0200             | DOORBELL0_ICSR     | DOORBELL Interrupt Condition Status Register 0     |
| 02D0 0204             | -                  | Reserved                                           |
| 02D0 0208             | DOORBELL0_ICCR     | DOORBELL Interrupt Condition Clear Register 0      |
| 02D0 020C             | -                  | Reserved                                           |
| 02D0 0210             | DOORBELL1_ICSR     | DOORBELL Interrupt Condition Status Register 1     |
| 02D0 0214             | -                  | Reserved                                           |
| 02D0 0218             | DOORBELL1_ICCR     | DOORBELL Interrupt Condition Clear Register 1      |
| 02D0 021C             | -                  | Reserved                                           |
| 02D0 0220             | DOORBELL2_ICSR     | DOORBELL Interrupt Condition Status Register 2     |
| 02D0 0224             | -                  | Reserved                                           |
| 02D0 0228             | DOORBELL2_ICCR     | DOORBELL Interrupt Condition Clear Register 2      |
| 02D0 022C             | -                  | Reserved                                           |
| 02D0 0230             | DOORBELL3_ICSR     | DOORBELL Interrupt Condition Status Register 3     |
| 02D0 0234             | -                  | Reserved                                           |
| 02D0 0238             | DOORBELL3_ICCR     | DOORBELL Interrupt Condition Clear Register 3      |
| 02D0 023C             | -                  | Reserved                                           |
| 02D0 0240             | RX_CPPI_ICSR       | RX CPPI Interrupt Condition Status Register        |
| 02D0 0244             | -                  | Reserved                                           |
| 02D0 0248             | RX_CPPI_ICCR       | RX CPPI Interrupt Condition Clear Register         |
| 02D0 024c             | -                  | Reserved                                           |
| 02D0 0250             | TX_CPPI_ICSR       | TX CPPI Interrupt Condition Status Register        |
| 02D0 0254             | -                  | Reserved                                           |
| 02D0 0258             | TX_CPPI_ICCR       | TX CPPI Interrupt Condition Clear Register         |
| 02D0 025C             | -                  | Reserved                                           |

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**Table 7-111 RapidIO Control Registers (Part 3 of 12)**

| Hex Address Range     | Acronym            | Register Name                                                          |
|-----------------------|--------------------|------------------------------------------------------------------------|
| 02D0 0260             | LSU_ICSR           | LSU Interrupt Condition Status Register                                |
| 02D0 0264             | -                  | Reserved                                                               |
| 02D0 0268             | LSU_ICCR           | LSU Interrupt Condition Clear Register                                 |
| 02D0 026C             | -                  | Reserved                                                               |
| 02D0 0270             | ERR_RST_EVNT_ICSR  | Error, Reset, and Special Event Interrupt Condition Status Register    |
| 02D0 0274             | -                  | Reserved                                                               |
| 02D0 0278             | ERR_RST_EVNT_ICCR  | Error, Reset, and Special Event Interrupt Condition Clear Register     |
| 02D0 027C             | -                  | Reserved                                                               |
| 02D0 0280             | DOORBELL0_ICRR     | DOORBELL0 Interrupt Condition Routing Register                         |
| 02D0 0284             | DOORBELL0_ICRR2    | DOORBELL 0 Interrupt Condition Routing Register 2                      |
| 02D0 0288 - 02D0 028C | -                  | Reserved                                                               |
| 02D0 0290             | DOORBELL1_ICRR     | DOORBELL1 Interrupt Condition Routing Register                         |
| 02D0 0294             | DOORBELL1_ICRR2    | DOORBELL 1 Interrupt Condition Routing Register 2                      |
| 02D0 0298 - 02D0 029C | -                  | Reserved                                                               |
| 02D0 02A0             | DOORBELL2_ICRR     | DOORBELL2 Interrupt Condition Routing Register                         |
| 02D0 02A4             | DOORBELL2_ICRR2    | DOORBELL 2 Interrupt Condition Routing Register 2                      |
| 02D0 02A8 - 02D0 02AC | -                  | Reserved                                                               |
| 02D0 02B0             | DOORBELL3_ICRR     | DOORBELL3 Interrupt Condition Routing Register                         |
| 02D0 02B4             | DOORBELL3_ICRR2    | DOORBELL 3 Interrupt Condition Routing Register 2                      |
| 02D0 02B8 - 02D0 02BC | -                  | Reserved                                                               |
| 02D0 02C0             | RX_CPPI_ICRR       | Receive CPPI Interrupt Condition Routing Register                      |
| 02D0 02C4             | RX_CPPI_ICRR2      | Receive CPPI Interrupt Condition Routing Register 2                    |
| 02D0 02C8 - 02D0 02CC | -                  | Reserved                                                               |
| 02D0 02D0             | TX_CPPI_ICRR       | Transmit CPPI Interrupt Condition Routing Register                     |
| 02D0 02D4             | TX_CPPI_ICRR2      | Transmit CPPI Interrupt Condition Routing Register 2                   |
| 02D0 02D8 - 02D0 02DC | -                  | Reserved                                                               |
| 02D0 02E0             | LSU_ICRR0          | LSU Interrupt Condition Routing Register 0                             |
| 02D0 02E4             | LSU_ICRR1          | LSU Interrupt Condition Routing Register 1                             |
| 02D0 02E8             | LSU_ICRR2          | LSU Interrupt Condition Routing Register 2                             |
| 02D0 02EC             | LSU_ICRR3          | LSU Interrupt Condition Routing Register 3                             |
| 02D0 02F0             | ERR_RST_EVNT_ICRR  | Error, Reset, and Special Event Interrupt Condition Routing Register   |
| 02D0 02F4             | ERR_RST_EVNT_ICRR2 | Error, Reset, and Special Event Interrupt Condition Routing Register 2 |
| 02D0 02F8             | ERR_RST_EVNT_ICRR3 | Error, Reset, and Special Event Interrupt Condition Routing Register 3 |
| 02D0 02FC             | -                  | Reserved                                                               |
| 02D0 0300             | INTDST0_DECODE     | INTDST Interrupt Status Decode Register 0                              |
| 02D0 0304             | INTDST1_DECODE     | INTDST Interrupt Status Decode Register 1                              |
| 02D0 0308             | INTDST2_DECODE     | INTDST Interrupt Status Decode Register 2                              |
| 02D0 030C             | INTDST3_DECODE     | INTDST Interrupt Status Decode Register 3                              |
| 02D0 0310             | INTDST4_DECODE     | INTDST Interrupt Status Decode Register 4                              |
| 02D0 0314             | INTDST5_DECODE     | INTDST Interrupt Status Decode Register 5                              |
| 02D0 0318             | INTDST6_DECODE     | INTDST Interrupt Status Decode Register 6                              |
| 02D0 031C             | INTDST7_DECODE     | INTDST Interrupt Status Decode Register 7                              |
| 02D0 0320             | INTDST0_RATE_CNTL  | INTDST Interrupt Rate Control Register 0                               |
| 02D0 0324             | INTDST1_RATE_CNTL  | INTDST Interrupt Rate Control Register 1                               |

**Table 7-111 RapidIO Control Registers (Part 4 of 12)**

| Hex Address Range     | Acronym           | Register Name                                         |
|-----------------------|-------------------|-------------------------------------------------------|
| 02D0 0328             | INTDST2_RATE_CNTL | INTDST Interrupt Rate Control Register 2              |
| 02D0 032C             | INTDST3_RATE_CNTL | INTDST Interrupt Rate Control Register 3              |
| 02D0 0330             | INTDST4_RATE_CNTL | INTDST Interrupt Rate Control Register 4              |
| 02D0 0334             | INTDST5_RATE_CNTL | INTDST Interrupt Rate Control Register 5              |
| 02D0 0338             | INTDST6_RATE_CNTL | INTDST Interrupt Rate Control Register 6              |
| 02D0 033C             | INTDST7_RATE_CNTL | INTDST Interrupt Rate Control Register 7              |
| 02D0 0340 - 02D0 03FC | -                 | Reserved                                              |
| 02D0 0400             | LSU1_REG0         | LSU1 Control Register 0                               |
| 02D0 0404             | LSU1_REG1         | LSU1 Control Register 1                               |
| 02D0 0408             | LSU1_REG2         | LSU1 Control Register 2                               |
| 02D0 040C             | LSU1_REG3         | LSU1 Control Register 3                               |
| 02D0 0410             | LSU1_REG4         | LSU1 Control Register 4                               |
| 02D0 0414             | LSU1_REG5         | LSU1 Control Register 5                               |
| 02D0 0418             | LSU1_REG6         | LSU1 Control Register 6                               |
| 02D0 041C             | LSU1_FLOW_MASKS1  | LSU1 Congestion Control Flow Mask Register            |
| 02D0 0420             | LSU2_REG0         | LSU2 Control Register 0                               |
| 02D0 0424             | LSU2_REG1         | LSU2 Control Register 1                               |
| 02D0 0428             | LSU2_REG2         | LSU2 Control Register 2                               |
| 02D0 042C             | LSU2_REG3         | LSU2 Control Register 3                               |
| 02D0 0430             | LSU2_REG4         | LSU2 Control Register 4                               |
| 02D0 0434             | LSU2_REG5         | LSU2 Control Register 5                               |
| 02D0 0438             | LSU2_REG6         | LSU2 Control Register 6                               |
| 02D0 043C             | LSU2_FLOW_MASKS2  | LSU2 Congestion Control Flow Mask Register            |
| 02D0 0440             | LSU3_REG0         | LSU3 Control Register 0                               |
| 02D0 0444             | LSU3_REG1         | LSU3 Control Register 1                               |
| 02D0 0448             | LSU3_REG2         | LSU3 Control Register 2                               |
| 02D0 044C             | LSU3_REG3         | LSU3 Control Register 3                               |
| 02D0 0450             | LSU3_REG4         | LSU3 Control Register 4                               |
| 02D0 0454             | LSU3_REG5         | LSU3 Control Register 5                               |
| 02D0 0458             | LSU3_REG6         | LSU3 Control Register 6                               |
| 02D0 045C             | LSU3_FLOW_MASKS3  | LSU3 Congestion Control Flow Mask Register            |
| 02D0 0460             | LSU4_REG0         | LSU4 Control Register 0                               |
| 02D0 0464             | LSU4_REG1         | LSU4 Control Register 1                               |
| 02D0 0468             | LSU4_REG2         | LSU4 Control Register 2                               |
| 02D0 046C             | LSU4_REG3         | LSU4 Control Register 3                               |
| 02D0 0470             | LSU4_REG4         | LSU4 Control Register 4                               |
| 02D0 0474             | LSU4_REG5         | LSU4 Control Register 5                               |
| 02D0 0478             | LSU4_REG6         | LSU4 Control Register 6                               |
| 02D0 047C             | LSU4_FLOW_MASKS4  | LSU4 Congestion Control Flow Mask Register            |
| 02D0 0480 - 02D0 04FC | -                 | Reserved                                              |
| 02D0 0500             | QUEUE0_TXDMA_HDP  | Queue Transmit DMA Head Descriptor Pointer Register 0 |
| 02D0 0504             | QUEUE1_TXDMA_HDP  | Queue Transmit DMA Head Descriptor Pointer Register 1 |
| 02D0 0508             | QUEUE2_TXDMA_HDP  | Queue Transmit DMA Head Descriptor Pointer Register 2 |
| 02D0 050C             | QUEUE3_TXDMA_HDP  | Queue Transmit DMA Head Descriptor Pointer Register 3 |

**Table 7-111 RapidIO Control Registers (Part 5 of 12)**

| Hex Address Range     | Acronym           | Register Name                                          |
|-----------------------|-------------------|--------------------------------------------------------|
| 02D0 0510             | QUEUE4_TXDMA_HDP  | Queue Transmit DMA Head Descriptor Pointer Register 4  |
| 02D0 0514             | QUEUE5_TXDMA_HDP  | Queue Transmit DMA Head Descriptor Pointer Register 5  |
| 02D0 0518             | QUEUE6_TXDMA_HDP  | Queue Transmit DMA Head Descriptor Pointer Register 6  |
| 02D0 051C             | QUEUE7_TXDMA_HDP  | Queue Transmit DMA Head Descriptor Pointer Register 7  |
| 02D0 0520             | QUEUE8_TXDMA_HDP  | Queue Transmit DMA Head Descriptor Pointer Register 8  |
| 02D0 0524             | QUEUE9_TXDMA_HDP  | Queue Transmit DMA Head Descriptor Pointer Register 9  |
| 02D0 0528             | QUEUE10_TXDMA_HDP | Queue Transmit DMA Head Descriptor Pointer Register 10 |
| 02D0 052C             | QUEUE11_TXDMA_HDP | Queue Transmit DMA Head Descriptor Pointer Register 11 |
| 02D0 0530             | QUEUE12_TXDMA_HDP | Queue Transmit DMA Head Descriptor Pointer Register 12 |
| 02D0 0534             | QUEUE13_TXDMA_HDP | Queue Transmit DMA Head Descriptor Pointer Register 13 |
| 02D0 0538             | QUEUE14_TXDMA_HDP | Queue Transmit DMA Head Descriptor Pointer Register 14 |
| 02D0 053C             | QUEUE15_TXDMA_HDP | Queue Transmit DMA Head Descriptor Pointer Register 15 |
| 02D0 0540 - 02D0 057C | -                 | Reserved                                               |
| 02D0 0580             | QUEUE0_TXDMA_CP   | Queue Transmit DMA Completion Pointer Register 0       |
| 02D0 0584             | QUEUE1_TXDMA_CP   | Queue Transmit DMA Completion Pointer Register 1       |
| 02D0 0588             | QUEUE2_TXDMA_CP   | Queue Transmit DMA Completion Pointer Register 2       |
| 02D0 058C             | QUEUE3_TXDMA_CP   | Queue Transmit DMA Completion Pointer Register 3       |
| 02D0 0590             | QUEUE4_TXDMA_CP   | Queue Transmit DMA Completion Pointer Register 4       |
| 02D0 0594             | QUEUE5_TXDMA_CP   | Queue Transmit DMA Completion Pointer Register 5       |
| 02D0 0598             | QUEUE6_TXDMA_CP   | Queue Transmit DMA Completion Pointer Register 6       |
| 02D0 059C             | QUEUE7_TXDMA_CP   | Queue Transmit DMA Completion Pointer Register 7       |
| 02D0 05A0             | QUEUE8_TXDMA_CP   | Queue Transmit DMA Completion Pointer Register 8       |
| 02D0 05A4             | QUEUE9_TXDMA_CP   | Queue Transmit DMA Completion Pointer Register 9       |
| 02D0 05A8             | QUEUE10_TXDMA_CP  | Queue Transmit DMA Completion Pointer Register 10      |
| 02D0 05AC             | QUEUE11_TXDMA_CP  | Queue Transmit DMA Completion Pointer Register 11      |
| 02D0 05B0             | QUEUE12_TXDMA_CP  | Queue Transmit DMA Completion Pointer Register 12      |
| 02D0 05B4             | QUEUE13_TXDMA_CP  | Queue Transmit DMA Completion Pointer Register 13      |
| 02D0 05B8             | QUEUE14_TXDMA_CP  | Queue Transmit DMA Completion Pointer Register 14      |
| 02D0 05BC             | QUEUE15_TXDMA_CP  | Queue Transmit DMA Completion Pointer Register 15      |
| 02D0 05D0 - 02D0 05FC | -                 | Reserved                                               |
| 02D0 0600             | QUEUE0_RXDMA_HDP  | Queue Receive DMA Head Descriptor Pointer Register 0   |
| 02D0 0604             | QUEUE1_RXDMA_HDP  | Queue Receive DMA Head Descriptor Pointer Register 1   |
| 02D0 0608             | QUEUE2_RXDMA_HDP  | Queue Receive DMA Head Descriptor Pointer Register 2   |
| 02D0 060C             | QUEUE3_RXDMA_HDP  | Queue Receive DMA Head Descriptor Pointer Register 3   |
| 02D0 0610             | QUEUE4_RXDMA_HDP  | Queue Receive DMA Head Descriptor Pointer Register 4   |
| 02D0 0614             | QUEUE5_RXDMA_HDP  | Queue Receive DMA Head Descriptor Pointer Register 5   |
| 02D0 0618             | QUEUE6_RXDMA_HDP  | Queue Receive DMA Head Descriptor Pointer Register 6   |
| 02D0 061C             | QUEUE7_RXDMA_HDP  | Queue Receive DMA Head Descriptor Pointer Register 7   |
| 02D0 0620             | QUEUE8_RXDMA_HDP  | Queue Receive DMA Head Descriptor Pointer Register 8   |
| 02D0 0624             | QUEUE9_RXDMA_HDP  | Queue Receive DMA Head Descriptor Pointer Register 9   |
| 02D0 0628             | QUEUE10_RXDMA_HDP | Queue Receive DMA Head Descriptor Pointer Register 10  |
| 02D0 062C             | QUEUE11_RXDMA_HDP | Queue Receive DMA Head Descriptor Pointer Register 11  |
| 02D0 0630             | QUEUE12_RXDMA_HDP | Queue Receive DMA Head Descriptor Pointer Register 12  |
| 02D0 0634             | QUEUE13_RXDMA_HDP | Queue Receive DMA Head Descriptor Pointer Register 13  |

**Table 7-111 RapidIO Control Registers (Part 6 of 12)**

| Hex Address Range      | Acronym             | Register Name                                         |
|------------------------|---------------------|-------------------------------------------------------|
| 02D0 0638              | QUEUE14_RXDMA_HDP   | Queue Receive DMA Head Descriptor Pointer Register 14 |
| 02D0 063C              | QUEUE15_RXDMA_HDP   | Queue Receive DMA Head Descriptor Pointer Register 15 |
| 02D0 0640 - 02D0 067C  | -                   | Reserved                                              |
| 02D0 0680              | QUEUE0_RXDMA_CP     | Queue Receive DMA Completion Pointer Register 0       |
| 02D0 0684              | QUEUE1_RXDMA_CP     | Queue Receive DMA Completion Pointer Register 1       |
| 02D0 0688              | QUEUE2_RXDMA_CP     | Queue Receive DMA Completion Pointer Register 2       |
| 02D0 068C              | QUEUE3_RXDMA_CP     | Queue Receive DMA Completion Pointer Register 3       |
| 02D0 0690              | QUEUE4_RXDMA_CP     | Queue Receive DMA Completion Pointer Register 4       |
| 02D0 0694              | QUEUE5_RXDMA_CP     | Queue Receive DMA Completion Pointer Register 5       |
| 02D0 0698              | QUEUE6_RXDMA_CP     | Queue Receive DMA Completion Pointer Register 6       |
| 02D0 069C              | QUEUE7_RXDMA_CP     | Queue Receive DMA Completion Pointer Register 7       |
| 02D0 06A0              | QUEUE8_RXDMA_CP     | Queue Receive DMA Completion Pointer Register 8       |
| 02D0 06A4              | QUEUE9_RXDMA_CP     | Queue Receive DMA Completion Pointer Register 9       |
| 02D0 06A8              | QUEUE10_RXDMA_CP    | Queue Receive DMA Completion Pointer Register 10      |
| 02D0 06AC              | QUEUE11_RXDMA_CP    | Queue Receive DMA Completion Pointer Register 11      |
| 02D0 06B0              | QUEUE12_RXDMA_CP    | Queue Receive DMA Completion Pointer Register 12      |
| 02D0 06B4              | QUEUE13_RXDMA_CP    | Queue Receive DMA Completion Pointer Register 13      |
| 02D0 06B8              | QUEUE14_RXDMA_CP    | Queue Receive DMA Completion Pointer Register 14      |
| 02D0 06BC              | QUEUE15_RXDMA_CP    | Queue Receive DMA Completion Pointer Register 15      |
| 02D0 06C0 - 02D0 006FC | -                   | Reserved                                              |
| 02D0 0700              | TX_QUEUE_TEAR_DOWN  | Transmit Queue Teardown Register                      |
| 02D0 0704              | TX_CPPI_FLOW_MASKS0 | Transmit CPPI Supported Flow Mask Register 0          |
| 02D0 0708              | TX_CPPI_FLOW_MASKS1 | Transmit CPPI Supported Flow Mask Register 1          |
| 02D0 070C              | TX_CPPI_FLOW_MASKS2 | Transmit CPPI Supported Flow Mask Register 2          |
| 02D0 0710              | TX_CPPI_FLOW_MASKS3 | Transmit CPPI Supported Flow Mask Register 3          |
| 02D0 0714              | TX_CPPI_FLOW_MASKS4 | Transmit CPPI Supported Flow Mask Register 4          |
| 02D0 0718              | TX_CPPI_FLOW_MASKS5 | Transmit CPPI Supported Flow Mask Register 5          |
| 02D0 071C              | TX_CPPI_FLOW_MASKS6 | Transmit CPPI Supported Flow Mask Register 6          |
| 02D0 0720              | TX_CPPI_FLOW_MASKS7 | Transmit CPPI Supported Flow Mask Register 7          |
| 02D0 0724 - 02D0 073C  | -                   | Reserved                                              |
| 02D0 0740              | RX_QUEUE_TEAR_DOWN  | Receive Queue Teardown Register                       |
| 02D0 0744              | RX_CPPI_CNTL        | Receive CPPI Control Register                         |
| 02D0 0748 - 02D0 07DC  | -                   | Reserved                                              |
| 02D0 07E0              | TX_QUEUE_CNTL0      | Transmit CPPI Weighted Round Robin Control Register 0 |
| 02D0 07E4              | TX_QUEUE_CNTL1      | Transmit CPPI Weighted Round Robin Control Register 1 |
| 02D0 07E8              | TX_QUEUE_CNTL2      | Transmit CPPI Weighted Round Robin Control Register 2 |
| 02D0 07EC              | TX_QUEUE_CNTL3      | Transmit CPPI Weighted Round Robin Control Register 3 |
| 02D0 07F0 - 02D0 07FC  | -                   | Reserved                                              |
| 02D0 0800              | RXU_MAP_L0          | Mailbox-to-Queue Mapping Register L0                  |
| 02D0 0804              | RXU_MAP_H0          | Mailbox-to-Queue Mapping Register H0                  |
| 02D0 0808              | RXU_MAP_L1          | Mailbox-to-Queue Mapping Register L1                  |
| 02D0 080C              | RXU_MAP_H1          | Mailbox-to-Queue Mapping Register H1                  |
| 02D0 0810              | RXU_MAP_L2          | Mailbox-to-Queue Mapping Register L2                  |
| 02D0 0814              | RXU_MAP_H2          | Mailbox-to-Queue Mapping Register H2                  |

**Table 7-111 RapidIO Control Registers (Part 7 of 12)**

| Hex Address Range | Acronym     | Register Name                         |
|-------------------|-------------|---------------------------------------|
| 02D0 0818         | RXU_MAP_L3  | Mailbox-to-Queue Mapping Register L3  |
| 02D0 081C         | RXU_MAP_H3  | Mailbox-to-Queue Mapping Register H3  |
| 02D0 0820         | RXU_MAP_L4  | Mailbox-to-Queue Mapping Register L4  |
| 02D0 0824         | RXU_MAP_H4  | Mailbox-to-Queue Mapping Register H4  |
| 02D0 0828         | RXU_MAP_L5  | Mailbox-to-Queue Mapping Register L5  |
| 02D0 082C         | RXU_MAP_H5  | Mailbox-to-Queue Mapping Register H5  |
| 02D0 0830         | RXU_MAP_L6  | Mailbox-to-Queue Mapping Register L6  |
| 02D0 0834         | RXU_MAP_H6  | Mailbox-to-Queue Mapping Register H6  |
| 02D0 0838         | RXU_MAP_L7  | Mailbox-to-Queue Mapping Register L7  |
| 02D0 083C         | RXU_MAP_H7  | Mailbox-to-Queue Mapping Register H7  |
| 02D0 0840         | RXU_MAP_L8  | Mailbox-to-Queue Mapping Register L8  |
| 02D0 0844         | RXU_MAP_H8  | Mailbox-to-Queue Mapping Register H8  |
| 02D0 0848         | RXU_MAP_L9  | Mailbox-to-Queue Mapping Register L9  |
| 02D0 084C         | RXU_MAP_H9  | Mailbox-to-Queue Mapping Register H9  |
| 02D0 0850         | RXU_MAP_L10 | Mailbox-to-Queue Mapping Register L10 |
| 02D0 0854         | RXU_MAP_H10 | Mailbox-to-Queue Mapping Register H10 |
| 02D0 0858         | RXU_MAP_L11 | Mailbox-to-Queue Mapping Register L11 |
| 02D0 085C         | RXU_MAP_H11 | Mailbox-to-Queue Mapping Register H11 |
| 02D0 0860         | RXU_MAP_L12 | Mailbox-to-Queue Mapping Register L12 |
| 02D0 0864         | RXU_MAP_H12 | Mailbox-to-Queue Mapping Register H12 |
| 02D0 0868         | RXU_MAP_L13 | Mailbox-to-Queue Mapping Register L13 |
| 02D0 086C         | RXU_MAP_H13 | Mailbox-to-Queue Mapping Register H13 |
| 02D0 0870         | RXU_MAP_L14 | Mailbox-to-Queue Mapping Register L14 |
| 02D0 0874         | RXU_MAP_H14 | Mailbox-to-Queue Mapping Register H14 |
| 02D0 0878         | RXU_MAP_L15 | Mailbox-to-Queue Mapping Register L15 |
| 02D0 087C         | RXU_MAP_H15 | Mailbox-to-Queue Mapping Register H15 |
| 02D0 0880         | RXU_MAP_L16 | Mailbox-to-Queue Mapping Register L16 |
| 02D0 0884         | RXU_MAP_H16 | Mailbox-to-Queue Mapping Register H16 |
| 02D0 0888         | RXU_MAP_L17 | Mailbox-to-Queue Mapping Register L17 |
| 02D0 088C         | RXU_MAP_H17 | Mailbox-to-Queue Mapping Register H17 |
| 02D0 0890         | RXU_MAP_L18 | Mailbox-to-Queue Mapping Register L18 |
| 02D0 0894         | RXU_MAP_H18 | Mailbox-to-Queue Mapping Register H18 |
| 02D0 0898         | RXU_MAP_L19 | Mailbox-to-Queue Mapping Register L19 |
| 02D0 089C         | RXU_MAP_H19 | Mailbox-to-Queue Mapping Register H19 |
| 02D0 08A0         | RXU_MAP_L20 | Mailbox-to-Queue Mapping Register L20 |
| 02D0 08A4         | RXU_MAP_H20 | Mailbox-to-Queue Mapping Register H20 |
| 02D0 08A8         | RXU_MAP_L21 | Mailbox-to-Queue Mapping Register L21 |
| 02D0 08AC         | RXU_MAP_H21 | Mailbox-to-Queue Mapping Register H21 |
| 02D0 08B0         | RXU_MAP_L22 | Mailbox-to-Queue Mapping Register L22 |
| 02D0 08B4         | RXU_MAP_H22 | Mailbox-to-Queue Mapping Register H22 |
| 02D0 08B8         | RXU_MAP_L23 | Mailbox-to-Queue Mapping Register L23 |
| 02D0 08BC         | RXU_MAP_H23 | Mailbox-to-Queue Mapping Register H23 |
| 02D0 08C0         | RXU_MAP_L24 | Mailbox-to-Queue Mapping Register L24 |
| 02D0 08C4         | RXU_MAP_H24 | Mailbox-to-Queue Mapping Register H24 |



**Table 7-111 RapidIO Control Registers (Part 8 of 12)**

| Hex Address Range                            | Acronym      | Register Name                                |
|----------------------------------------------|--------------|----------------------------------------------|
| 02D0 08C8                                    | RXU_MAP_L25  | Mailbox-to-Queue Mapping Register L25        |
| 02D0 08CC                                    | RXU_MAP_H25  | Mailbox-to-Queue Mapping Register H25        |
| 02D0 08D0                                    | RXU_MAP_L26  | Mailbox-to-Queue Mapping Register L26        |
| 02D0 08D4                                    | RXU_MAP_H26  | Mailbox-to-Queue Mapping Register H26        |
| 02D0 08D8                                    | RXU_MAP_L27  | Mailbox-to-Queue Mapping Register L27        |
| 02D0 08DC                                    | RXU_MAP_H27  | Mailbox-to-Queue Mapping Register H27        |
| 02D0 08E0                                    | RXU_MAP_L28  | Mailbox-to-Queue Mapping Register L28        |
| 02D0 08E4                                    | RXU_MAP_H28  | Mailbox-to-Queue Mapping Register H28        |
| 02D0 08E8                                    | RXU_MAP_L29  | Mailbox-to-Queue Mapping Register L29        |
| 02D0 08EC                                    | RXU_MAP_H29  | Mailbox-to-Queue Mapping Register H29        |
| 02D0 08F0                                    | RXU_MAP_L30  | Mailbox-to-Queue Mapping Register L30        |
| 02D0 08F4                                    | RXU_MAP_H30  | Mailbox-to-Queue Mapping Register H30        |
| 02D0 08F8                                    | RXU_MAP_L31  | Mailbox-to-Queue Mapping Register L31        |
| 02D0 08FC                                    | RXU_MAP_H31  | Mailbox-to-Queue Mapping Register H31        |
| 02D0 0900                                    | FLOW_CNTL0   | Flow Control Table Entry Register 0          |
| 02D0 0904                                    | FLOW_CNTL1   | Flow Control Table Entry Register 1          |
| 02D0 0908                                    | FLOW_CNTL2   | Flow Control Table Entry Register 2          |
| 02D0 090C                                    | FLOW_CNTL3   | Flow Control Table Entry Register 3          |
| 02D0 0910                                    | FLOW_CNTL4   | Flow Control Table Entry Register 4          |
| 02D0 0914                                    | FLOW_CNTL5   | Flow Control Table Entry Register 5          |
| 02D0 0918                                    | FLOW_CNTL6   | Flow Control Table Entry Register 6          |
| 02D0 091C                                    | FLOW_CNTL7   | Flow Control Table Entry Register 7          |
| 02D0 0920                                    | FLOW_CNTL8   | Flow Control Table Entry Register 8          |
| 02D0 0924                                    | FLOW_CNTL9   | Flow Control Table Entry Register 9          |
| 02D0 0928                                    | FLOW_CNTL10  | Flow Control Table Entry Register 10         |
| 02D0 092C                                    | FLOW_CNTL11  | Flow Control Table Entry Register 11         |
| 02D0 0930                                    | FLOW_CNTL12  | Flow Control Table Entry Register 12         |
| 02D0 0934                                    | FLOW_CNTL13  | Flow Control Table Entry Register 13         |
| 02D0 0938                                    | FLOW_CNTL14  | Flow Control Table Entry Register 14         |
| 02D0 093C                                    | FLOW_CNTL15  | Flow Control Table Entry Register 15         |
| 02D0 0940 - 02D0 09FC                        | -            | Reserved                                     |
| <b>RapidIO Peripheral-Specific Registers</b> |              |                                              |
| 02D0 1000                                    | DEV_ID       | Device Identity CAR                          |
| 02D0 1004                                    | DEV_INFO     | Device Information CAR                       |
| 02D0 1008                                    | ASBLY_ID     | Assembly Identity CAR                        |
| 02D0 100C                                    | ASBLY_INFO   | Assembly Information CAR                     |
| 02D0 1010                                    | PE_FEAT      | Processing Element Features CAR              |
| 02D0 1014                                    | -            | Reserved                                     |
| 02D0 1018                                    | SRC_OP       | Source Operations CAR                        |
| 02D0 101C                                    | DEST_OP      | Destination Operations CAR                   |
| 02D0 1020 - 02D0 1048                        | -            | Reserved                                     |
| 02D0 104C                                    | PE_LL_CTL    | Processing Element Logical Layer Control CSR |
| 02D0 1050 - 02D0 1054                        | -            | Reserved                                     |
| 02D0 1058                                    | LCL_CFG_HBAR | Local Configuration Space Base Address 0 CSR |



**Table 7-111 RapidIO Control Registers (Part 9 of 12)**

| Hex Address Range                                           | Acronym           | Register Name                                    |
|-------------------------------------------------------------|-------------------|--------------------------------------------------|
| 02D0 105C                                                   | LCL_CFG_BAR       | Local Configuration Space Base Address 1 CSR     |
| 02D0 1060                                                   | BASE_ID           | Base Device ID CSR                               |
| 02D0 1064                                                   | -                 | Reserved                                         |
| 02D0 1068                                                   | HOST_BASE_ID_LOCK | Host Base Device ID Lock CSR                     |
| 02D0 106C                                                   | COMP_TAG          | Component Tag CSR                                |
| 02D0 1070 - 02D0 10FC                                       | -                 | Reserved                                         |
| <b>RapidIO Extended Features -LP Serial Registers</b>       |                   |                                                  |
| 02D0 1100                                                   | SP_MB_HEAD        | 1×/4× LP Serial Port Maintenance Block Header    |
| 02D0 1104 - 02D0 1118                                       | -                 | Reserved                                         |
| 02D0 1120                                                   | SP_LT_CTL         | Port Link Time-Out Control CSR                   |
| 02D0 1124                                                   | SP_RT_CTL         | Port Response Time-Out Control CSR               |
| 02D0 1128 - 02D0 1138                                       | -                 | Reserved                                         |
| 02D0 113C                                                   | SP_GEN_CTL        | Port General Control CSR                         |
| 02D0 1140                                                   | SP0_LM_REQ        | Port 0 Link Maintenance Request CSR              |
| 02D0 1144                                                   | SP0_LM_RESP       | Port 0 Link Maintenance Response CSR             |
| 02D0 1148                                                   | SP0_ACKID_STAT    | Port 0 Local Acknowledge ID Status CSR           |
| 02D0 114C - 02D0 1154                                       | -                 | Reserved                                         |
| 02D0 1158                                                   | SP0_ERR_STAT      | Port 0 Error and Status CSR                      |
| 02D0 115C                                                   | SP0_CTL           | Port 0 Control CSR                               |
| 02D0 1160                                                   | SP1_LM_REQ        | Port 1 Link Maintenance Request CSR              |
| 02D0 1164                                                   | SP1_LM_RESP       | Port 1 Link Maintenance Response CSR             |
| 02D0 1168                                                   | SP1_ACKID_STAT    | Port 1 Local Acknowledge ID Status CSR           |
| 02D0 116C - 02D0 1174                                       | -                 | Reserved                                         |
| 02D0 1178                                                   | SP1_ERR_STAT      | Port 1 Error and Status CSR                      |
| 02D0 117C                                                   | SP1_CTL           | Port 1 Control CSR                               |
| 02D0 1180                                                   | SP2_LM_REQ        | Port 2 Link Maintenance Request CSR              |
| 02D0 1184                                                   | SP2_LM_RESP       | Port 2 Link Maintenance Response CSR             |
| 02D0 1188                                                   | SP2_ACKID_STAT    | Port 2 Local Acknowledge ID Status CSR           |
| 02D0 118C - 02D0 1194                                       | -                 | Reserved                                         |
| 02D0 1198                                                   | SP2_ERR_STAT      | Port 2 Error and Status CSR                      |
| 02D0 119C                                                   | SP2_CTL           | Port 2 Control CSR                               |
| 02D0 11A0                                                   | SP3_LM_REQ        | Port 3 Link Maintenance Request CSR              |
| 02D0 11A4                                                   | SP3_LM_RESP       | Port 3 Link Maintenance Response CSR             |
| 02D0 11A8                                                   | SP3_ACKID_STAT    | Port 3 Local Acknowledge ID Status CSR           |
| 02D0 11AC - 02D0 11B4                                       | -                 | Reserved                                         |
| 02D0 11B8                                                   | SP3_ERR_STAT      | Port 3 Error and Status CSR                      |
| 02D0 11BC                                                   | SP3_CTL           | Port 3 Control CSR                               |
| 02D0 11C0 - 02D0 11FC                                       | -                 | Reserved                                         |
| <b>RapidIO Extended Feature -Error Management Registers</b> |                   |                                                  |
| 02D0 2000                                                   | ERR_RPT_BH        | Error Reporting Block Header                     |
| 02D0 2004                                                   | -                 | Reserved                                         |
| 02D0 2008                                                   | ERR_DET           | Logical/Transport Layer Error Detect CSR         |
| 02D0 200C                                                   | ERR_EN            | Logical/Transport Layer Error Enable CSR         |
| 02D0 2010                                                   | H_ADDR_CAPT       | Logical/Transport Layer High Address Capture CSR |

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**Table 7-111 RapidIO Control Registers (Part 10 of 12)**

| Hex Address Range     | Acronym                | Register Name                                    |
|-----------------------|------------------------|--------------------------------------------------|
| 02D0 2014             | ADDR_CAPT              | Logical/Transport Layer Address Capture CSR      |
| 02D0 2018             | ID_CAPT                | Logical/Transport Layer Device ID Capture CSR    |
| 02D0 201C             | CTRL_CAPT              | Logical/Transport Layer Control Capture CSR      |
| 02D0 2020 - 02D0 2024 | -                      | Reserved                                         |
| 02D0 2028             | PW_TGT_ID              | Port-Write Target Device ID CSR                  |
| 02D0 202C - 02D0 203C | -                      | Reserved                                         |
| 02D0 2040             | SP0_ERR_DET            | Port 0 Error Detect CSR                          |
| 02D0 2044             | SP0_RATE_EN            | Port 0 Error Enable CSR                          |
| 02D0 2048             | SP0_ERR_ATTR_CAPT_DBG0 | Port 0 Attributes Error Capture CSR 0            |
| 02D0 204C             | SP0_ERR_CAPT_DBG1      | Port 0 Packet/Control Symbol Error Capture CSR 1 |
| 02D0 2050             | SP0_ERR_CAPT_DBG2      | Port 0 Packet/Control Symbol Error Capture CSR 2 |
| 02D0 2054             | SP0_ERR_CAPT_DBG3      | Port 0 Packet/Control Symbol Error Capture CSR 3 |
| 02D0 2058             | SP0_ERR_CAPT_DBG4      | Port 0 Packet/Control Symbol Error Capture CSR 4 |
| 02D0 205C - 02D0 2064 | -                      | Reserved                                         |
| 02D0 2068             | SP0_ERR_RATE           | Port 0 Error Rate CSR 0                          |
| 02D0 206C             | SP0_ERR_THRESH         | Port 0 Error Rate Threshold CSR                  |
| 02D0 2070 - 02D0 207C | -                      | Reserved                                         |
| 02D0 2080             | SP1_ERR_DET            | Port 1 Error Detect CSR                          |
| 02D0 2084             | SP1_RATE_EN            | Port 1 Error Enable CSR                          |
| 02D0 2088             | SP1_ERR_ATTR_CAPT_DBG0 | Port 1 Attributes Error Capture CSR 0            |
| 02D0 208C             | SP1_ERR_CAPT_DBG1      | Port 1 Packet/Control Symbol Error Capture CSR 1 |
| 02D0 2090             | SP1_ERR_CAPT_DBG2      | Port 1 Packet/Control Symbol Error Capture CSR 2 |
| 02D0 2094             | SP1_ERR_CAPT_DBG3      | Port 1 Packet/Control Symbol Error Capture CSR 3 |
| 02D0 2098             | SP1_ERR_CAPT_DBG4      | Port 1 Packet/Control Symbol Error Capture CSR 4 |
| 02D0 209C - 02D0 20A4 | -                      | Reserved                                         |
| 02D0 20A8             | SP1_ERR_RATE           | Port 1 Error Rate CSR                            |
| 02D0 20AC             | SP1_ERR_THRESH         | Port 1 Error Rate Threshold CSR                  |
| 02D0 20B0 - 02D0 20BC | -                      | Reserved                                         |
| 02D0 20C0             | SP2_ERR_DET            | Port 2 Error Detect CSR                          |
| 02D0 20C4             | SP2_RATE_EN            | Port 2 Error Enable CSR                          |
| 02D0 20C8             | SP2_ERR_ATTR_CAPT_DBG0 | Port 2 Attributes Error Capture CSR 0            |
| 02D0 20CC             | SP2_ERR_CAPT_DBG1      | Port 2 Packet/Control Symbol Error Capture CSR 1 |
| 02D0 20D0             | SP2_ERR_CAPT_DBG2      | Port 2 Packet/Control Symbol Error Capture CSR 2 |
| 02D0 20D4             | SP2_ERR_CAPT_DBG3      | Port 2 Packet/Control Symbol Error Capture CSR 3 |
| 02D0 20D8             | SP2_ERR_CAPT_DBG4      | Port 2 Packet/Control Symbol Error Capture CSR 4 |
| 02D0 20DC - 02D0 20E4 | -                      | Reserved                                         |
| 02D0 20E8             | SP2_ERR_RATE           | Port 2 Error Rate CSR                            |
| 02D0 20EC             | SP2_ERR_THRESH         | Port 2 Error Rate Threshold CSR                  |
| 02D0 20F0 - 02D0 20FC | -                      | Reserved                                         |
| 02D0 2100             | SP3_ERR_DET            | Port 3 Error Detect CSR                          |
| 02D0 2104             | SP3_RATE_EN            | Port 3 Error Enable CSR                          |
| 02D0 2108             | SP3_ERR_ATTR_CAPT_DBG0 | Port 3 Attributes Error Capture CSR 0            |
| 02D0 210C             | SP3_ERR_CAPT_DBG1      | Port 3 Packet/Control Symbol Error Capture CSR 1 |
| 02D0 2110             | SP3_ERR_CAPT_DBG2      | Port 3 Packet/Control Symbol Error Capture CSR 2 |

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**Table 7-111 RapidIO Control Registers (Part 11 of 12)**

| Hex Address Range               | Acronym               | Register Name                                          |
|---------------------------------|-----------------------|--------------------------------------------------------|
| 02D0 2114                       | SP3_ERR_CAPT_DBG3     | Port 3 Packet/Control Symbol Error Capture CSR 3       |
| 02D0 2118                       | SP3_ERR_CAPT_DBG4     | Port 3 Packet/Control Symbol Error Capture CSR 4       |
| 02D0 211C - 02D0 2124           | -                     | Reserved                                               |
| 02D0 2128                       | SP3_ERR_RATE          | Port 3 Error Rate CSR                                  |
| 02D0 212C                       | SP3_ERR_THRESH        | Port 3 Error Rate Threshold CSR                        |
| 02D0 2130 - 02D1 0FFC           | -                     | Reserved                                               |
| <b>Implementation Registers</b> |                       |                                                        |
| 02D1 1000 - 02D1 1FFC           | -                     | Reserved                                               |
| 02D1 2000                       | SP_IP_DISCOVERY_TIMER | Port IP Discovery Timer in 4x mode                     |
| 02D1 2004                       | SP_IP_MODE            | Port IP Mode CSR                                       |
| 02D1 2008                       | IP_PRESCAL            | Port IP Prescaler Register                             |
| 02D1 200C                       | -                     | Reserved                                               |
| 02D1 2010                       | SP_IP_PW_IN_CAPT0     | Port-Write-In Capture CSR Register 0                   |
| 02D1 2014                       | SP_IP_PW_IN_CAPT1     | Port-Write-In Capture CSR Register 1                   |
| 02D1 2018                       | SP_IP_PW_IN_CAPT2     | Port-Write-In Capture CSR Register 2                   |
| 02D1 201C                       | SP_IP_PW_IN_CAPT3     | Port-Write-In Capture CSR Register 3                   |
| 02D1 2020 - 02D1 3FFC           | -                     | Reserved                                               |
| 02D1 4000                       | SP0_RST_OPT           | Port 0 Reset Option CSR                                |
| 02D1 4004                       | SP0_CTL_INDEP         | Port 0 Control Independent Register                    |
| 02D1 4008                       | SP0_SILENCE_TIMER     | Port 0 Silence Timer Register                          |
| 02D1 400C                       | SP0_MULT_EVTNT_CS     | Port 0 Multicast-Event Control Symbol Request Register |
| 02D1 4010                       | -                     | Reserved                                               |
| 02D1 4014                       | SP0_CS_TX             | Port 0 Control Symbol Transmit Register                |
| 02D1 4018 - 02D1 40FC           | -                     | Reserved                                               |
| 02D1 4100                       | SP1_RST_OPT           | Port 1 Reset Option CSR                                |
| 02D1 4104                       | SP1_CTL_INDEP         | Port 1 Control Independent Register                    |
| 02D1 4108                       | SP1_SILENCE_TIMER     | Port 1 Silence Timer Register                          |
| 02D1 410C                       | SP1_MULT_EVTNT_CS     | Port 1 Multicast-Event Control Symbol Request Register |
| 02D1 4110                       | -                     | Reserved                                               |
| 02D1 4114                       | SP1_CS_TX             | Port 1 Control Symbol Transmit Register                |
| 02D1 4118 - 02D1 41FC           | -                     | Reserved                                               |
| 02D1 4200                       | SP2_RST_OPT           | Port 2 Reset Option CSR                                |
| 02D1 4204                       | SP2_CTL_INDEP         | Port 2 Control Independent Register                    |
| 02D1 4208                       | SP2_SILENCE_TIMER     | Port 2 Silence Timer Register                          |
| 02D1 420C                       | SP2_MULT_EVTNT_CS     | Port 2 Multicast-Event Control Symbol Request Register |
| 02D1 4214                       | SP2_CS_TX             | Port 2 Control Symbol Transmit Register                |
| 02D1 4218 - 02D1 42FC           | -                     | Reserved                                               |
| 02D1 4300                       | SP3_RST_OPT           | Port 3 Reset Option CSR                                |
| 02D1 4304                       | SP3_CTL_INDEP         | Port 3 Control Independent Register                    |
| 02D1 4308                       | SP3_SILENCE_TIMER     | Port 3 Silence Timer Register                          |
| 02D1 430C                       | SP3_MULT_EVTNT_CS     | Port 3 Multicast-Event Control Symbol Request Register |
| 02D1 4310                       | -                     | Reserved                                               |
| 02D1 4314                       | SP3_CS_TX             | Port 3 Control Symbol Transmit Register                |

**Table 7-111 RapidIO Control Registers (Part 12 of 12)**

| Hex Address Range         | Acronym | Register Name |
|---------------------------|---------|---------------|
| 02D1 4318 - 02D2 0FFF     | -       | Reserved      |
| 02D2 1000 - 02DF FFFF     | -       | Reserved      |
| <b>End of Table 7-111</b> |         |               |

### 7.20.3 Serial RapidIO Electrical Data/Timing

The *TMS320TCI6484 and TMS320C6457 SerDes Implementation Guidelines* application report (literature number [SPRAAY1](#)) specifies a complete printed circuit board (PCB) solution for the C6457 as well as a list of compatible SRIO devices showing two DSPs connected via a 4× SRIO link. TI has performed the simulation and system characterization to ensure all SRIO interface timings in this solution are met; therefore, no electrical data/timing information is supplied here for this interface.



**Note**—TI supports *only* designs that follow the board design guidelines outlined in the application report.

Serial RapidIO is electrically compliant with the *RapidIO™ Interconnect Specification, Part VI: Physical Layer 1×/4× LP-Serial Specification*, Revision 1.3.

## 7.21 General-Purpose Input/Output (GPIO)

### 7.21.1 GPIO Device-Specific Information

On the TMS320C6457, the GPIO peripheral pins GP[15:0] are also used to latch configuration pins. For more detailed information on device/peripheral configuration and the C6457 device pin muxing, see Section 3 “[Device Configuration](#)” on page 59.

### 7.21.2 GPIO Peripheral Register Description(s)

**Table 7-112 GPIO Registers**

| Hex Address Range         | Acronym      | Register Name                              |
|---------------------------|--------------|--------------------------------------------|
| 02B0 0008                 | BINTEN       | GPIO interrupt per bank enable register    |
| 02B0 000C                 | -            | Reserved                                   |
| 02B0 0010                 | DIR          | GPIO Direction Register                    |
| 02B0 0014                 | OUT_DATA     | GPIO Output Data register                  |
| 02B0 0018                 | SET_DATA     | GPIO Set Data register                     |
| 02B0 001C                 | CLR_DATA     | GPIO Clear Data Register                   |
| 02B0 0020                 | IN_DATA      | GPIO Input Data Register                   |
| 02B0 0024                 | SET_RIS_TRIG | GPIO Set Rising Edge Interrupt Register    |
| 02B0 0028                 | CLR_RIS_TRIG | GPIO Clear Rising Edge Interrupt Register  |
| 02B0 002C                 | SET_FAL_TRIG | GPIO Set Falling Edge Interrupt Register   |
| 02B0 0030                 | CLR_FAL_TRIG | GPIO Clear Falling Edge Interrupt Register |
| 02B0 008C                 | -            | Reserved                                   |
| 02B0 0090 - 02B0 00FF     | -            | Reserved                                   |
| 02B0 0100 - 02B0 3FFF     | -            | Reserved                                   |
| <b>End of Table 7-112</b> |              |                                            |

## 7.21.3 GPIO Electrical Data/Timing

**Table 7-113 GPIO Input Timing Requirements** <sup>(1)</sup>  
(see Figure 7-50)

| No. |                                         | Min | Max | Unit |
|-----|-----------------------------------------|-----|-----|------|
| 1   | $t_{w(GPOH)}$ Pulse duration, GPOx high | 12C |     | ns   |
| 2   | $t_{w(GPOL)}$ Pulse duration, GPOx low  | 12C |     | ns   |

**End of Table 7-113**

1 If CORECLKSEL = 0, C = 1 ÷ CORECLK(NIP) frequency, in ns. If CORECLKSEL = 1, C = 1 ÷ ALT CORECLK frequency, in ns.

**Table 7-114 GPIO Output Switching Characteristics** <sup>(1) (2)</sup>  
(see Figure 7-50)

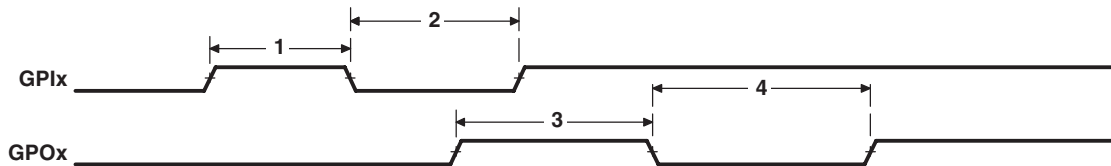
| No. | Parameter                               | Min     | Max | Unit |
|-----|-----------------------------------------|---------|-----|------|
| 1   | $t_{w(GPOH)}$ Pulse duration, GPOx high | 12C - 3 |     | ns   |
| 2   | $t_{w(GPOL)}$ Pulse duration, GPOx low  | 12C - 3 |     | ns   |

**End of Table 7-114**

1 Over recommended operating conditions.

2 If CORECLKSEL = 0, C = 1 ÷ CORECLK(NIP) frequency, in ns. If CORECLKSEL = 1, C = 1 ÷ ALT CORECLK frequency, in ns.

**Figure 7-50 GPIO Timing**



## 7.22 Emulation Features and Capability

### 7.22.1 Advanced Event Triggering (AET)

The TMS320C6457 device supports Advanced Event Triggering (AET). This capability can be used to debug complex problems as well as understand performance characteristics of user applications. AET provides the following capabilities:

- **Hardware Program Breakpoints:** specify addresses or address ranges that can generate events such as halting the processor or triggering the trace capture.
- **Data Watchpoints:** specify data variable addresses, address ranges, or data values that can generate events such as halting the processor or triggering the trace capture.
- **Counters:** count the occurrence of an event or cycles for performance monitoring.
- **State Sequencing:** allows combinations of hardware program breakpoints and data watchpoints to precisely generate events for complex sequences.

For more information on AET, see the following documents:

- *Using Advanced Event Triggering to Find and Fix Intermittent Real-Time Bugs* application report (literature number [SPRA753](#))
- *Using Advanced Event Triggering to Debug Real-Time Problems in High Speed Embedded Microprocessor Systems* application report (literature number [SPRA387](#))

## 7.22.2 Trace

The C6457 device supports Trace. Trace is a debug technology that provides a detailed, historical account of application code execution, timing, and data accesses. Trace collects, compresses, and exports debug information for analysis. Trace works in real-time and does not impact the execution of the system.

For more information on board design guidelines for Trace Advanced Emulation, see the *60-Pin Emulation Header Technical Reference* (literature number [SPRU655](#)).

### 7.22.2.1 Trace Electrical Data/Timing

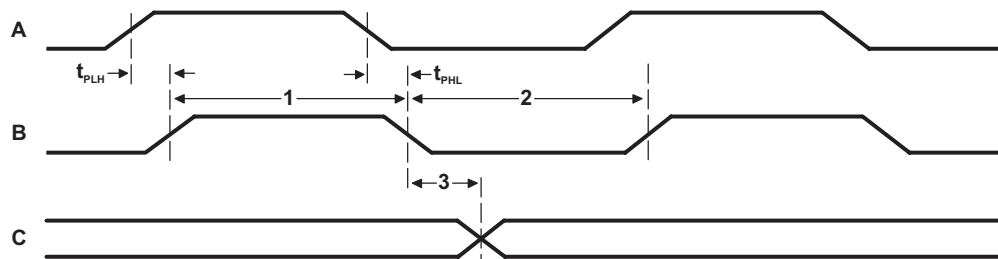
**Table 7-115 Switching Characteristics for Trace** <sup>(1)</sup>  
(see [Figure 7-51](#))

| No. | Parameter                                                                                               | Min  | Max | Unit |
|-----|---------------------------------------------------------------------------------------------------------|------|-----|------|
| 1   | $t_w(\text{DPnH})$ Pulse duration, DPn/EMUn high                                                        | 2.4  |     | ns   |
| 1   | $t_w(\text{DPnH})90\%$ Pulse duration, DPn/EMUn high detected at 90% Voh                                | 1.5  |     | ns   |
| 2   | $t_w(\text{DPnL})$ Pulse duration, DPn/EMUn low                                                         | 2.4  |     | ns   |
| 2   | $t_w(\text{DPnL})10\%$ Pulse duration, DPn/EMUn low detected at 10% Voh                                 | 1.5  |     | ns   |
| 3   | $t_{sko}(\text{DPn})$ Output skew time, time delay difference between DPn/EMUn pins configured as trace | -500 | 500 | ps   |

End of Table 7-115

<sup>1</sup> Over recommended operating conditions.

**Figure 7-51 Trace Timing**



### 7.22.3 IEEE 1149.1 JTAG

The JTAG interface is used to support boundary scan and emulation of the device. The boundary scan supported allows for an asynchronous TRST and only the 5 baseline JTAG signals (e.g., no EMU[1:0]) required for boundary scan. Most interfaces on the device follow the Boundary Scan Test Specification (IEEE1149.1), while all of the SerDes (SRIO and SGMII) support the AC-coupled net test defined in *AC-Coupled Net Test Specification* (IEEE1149.6).

It is expected that all compliant devices are connected through the same JTAG interface, in daisy-chain fashion, in accordance with the specification. The JTAG interface uses 1.8-V LVCMOS buffers, compliant with the *Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuit Specification* (EAI/JESD8-5).

#### 7.22.3.1 IEEE 1149.1 JTAG Compatibility Statement

For maximum reliability, the C6457 DSP includes an internal pulldown (IPD) on the TRST pin to ensure that TRST will always be asserted upon power up and the DSP's internal emulation logic will always be properly initialized when this pin is not routed out. JTAG controllers from Texas Instruments actively drive TRST high. However, some third-party JTAG controllers may not drive TRST high but expect the use of an external pullup resistor on TRST. When using this type of JTAG controller, assert TRST to initialize the DSP after powerup and externally drive TRST high before attempting any emulation or boundary scan operations.

### 7.22.3.2 JTAG Electrical Data/Timing

**Table 7-116 JTAG Test Port Timing Requirements**  
(see Figure 7-52)

| No. |                                                                    | Min | Max | Unit |
|-----|--------------------------------------------------------------------|-----|-----|------|
| 1   | $t_{c(TCK)}$ Cycle time, TCK                                       | 10  | 20  | ns   |
| 3   | $t_{su(TDIV-TCKH)}$ Setup time, TDI/TMS/TRST valid before TCK high | 2   |     | ns   |
| 4   | $t_{h(TCKH-TDIV)}$ Hold time, TDI/TMS/TRST valid after TCK high    | 5   |     | ns   |

End of Table 7-116

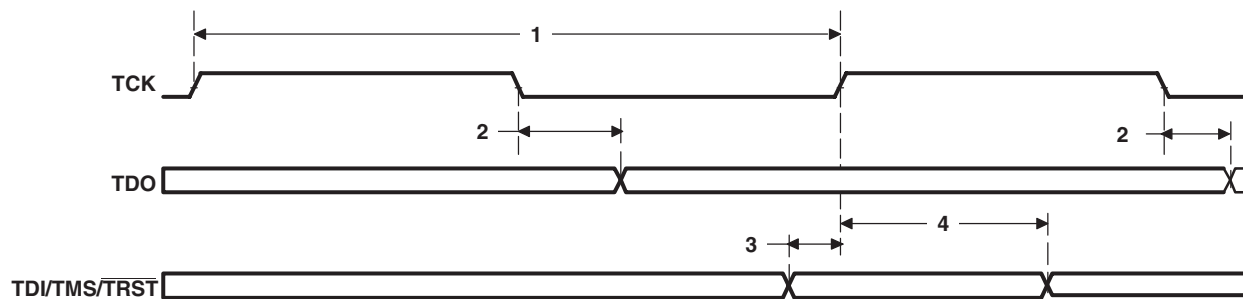
**Table 7-117 JTAG Test Port Switching Characteristics**<sup>(1)</sup>  
(see Figure 7-52)

| No. | Parameter                                           | Min | Max                      | Unit |
|-----|-----------------------------------------------------|-----|--------------------------|------|
| 2   | $t_{d(TCKL-TDOV)}$ Delay time, TCK low to TDO valid |     | $0.25 \times t_{c(TCK)}$ | ns   |

End of Table 7-117

<sup>1</sup> Over recommended operating conditions.

**Figure 7-52 JTAG Test-Port Timing**



### 7.22.3.3 HS-RTDX Electrical Data/Timing

**Table 7-118 Timing Requirements for HS-RTDX**  
(see Figure 7-53)

| No. |                                                            | Min | Max | Unit |
|-----|------------------------------------------------------------|-----|-----|------|
| 1   | $t_{c(TCK)}$ Cycle time, TCK                               | 20  |     | ns   |
| 2   | $t_{su(TDIV-TCKH)}$ Setup time, EMUn valid before TCK high | 1.5 |     | ns   |
| 3   | $t_{h(TCKH-TDIV)}$ Hold time, EMUn valid after TCK high    | 1.5 |     | ns   |

End of Table 7-118

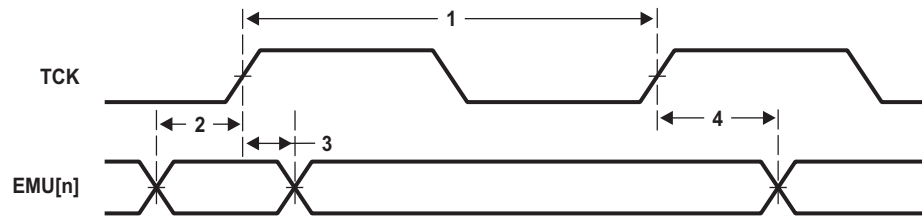
**Table 7-119 Switching Characteristics for HS-RTDX**<sup>(1)</sup>  
(see Figure 7-53)

| No. | Parameter                                             | Min | Max  | Unit |
|-----|-------------------------------------------------------|-----|------|------|
| 4   | $t_{d(TCKL-TDOV)}$ Delay time, TCK high to EMUn valid | 3   | 16.5 | ns   |

End of Table 7-119

<sup>1</sup> Over recommended operating conditions.

**Figure 7-53 HS-RTDX Timing**





## 8 Mechanical Data

### 8.1 Thermal Data

Table 8-1 shows the thermal resistance characteristics for the PBGA - CMH/GMH mechanical package.

**Table 8-1 Thermal Resistance Characteristics (PBGA Package) [CMH/GMH]**

| No.              |                                  | °C/W |
|------------------|----------------------------------|------|
| 1                | $R\theta_{JC}$ Junction-to-case  | 1.53 |
| 2                | $R\theta_{JB}$ Junction-to-board | 8.1  |
| End of Table 8-1 |                                  |      |

### 8.2 Packaging Information

The following packaging information reflects the most current released data available for the designated device(s). This data is subject to change without notice and without revision of this document.

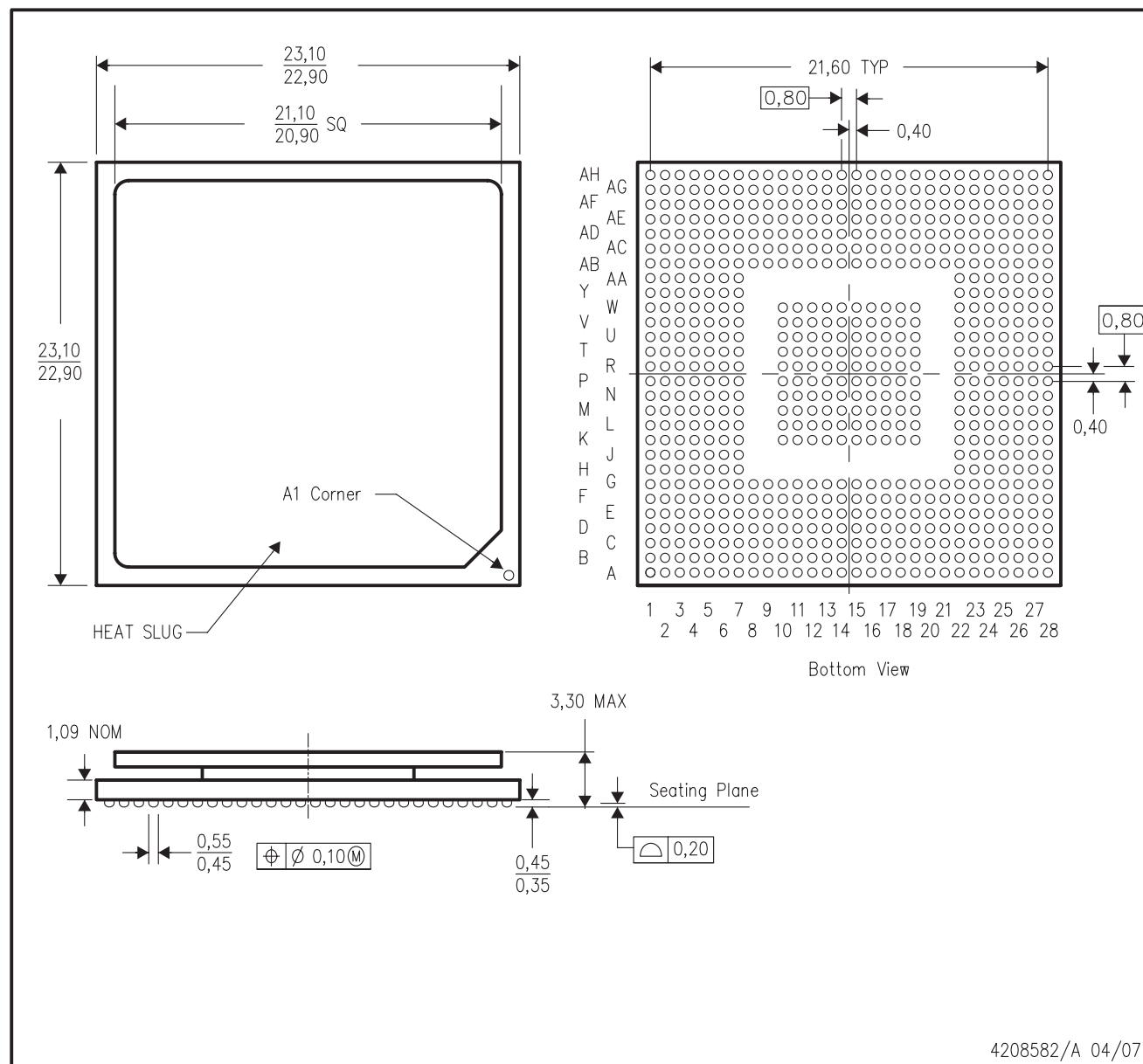


## 8.4 Package GMH

**Figure 8-2 GMH (S-PBGA-N688) Plastic Ball Grid Array**

**GMH (S-PBGA-N688)**

**PLASTIC BALL GRID ARRAY**



**PRODUCT PREVIEW**

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Thermally enhanced plastic package with heat slug (HSL).
  - D. Flip chip application only.



**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4)              | Samples                 |
|-------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|---------------------------------------|-------------------------|
| TMS320C6457CCMH   | ACTIVE        | FCBGA        | CMH                | 688  | 60          | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-4-245C-72HR    | 0 to 100     | TMS320C6457CMH<br>@2007 TI            | <a href="#">Samples</a> |
| TMS320C6457CCMH2  | ACTIVE        | FCBGA        | CMH                | 688  | 60          | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-4-245C-72HR    | 0 to 95      | TMS320C6457CMH<br>1.2GHZ<br>@2007 TI  | <a href="#">Samples</a> |
| TMS320C6457CCMH8  | ACTIVE        | FCBGA        | CMH                | 688  | 60          | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-4-245C-72HR    | 0 to 100     | TMS320C6457CMH<br>850MHZ<br>@2007 TI  | <a href="#">Samples</a> |
| TMS320C6457CCMHA  | ACTIVE        | FCBGA        | CMH                | 688  | 60          | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-4-245C-72HR    | -40 to 100   | TMS320C6457CCMH<br>A1GHZ<br>@2007 TI  | <a href="#">Samples</a> |
| TMS320C6457CCMHA2 | ACTIVE        | FCBGA        | CMH                | 688  | 60          | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-4-245C-72HR    | -40 to 95    | TMS320C6457CMH<br>A1.2GHZ<br>@2007 TI | <a href="#">Samples</a> |
| TMS320C6457CGMH   | ACTIVE        | FCBGA        | GMH                | 688  |             | TBD                        | Call TI          | Call TI              | 0 to 100     | TMS320C6457GMH<br>@2007 TI            | <a href="#">Samples</a> |
| TMS320C6457CGMH2  | ACTIVE        | FCBGA        | GMH                | 688  |             | TBD                        | Call TI          | Call TI              | 0 to 95      |                                       | <a href="#">Samples</a> |
| TMS320C6457CGMH8  | ACTIVE        | FCBGA        | GMH                | 688  |             | TBD                        | Call TI          | Call TI              | 0 to 100     |                                       | <a href="#">Samples</a> |
| TMS320C6457CGMHA  | ACTIVE        | FCBGA        | GMH                | 688  | 60          | TBD                        | Call TI          | Call TI              | -40 to 100   | TMS320C6457CGMH<br>@2007 TI<br>A1GHZ  | <a href="#">Samples</a> |
| TMS320C6457CGMHA2 | ACTIVE        | FCBGA        | GMH                | 688  | 60          | TBD                        | Call TI          | Call TI              | -40 to 95    |                                       | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

---

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

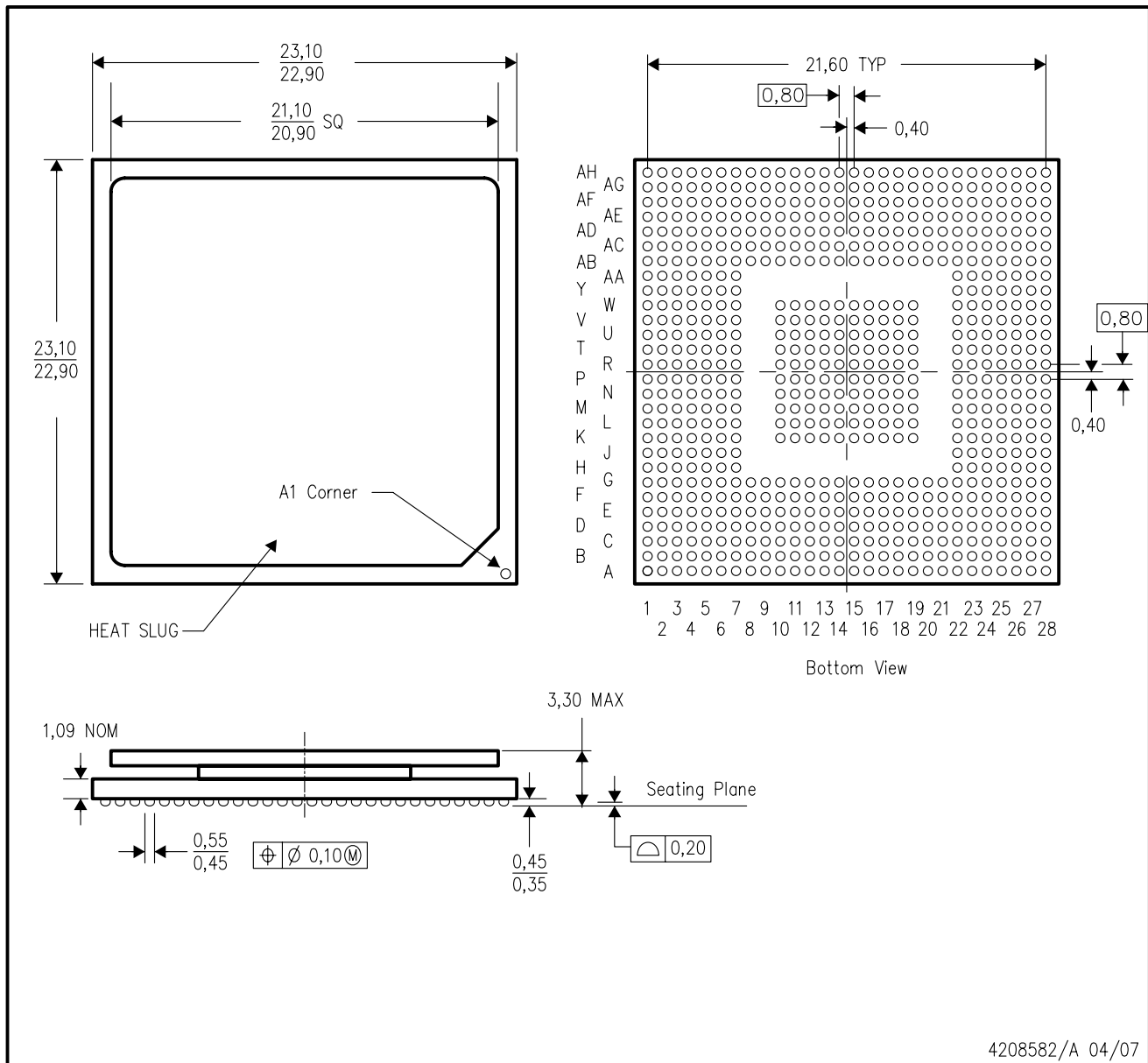
<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

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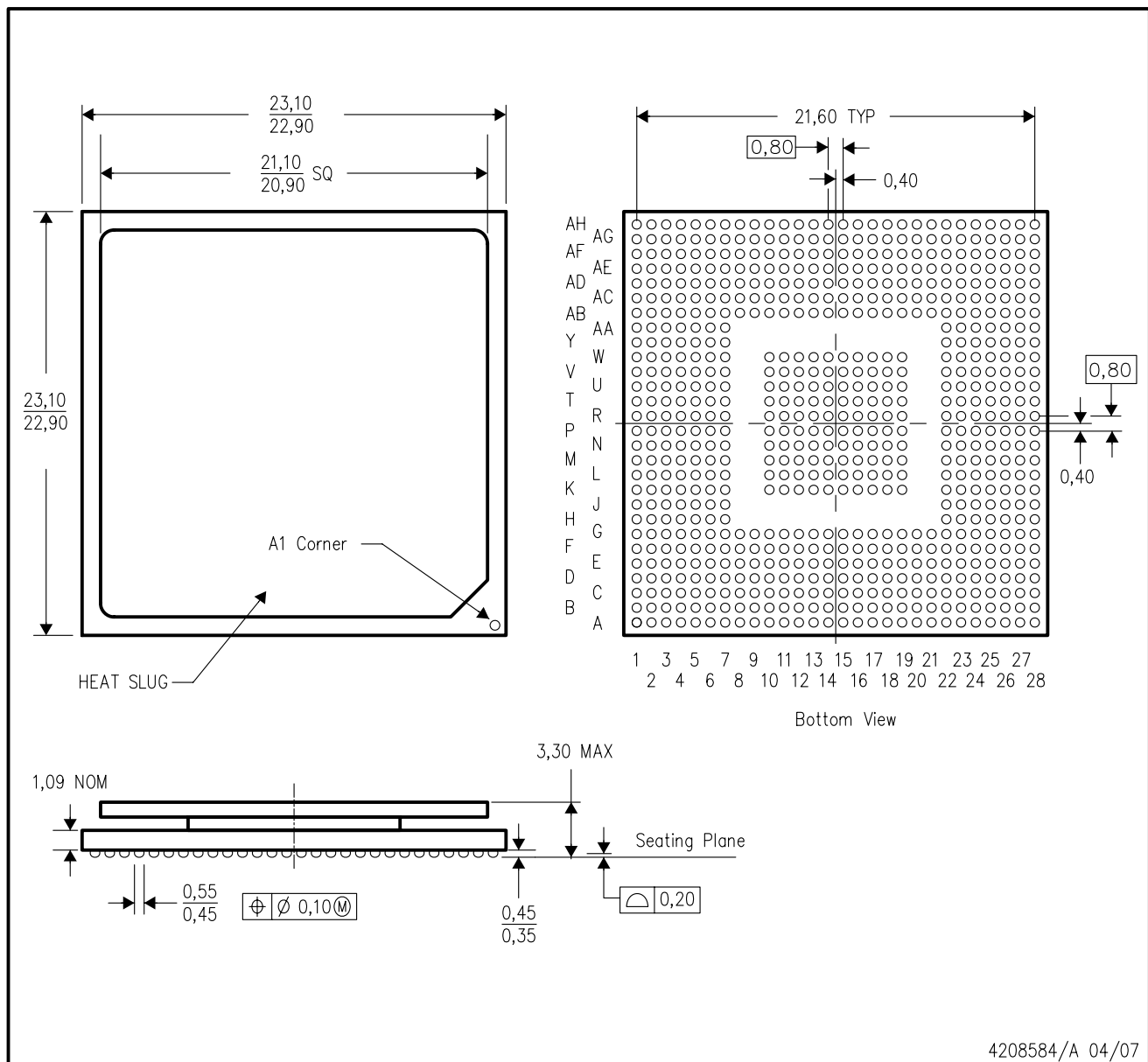
## GMH (S-PBGA-N688)

## PLASTIC BALL GRID ARRAY



CMH (S-PBGA-N688)

PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Flip chip application only.
  - Lead-free die bump and solder ball.
  - Thermally enhanced plastic package with heat slug (HSL).



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| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
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