KAF-8300

3326 (H) x 2504 (V) Full Frame CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAF−8300 Image Sensor is a 22.5 mm diagonal (Four Thirds Format) high performance color or monochrome full frame CCD (charge-coupled device) image sensor designed for a wide range of image sensing applications including digital imaging. Each pixel contains blooming protection by means of a lateral overflow drain thereby preventing image corruption during high light level conditions. For the color version, the 5.4 μm square pixels are patterned with an RGB mosaic color filter with overlying microlenses for improved color response and reproduction. Several versions of monochrome devices are available with or without microlenses.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Full Frame CCD; with Square Pixels
Total Number of Pixels	3448 (H) × 2574 (V) = approx. 8.9 Mp
Number of Effective Pixels Color Device Monochrome Device	 3358 (H) × 2536 (V) = approx. 8.6 Mp 3366 (H) × 2544 (V) = approx. 8.6 Mp
Number of Active Pixels	3326 (H) × 2504 (V) = approx. 8.3 Mp
Pixel Size	5.4 μm (H) × 5.4 μm (V)
Active Image Size	17.96 mm (H) × 13.52 mm (V) 22.5 mm (Diag.), 4/3″ Optical Format
Aspect Ratio	4:3
Horizontal Outputs	1
Saturation Signal	> 25.5 ke⁻
Output Sensitivity	23 μV/e⁻
Quantum Efficiency (Color) R (450 nm) G (550 nm) B (650 mm)	 33% 40% 33%
Quantum Efficiency (Monochrome) Microlens, Clear Glass (540 nm) Microlens, No Glass (540 nm) Microlens, AR Glass (540 nm) No Microlens, Clear G. (560 nm)	 54% 60% 56% 37%
Total Sensor Noise	16 e⁻
Dark Signal	< 200 e⁻/s
Dark Current Doubling Temp.	5.8°C
Linear Dynamic Range	64.4 dB
Linear Error at 12°C	±10%
Charge Transfer Efficiency	0.999995
Blooming Protection (1 ms Integration Time)	1000X Saturation Exposure
Maximum Date Rate	28 MHz
Package	32-pin CERDIP, 0.070″ Pin Spacing
Cover Glass	Clear or AR Coated, 2 Sides

NOTE: Parameters above are specified at T = 60°C and a data rate of 28 MHz unless otherwise noted

Figure 1. KAF−8300 Full Frame CCD Image Sensor

Features

- TRUESENSE Transparent Gate Electrode for High Sensitivity
- High Resolution
- High Dynamic Range
- Low Noise Architecture

Applications

- Digitization
- Medical
- Scientific

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

The sensor utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAF−8300 IMAGE SENSOR

Part Number	Description	Marking Code
KAF−8300−AAB−CB−AA	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Standard Grade	KAF−8300XE Serial Number
KAF−8300−AAB−CB−AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Engineering Grade	
KAF−8300−AXC−CB−AA	Monochrome, Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Standard Grade	KAF−8300−AXC Serial Number
KAF−8300−AXC−CB−AE	Monochrome, Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Engineering Grade	
KAF−8300−AXC−CP−AA	Monochrome, Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Standard Grade	
KAF−8300−AXC−CP−AE	Monochrome, Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Engineering Grade	
KAF−8300−AXC−CD−AA	Monochrome, Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coatings (Both Sides), Standard Grade	
KAF−8300−AXC−CD−AE	Monochrome, Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coatings (Both Sides), Engineering Grade	
KAF−8300−CXB−CB−AA−Offset	Color (Bayer RGB), Special Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Standard Grade, Offset	KAF−8300CE Serial Number
KAF−8300−CXB−CB−AE−Offset	Color (Bayer RGB), Special Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Engineering Grade, Offset	

Table 3. ORDERING INFORMATION − EVALUATION SUPPORT

Part Number	Description
KAF−8300−12−28−A−EVK	Evaluation Board (Complete Kit)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

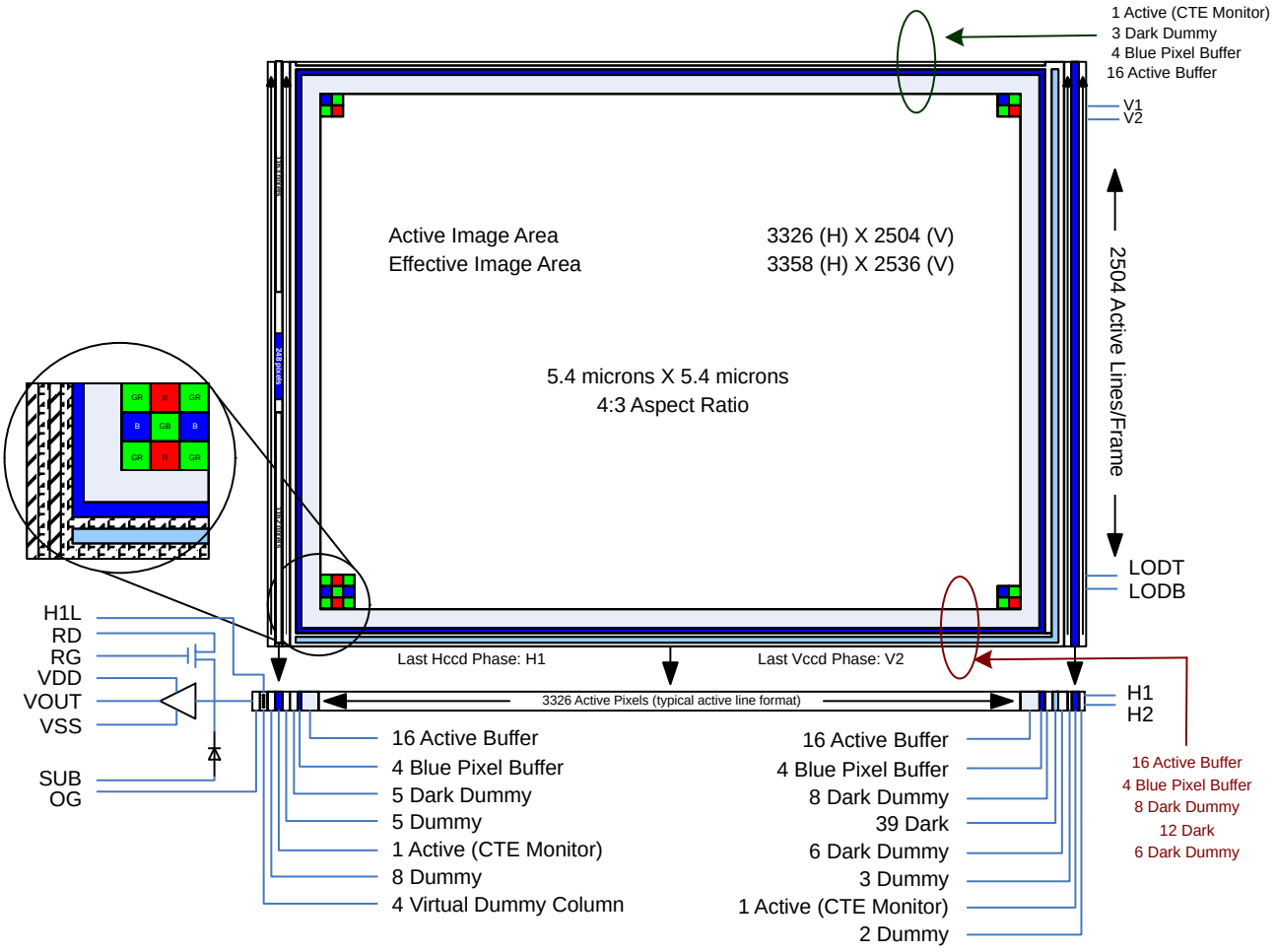


Figure 2. Block Diagram (Color)

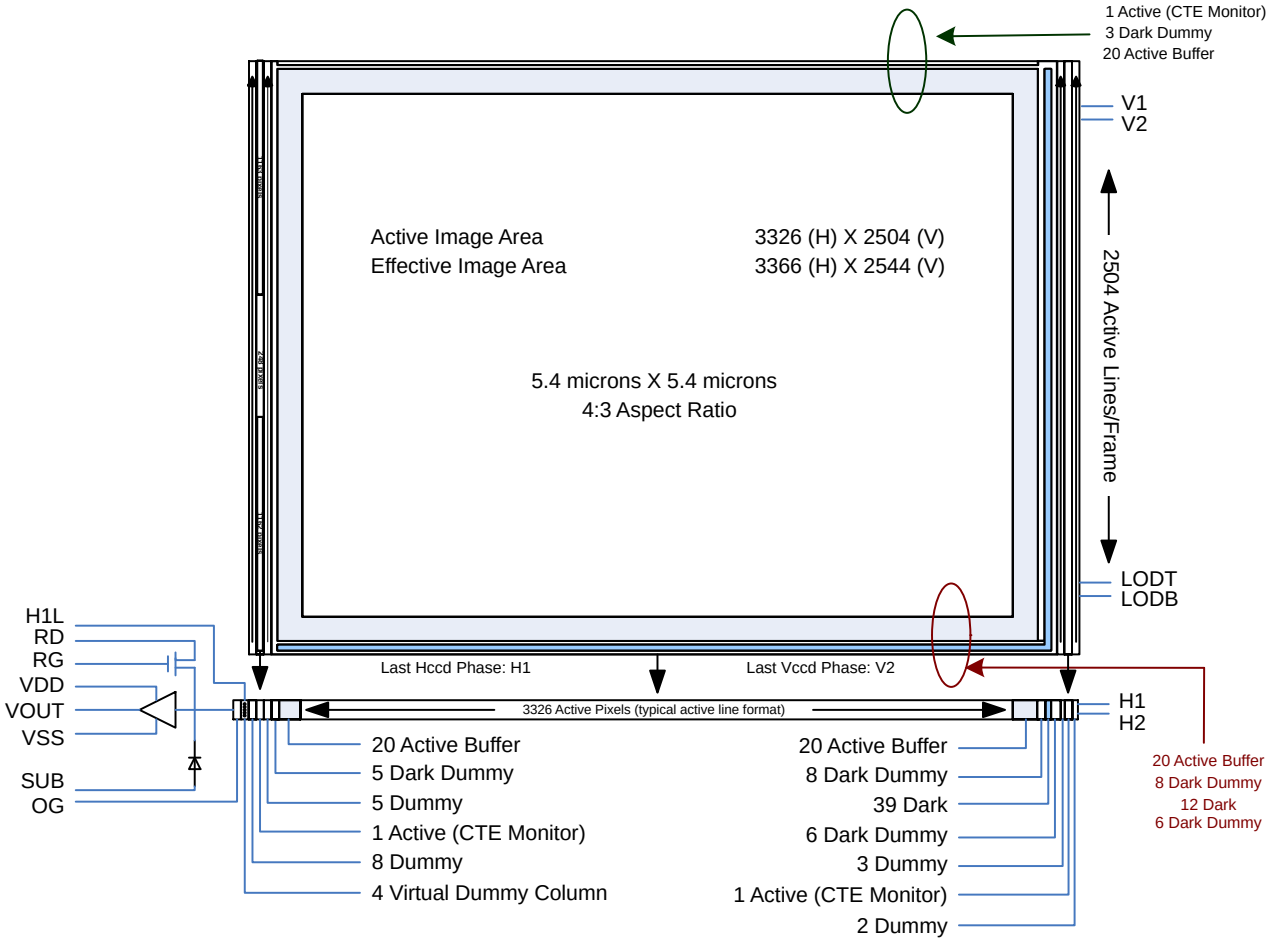


Figure 3. Block Diagram (Monochrome)

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region there are light shielded pixels that include 39 trailing dark pixels on every line. There are also 12 full dark lines at the start of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a dark reference.

Dark Dummy Pixels

Within the dark region some pixels are in close proximity to an active pixel, or the light sensitive regions that have been added for manufacturing test purposes, (CTE Monitor). In both cases, these pixels can scavenge signal depending on light intensity and wavelength. These pixels should not be used as a dark reference. These pixels are called dark dummy pixels.

Within the dark region, dark dummy pixels have been identified. There are 5 leading and 14 (6 + 8) trailing dark pixels on every line. There are also 14 (6 + 8) dark dummy lines at the start of every frame along with 3 dark dummy lines at the end of each frame.

Dummy Pixels

Within the horizontal shift register there are 13, (8 + 5), leading and 5, (2 + 3), trailing additional shift phases that are not electrically associated with any columns of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light and therefore, have been designated as dummy pixels. For this reason, they should not be used to determine a dark reference level.

Virtual Dummy Columns

Within the horizontal shift register there is 4 leading shift phases that are not physically associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light and therefore, have been designated as virtual dummy columns. For this reason, they also should not be used to determine a dark reference level.

Active Buffer Pixels

For color devices, sixteen buffer pixels adjacent to the blue pixel buffer region contain a RGB mosaic color pattern. This region is classified as active buffer pixels. These pixels are light sensitive but they are not tested for defects and

non-uniformities. The response of these pixels will not be uniform.

For monochrome devices, 20 buffer pixels adjacent to the dark dummy pixels are classified as active buffer pixels. These pixels are light sensitive but they are not tested for defects and non-uniformities. The response of these pixels will not be uniform.

Blue Pixel Buffer

For color devices, four buffer pixels adjacent to any leading or trailing dark reference regions contain a blue filter and is classified as a blue pixel buffer. These pixels are light sensitive but they are not tested for defects and non-uniformities. The response of these pixels will not be uniform.

Monochrome devices do not contain a blue pixel buffer.

CTE Monitor Pixels

Within the horizontal dummy pixel region two light sensitive test pixels (one each on the leading and trailing ends) are added and within the vertical dummy pixel region one light sensitive test pixel has been added. These CTE monitor pixels are used for manufacturing test purposes. In order to facilitate measuring the device CTE, the pixels in the CTE Monitor region in the horizontal and vertical portion is coated with blue pigment on the color version only. The monochrome device is uncoated).

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

Charge Transport

The integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD's to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented a new line on the falling edge of V2 while H1 is held high. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the floating diffusion. On each falling edge of H1 a new charge packet is dumped onto a floating diffusion and sensed by the output amplifier.

Horizontal Register

Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip load must be added to the VOUT pin of the device. See Figure 5.

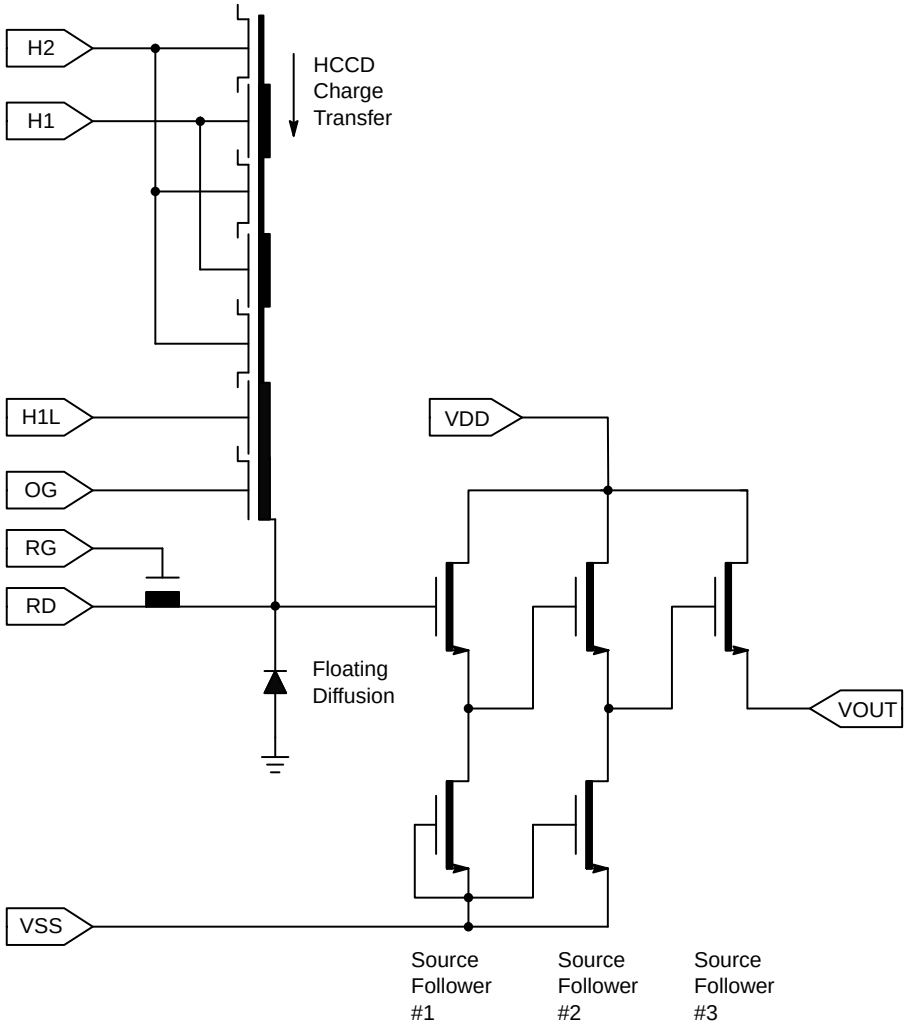
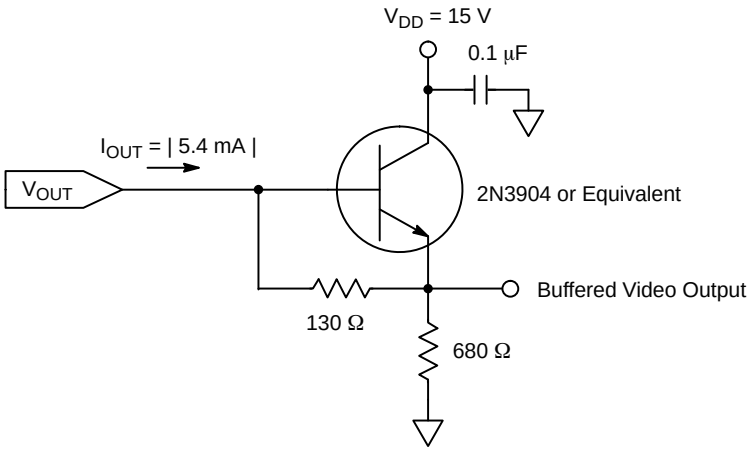


Figure 4. Output Architecture (Left of Right)

Output Load



NOTE: Component values may be revised based on operating conditions and other design considerations.

Figure 5. Recommended Output Structure Load Diagram

Physical Description

Pin Description and Device Orientation

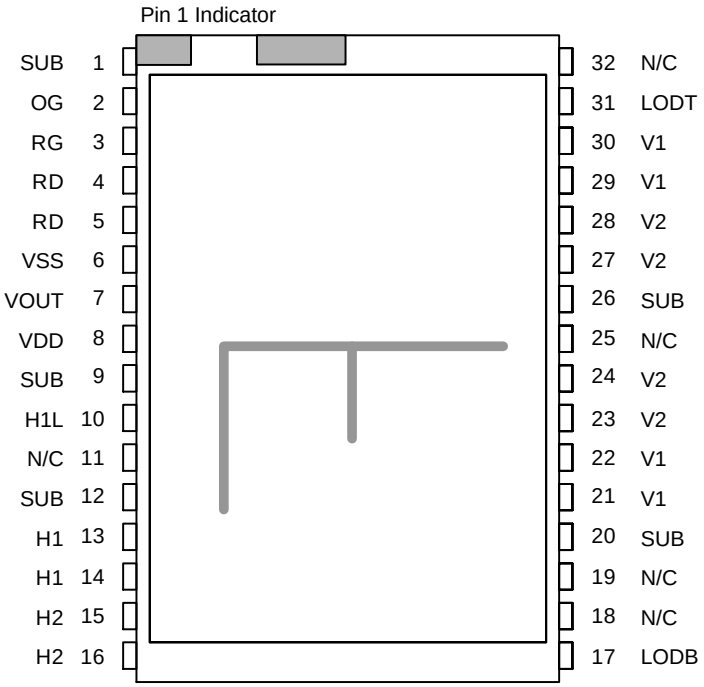


Figure 6. Pinout Diagram

Table 4. PIN DESCRIPTION

Pin	Name	Description
1	SUB	Substrate
2	OG	Output Gate
3	RG	Reset Gate
4	RD	Reset Drain Bias
5	RD	Reset Drain Bias
6	VSS	Output Amplifier Return
7	VOUT	Output
8	VDD	Output Amplifier Supply
9	SUB	Substrate
10	H1L	Horizontal Phase 1, Last Gate
11	N/C	No Connection
12	SUB	Substrate
13	H1	Horizontal Phase 1
14	H1	Horizontal Phase 1
15	H2	Horizontal Phase 2
16	H2	Horizontal Phase 2

Pin	Name	Description
17	LODB	Lateral Overflow Drain Bottom
18	N/C	No Connection
19	N/C	No Connection
20	SUB	Substrate
21	V1	Vertical Phase 1
22	V1	Vertical Phase 1
23	V2	Vertical Phase 2
24	V2	Vertical Phase 2
25	N/C	No Connection
26	SUB	Substrate
27	V2	Vertical Phase 2
28	V2	Vertical Phase 2
29	V1	Vertical Phase 1
30	V1	Vertical Phase 1
31	LODT	Lateral Overflow Drain Top
32	N/C	No Connection

1. Wherever possible, all N/C pins (11, 18, 19, 25, 32) should be connected to GND (0 V).

IMAGING PERFORMANCE

Table 5. TYPICAL OPERATIONAL CONDITIONS

Description	Condition − Unless otherwise Noted	Notes
Readout Time ($t_{READOUT}$)	370.36 ms	Includes $t_{Voverclock}$ & $t_{Hoverclock}$
Integration Time (t_{INT})	33 ms	
Horizontal Clock Frequency	28 MHz	
Light Source (LED)	Red, Green, Blue, Orange	
Mode	Flush − Integrate − Readout Cycle	

Table 6. SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes	Verification Plan
ALL DEVICES							
Minimum Column	MinColumn	575	−	−	mV	1, 4	Die[18]
Linear Saturation Signal	N_{e^-SAT}	25.5	−	−	ke$^-$	1, 3, 4	Design[19]
Charge to Voltage Conversion	Q−V	22.5	23.0	−	μV/e$^-$		Design[19]
Linearity Error	LeLow10 LeLow33 LeHigh	−10 −10 −10	− − −	10 10 10	%	2, 5, 6 2, 5, 6 2, 4, 5	Die[18]
Dark Signal (Active Area Pixels)	AA_DarkSig	−	−	200	e$^-$/s	4, 8	Die[18]
Dark Signal (Dark Reference Pixels)	DR_DarkSig	−	−	200	e$^-$/s	4, 8	Die[18]
Readout Cycle Dark Signal	Dark_Read	−	−	15	mV/s		Die[18]
Flush Cycle Dark Signal	Dark_Flush	−	43	90	mV/s		Die[18]
Dark Signal Non-Uniformity	DSNU DSNU_Step DSNU_H	− − −	1.30 0.14 0.40	3.0 0.5 1.0	mV p-p	4, 9	Die[18]
Dark Signal Doubling Temperature	ΔT	−	5.8	−	°C		Design[19]
Dark Reference Difference, Active Area	DarkStep	−3.5	0.15	3.5	mV	4	Die[18]
Total Noise	Dfld_noi	−	−	1.08	mV	4, 10	Die[18]
Total Sensor Noise	N	−	16	−	e$^-$ rms	19	Design[19]
Linear Dynamic Range	DR	−	64.4	−	dB	11	Design[19]
Horizontal Charge Transfer Efficiency	HCTE	0.999990	0.999995	−	%	4, 13, 21	Die[18]
Vertical Charge Transfer Efficiency	VCTE	0.999997	0.999999	−	%	4, 21	Die[18]
Blooming Protection	X_b	1,000	−	−	x E_{SAT}	14	Design[19]
Vertical Bloom on Transfer	VBloomF	−20	−	20	mV	4	Die[18]
Horizontal Crosstalk	H_Xtalk	−20	−	20	mV	4	Die[18]
Horizontal Overclock Noise	Hoclk_noi	0	−	1.08	mV	4	Die[18]
Output Amplifier Bandwidth	f_{-3dB}	88	−	159	MHz	4, 6, 16	Die[18]
Output Impedance, Amplifier	R_{OUT}	100	−	180	Ω	6	Die[18]
Hclk Feedthru	V_{HFT}	−	−	70	mV	4, 17	Die[18]
Reset Feedthru	V_{RFT}	500	710	1,000	mV		Design[19]

Table 6. SPECIFICATIONS (continued)

Description	Symbol	Min.	Nom.	Max.	Unit	Notes	Verification Plan
COLOR DEVICES							
Sensitivity					mV		Die[18]
Red	R_{RESP}	260	−	420			
Green	G_{RESP}	442	−	638			
Blue	B_{RESP}	230	−	420			
Quantum Efficiency					%		Design[19]
R (600 nm)	QE_{RED}	−	33	−			
G (540 nm)	QE_{GREEN}	−	40	−			
B (480 nm)	QE_{BLUE}	−	33	−			
Off-Band Response					mV		Die[18]
Green Inband	Gr_G_{RESP}	362	−	630			
Red Response	Gr_R_{RESP}	0	−	130			
Blue Response	Gr_B_{RESP}	0	−	260			
Red Inband	Rd_R_{RESP}	180	−	430			
Green Response	Rd_G_{RESP}	0	−	120			
Blue Response	Rd_B_{RESP}	0	−	45			
Blue Inband	Bl_B_{RESP}	90	−	420			
Red Response	Bl_R_{RESP}	0	−	40			
Green Response	Bl_G_{RESP}	0	−	120			
Linearity Balance	Red_Bal	−14	6.4	14	&	2, 6	Die[18]
	Blu_Bal	−8	0.2	8			
Photo Response Non-Uniformity	R_PRNU	−	−	15	% p-p	7	Die[18]
	G_PRNU	−	−	15			
	B_PRNU	−	−	15			
High Frequency Noise	R_Nois	−	−	2	% rms		Die[18]
	GRr_Nois	−	−	2			
	GBr_Nois	−	−	2			
	B_Nois	−	−	2			
Red-Green Hue Shift	RGHueUnif	−	−	10	%	12	Die[18]
Blue-Green Hue Shift	BGHueUnif	−	−	12	%	12	Die[18]
GRr/GBr Hue Uniformity	GrGbHueUnf	−	−	7	%	12	Die[18]
Green Light GRr/GBr Hue Uniformity	Gr_GHueUnf	−	−	9	%		Die[18]
Low Hue Uniformity	RGLoHueUnf	−	−	12	%		Die[18]
	BGLoHueUnf	−	−	10			
Streak/Spot	GrnStreak	−	−	40	%		
	RedStreak	−	−	20			
	BluStreak	−	−	20			
Local Green Difference					%		Die[18]
White Light, min	W_GNU_Min	−	−	4			
White Light, max	W_GNU_Max	−	−	6			
Green Light, min	Gr_GNU_Min	−	−	4			
Green Light, max	Gr_GNU_Max	−	−	4			
Red Light, min	R_GNU_Min	−	−	65			
Red Light, max	R_GNU_Max	−	−	65			
Blue Light, min	B_GNU_Min	−	−	40			
Blue Light, max	B_GNU_Max	−	−	40			
Chroma Test	UL_Chroma	−	−	7	%		Die[18]
	UR_Chroma	−	−	7			
	LL_Chroma	−	−	7			
	LR_Chroma	−	−	7			
Hue Test	UL_UR_Hue	−	−	6	%		Die[18]
	UL_LR_Hue	−	−	6			
	UL_LL_Hue	−	−	6			
	UR_LR_Hue	−	−	6			
	UR_LL_Hue	−	−	6			
	LR_LL_Hue	−	−	6			

Table 6. SPECIFICATIONS (continued)

Description	Symbol	Min.	Nom.	Max.	Unit	Notes	Verification Plan
MONOCHROME DEVICES							
Sensitivity − Monochrome	Resp	465	−	655	mV		Die[18]
Quantum Efficiency	QE				%		Design[19]
Microlens, Clear Glass (540 nm)		−	54	−			
Microlens, No Glass (540 nm)		−	60	−			
Microlens, AR Glass (540 nm)		−	56	−			
No Microlens, Clear G. (560 nm)		−	37	−			

1. Increasing output load currents to improve bandwidth will decrease these values.
2. Specified from 12°C to 60°C.
3. Saturation signal level achieved while meeting Le specification. Specified from 0°C to 40°C.
4. Operating temperature = 60°C.
5. Worst case deviation, (from 10 mV to V_{SAT} min), relative to a linear fit applied between 0 and 500 mV exposure.
6. Operating temperature = 25°C.
7. Peak to peak non-uniformity test based on an average of 185 × 185 blocks.
8. Average non-illuminated signal with respect to over clocked horizontal register signal.
9. Absolute difference between the maximum and minimum average signal levels of 185 × 185 blocks within the sensor.
10. Dark rms deviation of a multi-sampled pixel as measured using the KAF−8300 Evaluation Board.
11. 20Log (V_{SAT} / N).
12. Gradual variations in hue (red with respect to green pixels and blue with respect to green pixels) in regions of interest of 185 × 185 blocks.
13. Measured per transfer at 80% of V_{SAT}.
14. E_{SAT} equals the exposure required to achieve saturation. X_b represents the number of E_{SAT} exposures the sensor can tolerate before failure. X_b characterized at 25°C.
15. Video level DC offset with respect to ground at clamp position. Refer to Figure 17.
16. Last stage only. C_{LOAD} = 10 pF. Then $f_{-3dB} = (1 / (2p \cdot R_{OUT} \cdot C_{LOAD}))$.
17. Amount of artificial signal due to H1 coupling.
18. A parameter that is measured on every sensor during production testing.
19. A parameter that is quantified during the design verification activity.
20. Calculated value subtracting the noise contribution from the KAF−8300 Evaluation Board.
21. Process optimization has effectively eliminated vertical striations.
22. CTE = 1 − CTI. Where CTE is charge transfer efficiency and CTI is charge transfer inefficiency. CTI is the measured value.

TYPICAL PERFORMANCE CURVES

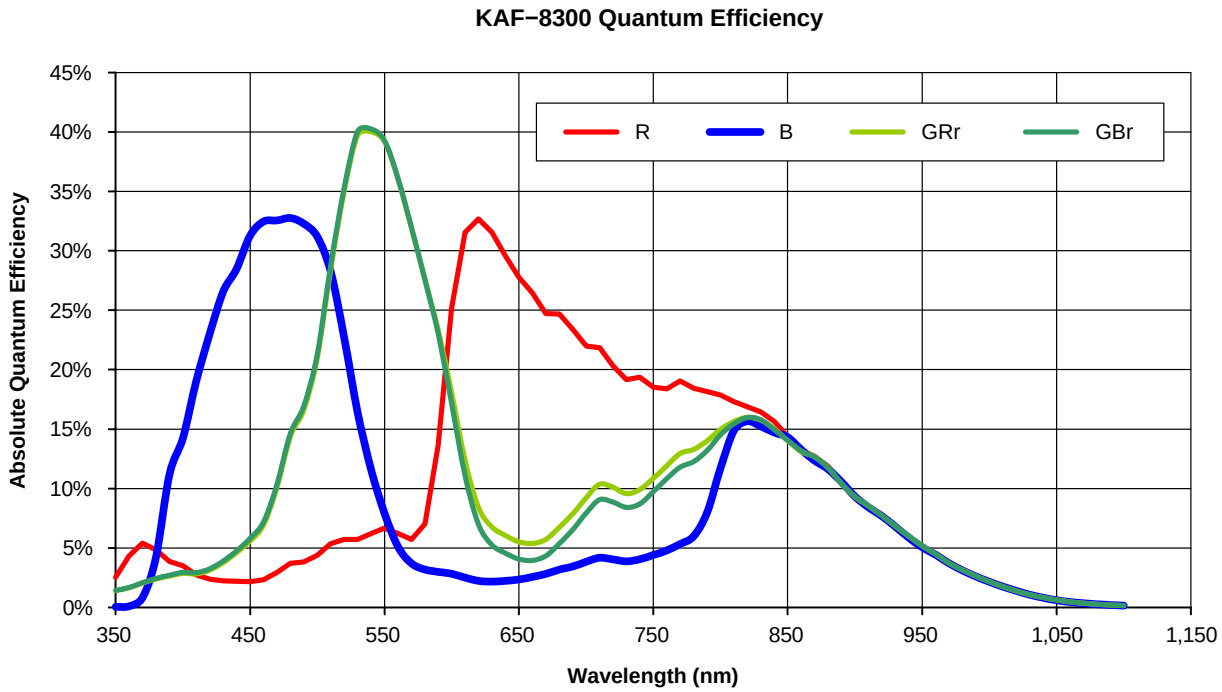


Figure 7. Typical Quantum Efficiency (Color Version)

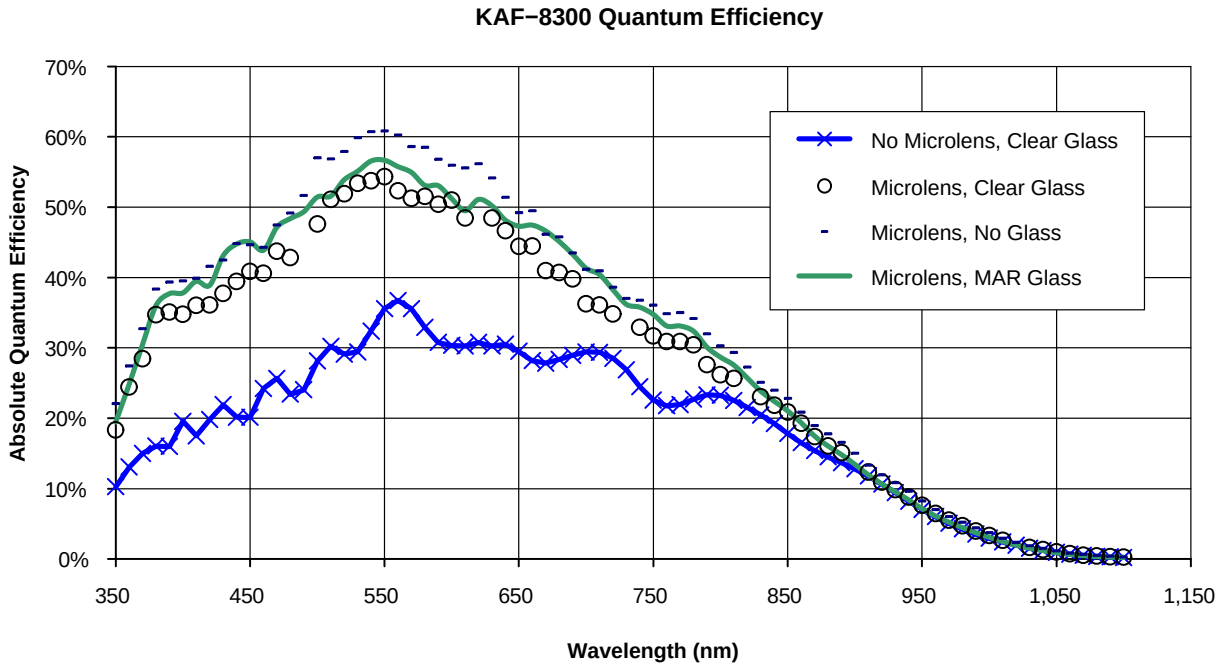
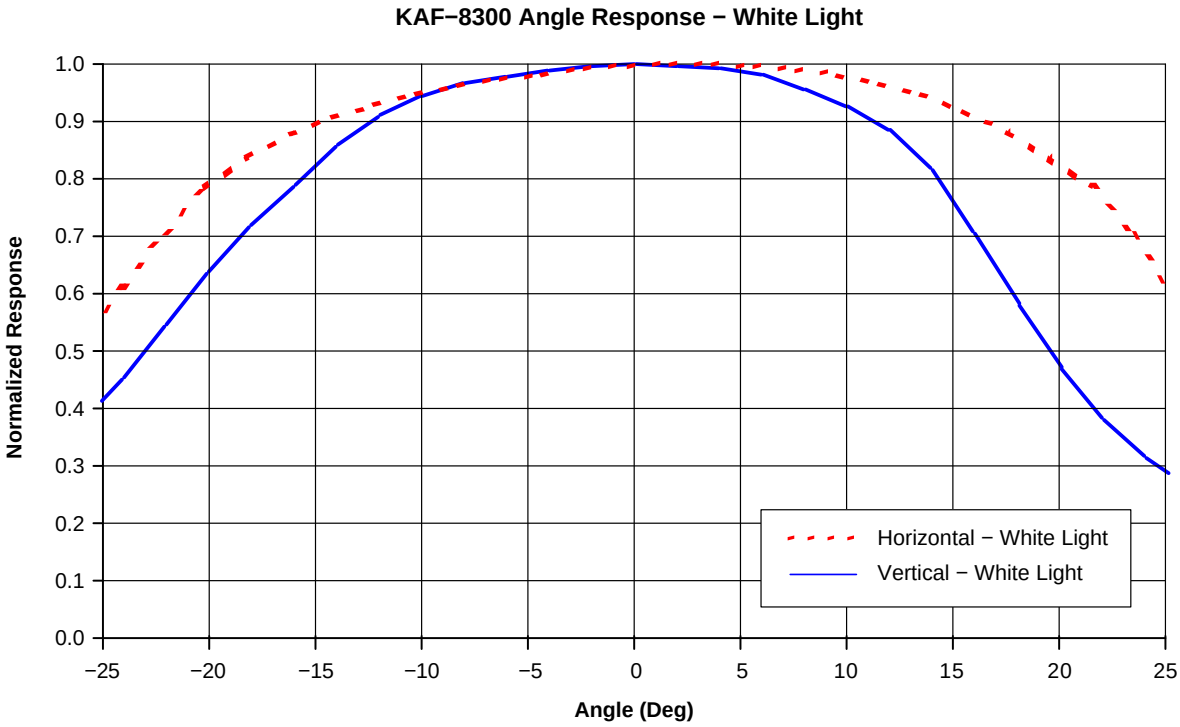
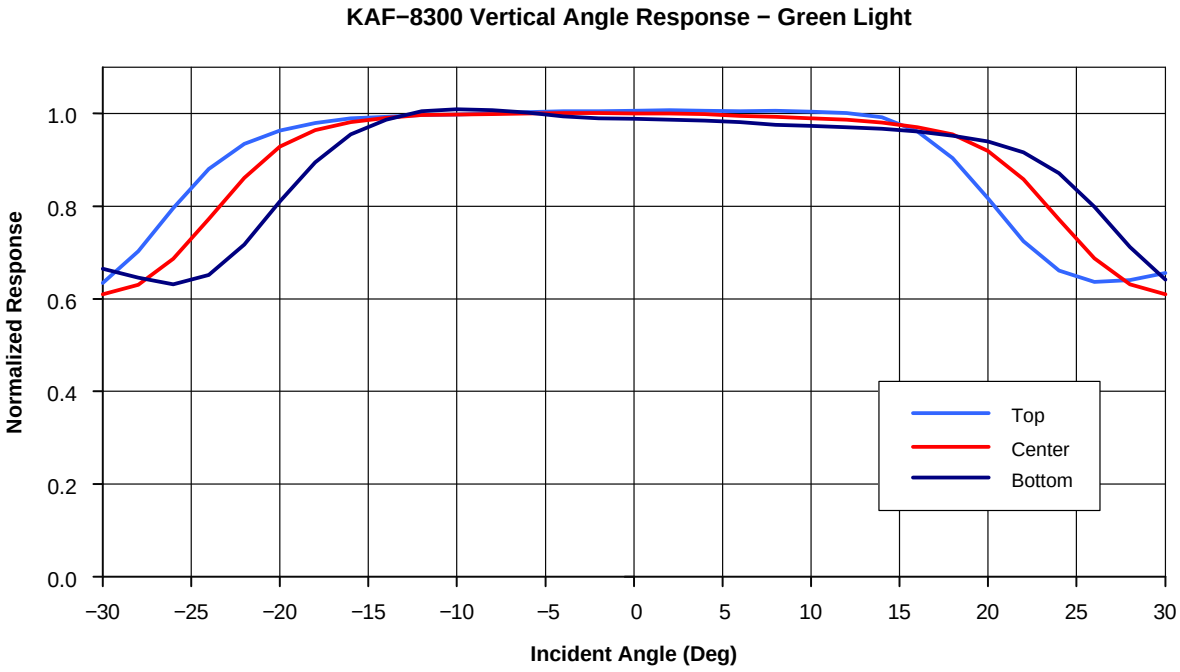


Figure 8. Typical Quantum Efficiency (All Monochrome Versions)



NOTE: The center location of the die is as shown. The effective optical shift is 6° center-to-edge, along the diagonal.

Figure 9. Typical Angular Response (Color Version)



NOTE: The effective optical shift is 6° center-to-edge, along the diagonal.

Figure 10. Typical Angular Response (Monochrome with Microlens)

DEFECT DEFINITIONS

Table 7. OPERATIONAL CONDITIONS

(The Defect Specifications are measured using the following conditions.)

Description	Test Condition	Notes
Integration Time (t_{INT})	33 ms	Unless Otherwise Noted
Operating Temperature	60°C	Unless Otherwise Noted

Table 8. SPECIFICATIONS

Description	Symbol	Definition	Threshold	Maximum Number Allowed	Notes
COLOR DEVICES					
Point Defect	BPnt33_7	Dark Field, Minor, Short Integration Time	7.5 mV	800 Total Points Allowed for this Group of Tests	3
Point Defect	Bfld_Pnt_D	Dark Point in an Illuminated Field	11%		3
Point Defect	Bfld_Pnt_B	Bright Point in an Illuminated Field	7%		3
Point Defect	BPnt33_100	Dark Field, Major, Short Integration Time	10 mV		3
Point Defect	BPnt33_500	Dark Field, Major, Short Integration Time	500 mV	0	3
Point Defect	BPnt333_13	Dark Field, Minor, Long Integration Time, t_{INT} = 1/3 s	13 mV	32,500	1, 3, 4
Point Defect	DR_BPnts	Bright Point in the Dark Reference Region	7.5 mV	0	5
Cluster Defect	Total_Clst	A Cluster is a Group of 2 or more Defective Pixels that do not Exceed the Perpendicular Pattern Defect	−	6 Total	3
Cluster Defect	Dfld_Vperp	Dark Field Very Long Exposure Bright Cluster where 9 or more Adjacent Point Defects Exist, Very Long Integration Time, t_{INT} = 1 s	3.04 mV	0	3
Cluster Defect − Perpendicular Pattern Defect	Dfld_Perp Bfld_Perp Total_Perp	Three or more Adjacent Point Defects in the Same Color Plane, along a Row or Column	−	0	2, 3
Column Defect, Illuminated	Bfld_Col_D Bfld_Col_B	A Column which Deviates above or below Neighboring Columns under Illuminated Conditions (> 300 mV Signal) greater that the Threshold	1.5% 1.5%	0	3
Column Defect, Dark Field	Dfld_Col2 Dfld_Col4 Lo_Col_B Lo_Col_D Lo_Col_B1 Lo_Col_D1	A Column which Deviates above or below Neighboring Columns under Non-Illuminated or Low Light Level Conditions (~10 mV) greater than the Threshold	1 mV 1 mV 1 mV 1 mV 1 mV 1 mV	0	3 3 5 5 5 5
Row Defect	Dfld_Row	Row Defect if Row Average Deviates above Threshold	1 mV	0	3
LOD Bright Col, Dark	Dfld_LodCol	Defines Functionality and Uniform Efficiency of LOD Structure	1.5 mV	0	3
Streak Test, Color	GrnStreak RedStreak BluStreak	Maximum Defect Density Gradient Allowed in a Color Bit Plane (Note 4)	40% 20% 20%	0	Streak Test, Color
MONOCHROME DEVICES					
Point Defect, Dark Field	BPnt33_7	Dark Field, Minor, Short Integration Time	7.5 mV	800	
Point Defect, Dark Field	BPnt33_100	Dark Field, Major, Short Integration Time	100 mV	6	
Point Defect, Dark Field	DfBP_33_200	Dark Field, Major, Short Integration Time	200 mV	0	
Point Defect, Dark Field	BPnt33_500	Dark Field, Major, Short Integration Time	500 mV	0	
Point Defect, Bright Field	Bfld_Pnt_D	Dark Point in an Illuminated Field, Short Integration Time	11%	800	
Point Defect, Bright Field	Bfld_Pnt_B	Bright Point in an Illuminated Field, Short Integration Time	7%	800	

Table 8. SPECIFICATIONS (continued)

Description	Symbol	Definition	Threshold	Maximum Number Allowed	Notes
MONOCHROME DEVICES					
Point Defect, Dark Reference	DR_BPnts	Bright Point in the Dark Reference Region	7.5 mV	0	5
Dim Points, Dark Field	BPnt333_13	Dark Field, Minor, Long Integration Time, t_{INT} = 1/3 s	13 mV	32,500	
Total Points	Bright and Dark Points	BPnt33_7 + Bfld_Pnt_D + Bfld_Pnt_B	−	800	
Cluster Defect	Total_Clst	A Cluster is a Group of 2 or 10 Adjacent Defective Dark or Bright Points	−	6	
Perpendicular Pattern Defect	Total_Perp	Dark Field Very Long Exposure Bright Cluster where 9 or more Adjacent Point Defects Exist, Very Long Integration Time, t_{INT} = 1 s	3.04 mV	0	
Column Defect, Bright Field	Bfld_Col_D Bfld_Col_B	A Column which Deviates above or below Neighboring Columns under Illuminated Conditions (> 300 mV Signal) greater that the Threshold	1.5% 1.5%	0	
Column Defect, Dark Field	Dfld_Col2 Dfld_Col4 Lo_Col_B Lo_Col_D Lo_Col_B1 Lo_Col_D1	A Column which Deviates above or below Neighboring Columns under Non-Illuminated or Low Light Level Conditions (~10 mV) greater than the Threshold	1 mV 1 mV 1 mV 1 mV 1 mV 1 mV	0	 5 5 5 5
Row Defect	Dfld_Row	Row Defect if Row Average Deviates above Threshold	1 mV	0	
LOD Bright Col, Dark	Dfld_LodCol	Defines Functionality and Uniform Efficiency of LOD Structure	1.5 mV	0	

1. This parameter is only a quality metric and these points will not be considered for cluster and point criteria.
2. For the color version of this device, the green pixels in a red row (GR) are considered a different color plane than the green pixels in a blue row (GB). For monochrome version the entire active area is treated as a single color plane.
3. Operating temperature = 60°C.
4. As the gradient threshold is defined as 8.5 mV maximum across a 16 × 16 pixel region about each pixel.
5. Operating temperature = 25°C.

OPERATION

Table 9. ABSOLUTE MAXIMUM RATINGS

Description (Note 9)	**Symbol**	**Minimum**	**Maximum**	**Unit**	**Notes**
Diode Pin Voltages	V_{DIODE}	−17.5	17.5	V	1, 2
Gate Pin Voltages	V_{GATE1}	−13.5	13.5	V	1, 3
Overlapping Gate Voltages	$V_{1−2}$	−13.5	13.5	V	4
Non-Overlapping Gate Voltages	$V_{g−g}$	−13.5	13.5	V	5
V1, V2 − LOD Voltages	VV_{VL}	−13.5	13.5	V	6
Output Bias Current	I_{OUT}	−	−30	mA	7
LODT Diode Voltage	V_{LODT}	−13.0	13.0	V	8
LODB Diode Voltage	V_{LODB}	−18.0	18.0	V	8
Operating Temperature	T_{OP}	−10	70	°C	10
Guaranteed Temperature of Performance	T_{SP}	0	60	°C	11

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to pin SUB.
2. Includes pins: RD, VDD, VSS, and VOUT.
3. Includes pins: V1, V2, H1, H1L, H2, RG, OG.
4. Voltage difference between overlapping gates. Includes: V1 to V2; H1, H1L to H2; H1L to OG; V1 to H2.
5. Voltage difference between non-overlapping gates. Includes: V1 to H1, H1L; V2, OG to H2.
6. Voltage difference between V1 and V2 gates and LODT, LODB diode.
7. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTF.
8. V1, H1, V2, H2, H1L, OG, and RD are tied to 0 V.
9. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.
10. Noise performance will degrade at higher temperatures.
11. See section for Imaging Performance Specifications.

Power-Up Sequence

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (SUB).
2. Supply the appropriate biases and clocks to the remaining pins.

Table 10. DC BIAS OPERATING CONDITIONS

Description	**Symbol**	**Minimum**	**Nominal**	**Maximum**	**Unit**	**Maximum DC Current (mA)**	**Notes**
Reset Drain	RD	11.3	11.5	11.7	V	I_{RD} = 0.01	
Output Amplifier Return	V_{SS}	1.05	1.25	1.45	V	I_{SS} = −3.0	
Output Amplifier Supply	V_{DD}	14.5	15.0	15.5	V	I_{OUT} + I_{SS}	
Substrate	SUB	−	GND	−	V	−0.01	2
Output Gate	OG	−3.0	−2.8	−2.6	V	0.1	
Lateral Drain	LODT, LODB	9.5	9.75	10.0	V	0.2	2
Video Output Current	I_{OUT}	−3	−5	−8	mA	−	1

1. An output load sink must be applied to VOUT to activate output amplifier − see Figure 5.
2. Maximum current expected up to saturation exposure (E_{SAT}).

AC Operating Conditions

Table 11. CLOCK LEVELS

Description	Symbol	Level	Min.	Nom.	Max.	Unit	Effective Capacitance	Notes
V1 Low Level	$V1_L$	Low	−9.5	−9.25	−9.0	V	76 nF	1
V1 High Level	$V1_H$	High	2.4	2.6	2.85	V		1
V2 Low Level	$V2_L$	Low	−9.5	−9.25	−9.0	V	81 nF	1
V2 High Level	$V2_H$	High	2.4	2.6	2.8	V		1
RG, H1, H2, Amplitude	RG_{AMP} $H1_{AMP}$ $H2_{AMP}$	Amplitude	5.5	6.0	6.5	V	RG = 7 pF H1 = 224 pF H2 = 168 pF	1
H1L, Amplitude	$H1L_{AMP}$	Amplitude	7.5	8.0	8.5	V	7 pF	1
H1 Low Level	$H1_{LOW}$	Low	−4.7	−4.5	−4.3	V		1
H1L Low Level	$H1L_{LOW}$	Low	−6.7	−6.5	−6.3	V		
H2 Low Level	$H2_{LOW}$	Low	−5.2	−5.0	−4.8	V		
RG Low Level	RG_{LOW}	Low	1.8	2.0	2.2	V		1

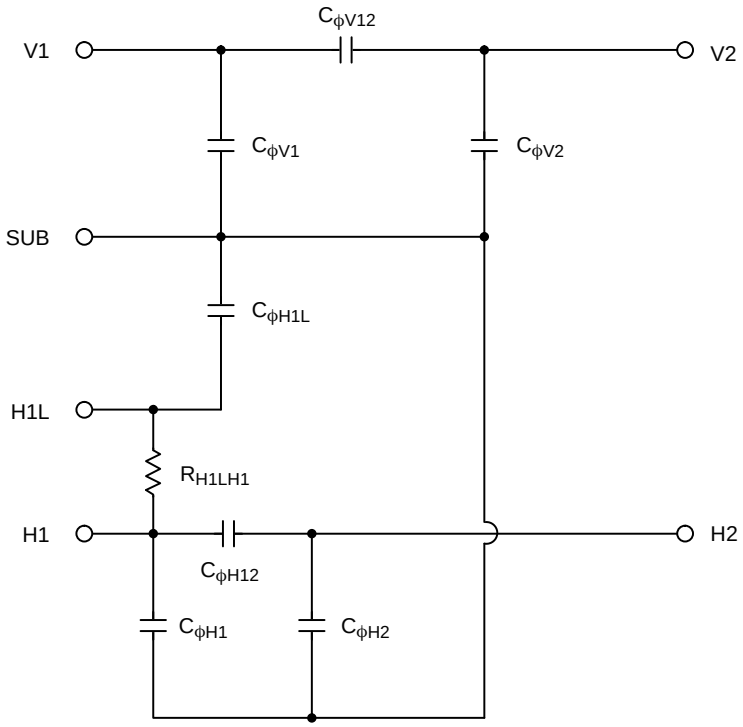
1. All pins draw less than 10 μA DC current. Capacitance values relative to SUB (substrate).

Table 12. CLOCK VOLTAGE DETAIL CHARACTERISTICS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
V1 High-Level Variation	$V1_{HH}$	−	0.50	1.0	V	High-Level Coupling
V2 High-Level Variation	$V2_{HL}$	−	0.28	1.0	V	High-Level Coupling
V2 Low-Level Variation	$V2_{LH}$	−	0.46	1.0	V	Low-Level Coupling
V1 Low-Level Variation	$V1_{LL}$	−	0.14	1.0	V	Low-Level Coupling
V1−V2 Cross-Over	$V1_{CR}$	−2.0	−0.5	1.0	V	Referenced to Ground
H1 High-Level Variation	$H1_{HH}$	−	0.30	1.0	V	
H1 High-Level Variation	$H1_{HL}$	−	0.07	1.0	V	
H1 Low-Level Variation	$H1_{LH}$	−	0.16	1.0	V	
H1 Low-Level Variation	$H1_{LL}$	−	0.25	1.0	V	
H2 High-Level Variation	$H2_{HH}$	−	0.40	1.0	V	
H2 High-Level Variation	$H2_{HL}$	−	0.06	1.0	V	
H2 Low-Level Variation	$H2_{LH}$	−	0.10	1.0	V	
H2 Low-Level Variation	$H2_{LL}$	−	0.27	1.0	V	
H1−H2 Cross-Over	$H1_{CR1}$	−3.0	−1.23	0	V	Rising Side of H1
H1−H2 Cross-Over	$H1_{CR2}$	−3.0	−0.59	0	V	Falling Side of H1
H1L High-Lever Variation	$H1L_{HH}$	−	0.64	1.0	V	
H1L High-Lever Variation	$H1L_{HL}$	−	0.32	1.0	V	
H1L Low-Lever Variation	$H1L_{LH}$	−	0.27	1.0	V	
H1L Low-Lever Variation	$H1L_{LL}$	−	0.23	1.0	V	
H1L−H2 Cross-Over	$H1L_{CR1}$	−1.0	−	−3.0	V	Rising Side of H1L
RG High-Level Variation	RG_{HH}	−	0.19	1.0	V	
RG High-Level Variation	RG_{HL}	−	0.20	1.0	V	
RG Low-Level Variation	RG_{LH}	−	0.11	1.0	V	
RG Low-Level Variation	RG_{LL}	−	0.30	1.0	V	

1. H1, H2 clock frequency: 28 MHz. The maximum and minimum values in this table are supplied for reference. The actual clock levels were measured using the KAF−8300 Evaluation Board. Testing against the device performance specifications is performed using the nominal values.

Capacitance Equivalent Circuit



Notes:
1. The external pin names are actual pins on this image sensor. See the pinout diagram (Figure 6) for more information.
2. The components shown in this schematic model do not correspond to actual components inside the image sensor.

Figure 11. Equivalent Circuit Model

Table 13.

Parameter	Value (Typical)	Unit
$C_{\phi V1}$	61	nF
$C_{\phi V12}$	15	nF
$C_{\phi V2}$	67	nF
$C_{\phi H1}$	153	pF
$C_{\phi H12}$	36	pF
$C_{\phi H2}$	97	pF
$C_{\phi H1L}$	7	pF
R_{H1LH1}	52	kΩ

TIMING

Table 14. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Unit	Notes
H1, H2 Clock Frequency	f_H	−	−	28	MHz	1, 2
V1, V2 Clock Frequency	f_V	−	−	125	kHz	2
Pixel Period (1 Count)	t_e	35.7	−	−	ns	2
H1, H2 Set-up Time	t_{HS}	1	−	−	μs	
H1L−VOUT Delay	t_{HV}	0	3	−	ns	
RG−VOUT Delay	t_{RV}	0	1	−	ns	
Readout Time	$t_{READOUT}$	340.2	−	−	ms	4, 5
Integration Time	t_{INT}	−	−	−		3, 4
Line Time	t_{LINE}	132.2	−	−	ms	4
Flush Time	t_{FLUSH}	21.23	−	−	ms	6

1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Integration time is user specified.
4. Longer times will degrade noise performance.
5. $t_{READOUT} = t_{LINE} \cdot 2574$ lines.
6. See Figure 19 for a detailed description.

Table 15. CLOCK SWITCHING CHARACTERISTICS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
V1 Rise Time	t_{V1r}	−	0.26	1	μs	3
V2 Rise Time	t_{V2r}	−	0.55	1	μs	3
V1 Fall Time	t_{V1f}	−	0.43	1	μs	3
V2 Fall Time	t_{V2f}	−	0.31	1	μs	3
V1 Pulse Width	t_{V1w}	5.0	−	−	μs	4, 5
V2 Pulse Width	t_{V2w}	3.0	−	−	μs	4, 5
H1 Rise Time	t_{H1r}	−	9.0	10	ns	3
H2 Rise Time	t_{H2r}	−	6.9	10	ns	3
H1 Fall Time	t_{H1f}	−	5.8	10	ns	3
H2 Fall Time	t_{H2r}	−	5.4	10	ns	3
H1−H2 Pulse Width	t_{H1w}, t_{H2w}	14	18	22	ns	
H1L Rise Time	t_{H1Lr}	−	1.8	4	ns	3
H1L Fall Time	t_{H1Lf}	−	2.5	4	ns	3
H1L Pulse Width	t_{H1Lw}	14	19	22	ns	
RG Rise Time	t_{RGr}	−	2.0	4	ns	3
RG Fall Time	t_{RGf}	−	2.2	4	ns	3
RG Pulse Width	t_{RGw}	−	6.7	−	ns	2

1. H1, H2 clock frequency: 28 MHz. The maximum and minimum values in this table are supplied for reference. The actual clock timing was measured using the KAF−8300 Evaluation Board. Testing against the device performance specifications is performed using the nominal values.
2. RG should be clocked continuously.
3. Relative to the pulse width (based on 50% of high/low levels).
4. CTE
5. Longer times will degrade noise performance.

Edge Alignment

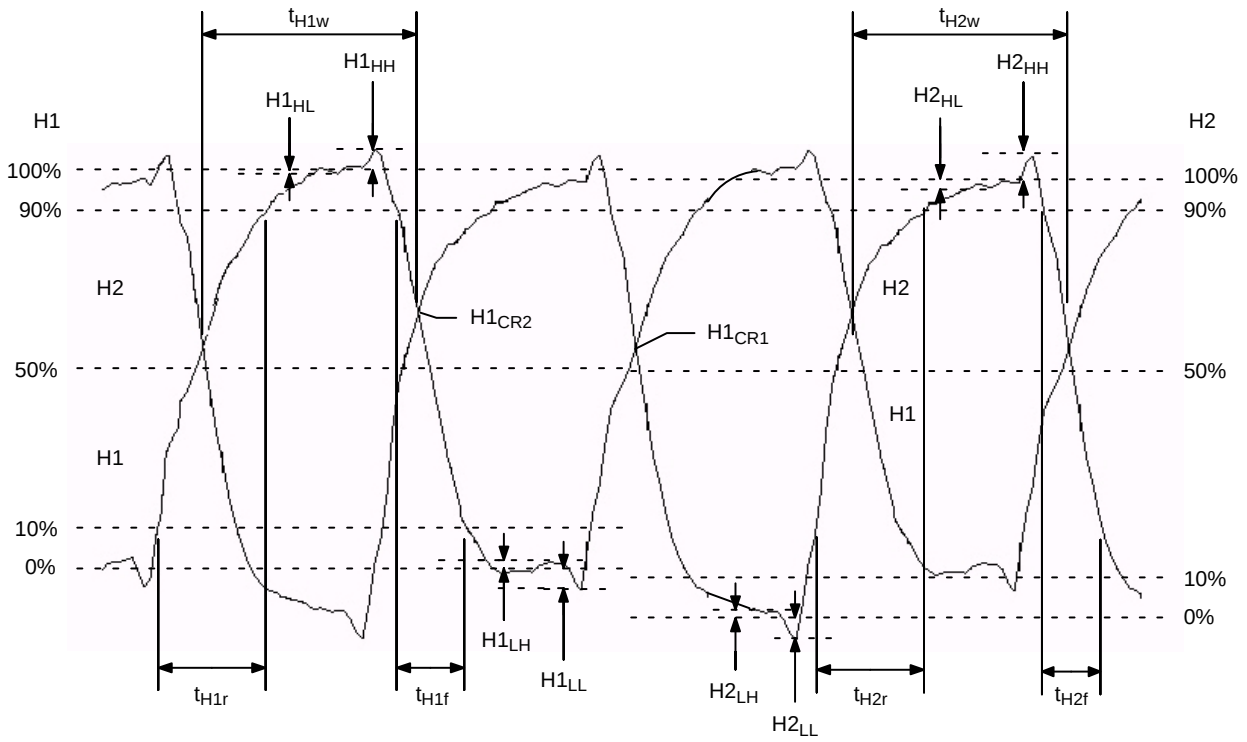


Figure 12. H1 and H2 Edge Alignment

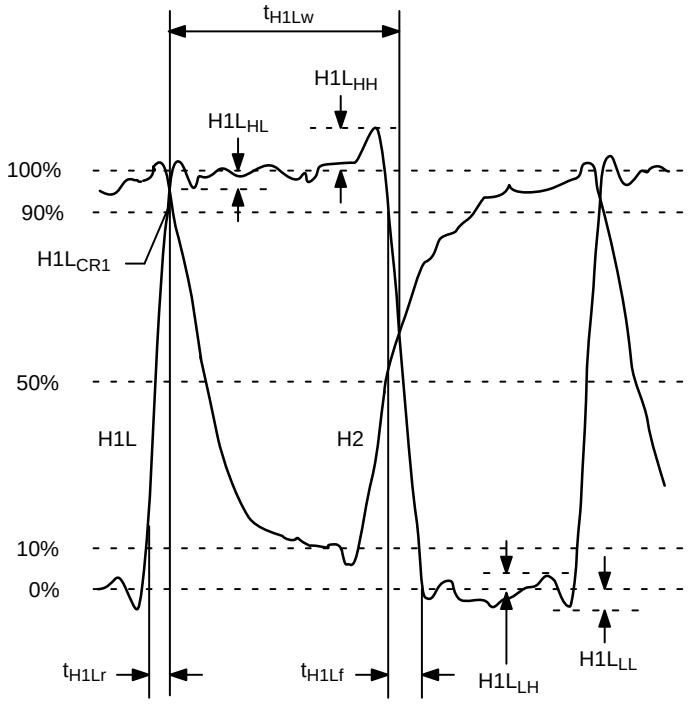


Figure 13. H1L and H2 Edge Alignment

Frame Timing

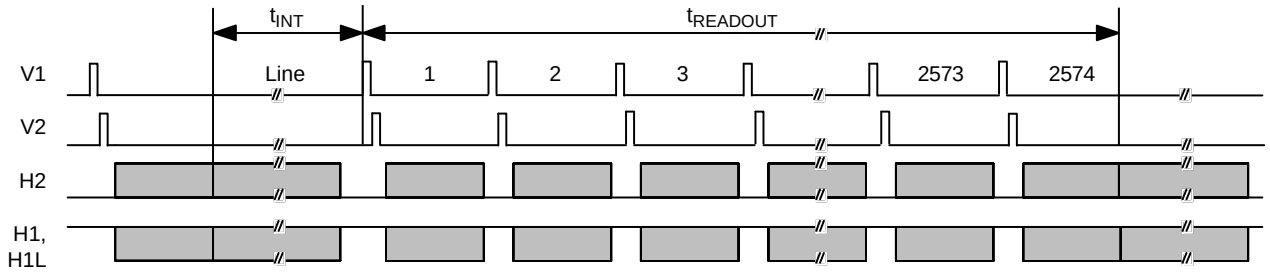


Figure 14. Frame Timing (Minimum)

Frame Timing Detail

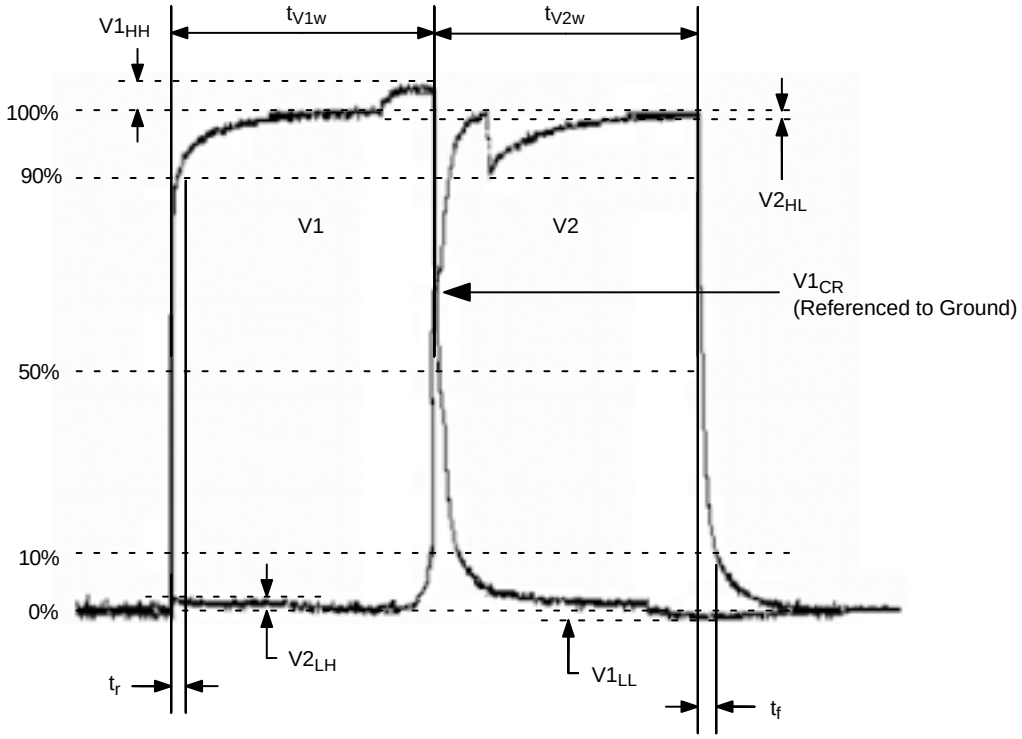
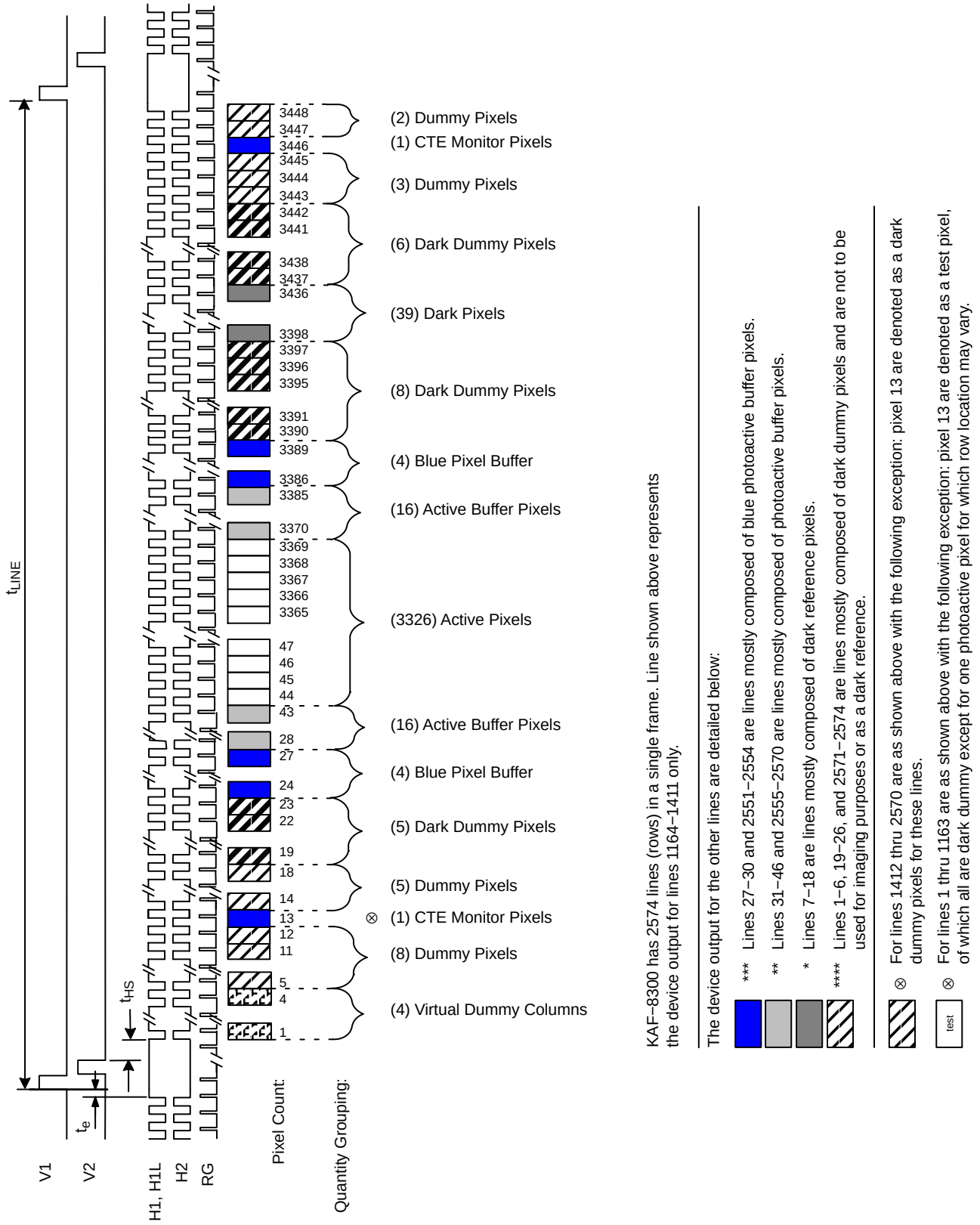


Figure 15. Frame Timing Edge Alignment

Line Timing



NOTE: Schematic reference regions that contain a blue filter represent the color version only; monochrome version is uncoated for these pixels.

Figure 16. Line Timing

Pixel Timing

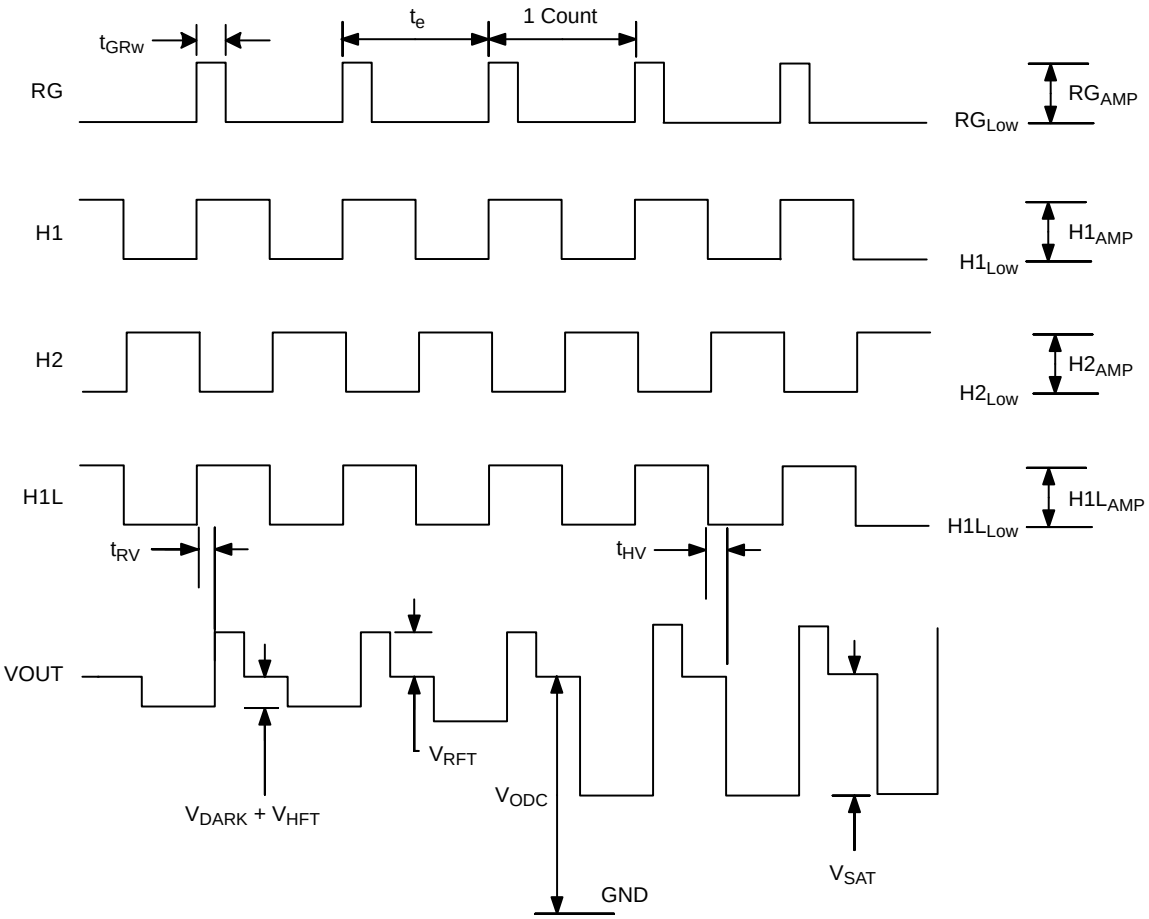


Figure 17. Pixel Timing

Pixel Timing Detail

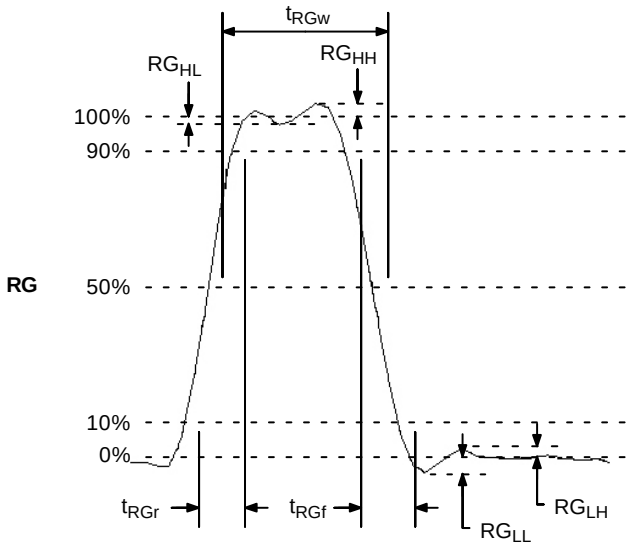


Figure 18. Pixel Timing Detail

MODE OF OPERATION

Power-Up Flush Cycle

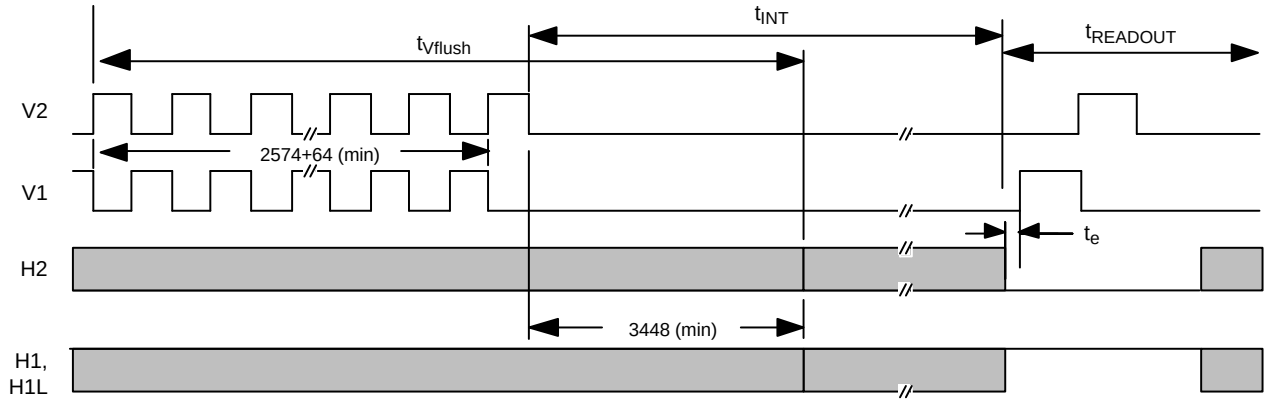


Figure 19. Power-Up Flush Cycle

MECHANICAL INFORMATION

Visual Mechanical Specifications

Table 16. LASER MARK

Item	Description
Device Name	KAF−8300CE, KAF−8300XE, KAF−8300−AXC (Multiple versions available). See Ordering Information section of this document.
Serial Number	nnn −a numeric field containing a maximum of three characters denoting a unique unit identifier for a device from the before mentioned production lot. The start of the sequence starts with “1”. “001” is not a valid marking.

NOTE: All markings shall be readable, consistent in size with no unusual debris left on the package.

Table 17. ASSEMBLY/PACKAGE INTEGRITY

Criteria	Description
Cracks	None allowed.
Corner and Edge Chip-Outs	None − exceeding 0.020″ (0.50 mm).
Chip-Outs Exposing Buried Metal Traces	None allowed.
Chip-Outs, Other	None allowed deeper than 50% of the ceramic layer thickness in which it resides.
Scratches	None − that exceed 0.020″ (0.50 mm) in the major dimension and are deeper than 50% of the ceramic layer thickness in which it resides.
Lead Conditions	No bent, missing, damaged, or short leads. No lead cut-off burrs exceeding 0.005″ (0.13 mm) in the dimension away from the lead.
Internal Appearance and Die Condition	Local Non-Uniformity: Local Non-Uniformity region (LNU) is allowed whose size is not greater than 200 μm^2 within the effective image area. Inspection equipment for these steps are performed using a microscope 7−50X and direct lighting (ring-light). LNU is described as a spot or streak that tends to change from light to dark in appearance as the operator rotates the part under angled lighting conditions. These non-uniformities are not visible or very hard to see under direct lighting. They tend to disappear or become much less visible under higher magnification. Conditions Other than LNU: No scratches, digs, contamination, marks, or blemishes that is attached to the die that touches 9 or more pixels in the effective image area. No loose contamination allowed when viewed at 7X and 50X magnification. No scratches, digs, contamination, marks, or blemishes greater than 10 μm are allowed on the bottom side of the cover glass region that is contained in or extends into the effective image area. Tools used to verify are 7X and 50X magnification.

Table 18. GLASS

Criteria	Description
Tilt	The reject condition is when the glass is incorrectly seated on the package or is not parallel to glass seal area. (“parallel” is defined as 0.25 mm maximum end to end).
Seal	Glass seal must be greater than 50% of the width of the epoxy bond line and must not extend over the ceramic package.
Alignment	There are 4 “+” fiducials on the corners the die that must not be covered by the epoxy light shield. The 4 “+” marks must be in total view when the lid is placed looking directly down on the device with a microscope. All 4 “+” alignment marks are required to be visible in their entirety with a zero clearance tolerance.
Chips	None allowed.
Appearance	No fogged cover allowed.
Contamination	No immobile scratches, digs, contamination, marks, or blemishes are allowed on the cover glass region that is contained in or extends into the effective image area. Within the effective image area, the limit for such conditions is 10 μm or less. This criterion pertains to either the top or the bottom glass surface. Tools used to verify are 7X and 50X magnification.

Completed Assembly

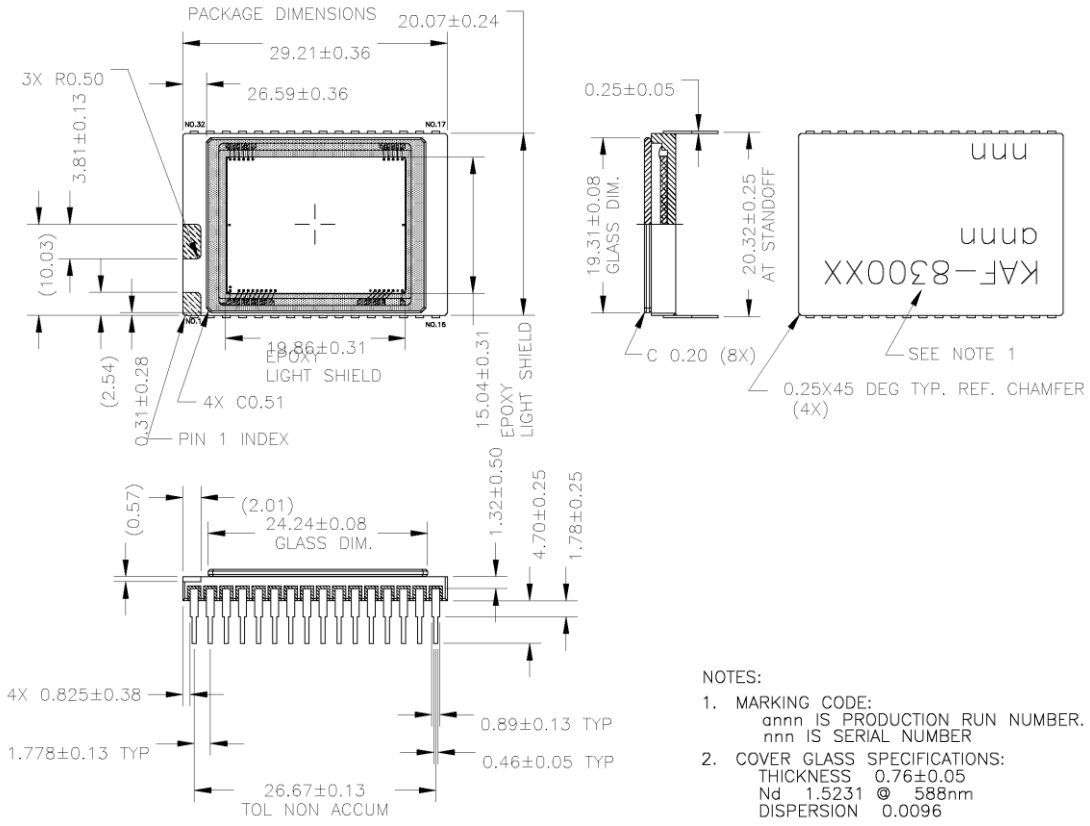
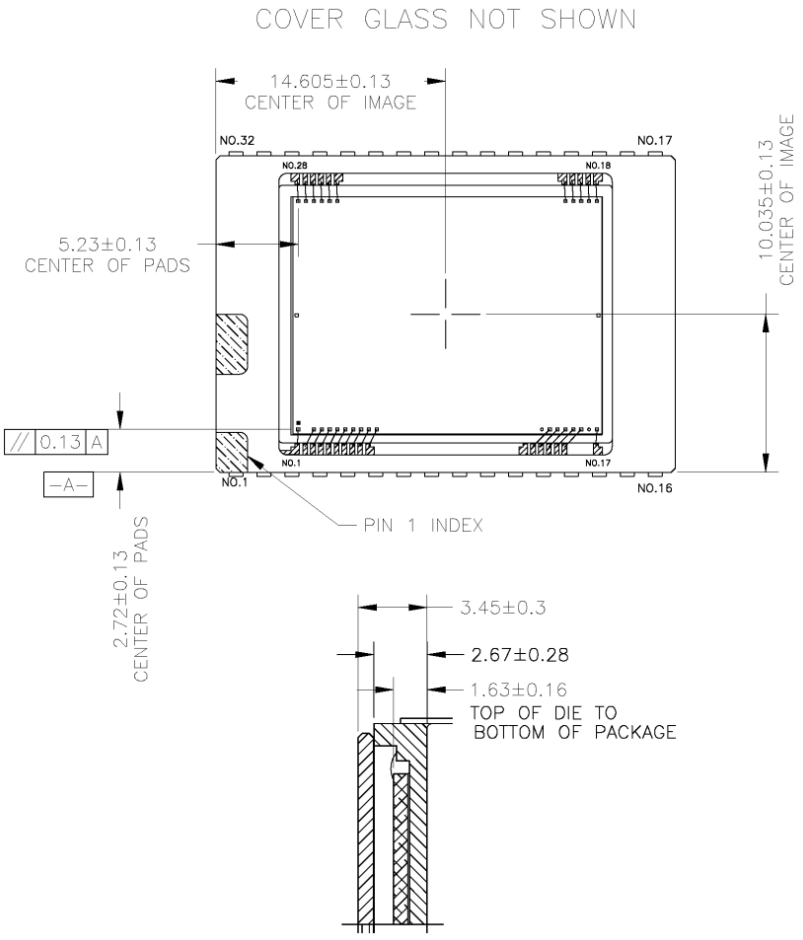


Figure 20. Completed Assembly (1 of 2)



NOTES:
1. CENTER OF IMAGE AREA IS OFFSET FROM CENTER OF PACKAGE BY (0.00,0.00)MM NOMINAL.
2. ANGULAR SPECIFICATION: DIE TO PACKAGE < 1DEGREE.

Figure 21. Completed Assembly (2 of 2)

Cover Glass

Clear Cover Glass, AR Coated (Both Sides) − Specification

1. Scratch and Dig: 10 micron max
2. Substrate Material Schott D263T Eco or Equivalent
3. Multilayer Anti-Reflective Coating

Table 19.

Wavelength	Total Reflectance
420−450	≤ 2%
450−630	≤ 1%
630−680	≤ 2%

Clear Cover Glass − Specification

1. Scratch and Dig: 10 micron max
2. Substrate Material Schott D263T Eco or Equivalent

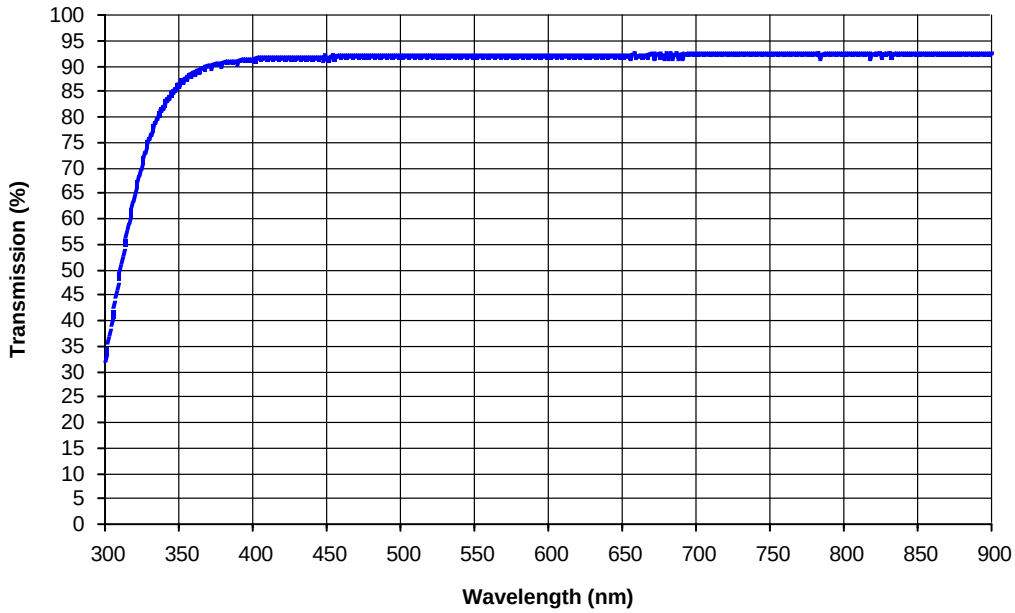


Figure 22. Clear Cover Glass Transmission (Typical)

REFERENCES

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

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