Power Matters.

Spaceflight FPGAs

RTAX™-S/SL

RTAX-DSP

RT-ProASIC®3

RTSX-SU

Microsemi

MICROSEMI 55 YEARS in SPACE 1957-2012

Microsemi®
SoC Products Group

The leader in programmable digital logic integration for spaceflight applications.

Taking Designs from Earth to Outer Space

Whether you're designing for low earth orbit, deep space, or anything in between, **Microsemi's high reliability, low power spaceflight FPGAs are your best choice.** With a history of providing the most reliable, robust, low power flash and antifuse-based FPGAs in the industry, Microsemi offers the best combination of features, performance and radiation tolerance.

Design high speed communications payloads, high resolution sensors and instruments, and flight-critical systems that enable tomorrow's space missions. Only Microsemi can meet the power, size, cost and reliability targets that reduce time-to-launch and minimize cost and schedule risks.

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Please refer to www.microsemi.com/soc and appropriate product datasheets for the latest device information and valid ordering codes.

RTAX-S/SL

Radiation-tolerant FPGA alternative to radiation-hardened ASICs

RTAX-S/SL radiation-tolerant FPGAs offer industry-leading advantages for designers of spaceflight systems. High performance and low power consumption, true single-chip form factor and live-at-power-up operation all combine to make RTAX-S/SL devices the FPGAs of choice for space designers.

- Single event latch-up (SEL) immune to LET_{TH} in excess of 117 MeV-cm^2/mg
- Single event upset (SEU) less than 1E^{-10} errors per bit-day (worst-case geosynchronous orbit)
- Total ionizing dose (TID): 300 Krad functional, 200 Krad parametric
- Pin-compatible commercial devices for easy and inexpensive prototyping
- Ceramic package offerings (CQFP, CCGA, CLGA)
- Prototype units with same footprint and timing as flight units
- Up to 840 user-programmable I/Os
- Screening:
  B Flow: MIL-STD-883B
  E Flow: Microsemi Extended Flow
  V Flow: MIL-PRF-38535 QML Class V

RTAX-S/SL Devices

RTAX-S/SL Devices	RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX4000S/SL
Capacity				
Equivalent System Gates	250,000	1,000,000	2,000,000	4,000,000
Modules				
Register (R-cells)	1,408	6,048	10,752	20,160
Combinatorial (C-cells)	2,816	12,096	21,504	40,320
Embedded RAM/FIFO (without EDAC)				
RAM Blocks	12	36	64	120
RAM (k = 1,024 bits)	54 k	162 k	288 k	540 k
Clocks (segmentable)				
Hardwired	4	4	4	4
Routed	4	4	4	4
I/Os				
I/O Banks	8	8	8	8
User I/Os (maximum)	248	418	684	840
I/O Registers	744	1,548	2,052	2,520
Package Pins CG/LG CQ	 624 208, 352	 624 352	 624, 1152 256, 352	 1272 352

I/Os Per Package

RTAX-S/SL Devices	RTAX250S/SL				RTAX1000S/SL				RTAX2000S/SL				RTAX4000S/SL			
I/O Type	Single-Ended I/Os	Differential I/O Pairs	Non-Adjacent I/O Pairs	Total I/Os	Single-Ended I/Os	Differential I/O Pairs	Non-Adjacent I/O Pairs	Total I/Os	Single-Ended I/Os	Differential I/O Pairs	Non-Adjacent I/O Pairs	Total I/Os	Single-Ended I/Os	Differential I/O Pairs	Non-Adjacent I/O Pairs	Total I/Os
CQ208	7	41	13	115	–	–	–	–	–	–	–	–	–	–	–	–
CQ256	–	–	–	–	–	–	–	–	4	66	0	136	–	–	–	–
CQ352	2	98	0	198	2	98	0	198	2	98	0	198	4	81	0	166
CG624	0	124	0	248	68	170	5	418	52	178	5	418	–	–	–	–
CG1152	–	–	–	–	–	–	–	–	0	342	0	684	–	–	–	–
CG1272	–	–	–	–	–	–	–	–	–	–	–	–	0	420	0	840

Note:
An em dash (–) indicates that the device/package combination is not available.

RTAX-DSP

Industry's most reliable spaceflight FPGAs with DSP capabilities

RTAX-DSP spaceflight FPGAs add embedded radiation-tolerant multiply-accumulate blocks to the tried-and-trusted industry-standard RTAX-S/SL product family. The result is a dramatic increase in device performance and utilization when implementing arithmetic functions, such as those encountered in DSP algorithms, without sacrificing reliability or radiation tolerance. RTAX-DSP integrates complex DSP functions into a single device without any external components for code storage and without multiple-chip implementations for radiation mitigation.

- Highly reliable, nonvolatile antifuse technology
- 2,000,000 to 4,000,000 system gates
- Up to 120 DSP Mathblocks with 125 MHz 18x18 bit multiply-accumulate
- Up to 540 Kbits of embedded memory with optional EDAC protection
- Up to 840 user-programmable I/Os
- RTAX-DL version with low static power
- Total dose: 300 Krad (functional) and 200 Krad (parametric)
- SEU less than $1E^{-10}$ errors per bit-day (worst-case GEO)
- SEL immune to LET_{TH} in excess of 117 MeV-cm^2/mg
- Enhanced SET for R-cells: 0.12 events / RTAX2000D device / 100 years at 120 MHz
- Advanced CCGA and LGA packaging for space applications
- Screening: E-Flow (Microsemi Extended Flow), B-Flow (MIL-STD-883B) and EV-Flow (Class V Flow processing as per MIL-PRF-38535)

RTAX-DSP Devices

RTAX-DSP Devices	RTAX2000D/DL	RTAX4000D/DL
Capacity		
Equivalent System Gates	2,000,000	4,000,000
Modules		
Register (R-cells)	9,856	18,480
Combinatorial (C-cells)	19,712	36,960
Embedded Multiply-Accumulate Blocks		
DSP Mathblocks	64	120
Embedded RAM/FIFO (without EDAC)		
RAM Blocks	64	120
RAM (k=1,024 bits)	288 k	540 k
Clocks (segmentable)		
Hardwired	4	4
Routed	4	4
I/Os		
I/O Banks	8	8
User I/Os (maximum)	684	840
I/O Registers	2,052	2,520
Package Pins CG/LG (DSP)* CQ	 1272 352	 1272 352

Note:
** The body size of the 1272-pin CCGA and LGA packages used on the RTAX-DSP devices is slightly larger than the body size of the 1272-pin CCGA and LGA used on the RTAX4000S/SL devices.*

I/Os Per Package

RTAX-DSP Devices	RTAX2000D	RTAX4000D
CQ352	166	166
CG1272/LG1272	684	840

Note:
The user I/Os include clock buffers.

RT ProASIC3

Low power, reprogrammable FPGAs for space

Radiation-tolerant (RT) ProASIC3 FPGAs are the first to offer designers of spaceflight hardware a radiation-tolerant, reprogrammable, nonvolatile logic integration vehicle. They are intended for low power space applications requiring up to 350 MHz operation and up to 3,000,000 system gates.

- Ceramic column grid array with Six Sigma copper-wrapped lead-tin columns
- Supports single-voltage system operation
- Total ionizing dose: 25 Krad to 30 Krad with less than 10% propagation delay change at standard test dose rate; up to 40 Krad at low dose rate
- Up to 504 Kbits of true dual-port SRAM
- Live-at-power-up (LAPU) level 0 support
- ISP protected with industry standard on-chip 128-bit advanced encryption
- Standard (AES) decryption via JTAG (IEEE 1532–compliant)

RT ProASIC3 Devices

RT ProASIC3 Devices	RT3PE600L	RT3PE3000L
System Gates	600,000	3,000,000
VersaTiles (D-flip-flops)	13,824	75,264
RAM (k = 1,024 bits)	108 k	504 k
RAM Blocks (4,608 bits)	24	112
FlashROM (Kbits)	1	1
Secure (AES) ISP	Yes	Yes
Integrated PLL in CCCs	6	6
VersaNet Globals	18	18
I/O Banks	8	8
Maximum User I/Os	270	620
Package Pins CG/LG CQ	 484 256	 484, 896 256

I/Os Per Package

RT ProASIC3 Devices	RT3PE600L		RT3PE3000L	
I/O Type	Single-Ended I/Os	Differential I/O Pairs	Single-Ended I/Os	Differential I/O Pairs
CG/LG484	270	135	341	168
CG/LG896	–	–	620	310
CQ256	166	82	166	82

RTSX-SU

Flight-proven in space—time after time

RTSX-SU radiation-tolerant FPGAs are enhanced versions of Microsemi's commercial SX-A family of devices, specifically designed for enhanced radiation performance. Featuring SEU-hardened D-type flip-flops that offer the benefits of triple module redundancy (TMR) without requiring cumbersome user intervention, the RTSX-SU family is a unique product offering for space applications.

- 230 MHz system performance (310 MHz internal)
- Very low power consumption (up to 68 µW at standby)
- 3.3 V and 5.0 V mixed voltage
- Configurable I/O support for 3.3 V / 5 V PCI, LVTTL, TTL and CMOS
- Secure programming technology protects against reverse engineering and design theft
- 100% circuit resource utilization with 100% pin locking
- Unique in-system diagnostic and verification capability with Silicon Explorer II
- Low cost prototyping option
- Deterministic, user-controllable timing
- JTAG boundary scan testing in compliance with IEEE Standard 1149.1—dedicated JTAG reset (TRST) pin
- Highly reliable, nonvolatile antifuse technology
- 32,000 to 72,000 ASIC gates (48,000 to 108,000 system gates)
- Up to 360 user-programmable I/Os
- Hermetically-sealed packages for space applications (CQFP, CCGA/CLGA, CCLG)

RTSX-SU Devices

RTSX-SU Devices	RTSX32SU	RTSX72SU
Capacity		
Typical Gates	32,000	72,000
System Gates	48,000	108,000
Logic Modules		
Combinatorial Cells	1,800	4,024
SEU-Hardened Register Cells (D-flip-flops)	1,080	2,012
Maximum Flip-Flops	1,980	4,024
Maximum User I/Os	227	360
Clocks	3	3
Quadrant Clocks	0	4
Speed Grades	Std., –1	Std., –1
Package Pins CQ CG CC	 84, 208, 256 256	 208, 256 624

I/Os Per Package

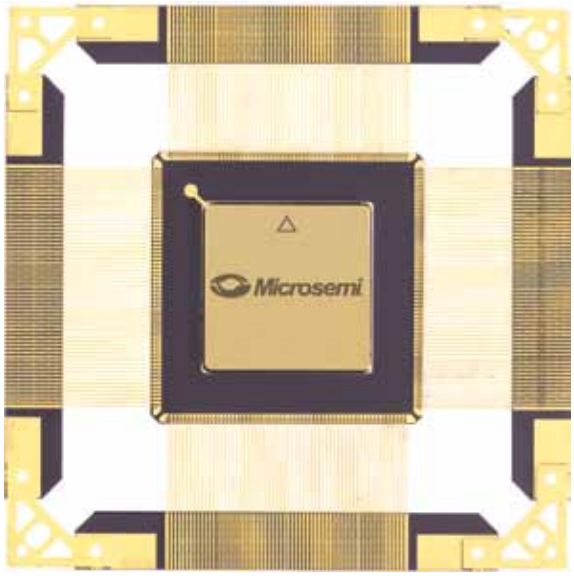
RTSX-SU Devices	RTSX32SU	RTSX72SU
CQ84	62	—
CQ208	173	170
CQ256	227	212
CC256	202	—
CG624	—	360

Note:
The user I/Os include clock buffers.

FPGA Packages

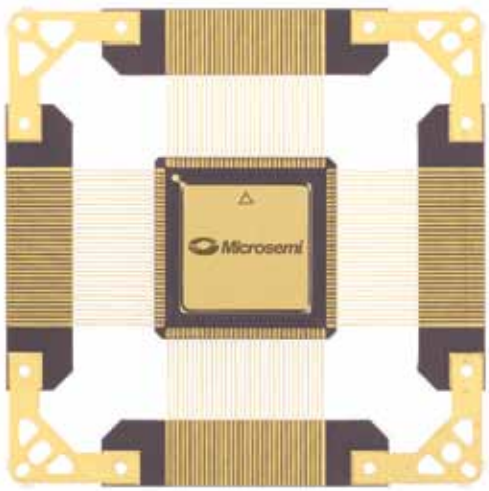
Key: **bs** – package body size excluding leads **h** – package thickness **p** – pin pitch / ball pitch Chips shown at actual size.

CQ352 **b.s.** 1.890x1.890" (48.00x48.00 mm)
h. 105 mils (2.67 mm) **p.** 20 mils (0.50 mm)

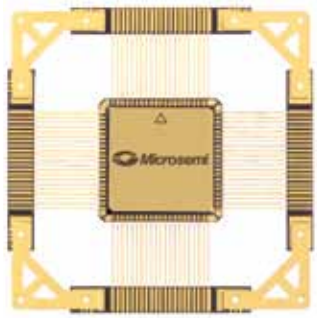


CQ256 **b.s.** 1.417x1.417" (36.00x36.00 mm)
h. 105 mils (2.67 mm) **p.** 20 mils (0.50 mm)

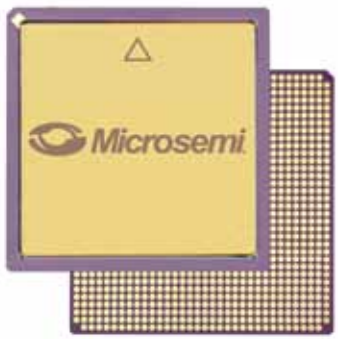
CQ172 **b.s.** 1.18x1.18" (29.972x29.972 mm)
h. 105 mils (2.67 mm) **p.** 25 mils (0.64 mm)



CQ132 **b.s.** 0.95x0.95" (24.13x24.13 mm)
h. 105 mils (2.67 mm) **p.** 25 mils (0.64 mm)

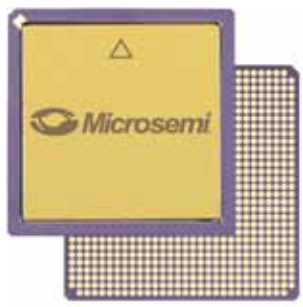


CQ84 **b.s.** 0.65x0.65" (16.51x16.51 mm)
h. 90 mils (2.29 mm) **p.** 25 mils (0.64 mm)



CG1152/LG1152
RTAX2000S and
RTAX2000SL only

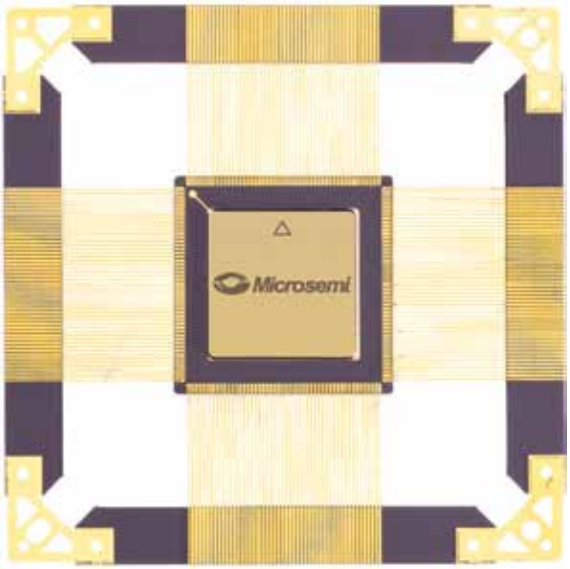
b.s.1.378x1.378"
(35.00x35.00 mm)
h. CCGA – 218 mils
(5.535 mm)
h. LGA – 129 mils
(3.28 mm)
p. 39 mils
(1.00 mm)



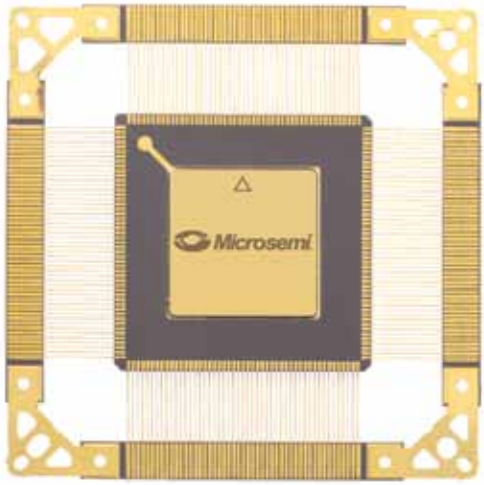
CG896/LG896

b.s. 1.220x1.220"
(31.00x31.00 mm)
h. CCGA – 218 mils
(5.535 mm)
h. LGA – 129 mils
(3.28 mm)
p. 39 mils
(1.00 mm)

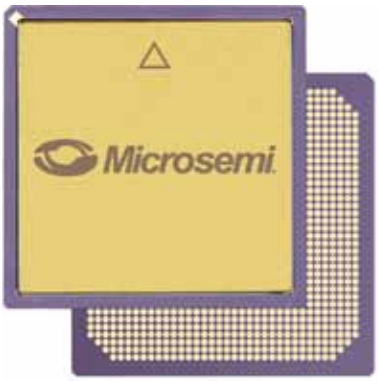
The **b.s.** dimension is the nominal package body dimension, exclusive of leads. For more information concerning package dimensions, refer to the ***Microsemi Package Mechanical Drawings*** document located at www.microsemi.com/soc/documents/PckgMechDrwngs.pdf.



CQ208 **b.s.** 1.15x1.15" (29.21x29.21 mm)
h. 105 mils (2.67 mm) **p.** 20 mils (0.50 mm)



CQ196 **b.s.** 1.35x1.35" (34.29x34.29 mm)
h. 105 mils (2.67 mm) **p.** 25 mils (0.64 mm)



CGD1272/LGD1272

RTAX2000D and
RTAX4000D only

b.s. TBD
h. TBD
h. TBD
p. TBD

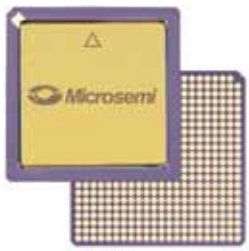
CG1272/LG1272

RTAX4000S and
RTAX4000SL only

b.s. 1.457x1.457"
(37.00x37.00 mm)
h. CCGA – 218 mils
(5.535 mm)
h. CLGA – 129 mils
(3.28 mm)
p. 39 mils
(1.00 mm)

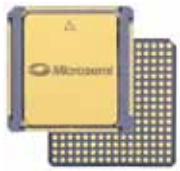
CG624/LG624

b.s. 1.27x1.27"
(32.50x32.50 mm)
h. CCGA – 194 mils
(4.94 mm)
h. LGA – 90 mils
(2.30 mm)
p. 50 mils
(1.27 mm)



CG484/LG484

b.s. 0.91x0.91"
(23.00x23.00 mm)
h. CCGA – 225 mils
(5.72 mm)
h. LGA – 138 mils
(3.51 mm)
p. 7.5 mils
(0.19 mm)



CC256

b.s. 0.67x0.67"
(17.00x17.00 mm)
h. 72 mils
(1.847 mm)
p. 7.5 mils
(0.19 mm)

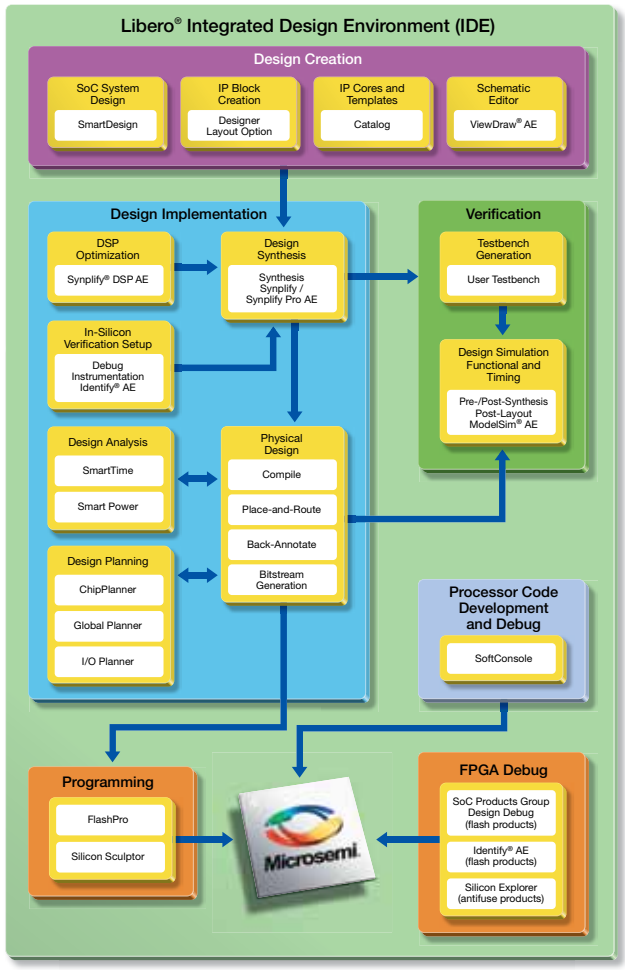
Design Environment for Microsemi System Critical Devices

Microsemi system critical FPGAs are fully supported by Microsemi's Libero® Integrated Design Environment (IDE) software. Libero IDE is an integrated design manager that integrates design tools while guiding the user through the design flow, managing all design and log files and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify Pro® AE from Synopsys,® ModelSim® HDL Simulator from Mentor Graphics and Designer design implementation software from Microsemi.

Designer software includes sophisticated place-and-route features plus a comprehensive suite of backend support tools for timing constraints, timing and power analysis, I/O attribute and pin assignment, and much more.

Microsemi's SmartDesign tool simplifies the use of Microsemi's IP in user designs as well as offering a simple way to build on-chip processors with custom peripherals. Most Microsemi IP cores are now included by default in Libero IDE as either obfuscated or RTL versions, depending on the license selected.

For embedded designers, Microsemi offers FREE SoftConsole Eclipse-based IDE for use with ARM® Cortex™-M1 and Cortex-M3, and Core8051s as well as evaluation versions from Keil™ and IAR Systems.® Full versions are available from the respective suppliers.



FPGA Design Support

Libero IDE Licenses		Gold (FREE)	Platinum	Platinum Evaluation	Standalone
Device Support	All families	Up to 1,500,000 gates	All devices	All devices	All devices
Microsemi IP		Obfuscated	RTL	Obfuscated	RTL
Synthesis	Synplify® Pro AE	x	x	x	
Simulation	ModelSim® AE	x	x	x	
Debug	Identify® AE	x	x	x	
	Microsemi Debug	x	x	x	x
Program File		x	x		

Operating System Support*

Tool	Libero IDE	SoftConsole	Keil	IAR	FlashPro	FlashPro USB Driver
Windows® XP Professional	Now	Now	Now	Now	Now	Now (32-bit and 64-bit)
Windows Vista Business	Now	Now	Now	Now	Now	Now (32-bit and 64-bit)
Windows 7 Professional	Now	Now	Now	Now	Now	Now (32-bit and 64-bit)
RedHat Linux® WS 4.0	Now	N/A	N/A	N/A	N/A	N/A
RedHat Linux WS 5.0	Now	N/A	N/A	N/A	N/A	N/A
RedHat Linux WS 5.2	Now	N/A	N/A	N/A	N/A	N/A

Note:
** FPGA programming is only supported in Windows XP Pro, Windows Vista, and Windows 7.*

Intellectual Property Cores for System Critical FPGAs

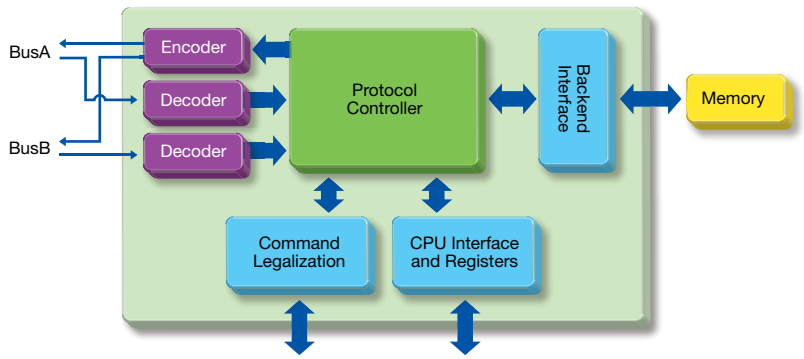
Microsemi has more than 180 intellectual property (IP) products designed and optimized to support communications, consumer, military, industrial, automotive and aerospace markets. Microsemi IP solutions streamline your designs, enable faster time-to-market and minimize design costs and risk. You can access Microsemi IP cores through the Microsemi Libero IDE suite of development tools via the SmartDesign IP design interface. Many Microsemi cores feature firmware drivers accessible through the Firmware Catalog tool. Integrated solutions are also available, featuring Microsemi IP and highlighting the advantages of Microsemi's intrinsically low power FPGAs. A few key IP cores for system critical applications are shown below, and you can view the entire library of cores at www.microsemi.com/soc.

MIL-STD-1553B IP Cores

MIL-STD-1553 is a command/response, dual-redundant, time-multiplexed serial data bus used in severe environments. Microsemi Core1553 IP cores provide robust, fully tested MIL-STD-1553A and B implementations that are compatible with legacy 1553 solutions. Microsemi provides everything needed to incorporate one or more 1553B cores into a system design. Core1553BRM, Core1553BRT, Core1553BRT-EBR and Core1553BBC are available.

Core1553BRM

- **Compliant to MIL-STD-1553A and B**
- **Bus Controller (BC), Remote Terminal (RT) and Monitor Terminal (MT)**
- **Simultaneous RT/MT operation**
- **12, 16, 20 or 24 MHz clock operation**
- **Built-in test capability**
- **Advanced RT functions**
- **Sophisticated BC reduces host overhead**
- **Interfaces to standard transceivers**
- **Redundancy for severe environments**
- **Low power operation**

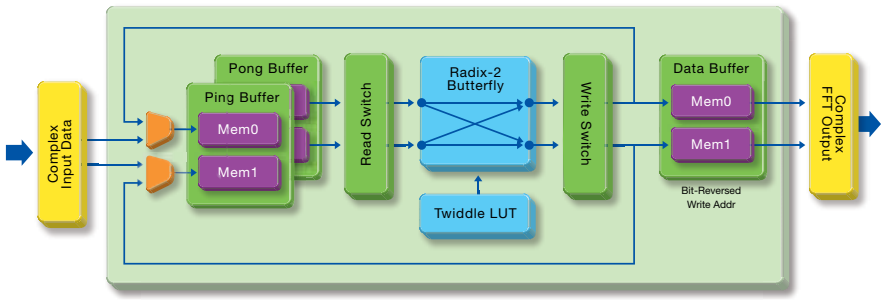


Digital Signal Processing IP Cores

Microsemi digital signal processing (DSP) cores deliver digital filtering and signal processing capabilities. Cores taking advantage of on-chip multiplier blocks in Microsemi's new RTAX-DSP devices offer outstanding performance in spaceflight applications.

CoreFFT

- **Highly parameterizable DirectCore RTL generator optimized for the RTAX-DSP family supports forward and inverse complex FFT**
- **Transforms sizes from 32 to 8,192 points**
- **8 to 32 bits I/O real and imaginary data and twiddle coefficients**
- **Two's complement I/O data**
- **Bit-reversed or natural output order**
- **Selection of unconditional or conditional block floating point scaling**
- **Embedded RAM-block-based twiddle LUT**
- **Built-in memory buffers with optional extensive or minimal memory buffering configurations**
- **Handshake signals to facilitate easy interface to user circuitry**



Buffered FFT Block Diagram

CoreFIR

- **Highly parameterizable DirectCore RTL generator optimized for the RTAX-DSP family implements a range of filter types, including single rate fully enumerated (parallel), single rate folded (semi-parallel) filter and multi-rate polyphase interpolation FIR filter**
- **Performance up to 124 MHz**
- **Supports up to 1,024 FIR filter taps**
- **Run-time reloadable coefficients, multiple coefficient sets, or fixed coefficients**
- **2-bit to 18-bit input data and coefficient precision**
- **Signed or unsigned data and coefficients**
- **Full precision output**
- **Coefficient symmetry optimization (on the fully enumerated filters)**

Prototyping Flows

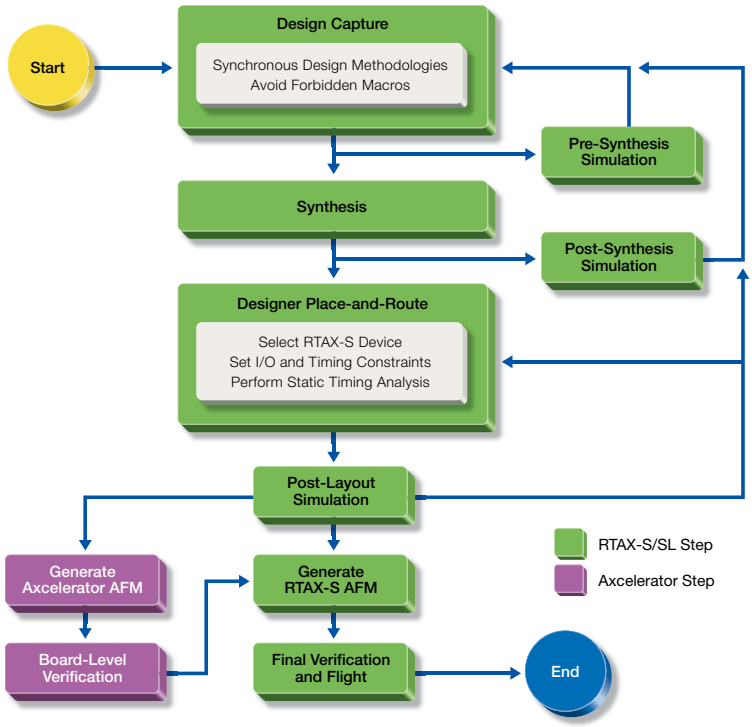
With the introduction of Microsemi's RTAX-S/SL devices, designers now have access to the most powerful FPGAs available for aerospace and radiation-intensive applications. Prototype verification is an important step in system integration where accurate behavioral simulation and static timing analysis are crucial. Since the enhanced radiation characteristics of radiation-tolerant devices are not required during the prototyping phase of the design, Microsemi has developed various prototyping options for RTAX-S/SL for early design development and functional verification.

Prototyping with Axcelerator Units

The prototyping solution using the commercial Axcelerator devices consists of two parts:

- **A well-documented design flow that allows the customer to target an RTAX-S/SL design to the equivalent commercial Axcelerator device**
- **A set of Microsemi Extender circuit boards that map the commercial device package to the appropriate RTAX-S/SL package footprint**

This methodology provides the user with a cost-effective solution while maintaining the short time-to-market associated with Microsemi FPGAs.



Prototyping with RTAX-S/SL/DSP or RTSX-SU PROTO Units

The RTAX-S/SL/DSP or RTSX-SU PROTO units offer a prototyping solution that can be used for final timing verification of the flight design. The RTAX-S/SL/DSP or RTSX-SU PROTO prototype units have the same timing attributes as the RTAX-S/SL/DSP or RTSX-SU flight units. Prototype units are offered in non-hermetic ceramic packages. The prototype units include "PROTO" in their part number, and "PROTO" is marked on devices to indicate that they are not intended for space flight. They also are not intended for applications that require the quality of spaceflight units, such as qualification of spaceflight hardware. RT-PROTO units offer no guarantee of hermeticity, and no MIL-STD-883B processing. At a minimum, users should plan on using class B level devices for all qualification activities. The RT-PROTO units are electrically tested in a manner to guarantee their performance over the full military temperature range. The RT-PROTO units will also be offered in –1 or standard speed grades, so as to enable customers to validate the timing attributes of their space designs using actual flight silicon.

RTAX-S/SL Prototyping with Flash Devices

Aldec's RTAX-S/SL prototyping solution allows customers to take advantage of Microsemi's flash-based reprogrammable ProASIC3 devices. Aldec provides software that remaps antifuse primitives to flash, which reduces design time and cost. In addition, the hardware adapter is footprint compatible with RTAX-S/SL; therefore, a customer does not need to redesign a new board for prototyping.

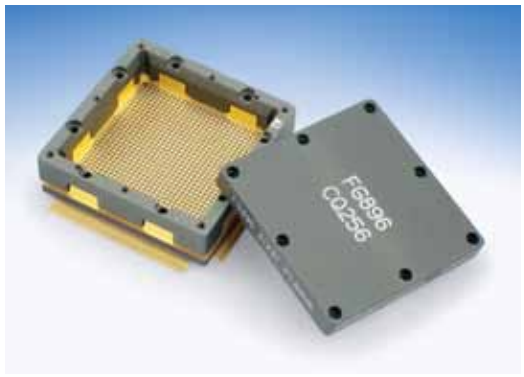
Package Prototyping Solutions

Microsemi has developed multiple low-cost prototyping solutions for RTAX-S/SL devices that ultimately are packaged in CQFP or CCGA for the production system. These solutions utilize Axcelerator family Fine Pitch Ball Grid Array (FBGA) or Ceramic Land Grid Array (CLGA) packages as prototyping vehicles:

- **CQFP to FBGA adapter socket**
- **CQFP to CLGA adapter socket**
- **CCGA to FBGA adapter socket**
- **CCGA to CLGA adapter socket**

The CQFP to FBGA adapter sockets have an FBGA configuration on the top and a CQFP configuration on the bottom. The adapter sockets enable customers to use a commercial Axcelerator FG package during prototyping, and then switch to an equivalent CQ256 or CQ352 package for production.

Adapter Socket	Ordering Part Number	Prototyped and Prototype Device
CQ352 to FG484	SK-AX250-CQ352RTFG484S	For prototyping RTAX250S/L-CQ352 or AX250-CQ352 using AX250-FG484 package
CQ352 to FG896	SK-AX1-AX2-KITTOP and SK-AX1-CQ352-KITBTM	For prototyping RTAX1000S/L-CQ352 or AX1000-CQ352 using AX1000-FG896 package
CQ352 to FG896	SK-AX1-AX2-KITTOP and SK-AX2-CQ352-KITBTM	For prototyping RTAX2000S/L-CQ352 or AX2000-CQ352 using AX2000-FG896 package
CQ256 to FG896	SH-AX2-CQ256-KITTOP and SK-AX2-CQ256-KITBTM	For prototyping RTAX2000S/L-CQ352 or AX2000-CQ256 using AX2000-FG896 package
CG624 to FG484	SK-SX72-CG624RTFG484	For prototyping RTSX72SU-CG624 or A54SX72A-CG624 using A54SX72A-FG484 package
CG624 to FG896	SK-AX1-AX2-KITTOP and SK-AX1-CG624-KITBTM	For prototyping RTAX1000S-CG624, RTAX1000SL-CG624, or AX1000-CG624 using AX1000-FG896 package
CG624 to FG896	SK-AX1-AX2-KITTOP and SK-AX2-CG624-KITBTM	For prototyping RTAX2000S-CG624, RTAX2000SL-CG624, or AX2000-CG624 using AX2000-FG896 package

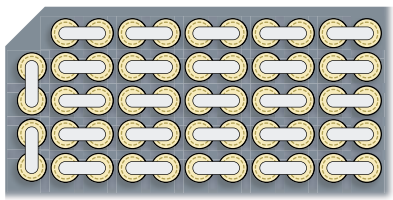


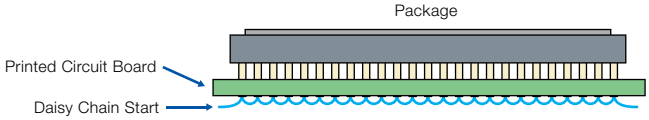
RTAX2000S CQ256 to FG896 Ceramic Adapter, Top and Bottom

Daisy-Chained Packages

To facilitate the qualification of target FPGA device socket and board assembly practices without using costly flight-quality parts, Microsemi offers certain Ceramic Column Grid Array (CCGA) and Ceramic Land Grid Array (CLGA) packages with adjacent pairs of pins tied together. By assembling these packages onto a qualification PC board that is laid out with adjacent pairs of solder pads tied together but offset by one pin as compared to the package, a single signal can be fed into one pin of the package and routed into and out of the entire package in a serial daisy chain fashion so all pins of the package are used. This is useful for performing continuity and impedance tests to validate board assembly techniques with surface-mount grid array packages. Microsemi's daisy chain packages feature metal routing tracks between adjacent pairs of package pins, internal to the package. For package qualification, an unbonded silicon die is included in the package.

Microsemi Part Number	Description
LG624 DAISY CHAIN-1	624-pin CLGA mechanical package
LG1152 DAISY CHAIN	1152-pin CLGA mechanical package
LG1272 DAISY CHAIN	1272-pin CLGA mechanical package
CG484 DAISY CHAIN	484-pin CCGA mechanical package
CG624 DAISY CHAIN SIX	624-pin CCGA mechanical package
CG896 DAISY CHAIN	896-pin CCGA mechanical package
CG1152 DAISY CHAIN	1152-pin CCGA mechanical package
CG1272 DAISY CHAIN	1272-pin CCGA mechanical package


Partial View of 624 CGA with Adjacent Pin Pairs Tied Together



All Pins are Connected Serially

Device Programming

Silicon Sculptor 3

The Silicon Sculptor 3 programmer, which supports both antifuse and flash FPGAs, delivers high data throughput and promotes ease of use, while lowering the overall cost of ownership. The Silicon Sculptor 3 programmer includes a high-speed USB 2.0 interface that enables customers to connect as many as 12 programmers to a single PC. This enables an easily expandable, low to medium volume production programming system to be dynamically assembled. Through the use of universal Microsemi socket adapters, the Silicon Sculptor 3 device programs all Microsemi packages, including PLCC, PQFP, VQFP, TQFP, QFN, PBGA, FBGA, CSP, CPGA, CQFP, CCGA, and CLGA.

FlashPro4

The FlashPro4 programmer for flash FPGAs utilizes a JTAG interface, where a single JTAG chain can be used for multiple Microsemi flash devices on a JTAG chain. In-system programming using the JTAG port adds the flexibility of field upgrades or post-assembly production-line characterization. Production costs are significantly reduced as a result of elimination of expensive sockets on the board.

All FlashPro programmers use JEDEC-standard STAPL files, meaning there are no algorithms built into the software. The FlashPro software and user interface support FlashPro4 and FlashPro Lite programmers, so you do not have to learn new software to switch from one hardware programmer to another.

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55700043-6/4.12 MS2-003-12

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