

# DATA SHEET

## **74LVC273**

Octal D-type flip-flop with reset;  
positive-edge trigger

Product specification  
Supersedes data of 1996 Jun 06  
IC24 Data Handbook

1998 May 20

## Octal D-type flip-flop with reset; positive-edge trigger

74LVC273

## FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Conforms to JEDEC standard 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

## DESCRIPTION

The 74LVC273 is a low-voltage Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC273 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ( $\overline{MR}$ ) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the MR input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

## QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay CP to Qn; MR to Qn	$C_L = 50\text{pF}$ $V_{CC} = 3.3\text{V}$	6.0 6.0	ns
$f_{max}$	Maximum clock frequency		230	MHz
$C_I$	Input capacitance		5.0	pF
$C_{PD}$	Power dissipation capacitance per flip-flop	$V_I = \text{GND to } V_{CC}^1$	22	pF

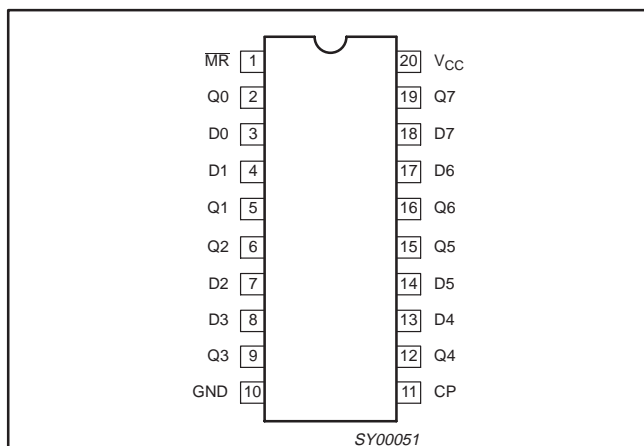
## NOTE:

- <sup>1</sup>  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SO	-40°C to +85°C	74LVC273 D	74LVC273 D	SOT163-1
20-Pin Plastic SSOP Type II	-40°C to +85°C	74LVC273 DB	74LVC273 DB	SOT339-1
20-Pin Plastic TSSOP Type I	-40°C to +85°C	74LVC273 PW	74LVC273PW DH	SOT360-1

## PIN CONFIGURATION



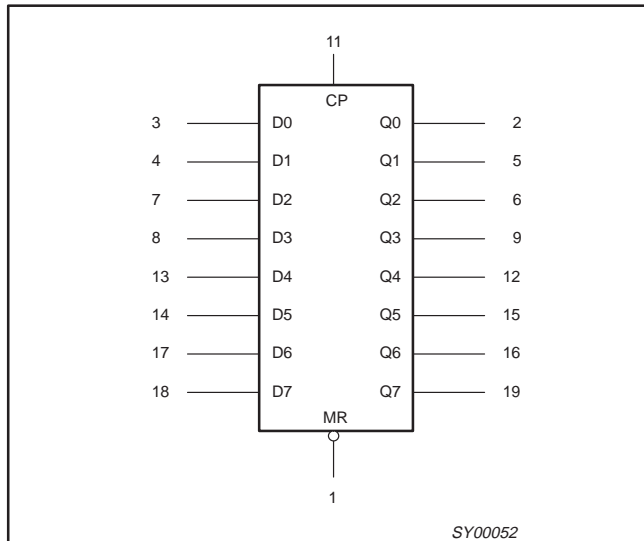
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{MR}$	Master reset input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 – Q7	Flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 – D7	Data inputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	$V_{CC}$	Positive power supply

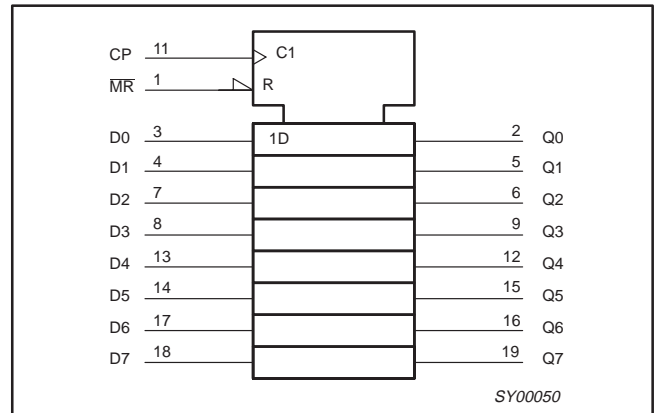
# Octal D-type flip-flop with reset; positive-edge trigger

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### LOGIC SYMBOL



### IEEE/IEC LOGIC SYMBOL



### FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUT
	MR	CP	Dn	Q0 – Q7
Reset (clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
- L = LOW voltage level
- l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
- ↑ = LOW-to-HIGH transition
- X = Don't care

### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V <sub>CC</sub>	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V <sub>I</sub>	DC Input voltage range		0	5.5	V
V <sub>I/O</sub>	DC Input voltage range for I/Os		0	V <sub>CC</sub>	V
V <sub>O</sub>	DC output voltage range		0	V <sub>CC</sub>	V
T <sub>amb</sub>	Operating free-air temperature range		-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	Input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7V	0	20	ns/V
		V <sub>CC</sub> = 2.7 to 3.6V	0	10	

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**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +6.5	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage	Note 2	-0.5 to +5.5	V
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	$\pm 50$	mA
$V_O$	DC output voltage	Note 2	-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	$\pm 50$	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		$\pm 100$	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K	500	mW
		above +60°C derate linearly with 5.5 mW/K	500	

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
$V_{IH}$	HIGH level Input voltage	$V_{CC} = 1.2V$	$V_{CC}$			V
		$V_{CC} = 2.7$ to $3.6V$	2.0			
$V_{IL}$	LOW level Input voltage	$V_{CC} = 1.2V$			GND	V
		$V_{CC} = 2.7$ to $3.6V$			0.8	
$V_{OH}$	HIGH level output voltage	$V_{CC} = 2.7V; V_I = V_{IH}$ or $V_{IL}; I_O = -12mA$	$V_{CC} - 0.5$			V
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = -100\mu A$	$V_{CC} - 0.2$	$V_{CC}$		
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = -12mA$	$V_{CC} - 0.6$			
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = -24mA$	$V_{CC} - 1.0$			
$V_{OL}$	LOW level output voltage	$V_{CC} = 2.7V; V_I = V_{IH}$ or $V_{IL}; I_O = 12mA$			0.40	V
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$			0.20	
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 24mA$			0.55	
$I_I$	Input leakage current	$V_{CC} = 3.6V; V_I = 5.5V$ or GND		$\pm 0.1$	$\pm 5$	$\mu A$
$I_{OZ}$	3-State output OFF-state current	$V_{CC} = 3.6V; V_I = V_{IH}$ or $V_{IL}; V_O = V_{CC}$ or GND		0.1	$\pm 10$	$\mu A$
$I_{CC}$	Quiescent supply current	$V_{CC} = 3.6V; V_I = V_{CC}$ or GND; $I_O = 0$		0.1	10	$\mu A$
$\Delta I_{CC}$	Additional quiescent supply current	$V_{CC} = 2.7V$ to $3.6V; V_I = V_{CC} - 0.6V; I_O = 0$		5	500	$\mu A$

**NOTE:**

- All typical values are at  $V_{CC} = 3.3V$  and  $T_{amb} = 25^\circ C$ .

# Octal D-type flip-flop with reset; positive-edge trigger

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### AC CHARACTERISTICS

GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$			
			MIN	TYP <sup>1</sup>	MAX	MIN	TYP	MAX	
$t_{PHL}$ $t_{PLH}$	Propagation delay CP to Qn	1		6.0	10.2		6.6	11.2	ns
$t_{PHL}$	Propagation delay MR to Qn	2		6.3	11.0		7.4	12.0	ns
$t_W$	Clock pulse width HIGH or LOW	1	4	1.2		5	1.8		ns
$t_W$	Master reset pulse width LOW	2	4	1.2		5	1.7		ns
$t_{\text{rem}}$	Removal time MR to CP	2	2	-1.0		3	-1.0		ns
$t_{\text{su}}$	Set-up time D <sub>n</sub> to CP	3	2	0.7		3	1.0		ns
$t_h$	Hold time D <sub>n</sub> to CP	3	0	-0.6		0	-0.9		ns
$f_{\text{max}}$	Maximum clock pulse frequency	1	125			100			MHz

**NOTE:**

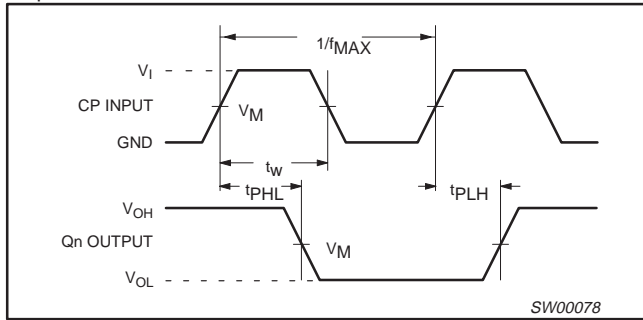
1. These typical values are at  $V_{CC} = 3.3V$  and  $T_{\text{amb}} = 25^\circ\text{C}$ .

### AC WAVEFORMS

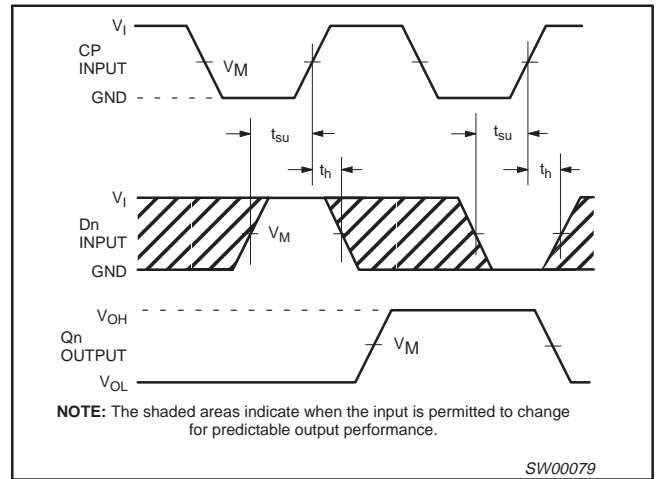
$V_M = 1.5V$  at  $V_{CC} \geq 2.7V$ .

$V_M = 0.5 V_{CC}$  at  $V_{CC} < 2.7V$ .

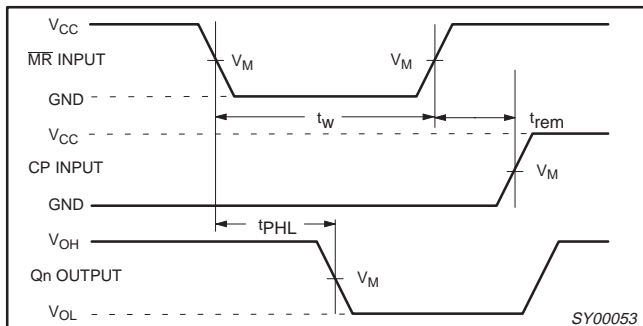
$V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.



**Waveform 1. Clock (CP) to output (Q<sub>n</sub>) propagation delays, the clock pulse width and the maximum clock pulse frequency**



**Waveform 3. Data set-up and hold times for the data input (D<sub>n</sub>)**

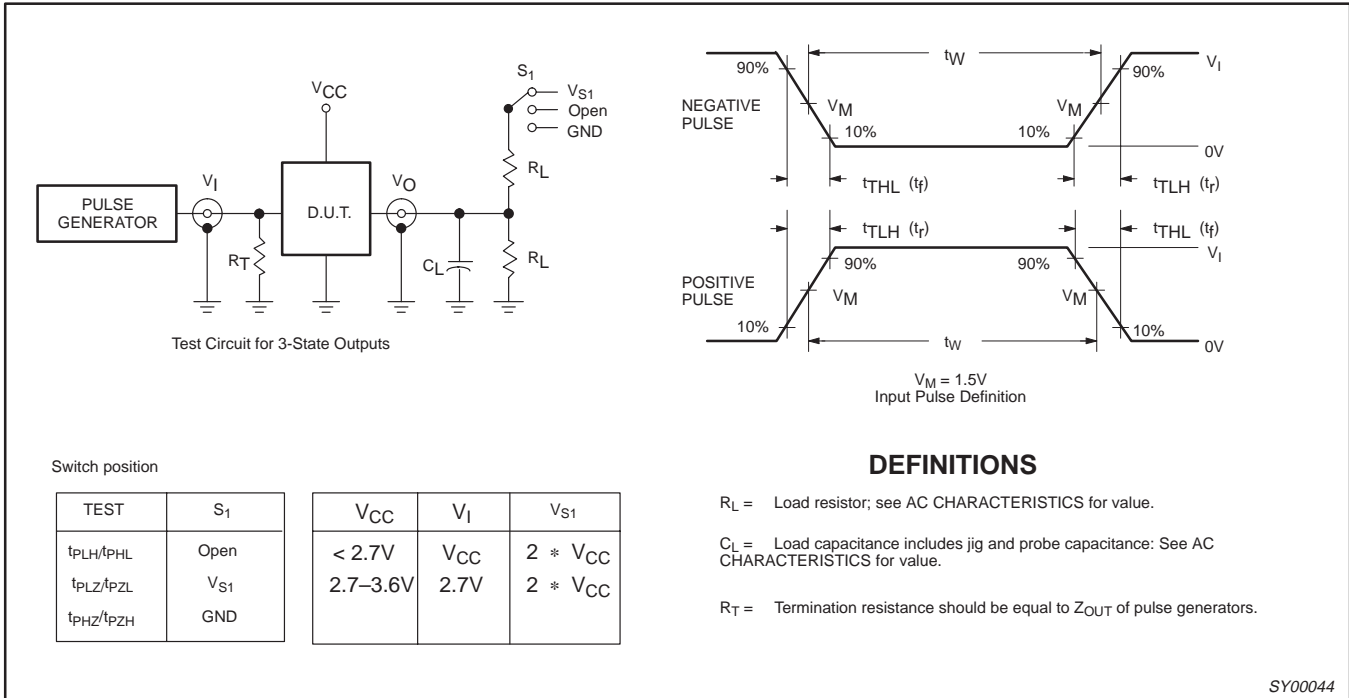


**Waveform 2. Master reset (MR) pulse width, the master reset to output (Q<sub>n</sub>) propagation delays and the master reset to clock (CP) removal time**

# Octal D-type flip-flop with reset; positive-edge trigger

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### TEST CIRCUIT



Switch position

TEST	$S_1$	$V_{CC}$	$V_I$	$V_{S1}$
$t_{PLH}/t_{PHL}$	Open	< 2.7V	$V_{CC}$	$2 * V_{CC}$
$t_{PLZ}/t_{PZL}$	$V_{S1}$	2.7–3.6V	2.7V	$2 * V_{CC}$
$t_{PHZ}/t_{PZH}$	GND			

Waveform 4. Load circuitry for switching times

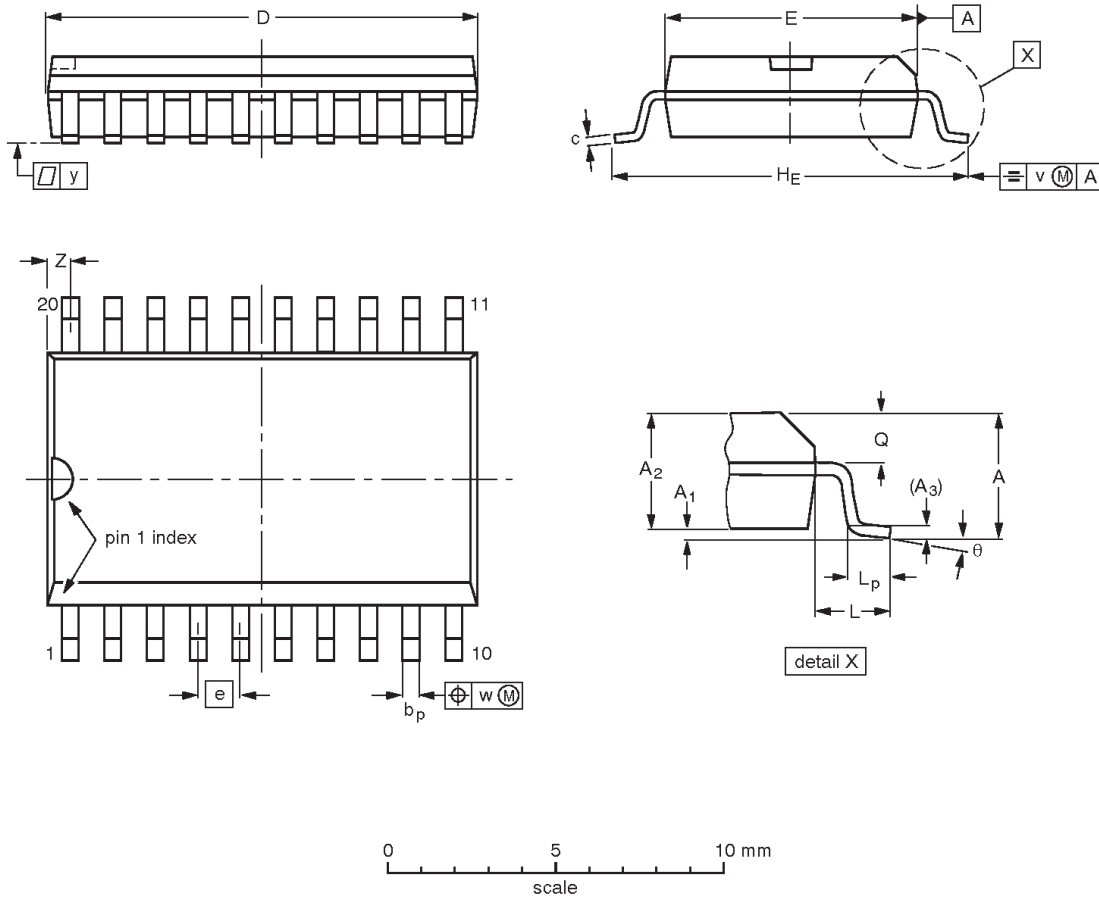
SY00044

# Octal D-type flip-flop with reset; positive-edge trigger

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**SO20: plastic small outline package; 20 leads; body width 7.5 mm**

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

# Octal D-type flip-flop with reset; positive-edge trigger

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**SSOP20:** plastic shrink small outline package; 20 leads; body width 5.3 mm

**SOT339-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04



# Octal D-type flip-flop with reset; positive-edge trigger

## 74LVC273

**TSSOP20:** plastic thin shrink small outline package; 20 leads; body width 4.4 mm

**SOT360-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16- 95-02-04

## Octal D-type flip-flop with reset; positive-edge trigger

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## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
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