RF2516

VHF/UHF TRANSMIITER

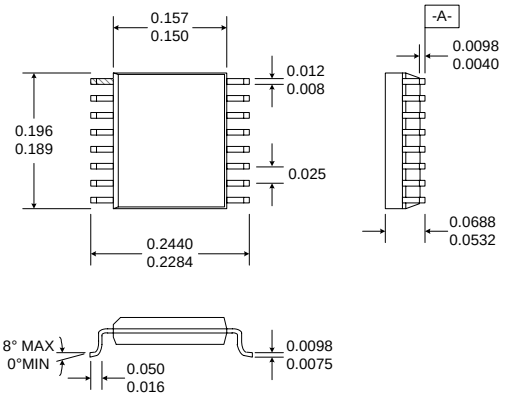
RoHS Compliant & Pb-Free Product

Typical Applications

- 315/433MHz Band Systems
- Local Oscillator Source
- Part 15.231 Applications
- Remote Keyless Entry
- Wireless Security Systems
- AM/ASK/OOK Transmitter

Product Description

The RF2516 is a monolithic integrated circuit intended for use as a low-cost AM/ASK transmitter. The device is provided in a 16-pin QSOP-16 package and is designed to provide a phased locked frequency source for use in local oscillator or transmitter applications. The chip can be used in applications in the North American and European VHF/UHF bands. The integrated VCO, phase detector, prescaler, and reference oscillator transistor require only the addition of an external crystal to provide a complete phase-locked loop. In addition to the standard power-down mode, the chip also includes an automatic lock-detect feature that disables the transmitter output when the PLL is out-of-lock.

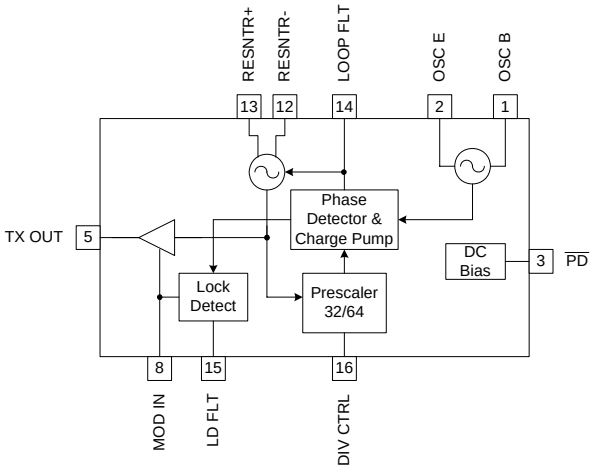


NOTES:
1. Shaded lead is Pin 1.
2. All dimensions are excluding mold flash.
3. Lead coplanarity - 0.005 with respect to datum "A".

Package Style: SSOP-16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ InGaP/HBT
- ☐ GaAs pHEMT
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaN HEMT
- ☐ GaAs MESFET
- ☐ Si CMOS
- ☐ SiGe Bi-CMOS



Functional Block Diagram

Features

- Fully Integrated PLL Circuit
- Integrated VCO and Reference Oscillator
- 2.25V to 3.6V Supply Voltage
- Low Current and Power Down Capability
- 100MHz to 500MHz Frequency Range
- Out-of-Lock Inhibit Circuit

Ordering Information

RF2516	VHF/UHF Transmiiter
RF2516PCBA-410	Fully Assembled Evaluation Board

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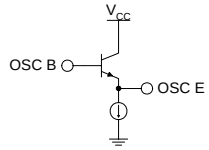
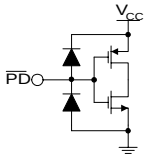
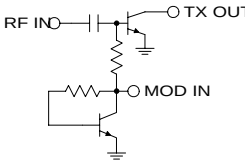
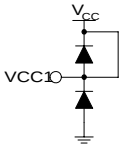
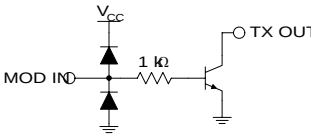
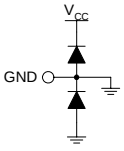
Absolute Maximum Ratings

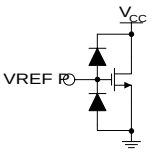
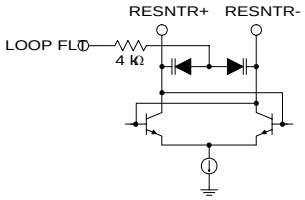
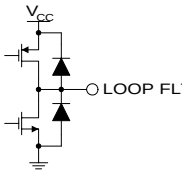
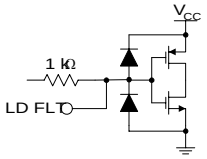
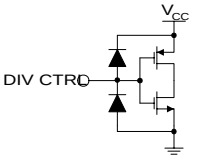
Parameter	Rating	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}	V
MOD IN	-0.5 to 1.1	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=2.8V, Freq=433MHz, R_{MODIN}=3kΩ
Frequency Range		100 to 500		MHz	
Modulation		AM/ASK			
Modulation Frequency			1	MHz	
Incidental FM			15	kHz p-p	
Output Power	+8.5	+10		dBm	50Ω load
ON/OFF Ratio		75		dB	
PLL and Prescaler					
Prescaler Divide Ratio		32/64			
VCO Gain, K_{VCO}		20		MHz/V	Frequency and board layout dependent.
PLL Phase Noise		-97		dBc/Hz	10kHz Offset, 50kHz loop bandwidth
		-102		dBc/Hz	100kHz Offset, 50kHz loop bandwidth
Harmonics		-60		dBc	With output tuning.
Reference Frequency			17	MHz	
Crystal Frequency Spurs		-50		dBc	50kHz PLL loop bandwidth
Max Crystal R_S	TBD	35	50	Ω	For a typ. 1ms turn-on time.
Max Crystal Motional Inductance		60		mH	For a typ. 1ms turn-on time.
Charge Pump Current		100		μA	K_{PD}=100μA/2π=0.0159mA/rad
Power Down Control					
Power Down "ON"	V_{CC}-0.3V			V	Voltage supplied to the input; device is "ON"
Power Down "OFF"			+0.3	V	Voltage supplied to the input; device is "OFF"
Control Input Impedance	100k			Ω	
Turn On Time		1	2	ms	Crystal start-up, 13.57734MHz crystal.
Turn Off Time		1	2	ms	
Power Supply					
Voltage		2.8		V	Specifications
	2.25		3.6	V	Operating limits
Current Consumption (Avg.)	6	10.5		mA	50% Duty Cycle 10kHz Data applied to the MOD IN input. R_{MODIN} (R10)=3kΩ. Output power/DC current consumption externally adjustable by modulation input resistor (see applicable Application Schematic).
Power Down Current	0		1	uA	$\overline{PD}$=0V, MOD IN=0V, DIV CTRL=0V

Pin	Function	Description	Interface Schematic
1	OSC B	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. A 68pF capacitor should be connected between pin 1 and pin 2.	
2	OSC E	This pin is connected directly to the emitter of the reference oscillator transistor. A 33pF capacitor should be connected from this pin to ground.	See pin 1.
3	$\overline{PD}$	Power Down control for all circuitry. When this pin is a logic “low” all circuits are turned off. When this pin is a logic “high”, all circuits are operating normally. A “high” is V_{CC}. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
4	GND	Ground connection for the TX OUT amp. Keep traces physically short and connect immediately to ground plane for best performance. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
5	TXOUT	Transmitter output. This output is an open collector and requires a pull-up inductor for bias/matching and a tapped capacitor for matching.	
6	GND1	Ground connection for the TX output buffer amplifier. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
7	VCC1	This pin is used to supply bias to the TX buffer amplifier. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
8	MOD IN	AM analog or digital modulation can be imparted to the carrier by an input to this pin. An external resistor is used to bias the output amplifiers through this pin. The voltage at this pin must not exceed 1.1V. Higher voltages may damage the device. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
9	VCC2	This pin is used to supply DC bias to the VCO, crystal oscillator, prescaler, phase detector, and charge pump. An IF bypass capacitor should be connected directly to this pin and returned to ground. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	See pin 7.
10	GND2	Digital PLL ground connection. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	

Pin	Function	Description	Interface Schematic
11	VREF P	Bias voltage reference pin for bypassing. The bypass capacitor should be of appropriate size to provide filtering of the reference crystal frequency and be connected directly to this pin. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
12	RESNTR-	The RESNTR pins are used to supply DC voltage to the VCO, as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 13.	
13	RESNTR+	See pin 12.	
14	LOOP FLT	Output of the charge pump. An RC network from this pin to ground is used to establish the PLL bandwidth. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
15	LD FLT	This pin is used to set the threshold of the lock-detect circuit. A shunt capacitor should be used to set an RC time constant with the on-chip series 1k resistor. This signal is used to clamp (enable or disable) the MOD IN circuitry. The time constant should be approximately 10 times the reference period. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	
16	DIV CTRL	Logic “High” input selects divide-by-64 prescaler. Logic “Low” input selects divide-by-32 prescaler. Diodes shown in the interface schematic provide 3kV electrostatic discharge (ESD) protection using the human body model.	

RF2516 Theory of Operation

Introduction

Short range radio devices are becoming commonplace in today's environment. The most common examples are the remote keyless entry systems popular on many new cars and trucks, and the ubiquitous garage door opener. Other applications are emerging with the growth in home security, automation and the advent of various remote control applications. Typically these devices have been simplex, or one-way, links. They are also typically built using surface acoustic wave (SAW) devices as the frequency control elements. This approach has been attractive because the SAW devices have been readily available and a transmitter, for example, could be built with only a few additional components. Recently however, RF Micro Devices, Inc. (RFMD), has introduced several new components that enable a new class of short-range radio devices based on the use of crystals and phase-locked loops for frequency control. These devices are superior in performance and comparable in cost to the traditional SAW-based designs. The RF2516 is an example of such a device. The RF2516 is targeted for applications such as 315MHz and 433MHz band remote keyless entry systems and wireless security systems, as well as other remote control applications.

The RF2516 Transmitter

The RF2516 is a low-cost AM/ASK VHF/UHF transmitter designed for applications operating within the frequency range of 100MHz to 500MHz. In particular, it is intended for 315MHz to 433MHz band systems, remote keyless entry systems, and FCC Part 15.231 periodic transmitters. It can also be used as a local oscillator signal source. The integrated VCO, phase detector, prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked loop. In addition to the standard power-down mode, the chip also includes an automatic lock-detect feature that disables the transmitter output when the PLL is out-of-lock.

The device is manufactured on a 25GHz Silicon Bipolar-CMOS process and packaged in an industry standard SSOP-16 plastic package. This, combined with the low external parts count, enables the designer to achieve small-footprint, high-performance, low-cost designs.

The RF2516 is designed to operate from a supply voltage ranging from 2.25V to 3.6V, accommodating designs using three NiCd battery cells, two AAA flashlight cells, or a lithium button battery. The device is capable of providing up to +10dBm output power into a 50Ω load, and is intended to comply with FCC requirements for unlicensed remote control transmitters. ESD protection is provided on all pins except VCO and TX OUT.

While this device is intended for OOK operation, it is possible to use narrowband FM. This is accomplished by modulating the reference oscillator rather than applying the data to the MOD IN input pin. The MOD IN pin should be tied high to cause the device to transmit. The deviation will be set by pulling limits of the crystal. Deviation sufficient for the transmission of voice and other low data rate signals can therefore be accomplished. Refer to the Application Schematic in the data sheet for details.

The RF2516 Functional Blocks

A PLL consists of a reference oscillator, a phase detector, a loop filter, a voltage controlled oscillator (VCO), and a programmable divider in the feedback path. The RF2516 includes all of these internally, except for the loop filter and the reference oscillator's crystal and two feedback capacitors.

The **reference oscillator** is a Colpitts type oscillator. Pins 1 (OSC B) and 2 (OSC E) provide connections to a transistor that is used as the reference oscillator. The Colpitts configuration is a low parts count topology with reliable performance and reasonable phase noise. Alternatively, an external signal could be injected into the base of the transistor. The drive level should, in either case, be around $500mV_{PP}$. This level prevents overdriving the device and keeps the phase noise and reference spurs to a minimum.

The **prescaler** divides the VCO frequency by either 64 or 32, using a series of flip-flops, depending upon the logic level present at the DIV CTRL pin. A high logic level will select the 64 divisor. A low logic level will select the 32 divisor. This divided signal is then fed into the phase detector where it is compared with the reference frequency.

The RF2516 contains an onboard phase detector and charge pump. The **phase detector** compares the phase of the reference oscillator to the phase of the VCO. The phase detector is implemented using flip-flops in a topology referred to as either “digital phase/frequency detector” or “digital tri-state comparator”. The circuit consists of two D flip-flops whose outputs are combined with a NAND gate which is then tied to the reset on each flip-flop. The outputs of the flip-flops are also connected to the charge pump. Each flip-flop output signal is a series of pulses whose frequency is related to the flip-flop input frequency.

When both inputs of the flip-flops are identical, the signals are both frequency- and phase-locked. If they are different, they will provide signals to the charge pump which will either charge or discharge the loop filter, or enter into a high impedance state. The name “tri-state comparator” comes from this.

The main benefit of this type of detector is the ability to correct for errors in both phase and frequency. When locked, the detector uses phase error for correction. When unlocked, it uses frequency error for correction. This type of detector will lock under all conditions.

The **charge pump** consists of two transistors, one for charging the loop filter and the other for discharging the loop filter. Its inputs are the outputs of the phase detector flip-flops. Since there are two flip-flops, there are four possible states. If both amplifier inputs are low, then the amplifier pair goes into a high impedance state, maintaining the charge on the loop filter. The state where both inputs are high will not occur. The other states are either charging or discharging the loop filter. The loop filter integrates the pulses coming from the charge pump to create a control voltage for the voltage controlled oscillator.

The **VCO** is a tuned differential amplifier with the bases and collectors cross-coupled to provide positive feedback and a 360° phase shift. The tuned circuit is located in the collectors, and is comprised of internal varactors and external inductors. The designer selects the inductors for the desired frequency of operation. These inductors also provide DC bias for the VCO.

The output of the VCO is buffered and applied to the prescaler circuit, where it is divided by either 32 or 64, as selected by the designer, and compared to the reference oscillator frequency.

The **transmit amplifier** is a two-stage amplifier consisting of a driver and an open collector final stage. It is capable of providing 10dBm of output power into a 50Ω load while operating from a 3.6V power supply.

The **lock-detect circuitry** connects to the output of the phase detector circuitry and is used to disable the transmitter when the VCO is not phase-locked to the reference oscillator. This is necessary to avoid unwanted out-of-band transmission and to provide compliance with regulatory limits during an unlocked condition.

There are many possible reasons for the PLL not to be locked. For instance, there is a short period during the start of any VCO in which the VCO begins oscillating and the reference oscillator builds up to full amplitude. During this period, the frequency will likely be outside the authorized band. Typically, the VCO starts much faster than the reference oscillator. Once both VCO and reference oscillators are running, the phase detector can start slewing the VCO to the correct frequency, slowly sliding across 200MHz of occupied spectrum. In competitive devices, the VCO radiates at full power under all of these conditions.

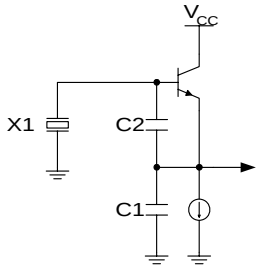
The lock protection circuit in the RF2516 is intended to stabilize quickly after power is applied to the chip, and to disable the base drive to the transmit amplifier. This attenuates the output to levels that will be generally acceptable to regulatory boards as spurious emissions. Once the phase detector has locked the oscillators, then the lock circuit enables the MOD IN pin for transmission of the desired data. There is no need for an external microprocessor to monitor the lock status, although that can be done with a low current A/D converter in a system micro, if needed. The lock-detect circuitry contains an internal resistor which, combined with a designer-chosen capacitor for a particular RC time constant, filters the lock-detect signal. This signal is then passed through an internal Schmitt trigger and used to enable or disable the transmit amplifier.

If the oscillator unlocks, even momentarily, the protection circuit quickly disables the output until the lock is stable. These unlocks can be caused by low battery voltage, poor power supply regulation, severe shock of the crystal or VCO, antenna loading, component failure, or a myriad of unexpected single-point failures.

The RF2516 contains onboard band gap reference voltage circuitry which provides a stable **DC bias** over varying temperature and supply voltages. Additionally, the device features a power-down mode, eliminating battery disconnect switches.

Designing With the RF2516

The **reference oscillator** is built around the onboard transistor at pins 1 and 2. The intended topology is that of a Colpitts oscillator. The Colpitts oscillator is quite common and requires few external components, making it ideal for low-cost solutions. The topology of this type of oscillator is as seen in the following figure.



This type of oscillator is a parallel resonant circuit for a fundamental mode crystal. The transistor amplifier is an emitter follower and the voltage gain is developed by the tapped capacitor impedance transformer. The series combination of C_1 and C_2 act in parallel with the input capacitance of the transistor to capacitively load the crystal.

The nominal capacitor values can be calculated with the following equations[6]:

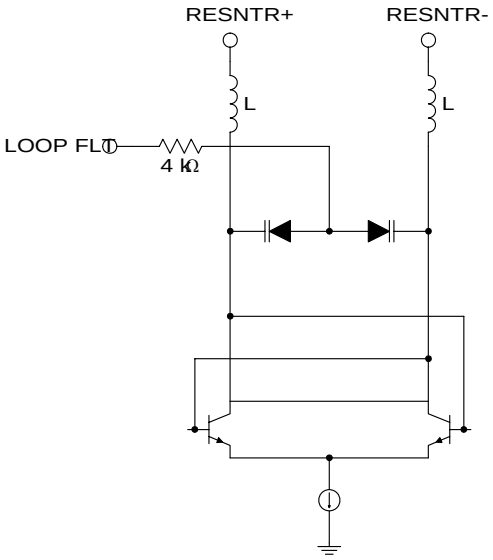
$$C_1 = \frac{60 \cdot C_{load}}{freq_{MHz}} \text{ and } C_2 = \frac{1}{\frac{1}{C_{load}} - \frac{1}{C_1}}$$

The load capacitance is usually 32pF. The variable freq is the oscillator frequency in MHz. The frequency can be adjusted by either changing C_2 or by placing a variable capacitor in series with the crystal. As an example, assume a desired frequency of 14MHz and a load capacitance of 32pF. C_1=137.1pF and C_2=41.7pF.

These capacitor values provide a starting point. The drive level of the oscillator should be checked by looking at the signal at pin 2 (OSC E). It has been found that the level at this pin should generally be around 500mV$_{PP}$ or less. This will reduce the reference spur levels and reduce noise from distortion. If this level is higher than 500mV$_{PP}$ then increase the value of C_1. The values of these capacitors are usually tweaked during design to meet performance goals, such as minimizing the start-up time.

Additionally, by placing a variable capacitor in series with the crystal, one is able to adjust the frequency. This will also alter the drive level, so it should be checked again.

An important part of the overall design is the **voltage controlled oscillator**. The VCO is configured as a differential amplifier. The VCO is tuned via internal varactors. The varactors are tuned by the loop filter output voltage through a 4kΩ resistor.



As mentioned earlier, the inductors and the varactors are tuning a differential amplifier. To tune the VCO the designer only needs to calculate the value of the inductors connected to pins 12 and 13 (RESNTR- and RESNTR+). The inductor value is determined by the equation:

$$L = \left(\frac{1}{2 \cdot \pi \cdot f}\right)^2 \cdot \frac{1}{C} \cdot \frac{1}{2}$$

In this equation, ***f*** is the desired operating frequency and ***L*** is the value of the inductor required. The value ***C*** is the amount of capacitance presented by the varactors and parasitics. For calculation purposes 1.5pF should be used. The factor of one-half is due to the inductors being in each leg. As an example, assume an operating frequency of 433MHz. The calculated value of each inductor is 45nH. A 47nH inductor would be appropriate as the closest available value.

The setup of the VCO can be summarized as follows. First, open the loop. Next, get the VCO to run on the desired frequency by selecting the proper inductor and capacitor values. The capacitor value will need to include the varactor and circuit parasitics.

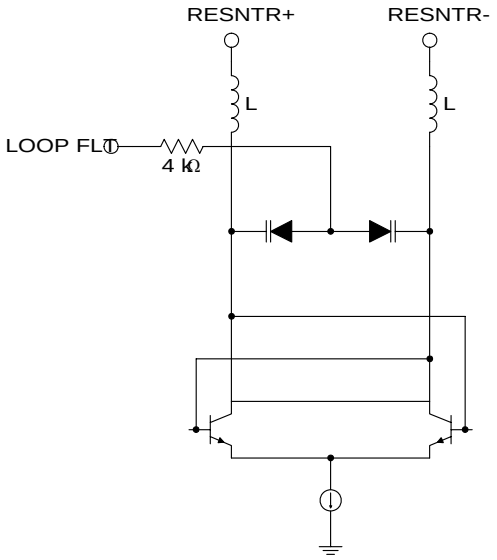
After the VCO is running at the desired frequency, set the VCO sensitivity. The sensitivity is determined by connecting the control voltage input point to ground and noting the frequency.

Connect the same point to the supply, and again note the frequency. The difference between these two frequencies divided by the supply voltage is the VCO sensitivity expressed in Hz/V. Increasing the inductor value while decreasing the capacitor value will increase the sensitivity. Decreasing the inductor value while increasing the capacitor value will lower the sensitivity.

When increasing or decreasing component values, make sure that the center frequency remains constant. Finally, close the loop.

External to the part, the designer needs to implement a **loop filter** to complete the PLL. The loop filter converts the output of the charge pump into a voltage that is used to control the VCO. Internally, the VCO is connected to the charge pump output through a 4kΩ resistor. The loop filter is then connected in parallel to this point at pin 14 (LOOP FLT). This limits the loop filter topology to a second order filter usually consisting of a shunt capacitor and a shunt series RC. A passive filter is most common, as it is a low-cost and low-noise design. An additional pole could be used for reducing the reference spurs, however there is not a way to add the series resistor. However, this should not be a reason for concern.

The schematic of the loop filter is:



The transfer function is:

$$F(s) = R_2 \cdot \left[\frac{s \cdot \tau_2 + 1}{s \cdot \tau_2 \cdot (s \cdot \tau_1 + 1)} \right]$$

where the time constants are defined as:

$$\tau_2 = R_2 \cdot C_2 \text{ and } \tau_1 = R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2} \right)$$

The frequency at which unity gain occurs is given by:

$$\omega_{LBW} = \frac{1}{\sqrt{\tau_1 \cdot \tau_2}}$$

This is also the loop bandwidth.

If the phase margin (PM) and the loop bandwidth (ω_{LBW}) are known, it is possible to calculate the time constants. These are found using the equations[4]:

$$\tau_1 = \frac{\sec(PM) - \tan(PM)}{\omega_{LBW}} \text{ and } \tau_2 = \frac{1}{\omega_{LBW}^2 \cdot \tau_1}$$

With these known, it is then possible to determine the values of the filter components.[4]

$$C_1 = \frac{\tau_1}{\tau_2} \cdot \frac{K_{PD} \cdot K_{VCO}}{\omega_{LBW}^2 \cdot N} \cdot \sqrt{\frac{1 + (\omega_{LBW} \cdot \tau_2)^2}{1 + (\omega_{LBW} \cdot \tau_1)^2}}$$

$$C_2 = C_1 \cdot \left(\frac{\tau_2}{\tau_1} - 1\right) \qquad R_2 = \frac{\tau_2}{C_2}$$

As an example, consider a loop bandwidth of 50kHz, a phase margin of 45°, a divide ratio of 64, a K_{VCO} of 20MHz/V, and a KPD of 100μA/2πrad. Time constant τ1 is 1.31848μs, time constant τ2 is 7.68468μs, C_1 is 20.9pF, C_2 is 100.8pF, and R_2 is 76.2kΩ.

In order to perform these calculations, one will need to know the value of two constants, K_{VCO} and K_{PD}. K_{PD} is calculated by dividing the charge pump current by 2π. For the RF2516, the charge pump current is 100μA. K_{VCO} is best found empirically as it will change with frequency and board parasitics. By briefly connecting pin 14 (LOOP FLT) to VCC and then to ground, the frequency tuning range of the VCO can be seen. Dividing the difference between these two frequencies by the difference in the voltage gives K_{VCO} in MHz/V.

The control lines provide an **interface** for connecting the device to a microcontroller or other signal generating mechanism. The designer can treat pin 8 (MOD IN), pin 16 (DIV CTRL), and pin 3 (PD) as control pins whose voltage level can be set. The lock-detect voltage at pin 15 (LD FLT) is an output that can be monitored by the microcontroller.

Pin 15 (LD FLT) is used to set the threshold of the **lock-detect circuit**. A shunt capacitor is used to set an RC time constant with an on-chip series 1kΩ resistor. The time constant should be approximately 10 times the reference period.

General **RF bypassing** techniques must be observed to get the best performance. Choose capacitors such that they are series resonant near the frequency of operation.

Board layout is always an area in which great care must be taken. The board material and thickness are used in calculating the RF line widths. The use of vias for connection to the ground plane allows one to connect to ground as close as possible to ground pins. When laying out the traces around the VCO, it is desirable to keep the parasitics equal between the two legs. This will allow equal valued inductors to be used.

Pre-compliance testing should be performed during the design process. This can be done with a GTEM cell or at a compliance testing laboratory. It is recommended that pre-compliance testing be performed so that there are no surprises during final compliance testing. This will help keep the product development and release on schedule.

Working with a laboratory offers the benefit of years of compliance testing experience and familiarity with the regulatory issues. Also, the laboratory can often provide feedback that will help the designer make the product compliant.

On the other hand, having a GTEM cell or an open air test site locally offers the designer the ability to rapidly determine whether or not design changes impact the product's compliance. Set-up of an open air test site and the associated calibration is not trivial. An alternative is to use a GTEM test cell.

After the design has been completed and passes compliance testing, application will need to be made with the respective regulatory bodies for the geographic region in which the product will be operated to obtain final certifications.

RF2516 Typical Applications
FCC Part 15.231 Periodic Transmitter - 315MHz Automotive Keyless Entry Transmitter

The following information is taken or paraphrased from the Code of Federal Regulations Title 47, Part 15, Section 231 (47 CFR 15.231). Part 15 discusses radio frequency devices and section 231 discusses periodic transmissions. Please refer to the regulation itself as the final authority. Additional information may be found on the Internet at www.fcc.gov.

To highlight the main guidelines outlined by this section, there are five main limitations: operating frequency, transmission content, transmission duration, emission bandwidth, and spurious emissions.

Part 15.231 allows operation in two bands: 40.66MHz to 40.70MHz and above 70MHz. Transmission is limited to control signals such as alarm systems, door openers, remote switches, etc. Radio control of toys is not permitted, nor is continuous transmission such as voice or video. Data transmission other than a recognition code is not permitted. Transmission time is limited to 5 seconds (paragraph a) or for 1 second with greater than ten seconds off (paragraph e).

Emission bandwidth between 70MHz and 900MHz can not be more than 0.25% of the center frequency. Above 900MHz, the emission bandwidth cannot be greater than 0.50% of the center frequency. The emission bandwidth is determined from the points that are 20dB down from the modulated carrier. This corresponds to an occupied bandwidth of 4.5MHz at a center frequency of 902MHz, 1.1MHz at 433MHz, and 788kHz at 315MHz.

Spurious emissions limits are listed in tabular form for various frequency ranges in the Section 231. Above 470MHz with a manually activated transmitter, the fundamental field strength at a distance of 3 meters shall not exceed 12,500microvolts/meter. The spurious emissions shall not exceed 1,250microvolt/meter at a distance of 3meters above 470MHz. Refer to Appendix A for a method of converting field strength to power.

In the frequency range of 260MHz to 470MHz, one needs to linearly interpolate the maximum emissions level for both the fundamental and spurious emissions. The equation for this line is given by:

$$E_{\frac{\mu V}{m}} = 41\frac{2}{3} \cdot Freq_{MHz} - 7083\frac{1}{3}$$

This equation is derived from the endpoints of the frequency range and their respective field strengths. Note that the field strength is in microvolts per meter and the frequency is in megahertz. To determine the spurious level, divide the level calculated above for the spurious frequency by ten.

As an example, assume the fundamental is 315MHz and the reference frequency is 9.8MHz. The field strengths of the fundamental, the reference spurs, and the harmonics of the fundamental up through the tenth harmonic are calculated in the following table The occupied bandwidth limit is 787.5kHz. As shown in Table A, the fifth, seventh, and ninth harmonics fall into restricted bands as called out in section 15.205. The limits for these restricted bands are called out in section 15.209. The power level in the last column is the level if the output is connected directly to a spectrum analyzer. Refer to Appendix A as to how this column was calculated.

Local Oscillator Source
Since the RF2516 has a phase-locked VCO, it can be used as a signal source. The device is an ASK/OOK transmitter, with the data provided at the MOD IN pin. When the MOD IN is a high logic level, the carrier is transmitted. When MOD IN is a low logic level, then the carrier is not transmitted. Therefore, to use the RF2516 as signal source, simply tie the MOD IN pin to the supply voltage, through a suitable series resistor (minimum 3kΩ).

Conclusions

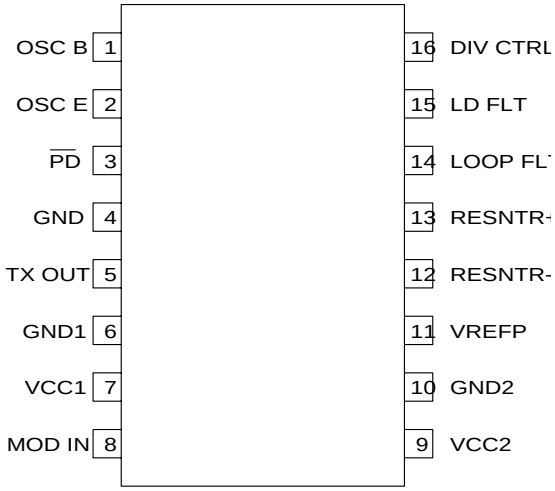
The RF2516 is an AM/OOK VHF/UHF transmitter that features a phase-locked output. This device is suitable for use in a CFR Part 15.231 compliant product as well as a local oscillator signal source. Two examples showing these applications were discussed.

The RF2516 is packaged in a low-cost plastic package and requires few external parts, thus making it suitable for low-cost designs.

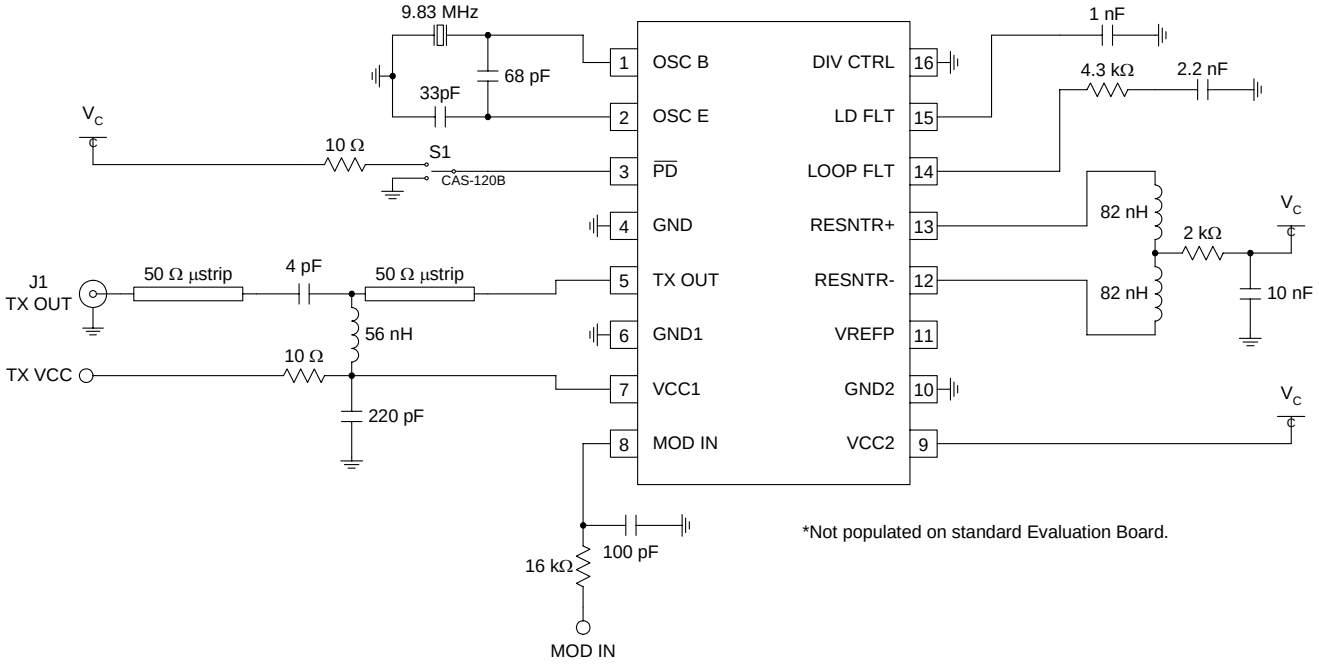
	Frequency (MHz)	15.205 Limits (μV/m@3m)	15.231 Limits (μV/m@3m)	Final FCC Mask (μV/m@3m)	Final FCC Mask (μV/m@3m)	Power Level (dBm, 50Ω)
Ref Spur	305.2	-	604.17	604.17	55.62	-39.61
1	315.0	-	6041.67	6041.67	75.62	-19.61
Ref Spur	324.8	-	604.17	604.17	55.62	-39.61
2	630.0	-	604.17	604.17	55.62	-39.61
3	945.0	-	604.17	604.17	55.62	-39.61
4	1260.0	-	604.17	604.17	55.62	-39.61
5	1575.0	500	-	500.00	53.98	-41.25
6	1890.0	-	604.17	604.17	55.62	-39.61
7	2205.0	500	-	500.00	53.98	-41.25
8	2520.0	-	604.17	604.17	55.62	-39.61
9	2835.0	500	-	500.00	53.98	-41.25
10	3150.0	-	604.17	604.17	55.62	-39.61

Table A

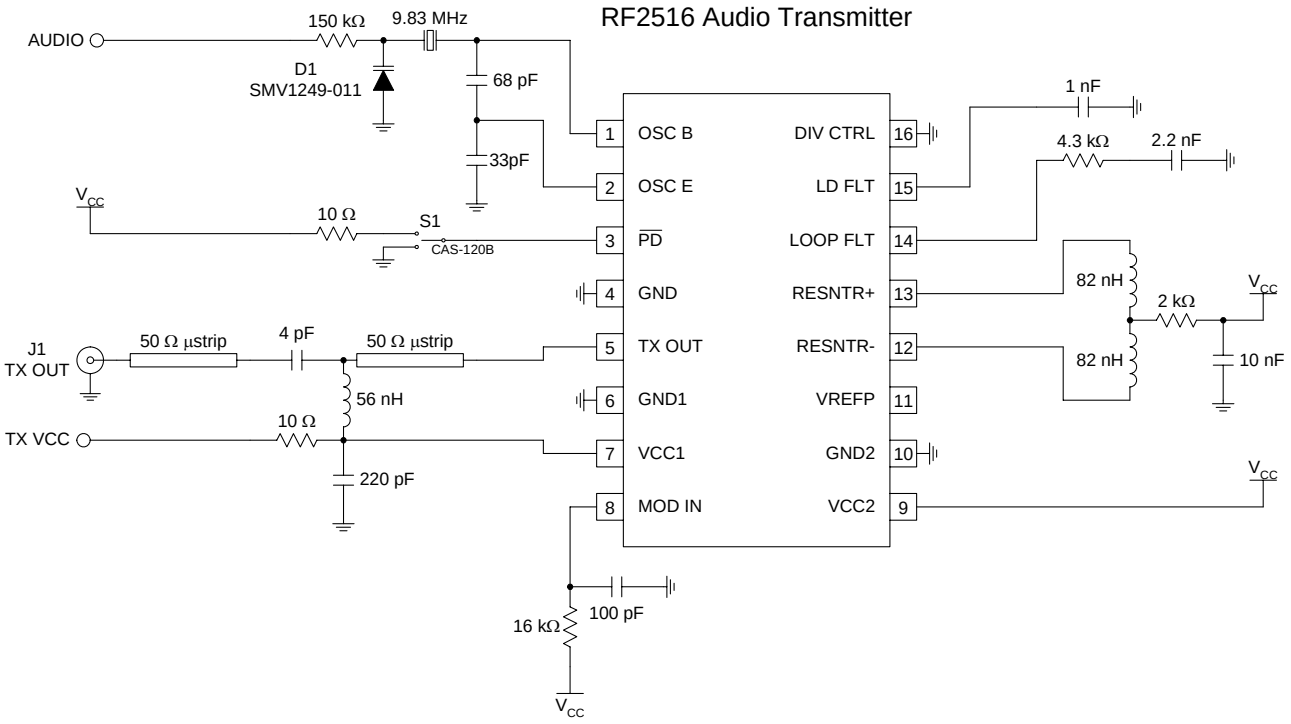
Pin Out


OSC B 1
OSC E 2
PD 3
GND 4
TX OUT 5
GND1 6
VCC1 7
MOD IN 8
16 DIV CTRL
15 LD FLT
14 LOOP FL
13 RESNTR-
12 RESNTR-
11 VREFP
10 GND2
9 VCC2

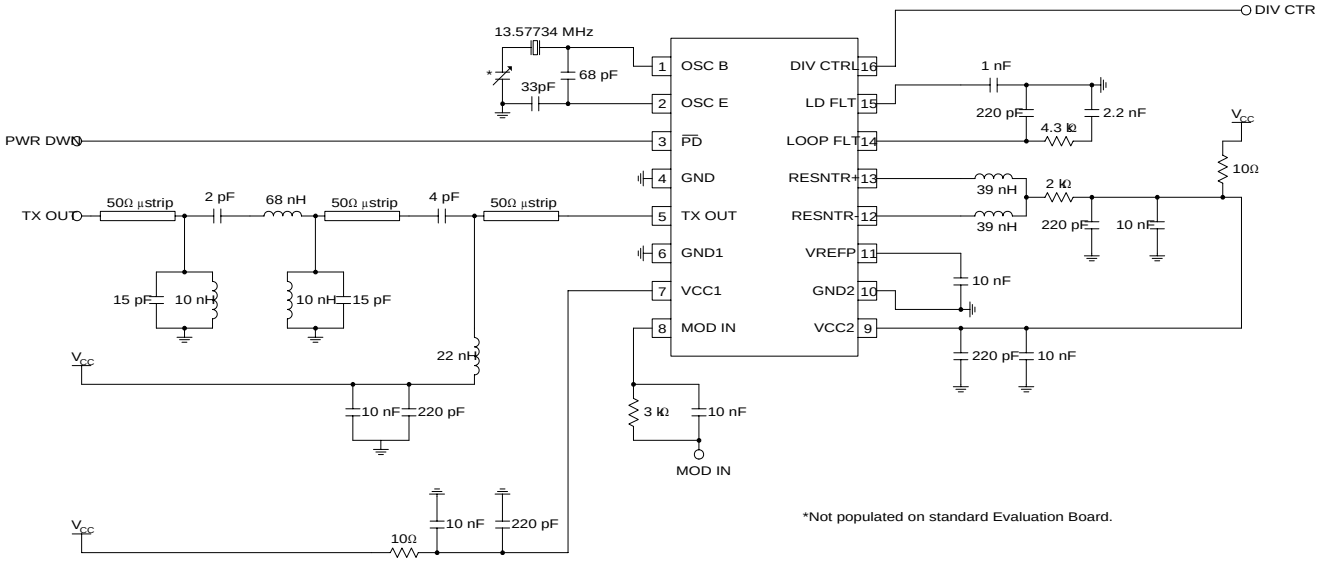
Application Schematic
315MHz



Application Schematic
315MHz



Application Schematic
433MHz



*Not populated on standard Evaluation Board.

V_{CC} (V)	Mod. in Res. Value (R5)	I_{CC} (mA)	P_{OUT} (dBm)
2.0	1k	11.08	-6.23
	3k	10.83	-4.40
	5k	4.61	-5.61
	7k	4.00	-6.66
	9k	3.63	-8.08
	11k	3.42	-8.93
	13k	3.26	-10.04
	15k	3.15	-10.71
	17k	3.07	-11.58
	19k	3.01	-12.32
	21k	2.95	-13.10

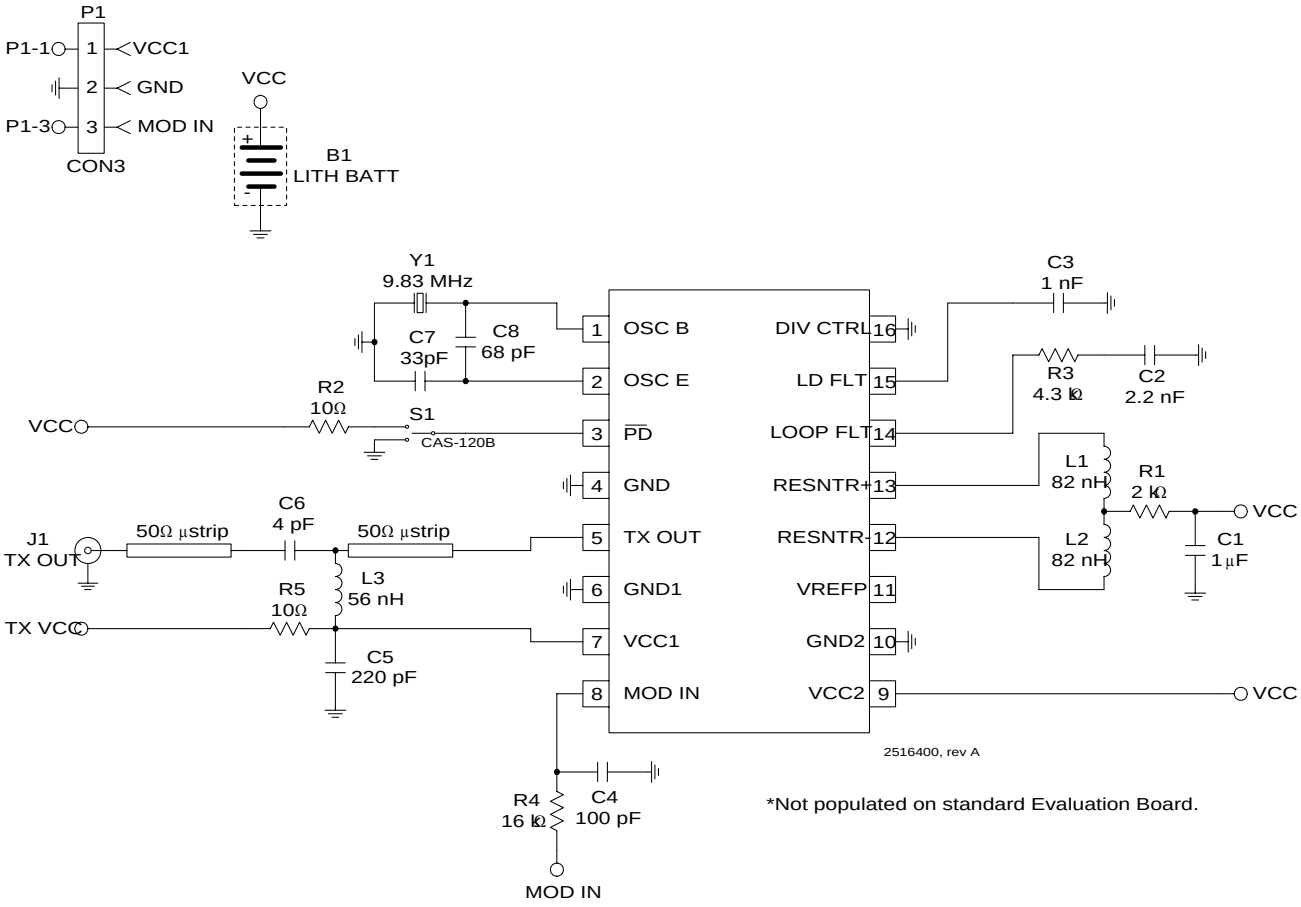
V_{CC} (V)	Mod. in Res. Value (R5)	I_{CC} (mA)	P_{OUT} (dBm)
2.4	1k	14.05	7.94
	3k	9.00	7.63
	5k	7.48	5.95
	7k	6.73	4.64
	9k	6.16	3.35
	11k	5.79	2.40
	13k	5.53	1.47
	15k	5.29	0.75
	17k	5.13	0.05
	19k	4.98	-0.60
	21k	4.86	-1.26

V_{CC} (V)	Mod. in Res. Value (R5)	I_{CC} (mA)	P_{OUT} (dBm)
2.8	1k	17.38	7.45
	3k	10.51	8.78
	5k	8.68	7.23
	7k	7.82	6.00
	9k	7.18	4.73
	11k	6.75	3.81
	13k	6.45	2.98
	15k	6.18	2.30
	17k	5.99	1.63
	19k	5.80	1.00
	21k	5.66	0.35

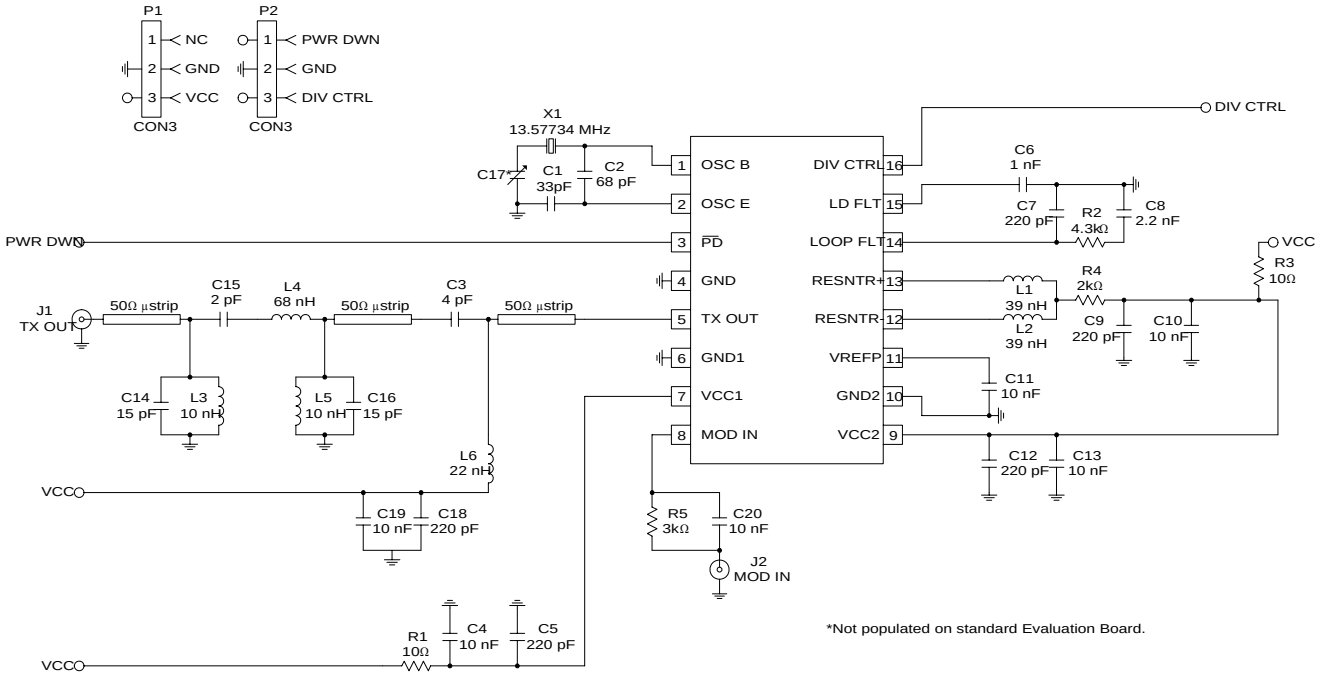
V_{CC} (V)	Mod. in Res. Value (R5)	I_{CC} (mA)	P_{OUT} (dBm)
3.2	1k	20.90	6.77
	3k	12.12	9.70
	5k	9.66	8.30
	7k	8.95	7.11
	9k	8.23	5.91
	11k	7.75	5.02
	13k	7.42	4.16
	15k	7.10	3.51
	17k	6.89	2.89
	19k	6.68	2.26
	21k	6.52	1.66

V_{CC} (V)	Mod. in Res. Value (R5)	I_{CC} (mA)	P_{OUT} (dBm)
3.6	1k	24.68	5.78
	3k	13.88	10.42
	5k	10.94	9.18
	7k	10.14	8.08
	9k	9.34	6.88
	11k	8.81	6.02
	13k	8.44	5.19
	15k	8.09	4.52
	17k	7.86	3.93
	19k	7.63	3.35
	21k	7.44	2.72

Evaluation Board Schematic
315MHz



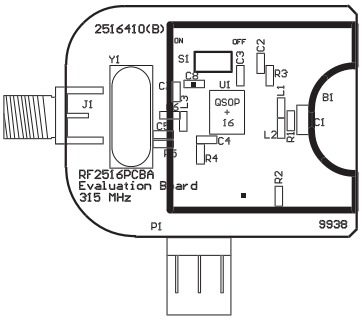
Evaluation Board Schematic
433MHz

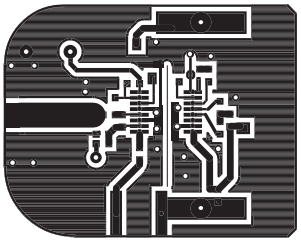


*Not populated on standard Evaluation Board.

Evaluation Board Layout (315MHz)
Board Size 1.285” x 1.018”

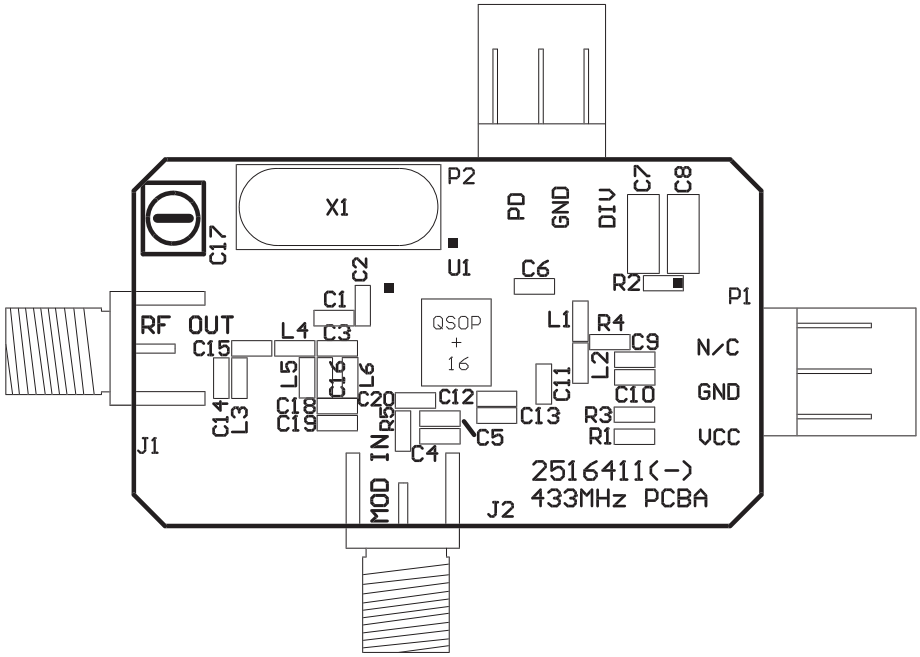
Board Thickness 0.062”, Board Material FR-4

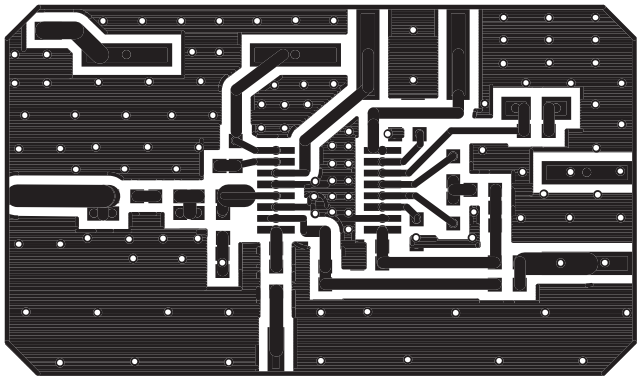




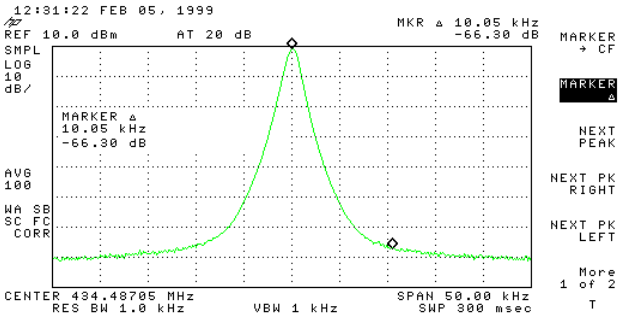
Evaluation Board Layout (433MHz)
Board Size 1.392” x 0.813”

Board Thickness 0.062”, Board Material FR-4

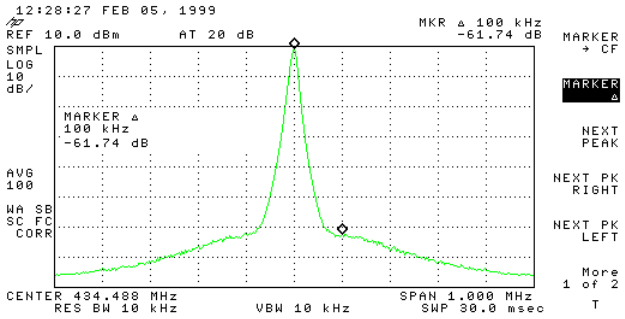




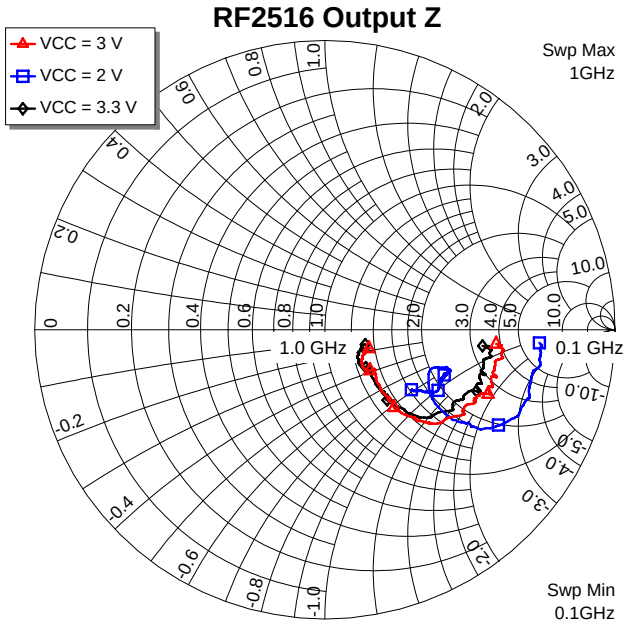
433MHz Phase Noise



3.5V Phase Noise MODIN=3k



3.5V Phase Noise MODIN=3k



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