3-Channel Laser Diode Driver with Oscillator

AD9662

FEATURES

Current-controlled current source with 3 input channels
Output current for Channel 3—315 mA
Output current for other channels—210 mA
Rise time/fall time of 0.8 ns
On-chip oscillator
Single 5 V power supply (±10%)
Low output overshoot
Low power consumption

APPLICATIONS

CD-RW drives
DVD-RW, DVD+RW, MO drives
Laser diode current switching

FUNCTIONAL BLOCK DIAGRAM

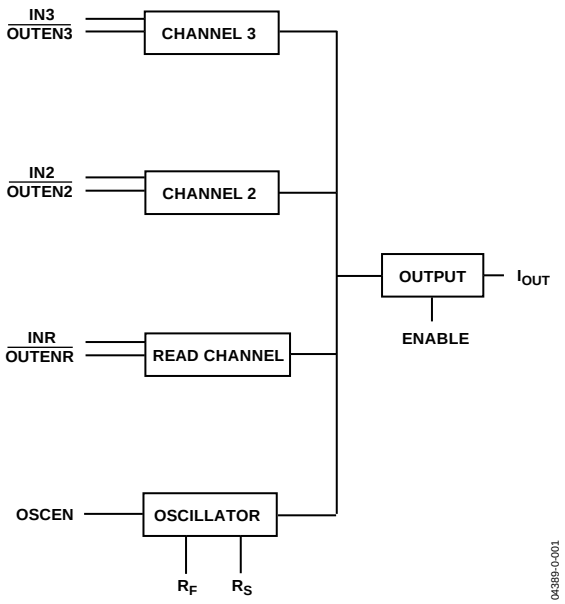


Figure 1. AD9662 3-Channel Laser Diode Driver

GENERAL DESCRIPTION

The AD9662 is a laser diode driver for high performance CD and DVD recordable drives. It includes three channels for three different optical power levels: the read channel generates a continuous output power level, whereas Channel 2 and Channel 3 are used as write channels having 0.8 ns rise/fall times. All channel currents are summed at the I_{OUT} pin. Each channel's output current is established by multiplying the channel's gain by the channel's input current. The input current for each of the input channels—INR, IN2, and IN3—can be set either by using an external resistor that converts an input voltage to a current or by directly using a current source.

An on-chip oscillator is provided to allow output current modulation (to reduce laser mode hopping). Two external resistors control the frequency and the amplitude swing of the oscillator. The push-pull oscillator can swing up to 100 mA p-p and has a frequency range of 200 MHz to 500 MHz.

Rev. C
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **© 2005 Analog Devices, Inc. All rights reserved.**

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REVISION HISTORY

11/05—Rev. SpB to Rev. C
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Changes to Absolute Maximum Ratings 5
Changes to Figure 17 12

12/03—Rev. SpA: Initial 2-Page Web Version

12/03—Rev. Sp0: Initial Full Version

SPECIFICATIONS

At T_{AMB}, V_{CC} = 5 V, ENABLE = 1, OSCEN = 0, $\overline{OUTENx}$ = 1, unless otherwise stated.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
LASER AMPLIFIER					
Output Current Read Channel	Output is sourcing, $\overline{OUTENR}$ = 0	210	235		mA
Output Current Channel 2	Output is sourcing, $\overline{OUTEN2}$ = 0	210	235		mA
Output Current Channel 3	Output is sourcing, $\overline{OUTEN3}$ = 0	315	340		mA
Total Output Current	Output is sourcing, $\overline{OUTEN3}$ = 0 and ($\overline{OUTENR}$ = 0 and/or $\overline{OUTEN2}$ = 0)		>550		mA
Output Current Linearity[1]	Read Channel, $\overline{OUTENR}$ = 0	−4	±0.6	+4	%
Output Current Linearity[1]	Write2 Channel, $\overline{OUTEN2}$ = 0	−4	±0.6	+4	%
Output Current Linearity[1]	Write3 Channel, $\overline{OUTEN3}$ = 0	−4	±0.1	+4	%
Best-Fit Current Gain[1]	Read Channel, $\overline{OUTENR}$ = 0	125	135	145	mA/mA
Best-Fit Current Gain[1]	Write2 Channel, $\overline{OUTEN2}$ = 0	120	130	140	mA/mA
Best-Fit Current Gain[1]	Write3 Channel, $\overline{OUTEN3}$ = 0	240	260	280	mA/mA
Best-Fit Current Offset[1]	Read Channel, $\overline{OUTENR}$ = 0	−7	±0.6	+7	mA
Best-Fit Current Offset[1]	Write2 Channel, $\overline{OUTEN2}$ = 0	−7	±0.6	+7	mA
Best-Fit Current Offset[1]	Write3 Channel, $\overline{OUTEN3}$ = 0	−30	−2	+15	mA
I_{OUT} Series Resistance	Total R_{OUT} to V_{CC} rail		6.5	10	Ω
Input Impedance (R_{IN}), Channel R, Channel 2	R_{IN} to GND	160	200	240	Ω
Input Impedance (R_{IN}), Channel 3	R_{IN} to GND	80	100	120	Ω
I_{OUT} Supply Sensitivity (PSRR) Read Mode	I_{OUT} = 50 mA (read-only), V_{CC} = 5 V ± 10% $\overline{OUTENR}$ = 0		10	15	%/V
I_{OUT} Supply Sensitivity (PSRR) Write Mode	I_{OUT} = 100 mA (50 mA read, 50 mA write) V_{CC} = 5 V ± 10%, $\overline{OUTENR}$ = 0 and ($\overline{OUTEN2}$ = 0 or $\overline{OUTEN3}$ = 0)		10	15	%/V
Output Current Noise	I_{OUT} = 50 mA (Read), $\overline{OUTENR}$ = 0, f = 300 MHz		150		pA/√Hz
I_{OUT} Temperature Sensitivity Read Mode	I_{OUT} = 50 mA (read-only) $\overline{OUTENR}$ = 0		100		ppm/°C
I_{OUT} Temperature Sensitivity Write Mode Channel 2	I_{OUT} = 100 mA (50 mA Read, 50 mA Write2) $\overline{OUTENR}$ = 0, $\overline{OUTEN2}$ = 0		100		ppm/°C
I_{OUT} Temperature Sensitivity Write Mode Channel 3	I_{OUT} = 100 mA (50 mA Read, 50 mA Write3) $\overline{OUTENR}$ = 0, $\overline{OUTEN3}$ = 0		100		ppm/°C
LASER AMPLIFIER AC SPECIFICATIONS					
Write Rise Time[2]	I_{OUT} = 50 mA dc (Read), 50 mA pulse W2 or W3 $\overline{OUTENR}$ = 0 and ($\overline{OUTEN2}$ = 0 or $\overline{OUTEN3}$ = 0)		0.8	1.8	ns
Write Fall Time[2]	I_{OUT} = 50 mA dc (Read), 50 mA pulse W2 or W3 $\overline{OUTENR}$ = 0		0.6	1.8	ns
Output Current Overshoot	I_{OUT} = 50 mA dc (Read), 50 mA pulse W2 or W3 $\overline{OUTENR}$ = 0 and ($\overline{OUTEN2}$ = 0 or $\overline{OUTEN3}$ = 0)		13		%
I_{OUT} ON Propagation Delay	$\overline{OUTENx}$ 50% H-L to I_{OUT} at 50% of final value		2.7		ns
I_{OUT} OFF Propagation Delay	$\overline{OUTENx}$ 50% L-H to I_{OUT} at 50% of initial value		2.7		ns
Disable Time	ENABLE 50% H-L to I_{OUT} at 50% of initial value		5.4		ns
Enable Time	ENABLE 50% L-H to I_{OUT} at 50% of final value		13.5		ns
OSCILLATOR SPECIFICATIONS	$\overline{OUTENR}$ = 0				
Oscillator Frequency	R_F = 9.53 kΩ, R_S = 23.7 kΩ	265	300	325	MHz
Oscillator Frequency Temperature Coefficient	R_F = 9.53 kΩ, R_S = 23.7 kΩ		600		ppm/°C
Disable Time Oscillator	OSCEN 50% H-L to amplitude at 50% of initial value		4		ns
Enable Time Oscillator	OSCEN 50% L-H to amplitude at 50% of final value		6		ns

Parameter	Conditions					Min	Typ	Max	Unit
LOGIC SPECIFICATIONS									
Logic HI Threshold						2.0			V
Logic LO Threshold								0.8	V
Input Impedance	$\overline{\text{OUTEN}}$x, ENABLE, OSCEN						>10		MΩ
Input Leakage Current	$\overline{\text{OUTEN}}$x, ENABLE, OSCEN						<1		µA
SUPPLY CURRENT	ENABLE	OSCEN	$\overline{\text{OUTENR}}$	$\overline{\text{OUTEN2}}$	$\overline{\text{OUTEN3}}$				
Power-Down	0	0	1	1	1		8.5	10	mA
Power-Up									
Inputs Disabled	1	0	1	1	1		18	22	mA
Inputs Disabled, OSC Enabled	1	1	1	1	1		52	62	mA
Read Mode, OSC Enabled[3]	1	1	0	1	1		55	65	mA
I_{OUT} = 50 mA									
Write Mode[3]	1	0	1	0	0		29	35	mA
I_{OUT} = 100 mA (50 mA W2, 50 mA W3)									
OPERATING CONDITIONS									
Supply Voltage Range						4.5		5.5	V
Operating Temperature Range						0		85	°C

[1] Output linearity, offset current, and gain are calculated using a best-fit method at 30 mA, 45 mA, 60 mA, 75 mA, and 90 mA for the Read and Write2 Channels and 90 mA, 105 mA, 120 mA, 135 mA, and 150 mA for Write Channel 3. Each channel's output current is given by $I_{OUT} = (I_{IN} \times \text{Gain}) + I_{OS}$.

[2] This parameter is guaranteed by design and characterization using six sigma. Rise and fall times are measured electrically from the 10% to 90% points using a Sharp GH0781JA2C diode as a load.

[3] The values specified do not include the output current.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Range
Supply Voltage $+V_S$	
Pin 9, Pin 15, and Pin 16	5.5 V
Input Pins	
Pin 1 and Pin 2	2.2 mA
Pin 5	1.6 mA
Pin 6, Pin 7, Pin 8, Pin 10, and Pin 11	−0.8 V to +5.5 V
Internal Power Dissipation[1]	
16-Lead QSOP	620 mW
Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, Soldering 60 sec	300°C

[1] Power dissipation is specified on SEMI standard 4-layer board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

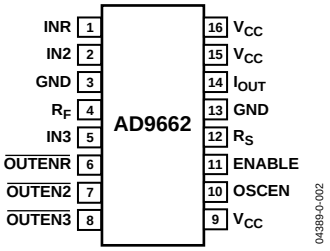


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INR	Input Current Pin for the Read Channel. Has a typical input impedance of 200 Ω.
2	IN2	Input Current Pin for Write Channel 2. Has a typical input impedance of 200 Ω.
3, 13	GND	Common External Ground Reference.
4	R_F	Pin Used to Set Oscillator Frequency by Connecting a Resistor from This Pin to Ground.
5	IN3	Input Current Pin for Write Channel 3. Has a typical input impedance of 100 Ω.
6	$\overline{\text{OUTENR}}$	TTL-Compatible Enable for the Read Channel. Logic low active.
7	$\overline{\text{OUTEN2}}$	TTL-Compatible Enable for Write Channel 2. Logic low active.
8	$\overline{\text{OUTEN3}}$	TTL-Compatible Enable for Write Channel 3. Logic low active.
9, 15, 16	V_{CC}	Power Supply Pins for the AD9662. Each pin needs to be decoupled with a 0.1 µF capacitor to ground.
10	OSCEN	TTL-Compatible Enable for the Oscillator. Logic high active.
11	ENABLE	TTL-Compatible Enable for the Device. Logic high active.
12	R_S	Pin Used to Set Oscillator Amplitude by Connecting a Resistor from This Pin to Ground.
14	I_{OUT}	Output Current Pin. This pin is connected to the anode of a laser diode.

TYPICAL PERFORMANCE CHARACTERISTICS

R_S = 23.7 kΩ, R_F = 9.53 kΩ, and read channel output current is 50 mA, unless otherwise noted.

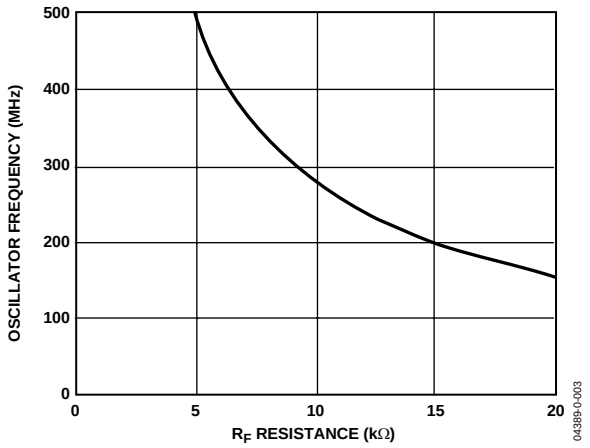


Figure 3. Oscillator Frequency vs. R_F

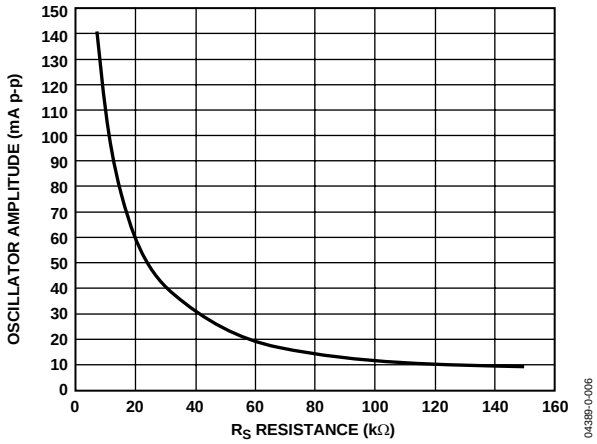


Figure 6. Oscillator Amplitude vs. R_S

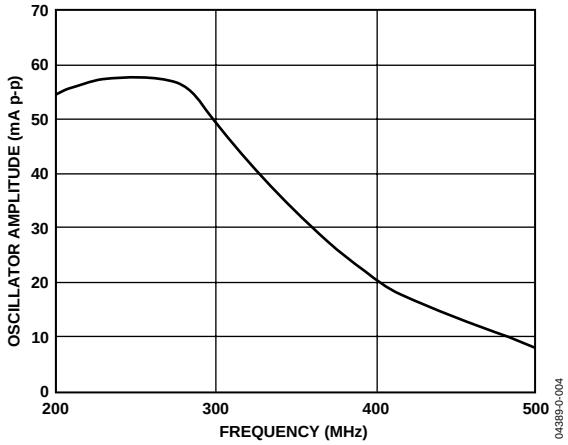


Figure 4. Oscillator Amplitude vs. Frequency

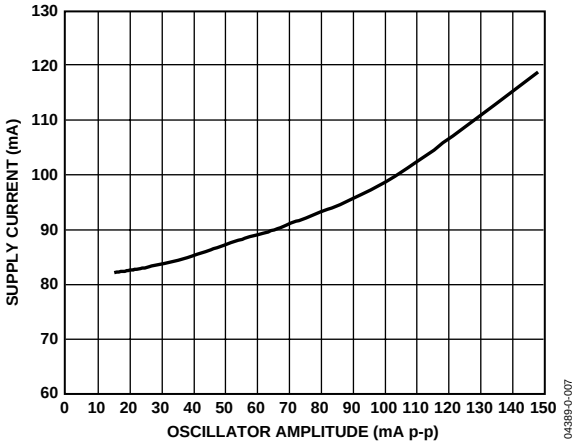


Figure 7. Supply Current vs. Oscillator Amplitude

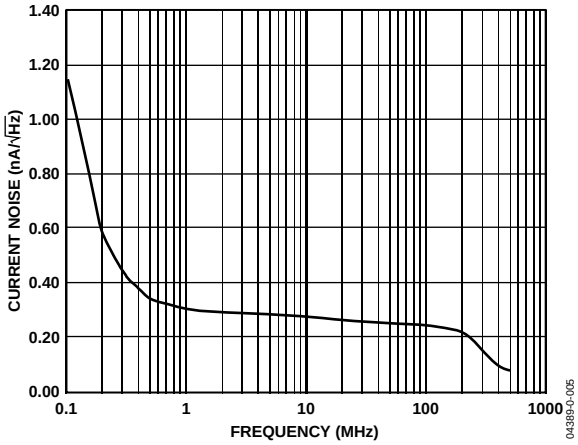


Figure 5. I_{OUT} Current Noise

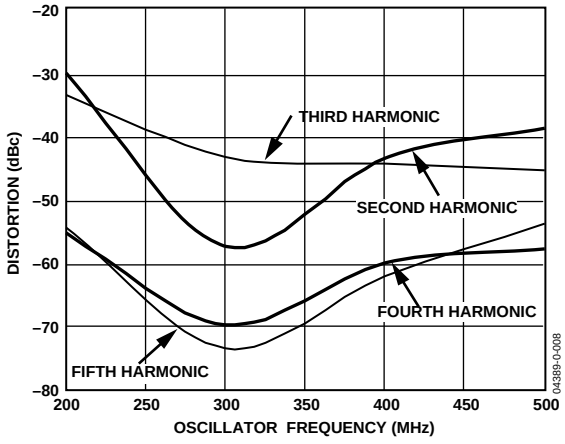


Figure 8. Oscillator Harmonic Distortion vs. Frequency

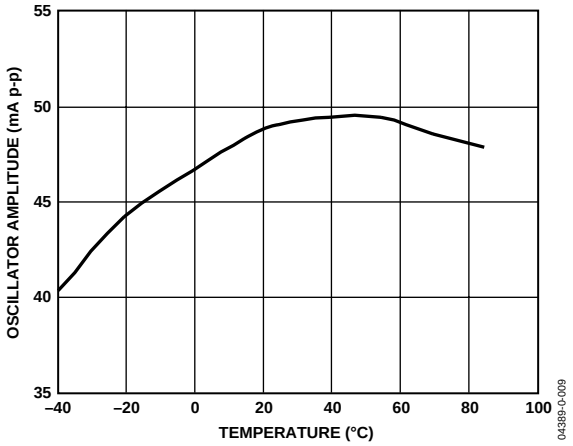


Figure 9. Oscillator Amplitude vs. Temperature

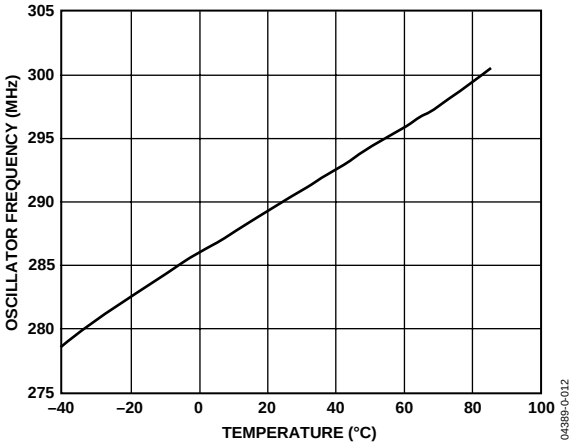


Figure 12. Oscillator Frequency vs. Temperature

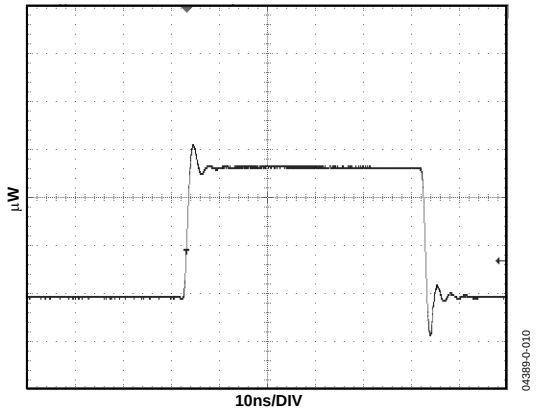


Figure 10. Optical Response 50 mA Read, 50 mA Write2, Sharp GH0781JA2C Diode

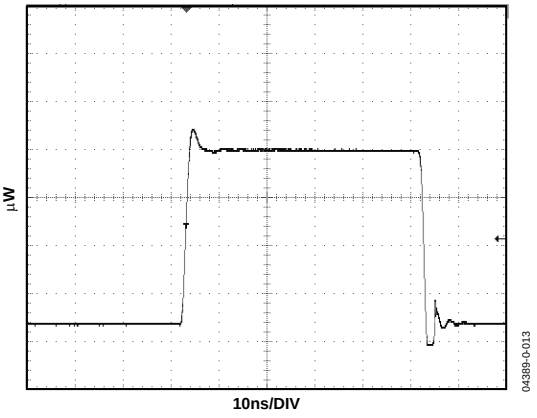


Figure 13. Optical Response 50 mA Read, 200 mA Write3, Sharp GH0781JA2C Diode

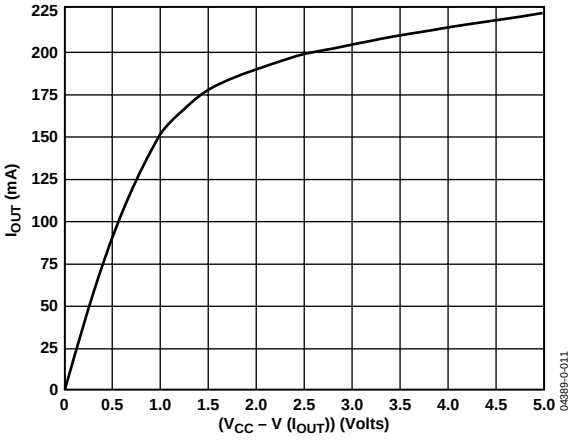


Figure 11. Output Current vs. Voltage Compliance

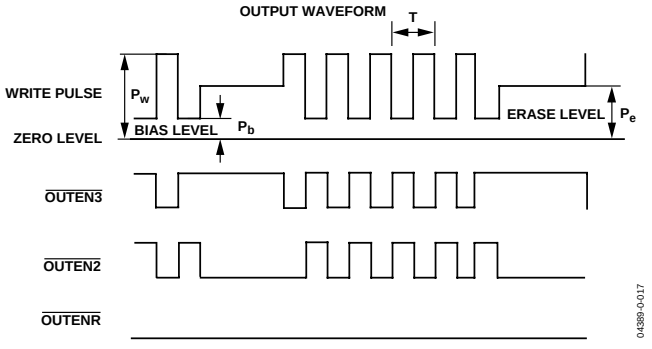


Figure 14. Typical Waveform

Table 4. I_{OUT} Control

ENABLE	$\overline{\text{OUTENR}}$	$\overline{\text{OUTEN2}}$	$\overline{\text{OUTEN3}}$	I_{OUT}
0	X	X	X	Off
1	1	1	1	Off
1	0	1	1	$(I_{INR} \times Gain_R) + I_{OSR}$
1	1	0	1	$(I_{IN2} \times Gain_2) + I_{OS2}$
1	1	1	0	$(I_{IN3} \times Gain_3) + I_{OS3}$

Table 5. Oscillator Control

ENABLE	OSCEN	$\overline{\text{OUTENR}}$	$\overline{\text{OUTEN2}}$	$\overline{\text{OUTEN3}}$	OSCILLATOR
0	X	X	X	X	Off
1	0	X	X	X	Off
1	1	1	1	1	On
1	1	0	X	X	On
1	1	X	0	X	On
1	1	X	X	0	On

APPLICATIONS

The AD9662 uses the current at one or more of its three inputs—I_{INR}, I_{IN2}, and I_{IN3}—and generates an output current proportional to the input currents. Channel R has a typical gain of 135 mA/mA, Channel 2 has a typical gain of 130 mA/mA, and Channel 3 has a typical gain of 260 mA/mA. The input impedance of Channel R and Channel 2 is typically 200 Ω, and the input impedance of Channel 3 is typically 100 Ω. In most cases, a voltage output DAC is used to set the dc current of these channels. A series resistor should be placed between each DAC's output and its respective input channel. These resistors should be chosen to properly scale the input current while not excessively loading the output of the DAC.

Channel R is used to provide bias current to the laser diode, and Channel 2 and Channel 3 are used to set the amplitudes of the current pulses that are required to write or erase the media. The output pulses are created by applying TTL level pulses to the channel enable pins while dc current is flowing into the input pins. Channel 2 and Channel 3 are turned on and off according to a predetermined write strategy (see Figure 14).

Due to the fast rise and fall time (<1 ns) required for the operation of higher speed drives, trace lengths carrying high speed signals, such as ENR, EN2, EN3, and the output current, should be kept as short as possible to minimize series inductance. A decoupling capacitor should be located near each V_{CC} pin, and the ground return for the cathode of the laser diode should be kept as short as possible.

Rise time, t_r, is defined as the time a pulse requires to transition from 10% of its final value to 90% of its final value. Appropriately, fall time, t_f, is defined as the time a pulse requires to go from 90% of its initial value to 10% of its initial value.

Propagation delay is defined as the time when a transitioning logic signal reaches 50% of its amplitude to when the output current, I_{OUT}, reaches 50% of its amplitude.

TEMPERATURE CONSIDERATIONS

The AD9662 is in a 16-lead QSOP. JEDEC methods were used to determine the θ_{JA} of the QSOP when mounted on a highly efficient thermally conductive test board (or 4-layer board). This board is made of FR4, is 1.60 mm thick, and consists of four copper layers. The two internal layers are solid copper (1 ounce/in^2 or 0.35 mm thick). The two surface layers (containing the component and back side traces) use 2 ounces/in^2 (0.70 mm thick) copper. This method of construction yields a θ_{JA} for the AD9662 of approximately 105°C/W. An integrated circuit dissipating 500 mW and packaged in a QSOP, while operating in an ambient environment of 85°C, has an internal junction temperature of approximately 138°C.

$$85°C + 0.500\ W \times 105°C/W = 138°C$$

This junction temperature is within the maximum recommended operating junction temperature of 150°C. Of course, this is not a realistic method for mounting a laser diode driver in an optical storage device. In an actual application, the laser diode driver would most likely be mounted to a flexible circuit board. The θ_{JA} of a system is highly dependent on board layout and material. The user must consider these conditions carefully.

Some of the circuitry of the AD9662 can be used to monitor the internal junction temperature. The AD9662 uses diodes to protect it from electrostatic discharge (ESD). Every input pin has a diode between it and ground, with the anode connected to ground and the cathode connected to the particular input pin. The base-emitter junction of a PNP transistor is used for ESD protection from each pin to V_{CC}. The collector is electrically connected to the substrate of the die (see Figure 15). The base-emitter junction of this transistor can be used to monitor the internal die temperature of the IC.

Using a 10 V source at the enable pin to forward-bias the base-emitter junction and a 1 MΩ resistor to limit the current, a 2-point measurement can be used to calculate the junction temperature of the IC. Because the enable pin (ENABLE) needs to be a logic high for normal operation, the AD9662 can be operated with the 10 V applied through the 1 MΩ resistor.

The first point is obtained by measuring the voltage, V1, with I_{OUT} = 0 immediately after the AD9662 is turned on. The case temperature, T1, can be measured using a thermocouple. The temperature of the case is measured immediately after the IC is turned on, and that temperature is the temperature of the transistor junction and of the die itself. Through characterization of the AD9662, it was determined that the forward-bias voltage of the base-emitter junction of the transistor decreases by 1.9 mV for every 1°C rise in junction temperature.

The second point of the 2-point measurement is obtained when the AD9662 is operated under load. I_{OUT} is adjusted until the increase in supply current is 200 mA. The AD9662 is allowed to reach thermal equilibrium, and then the voltage, V2, is measured.

The voltage measurements taken with the IC running are lower than the actual base-emitter drop across the transistor due to the voltage drops across the internal resistance that is in series with the supply current (see Figure 15). This finite resistance was calculated to be approximately 120 mΩ. Therefore, for a supply current change of 200 mA, the ΔV_{BE} calculation is 24 mV too low. Therefore, 24 mV must be added to the difference in measured voltages. The change in the base-emitter voltage is then calculated.

$$\Delta V_{BE} = (V2 + 24\ mV - V1)$$

The change in junction temperature can then be determined.

$$T_J = T1 + \Delta V_{BE}/(1.9\ \text{mV/°C})$$

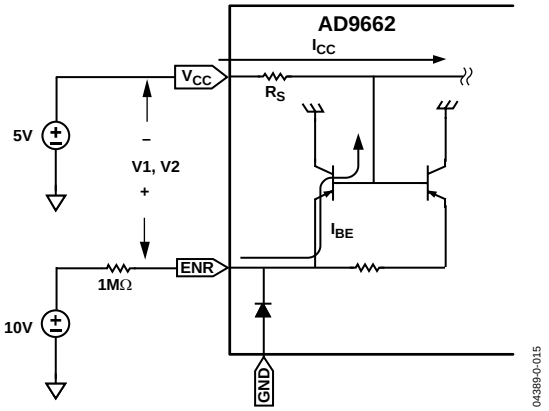


Figure 15. Junction Temperature Measurement Circuit

This 2-point measurement allows the rise in die temperature to be calculated for any given power dissipation. The θ_{JA} of the system can be calculated using the power dissipation of the LDD.

$$P_D = V_{CC} \times I_{CC} - V_{DIODE} \times I_{DIODE}$$

$$\theta_{JA} = (T_J - T1)/P_D$$

Figure 16 shows a graph of the measured voltage between ENR and V_{CC} ($V_{ENR} - V_{CC}$) vs. the die temperature. This graph was constructed using a 2-layer evaluation board for the AD9662 (see Figure 17).

Using the preceding method, actual data was taken to determine the θ_{JA} of the AD9662 in the evaluation board. Immediately after power-up, V1 was measured to be 593 mV. The supply current was 27 mA. The AD9662 was adjusted to deliver 200 mA into a 10 Ω load. This resulted in a total supply current of 244 mA. After allowing the part to reach thermal equilibrium, V2 measured 412 mV. The voltage drop across the 120 mΩ internal resistor due to the change in supply current was then calculated.

$$(244\ \text{mA} - 27\ \text{mA}) \times 120\ \text{m}\Omega = 26\ \text{mV}$$

This 26 mV internal voltage drop was then added to the measured voltage reduction to determine the actual ΔV_{BE}.

$$\Delta V_{BE} = (593\ \text{mV} - 412\ \text{mV} + 26\ \text{mV}) = 207\ \text{mV}$$

The die temperature change measured 82.4°C. The output of the AD9662 was at a voltage of 2 V. The part dissipated an additional 600 mW of power (3 V × 200 mA). The θ_{JA} for the AD9962 mounted on its 2-layer board was calculated to be: 600 mW/82.4°C = 137°C/W.

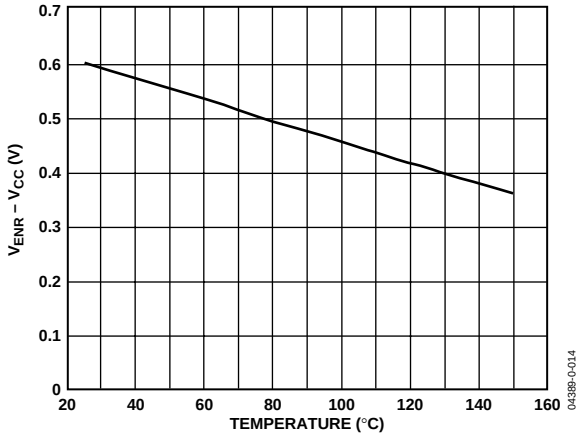


Figure 16. $V_{ENR} - V_{CC}$ vs. Internal Temperature

EVALUATION BOARD

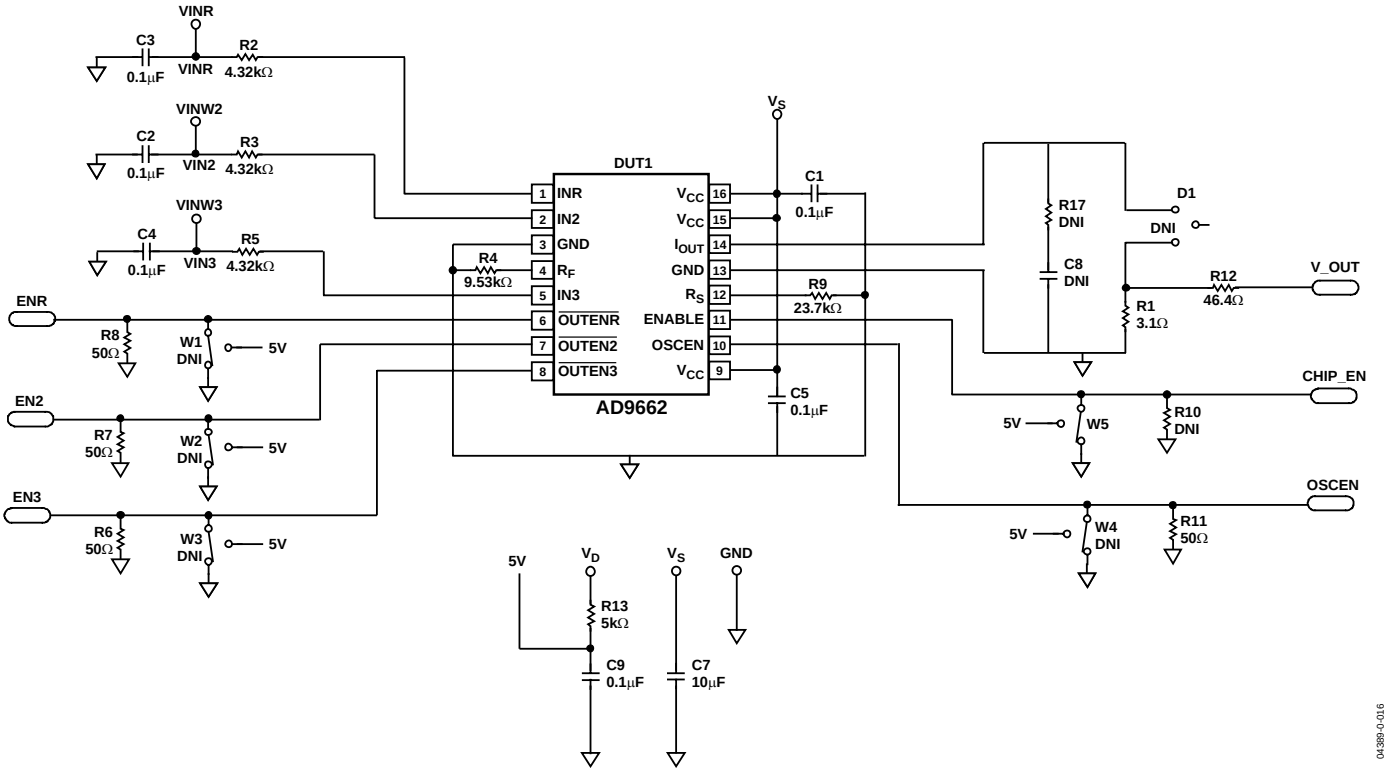
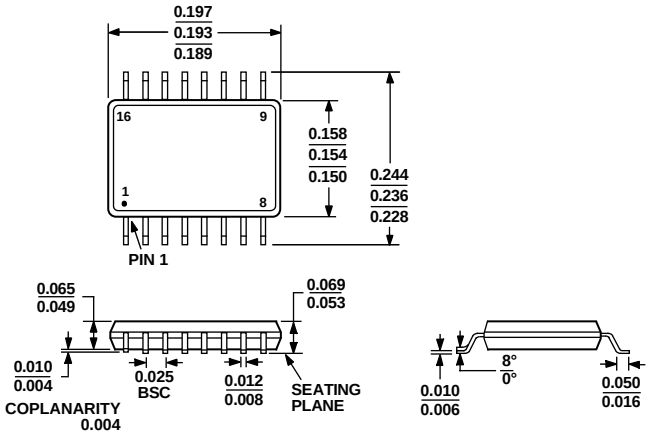


Figure 17. AD9662 QSOP-16 Evaluation Board Schematic

Note: If dc logic levels are desired on the enable pins, then Jumper W1 through Jumper W5 should be used, and Resistor R6 through Resistor R11 should not be installed. If the enable pins are driven from external signal sources, then these resistors should be installed, and the jumpers are not necessary.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AB

Figure 18.16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9662ARQZ[1]	0°C to 85°C	16-Lead QSOP	RQ-16
AD9662ARQZ-REEL[1]	0°C to 85°C	16-Lead QSOP	RQ-16
AD9662ARQZ-REEL7[1]	0°C to 85°C	16-Lead QSOP	RQ-16

[1] Z = Pb-free part.

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C04389-0-11/05(C)

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