CDCM7005-SP Evaluation Module Manual

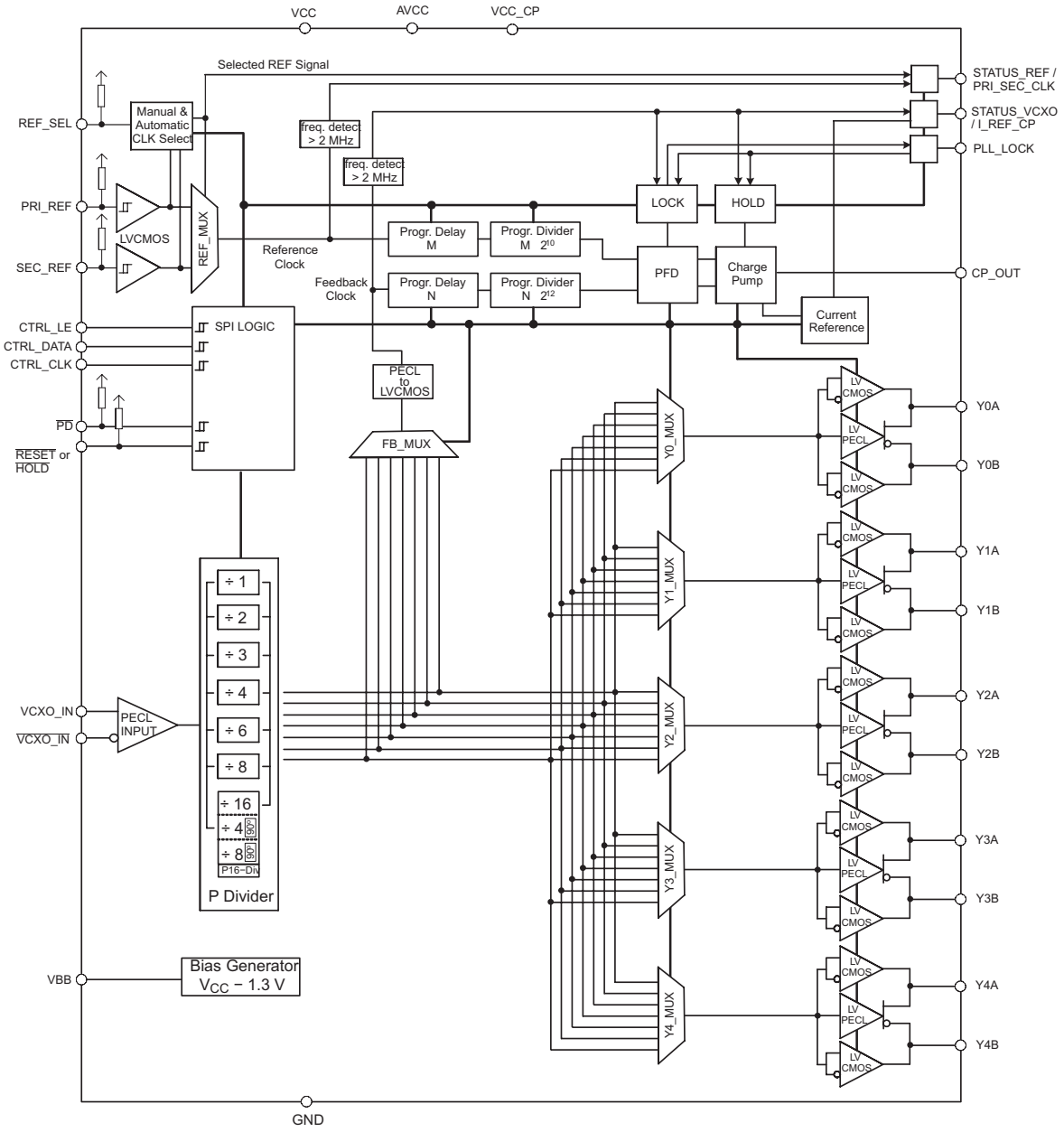
1 Overview

1.1 Purpose

The CDCM7005 is a high-performance, low phase noise and low skew clock synchronizer that synchronizes an on-board voltage controlled crystal oscillator (VC(X)O) frequency to an external reference clock. The device operates up to 2 GHz. The PLL loop bandwidth and damping factor can be adjusted to meet different system requirements by selecting the external VC(X)O, loop filter components, frequency for PFD, and charge pump current. Each of the five differential LVPECL and five LVCMOS pair outputs can be programmed by a serial peripheral interface (SPI). The SPI allows individual control of the frequency and enable/disable state of each output. As the system requires external components like a loop filter and VC(X)O, this EVM provides an easy method to evaluate and modify the performance and parameters of the clock system in conjunction with the specific customer application. Loop bandwidth can be selected as low as 10 Hz or less, allowing the device to clean the system's clock jitter.

In non PLL mode, the CDCM7005 can be used as a simple LVPECL or LVCMOS buffer with divider options.

1.2 CDCM7005 Functional Block Diagram



2 Quick Start

In order to setup the EVM quickly and to take some measurements at default settings, the following actions are required:

- Supply 3.3 V to P1, LED D4 will be on.
- Apply a single-ended reference clock to the reference clock input PRI_REF (pin A1) or SEC_REF (pin B1). For default setting, the reference clock must be 1/8th of the VC(X)O frequency. If REF_SEL is set to 1, then PRI_REF is selected. If REF_SEL is set to 0, then SEC_REF is selected. This selection can be realized via J26 (header 1 and 2 is high; header 2 and 3 is low). **The VCXO installed on the EVM is approximately 491.52 MHz. It may be necessary to adjust the 1/8 frequency applied to the reference clock by small amounts above or below 61.44 MHz to obtain lock.**
- Connect Y0/Y0B (or Y1/Y1B) to oscilloscope in order to check an output signal. Ensure the oscilloscope has 50 Ω to ground termination.

After power up, D1 is on if there is a valid reference clock and D2 is on if there is a valid VC(X)O clock for the CDCM7005. If D3 turns on, then the reference clock and the VC(X)O clocks are phase locked.

3 EVM Hardware

This chapter discusses the EVM hardware.

3.1 Board View and Connector Location

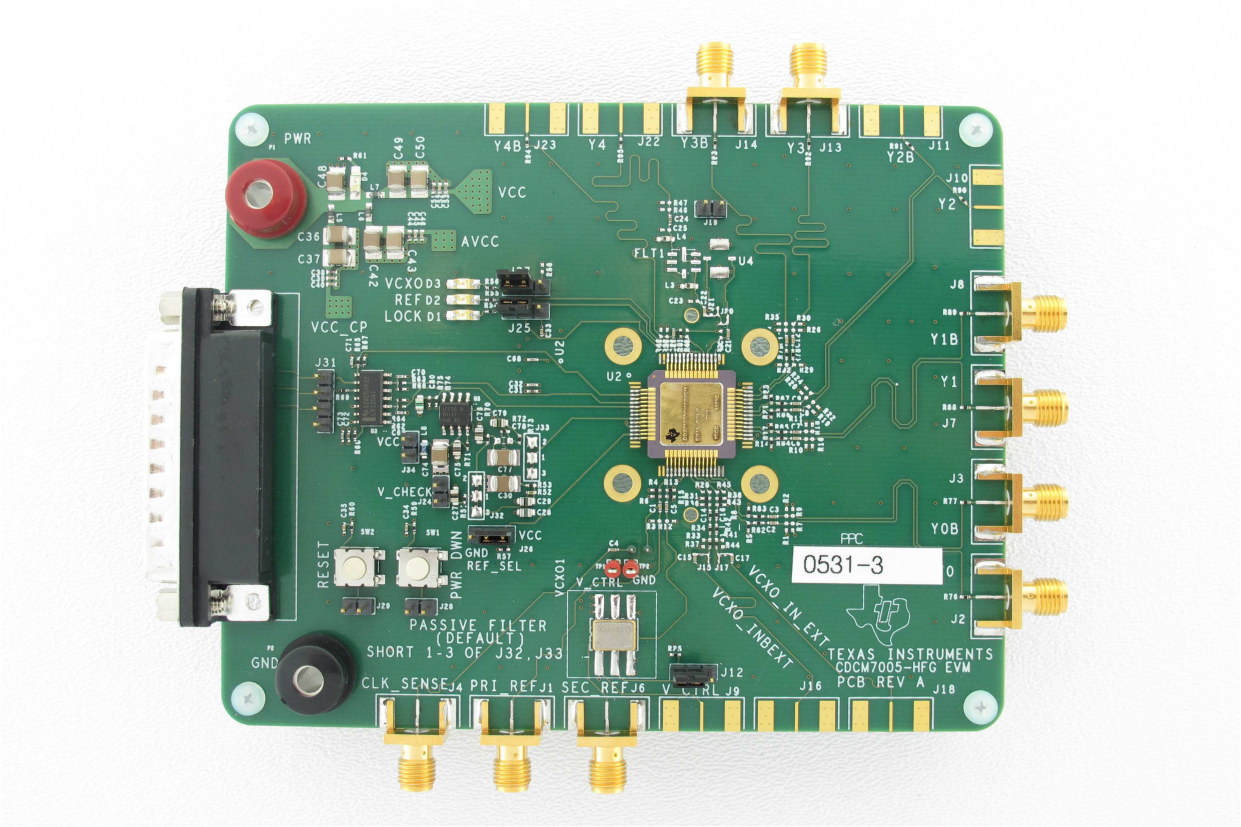


Figure 1. Board View

3.2 Hardware Configuration

This section describes the board configuration using on-board jumpers and solder bridges.

3.2.1 Power Supply (P1, P2)

- Supply 3.3 V ±10% on P1 and P2 using a stabilized external power supply.

WARNING

Never supply more than 3.6 V on P1.

3.2.2 Onboard Switches and Indicators (SW1−SW2, D1−D4)

- Push SW1 to enter the power-down mode of the CDCM7005 device. Then all current sources are switched off, all outputs are switched into 3-state, and all dividers (M, N, and P) are reset to default.
- Push SW2 to enter the reset mode of the device. The charge pump (CP) is switched to 3-state and all counters (N, M, P) are rest to zero (the initial divider settings are maintained in SPI.
- The three status outputs of the CDCM7005 are fed to LED indicators. D1 on indicates a valid reference input clock signal. D2 is on if the VC(X)O input clock is valid and D3 turns on if the PLL has been locked.
- D4 indicates power supply.

NOTE: In case of a low input impedance of the VC(X)O control voltage input, there is a possibility D3 may not turn on to indicate locking.

3.2.3 Programming Interfaces (J30, J31)

The SPI of the device is used for writing to the control register of the device. It consists of three control lines CTRL_CLK, CTRL_DATA, and CTRL_LE. There are four 30-bit wide RAM registers, which can be addressed by the two LSBs of a transferred word. Every transmitted word must have 32 bits, starting with MSB. After supplying power or activating the power-down mode, the registers are loaded with the device default values internally (see the CDCM7005 data sheet, SGLS390). However, if specific register settings are required for any applications, there are two ways to program the device externally:

- Connect the parallel port cable to the PC and EVM parallel port. This needs control S/W (see Chapter 4).

3.2.4 Loop Filter (J32−J34)

The loop filter is one of the key elements determining the loop bandwidth of the PLL. The loop filter converts the charge pump current into the control voltage for the voltage controlled oscillator. The phase difference between the input clocks of the phase frequency detector determines the width of the charge pump output current pulses. These high frequency pulses are transformed into a voltage to control the oscillator.

Basically, two types of loop filters are implemented on the EVM.

- Passive loop filter
- External active loop filter using an external low-noise OPA

Filter types can be selected by soldering bridges J32−J34, see Table 1. Control voltage of the VC(X)O can be measured at J9 or TP1. If an external OPA is used, it needs to be switched on by connecting J34. For example, passive filter operation is provided when pads 1 and 3 of J33 are solder bridged and pads 1 and 3 of J32 are solder bridged.

Default setting: Passive Loop Filter

Table 1. Filter Configurations

BRIDGE	PASSIVE FILTER	ACTIVE WITH AN EXTERNAL OPA
J33	1-3	1-2
J34	Open	Closed
J32	1-3	1-2

3.2.5 High-Speed Outputs and Inputs (J1−J4, J6−J11, J13, J14, J22, and J23)

The CDCM7005 drives five differential LVPECL outputs. All PECL outputs are ac-coupled and terminated with 150 Ω to GND. This is in contrast to typical LVPECL termination, which requires V_{CC} − 2 V as termination voltage. The reason is to simplify the power supply scheme. The device output's trace impedance is 50 Ω and traces are matched in length. All outputs have options for pullup and pulldown resistors.

When the CDCM7005 is powered up, it defaults to five LVPECL outputs. However, this EVM is configured as follows:

- Y0 − Y2 = LVPECL
- Y3, Y4 = LVCMOS (in addition Y4 has an option for a custom filter)

The reference input clock signal has to be applied to J1 or J6. The reference input clock signal can be sensed on J4. In this case, close the bridge J5 (the oscilloscope's 50 Ω may be used to terminate the 50-Ω trace). The reference input clock sense line is matched to the LVPECL outputs line to avoid any additional delay offset. The input is ac-coupled (C4).

3.2.6 VC(X)O Inputs and Outputs (J16−J18)

The CDCM7005 requires an external VC(X)O in order to complete the PLL loop. The VC(X)O adjusts the frequency and phase depending on the control voltage level coming from the loop filter and provide the input clock to the LVPECL block.

Another option would be to use an external source via J16 and J18.

3.2.7 AC-Coupling at PRI_REF (C1, R4, R6) and SEC_REF (C5, R13, R15)

An ac-coupling is provided at PRI_REF and SEC_REF to ease the use of the CDCM7005 with different signaling levels (LVCMOS, LVPECL, LVDS). However, the ac-coupling will increase the PLL stabilization time after power up due to transient effects. It also increases the switching time between PRI_REF and SEC_REF in case of automatic reference clock switching. Therefore, the ac-coupling must be removed for optimized system performance (C1 and C5 has to be replaced with a 0-Ω resistor and R4, R6, R13, and R15 have to be removed).

4 Serial Peripheral Interface (SPI) Software

This chapter discusses the serial peripheral interface software.

4.1 Functional Description

Programming software here as described is intended for programming the internal control register of the CDCM7005. The software runs under Windows® 2000 / XP / XP *64 (1). A quick installation is required prior to use. See the Software Installation section.

There are several cases where programming is mandatory.

As a rule of thumb here are some examples:

- Use of active loop filter
- Change of divider ratio or disable of certain LVPECL/LVCMOS outputs
- Select between LVPECL or LVCMOS output
- Change of phase offset, (Delay M/N), or selection of 90° or 180° phase shift
- Change of charge pump output current
- Widening the lock detect window

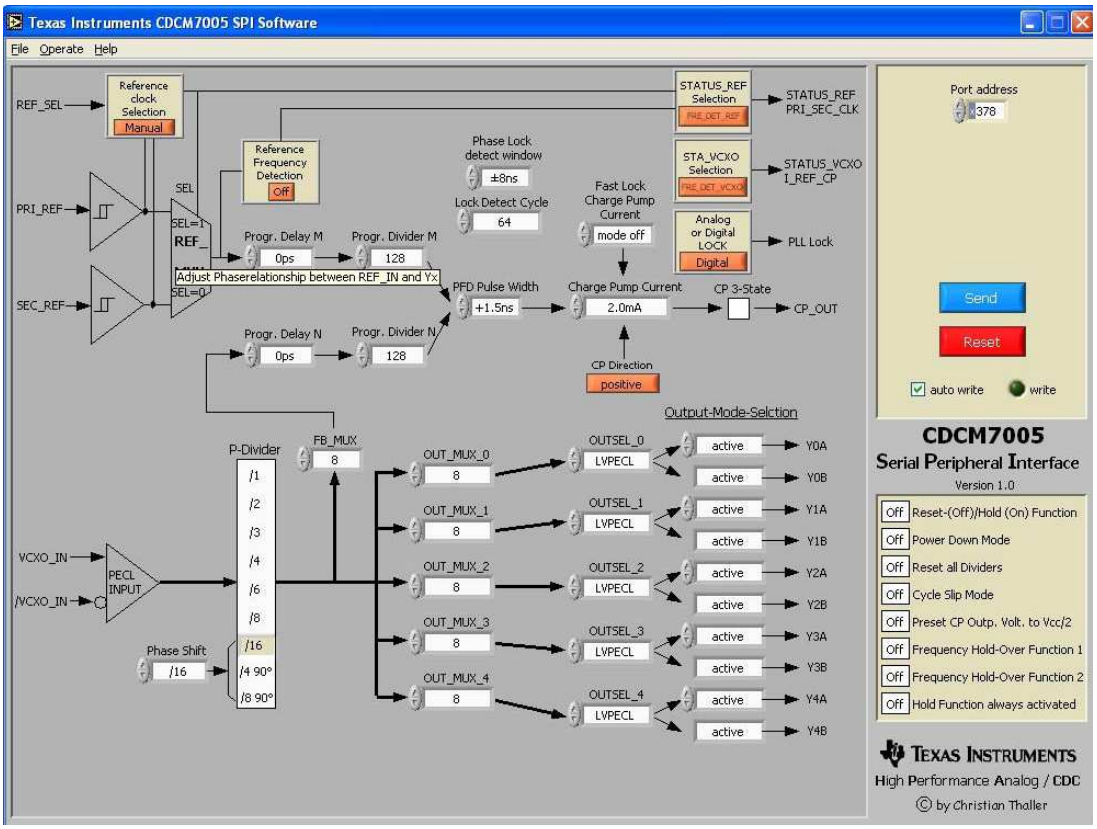


Figure 2. Screen View

(1) Windows is a registered trademark of Microsoft Corporation

4.2 Software Installation

Follow the steps below in order to install the SPI control software:

1. Download the CDCM7005 SPI Software from the TI Website (www.ti.com)
2. Run program setup.exe
3. Reboot your computer
4. Run the software from Start → Programs → CDCM7005 SPI

5 Application Circuit Diagram

This chapter discusses the two loop filter configurations.

5.1 Passive Loop Filter

The passive loop filter is a second order filter (two poles, one zero). The zero is required for the overall loop stability. R1, C1, and C2 generate the dominant pole of the system. A second pole is introduced by R2 and C3.

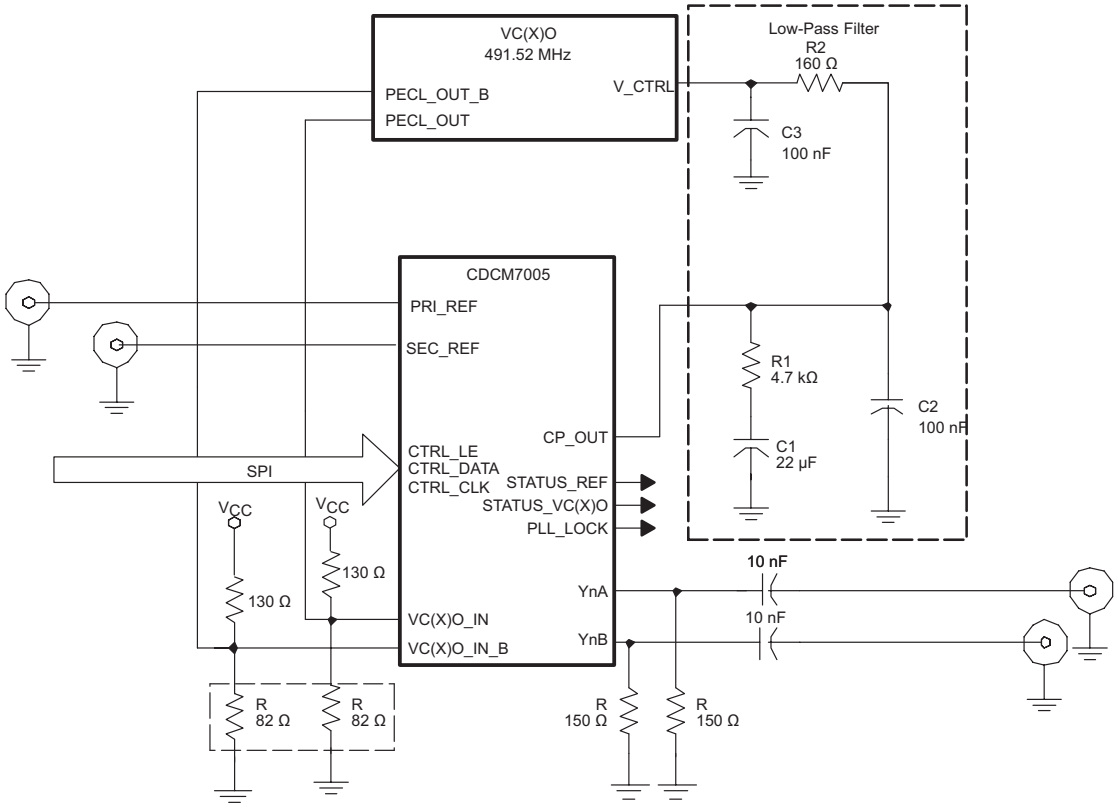


Figure 3. CDCM7005 With a Passive Loop Filter Configuration

5.2 External Active Loop Filter Using OPA341

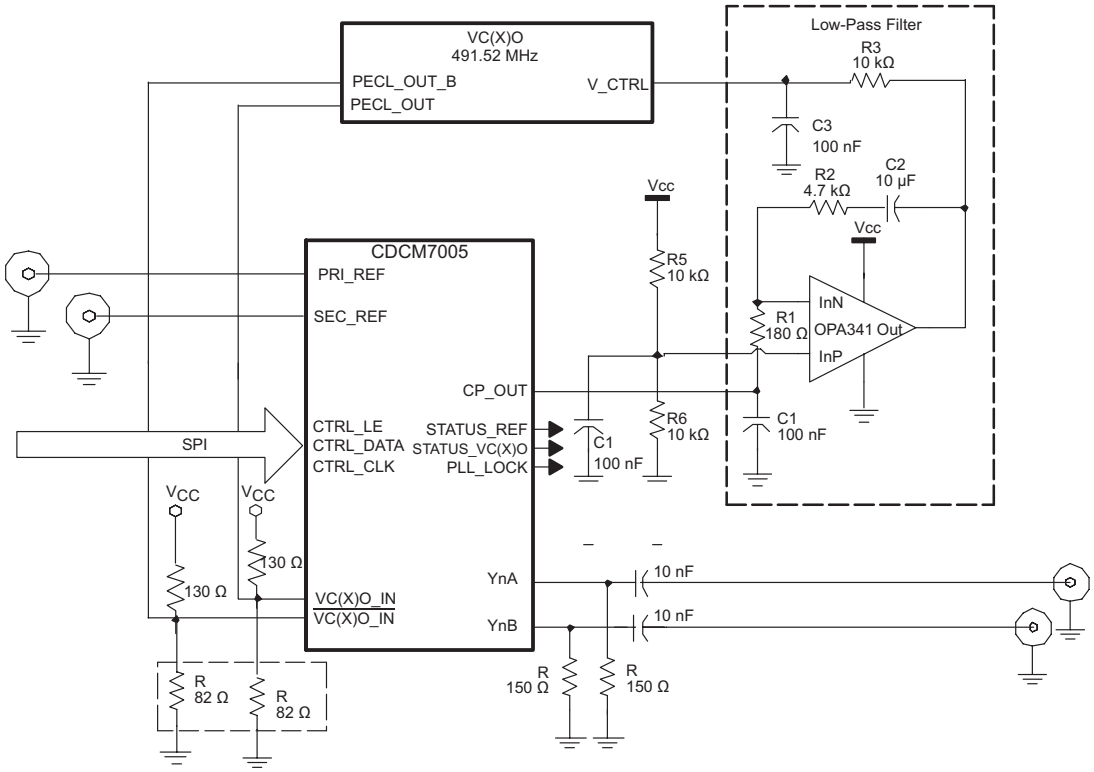


Figure 4. CDCM7005 With a External Active Loop Filter Using OPA341

6 Board Layout

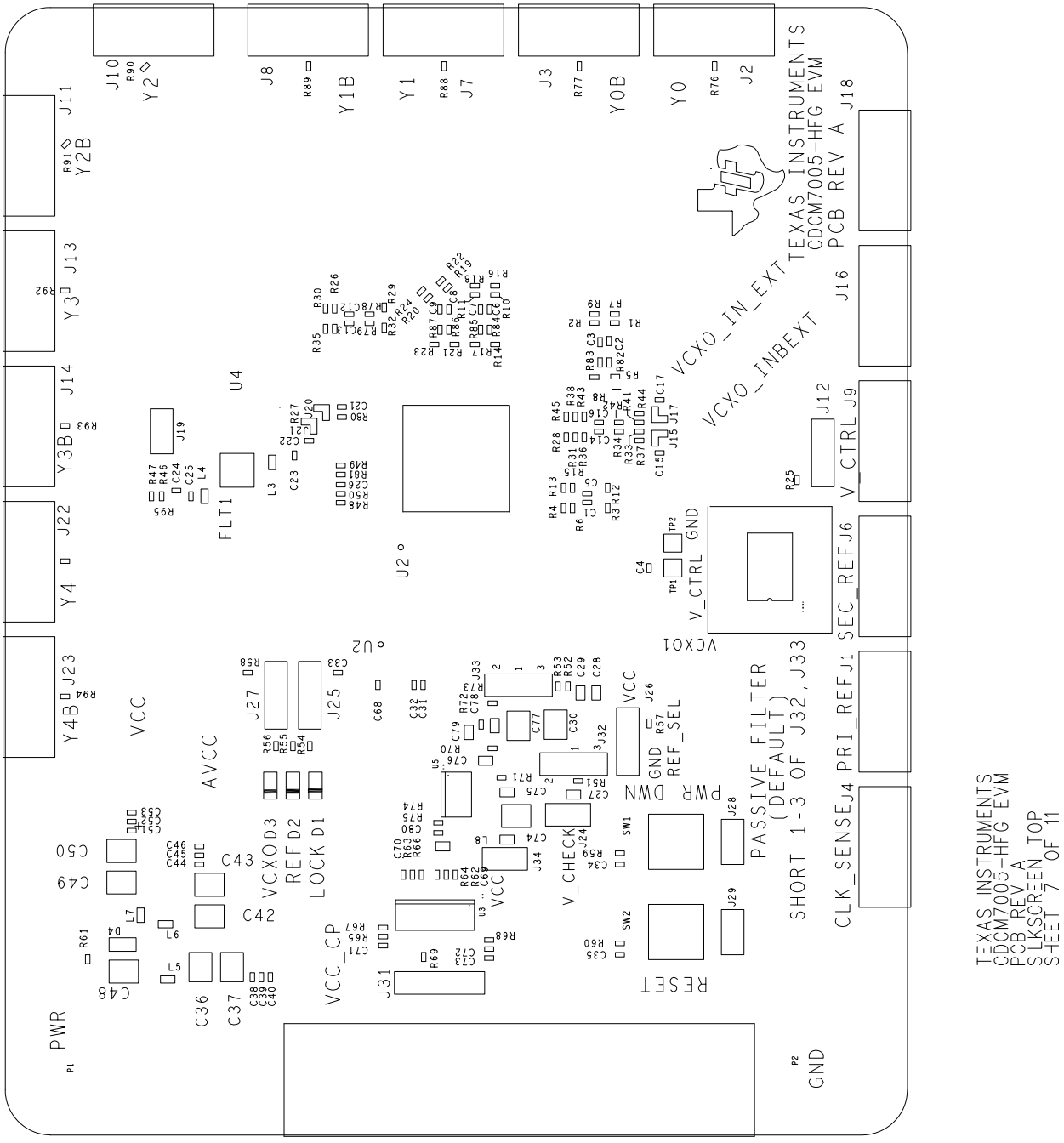


Figure 5. Component View and Silkscreen (Top View)

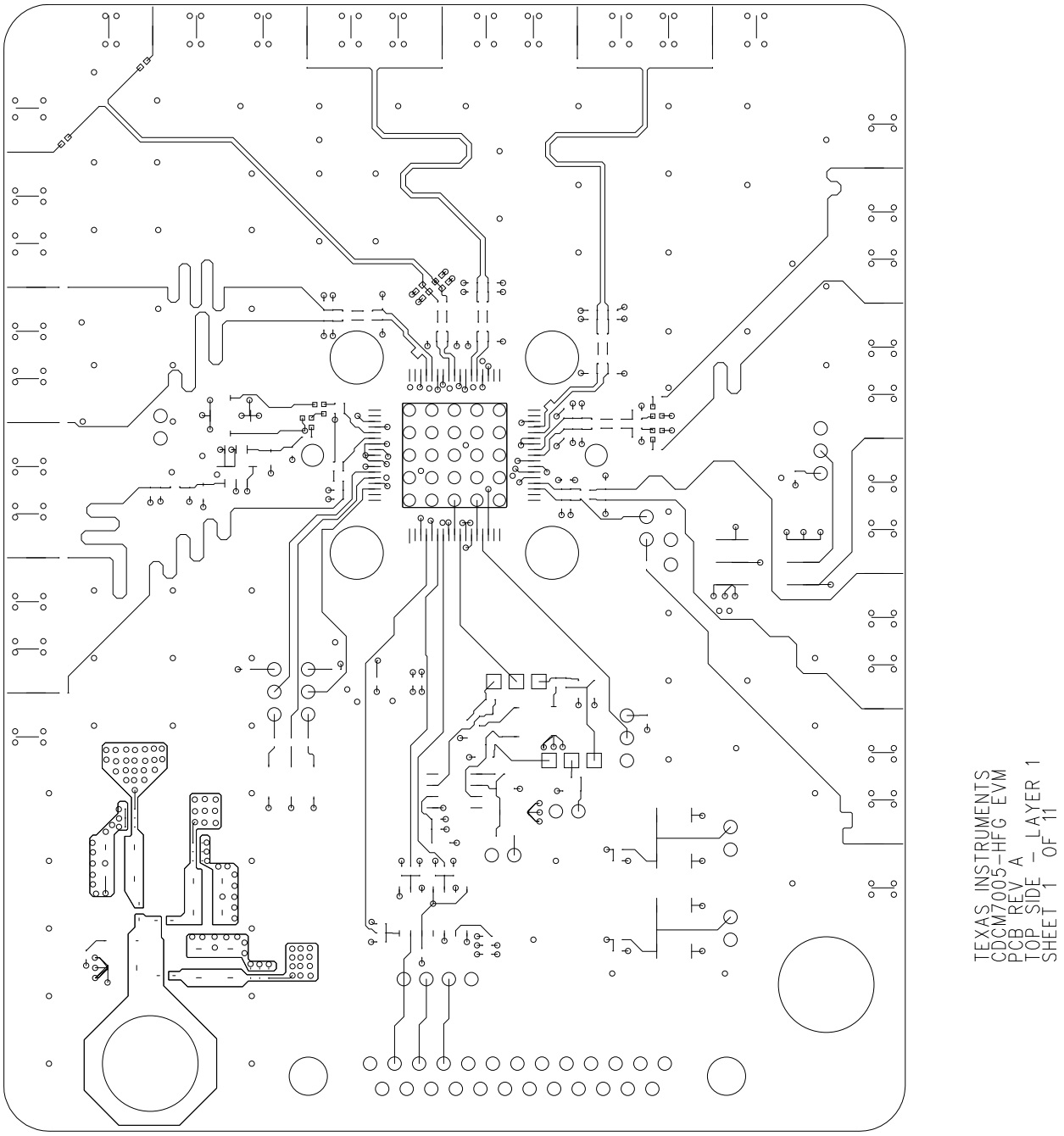


Figure 6. Top Layer View

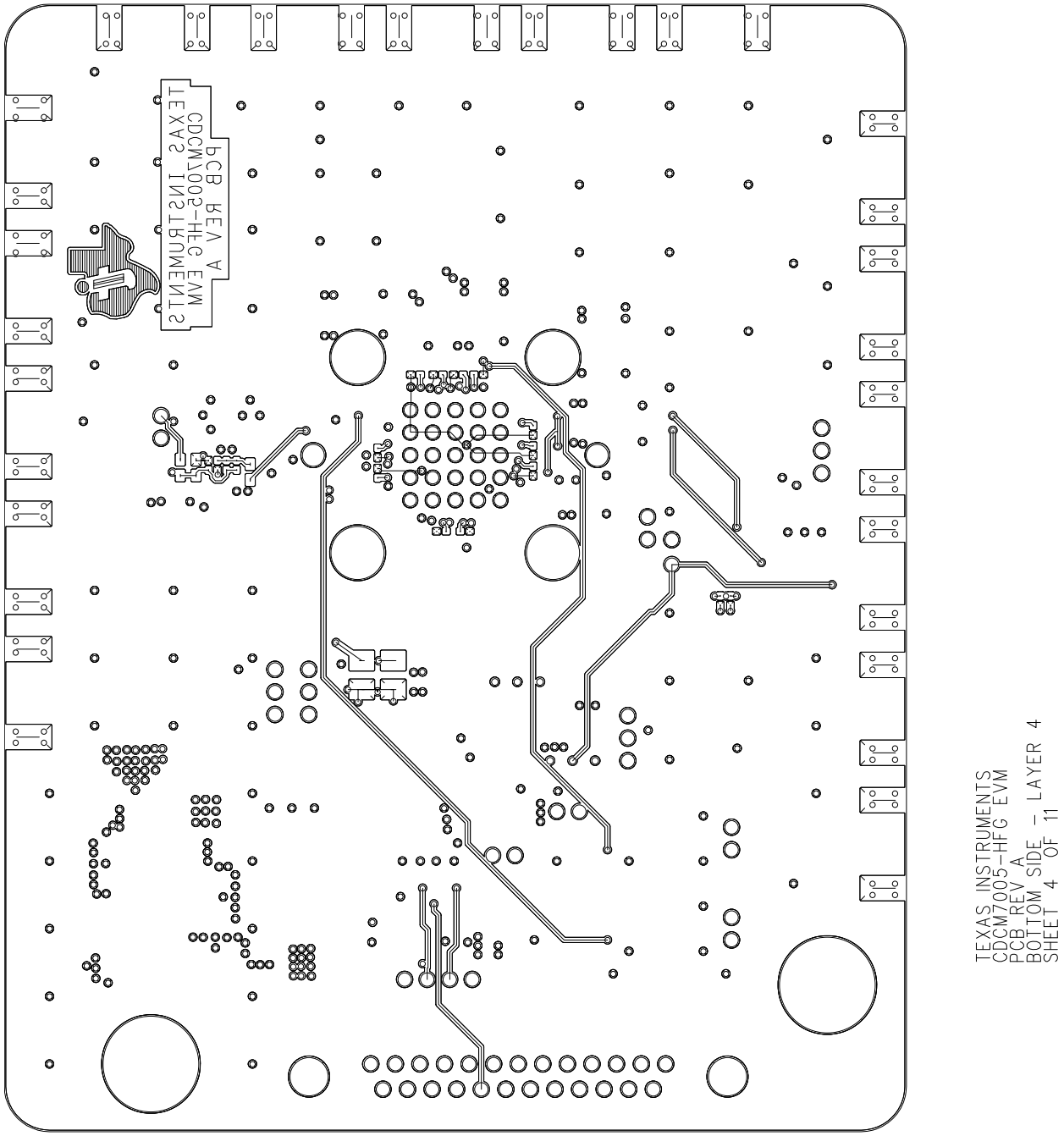


Figure 7. Bottom Layer View

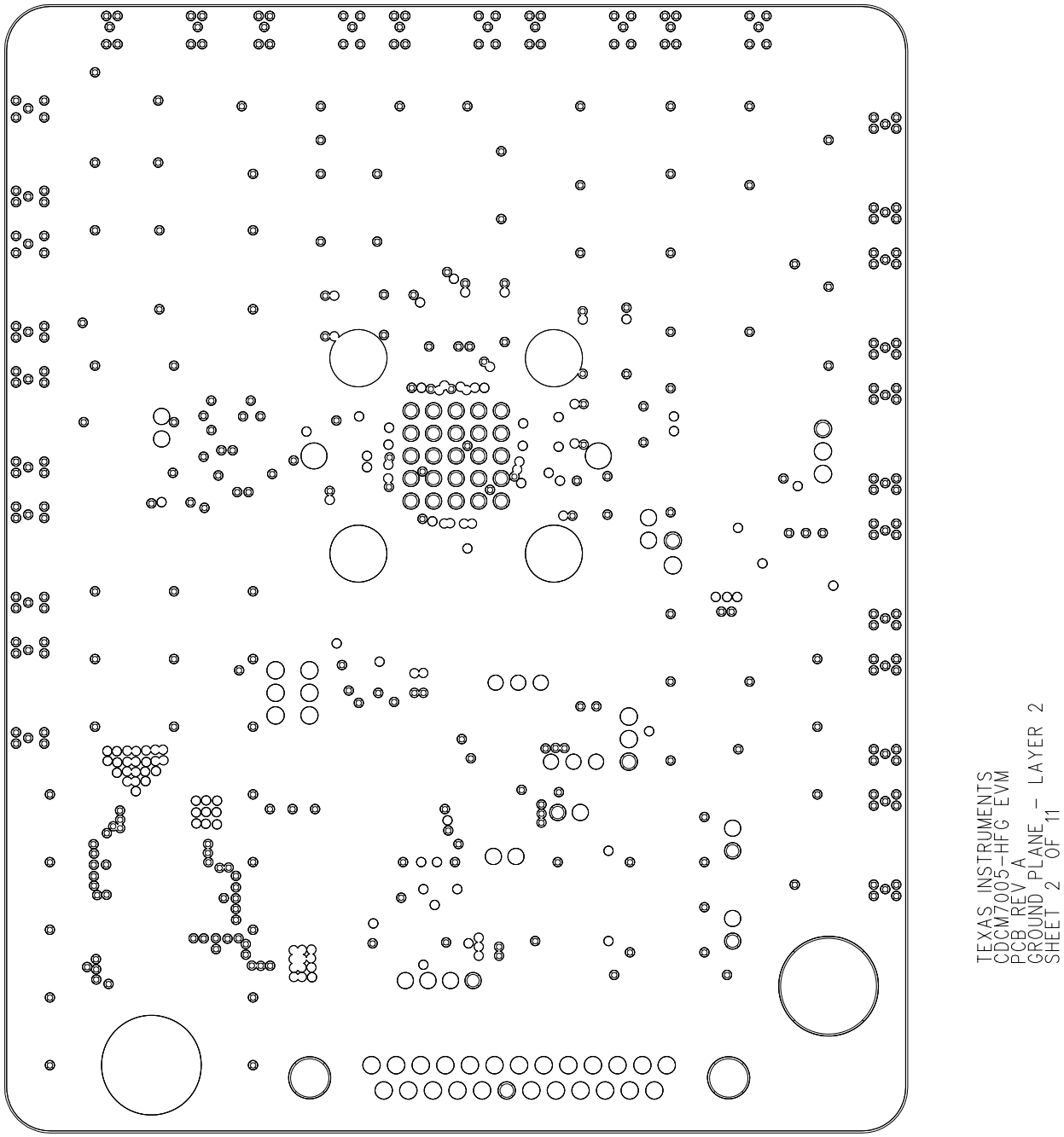


Figure 8. Ground Plane View

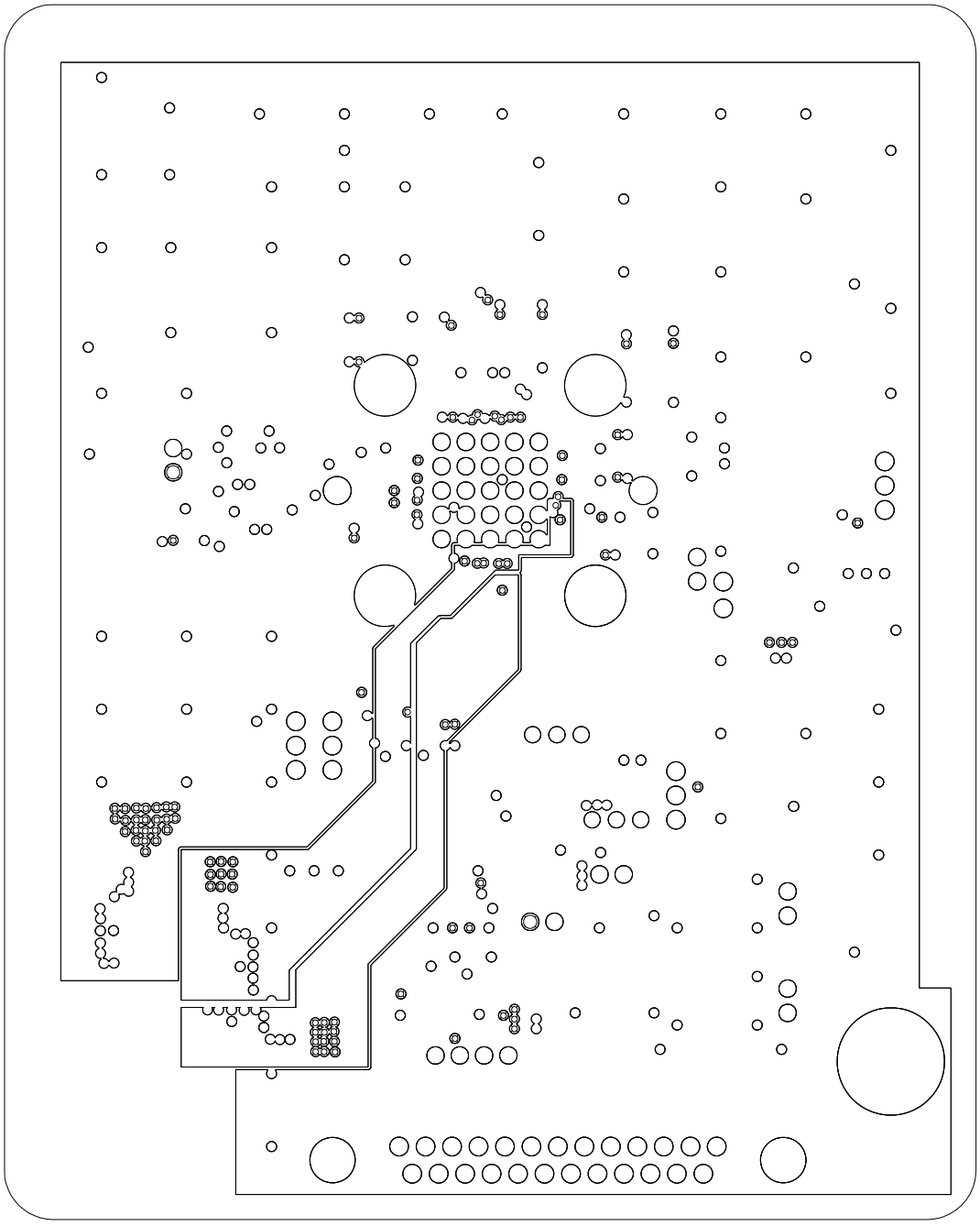
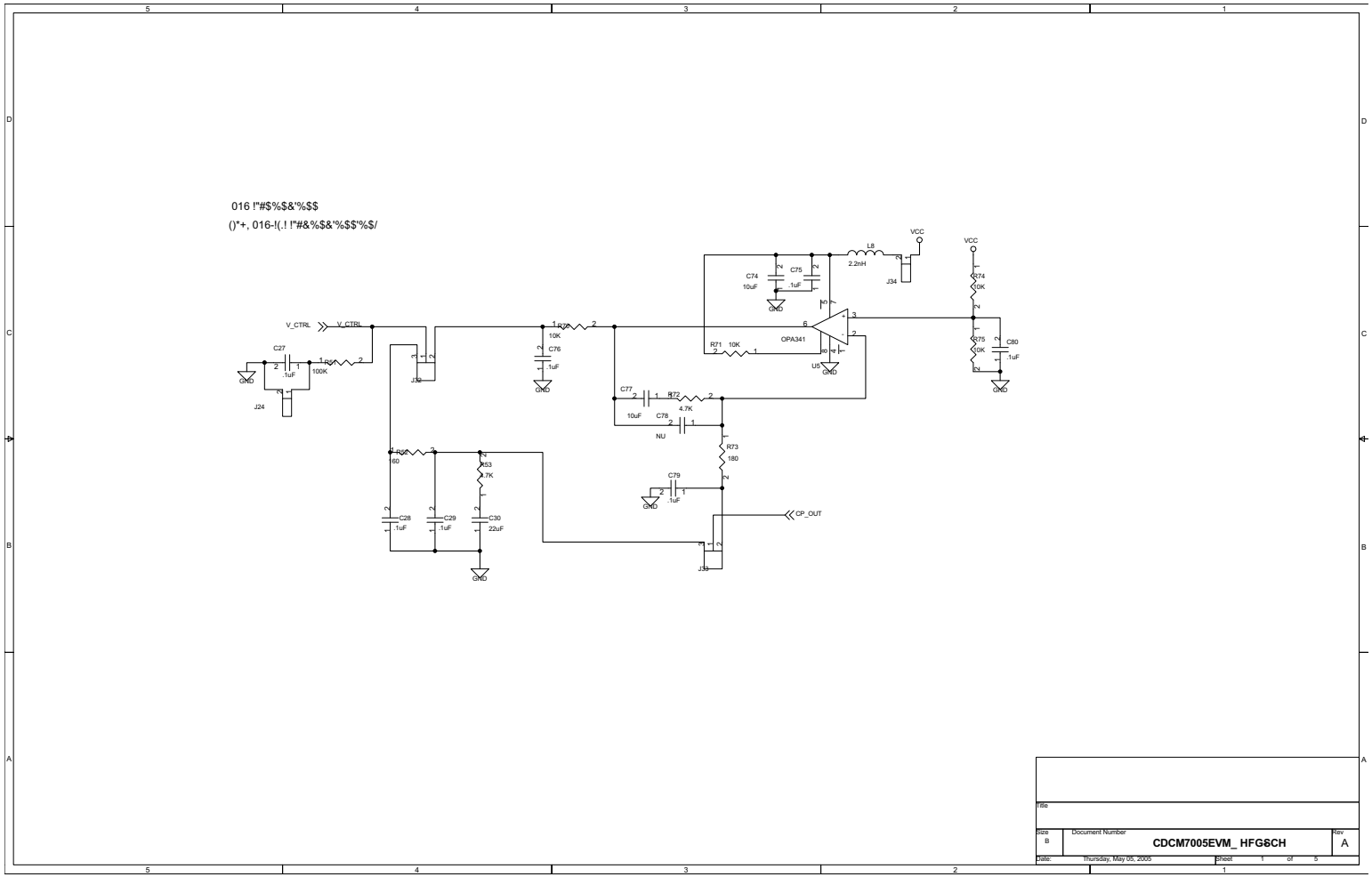
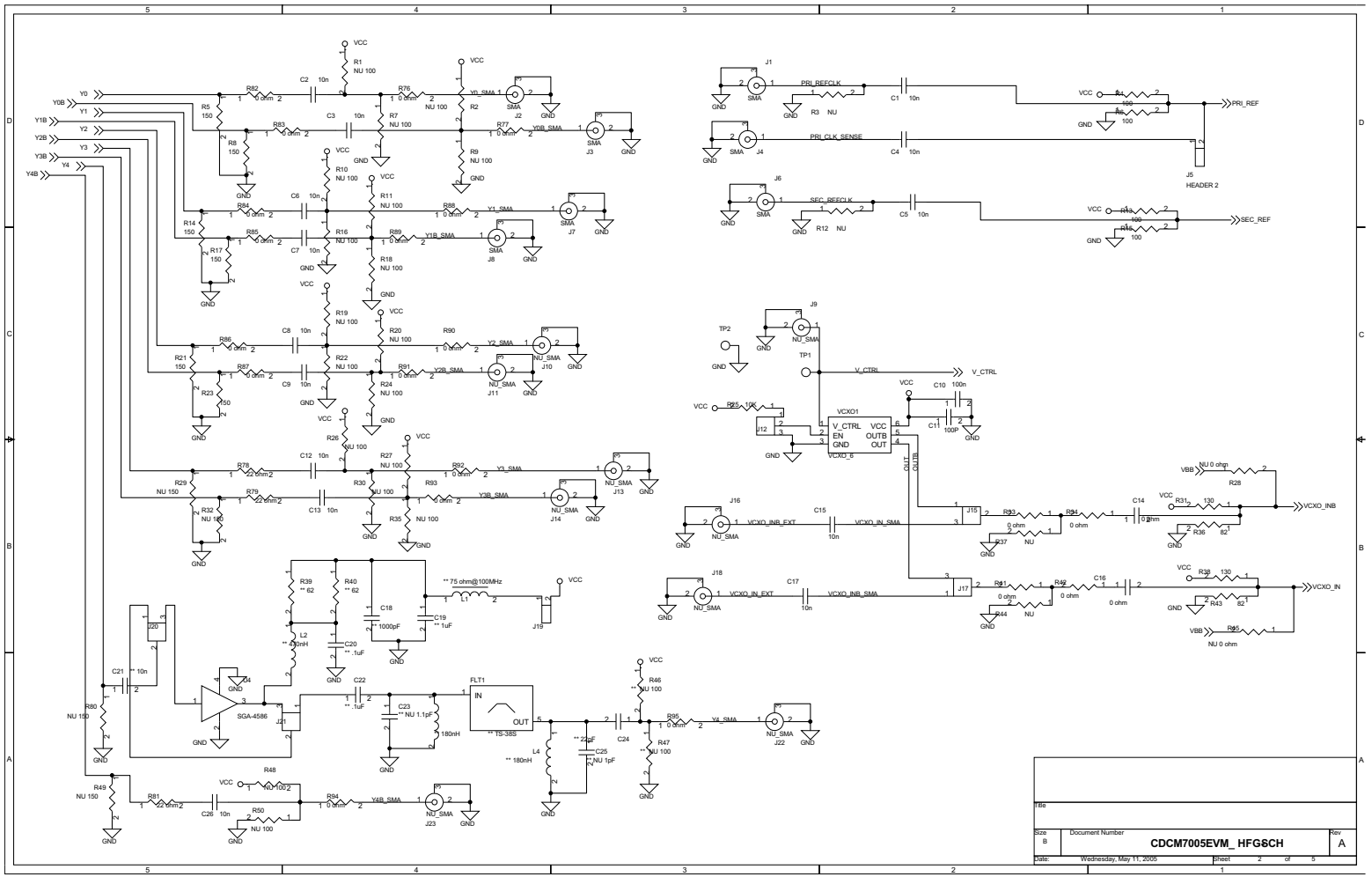


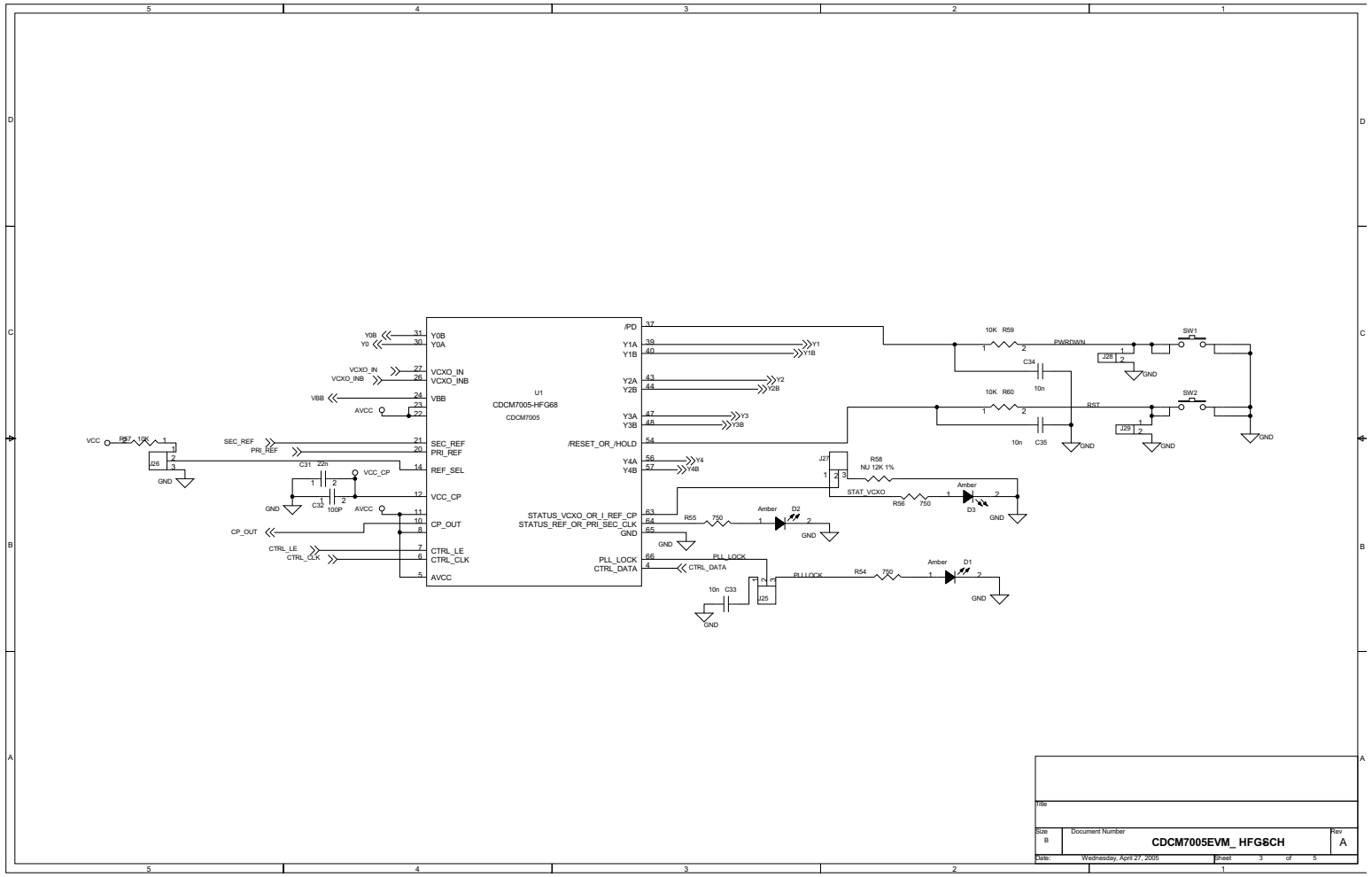
Figure 9. Power Layer View

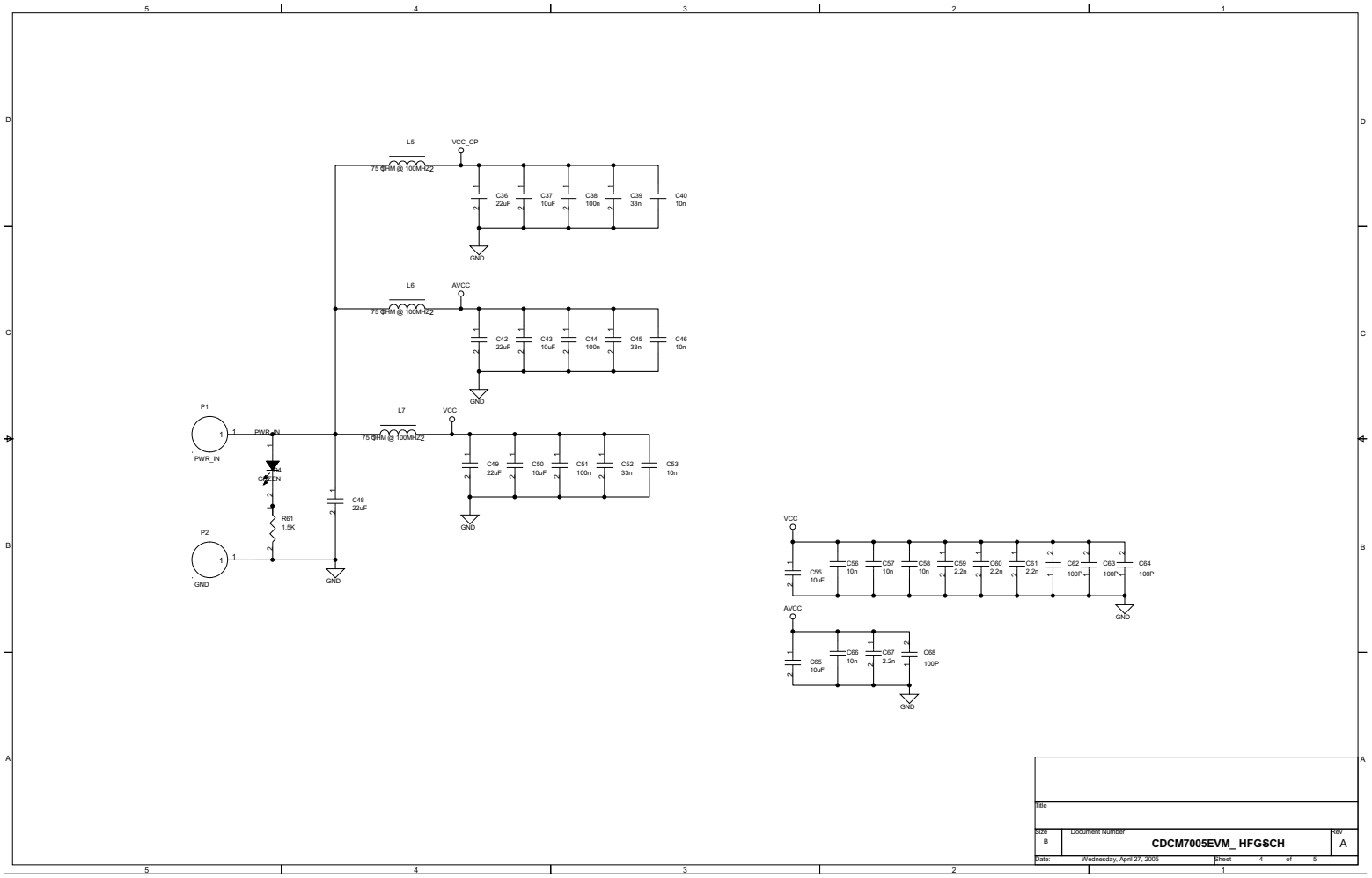
7 Schematics

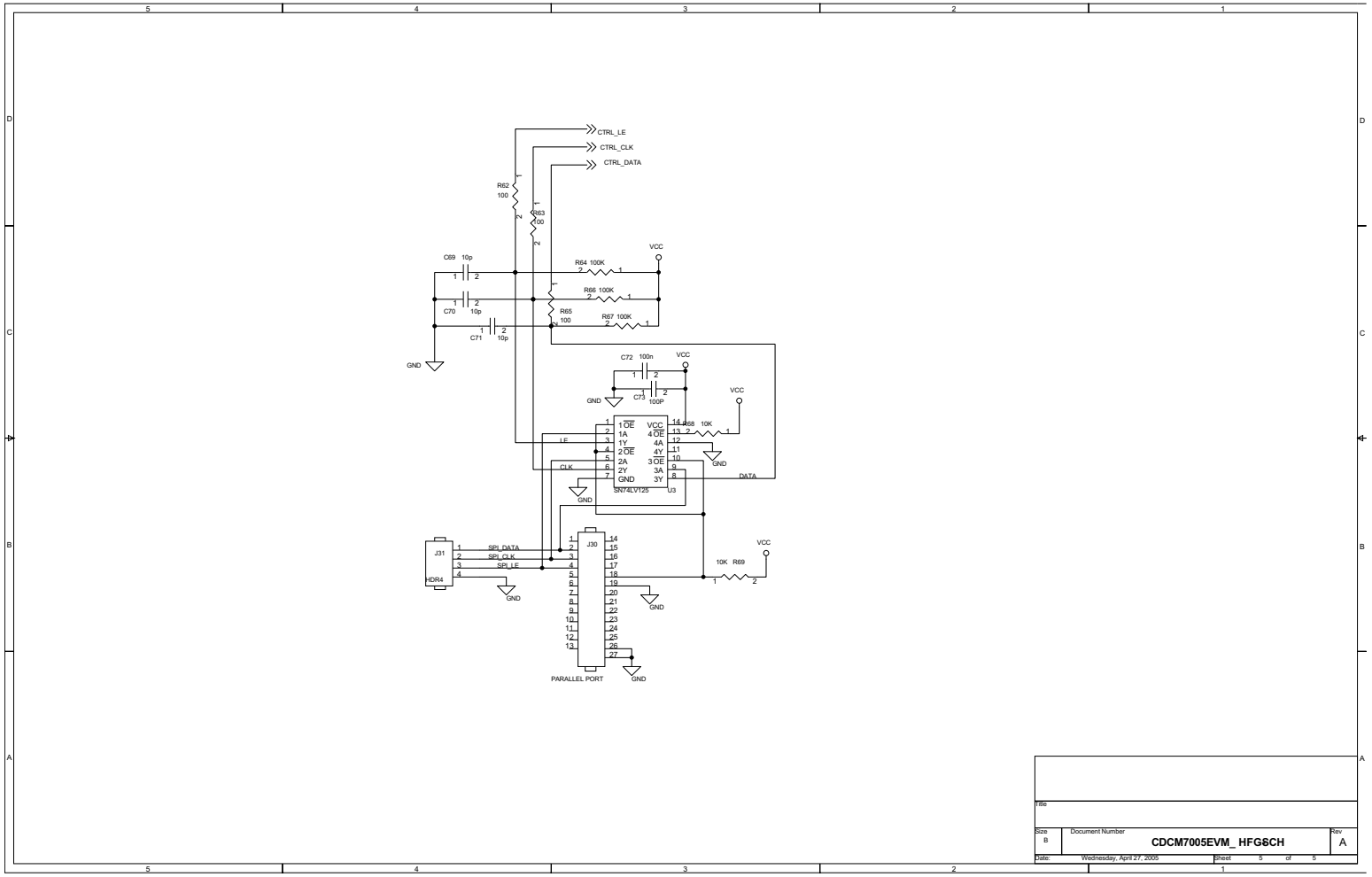
See the following pages for the CDCM7005 schematics.











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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

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