



EQCO30T5.2: 3G/HD/SDI Video Cable Driver

1.1 Introduction

The EQCO30T5 is a video cable driver for 3G/HD/SDI video with speeds up to 4.0 Gbps. It is designed to be a direct replacement for competing cable drivers. On top of this downlink functionality from camera to frame grabber, it further allows to receive in this chip a 5 Mbps uplink signal going from the frame-grabber to the camera. Also power can be provided over the same cable using the same chip and a few external components. The device operates with 8B/10B coded signals up to 4.0 Gbps and with SMPTE signals up to 3.0 Gbps.

1.2 Applications

This solution is useful and economical for many markets and applications, including the following:

- High Definition, high frame rate Pro-video HD/SDI frame store
- Surveillance, industrial/inspection, medical video inputs

1.3 Features

- Compatible with all SMPTE 3G-SDI data-rates
 - SMPTE 259M – SDI - 143 to 360 Mbps
 - SMPTE 344M – 540 Mbps
 - SMPTE292M - HD-SDI – 1.485 Gbps
 - SMPTE372M – dual link HD-SDI – 2.97 Gbps
 - SMPTE424M– dual speed HD-SDI - 2.97 Gbps
 - Supports DVB-ASI at 270 Mbps
- Pin compatible to Gennum and National Semiconductor parts
- Loss of signal detect at input, optional 3 dB input trace receive equalization
- Also operates with 8B/10B coding
- Single 3.3 V supply.
- Low Power 150 mW @ 3.3 V
- Output driver enable
- Selectable slew rate for SD and HD/3G
- -40 °C to + 85 °C temperature range
- 16-pin, 0.65 mm pin pitch, 4 mm QFN package
- Pb-free and RoHS compliant
- LF-Uplink receiver included , receiving 5 Mbps in full duplex communication for cable lengths in 0-450 m range (Belden1964A)
- up to 900 mA can be received for powering camera devices

The EQCO30T5 cable driver can be used in combination with the EQCO30R5 video equalizer.. This device also has the capability to transmit the uplink signal whilst other key parameters remain complying to the SMPTE specifications. Ask EqcoLogic for the EQCO30R5 datasheet.

2 Functional Description

2.1 Overview

The EQCO30T5 is a dual slew rate cable driver, designed to drive digital signals over coaxial cable. The EQCO30T5 chip is optimized for driving SMPTE HD/SDI signals but works equally well with 8B/10B coded signals.

The EQCO30R5 is a video equalizer that matches to the EQCO30T5 since it can transmit the uplink signal. Implementing the uplink requires very few additional components on both sides of the link and complies with the SMPTE specifications. The EQCO30T5 datasheet is available separately from EqcoLogic.

Figure 1 shows a typical communication link using the EQCO30T5 and EQCO30R5 chips:

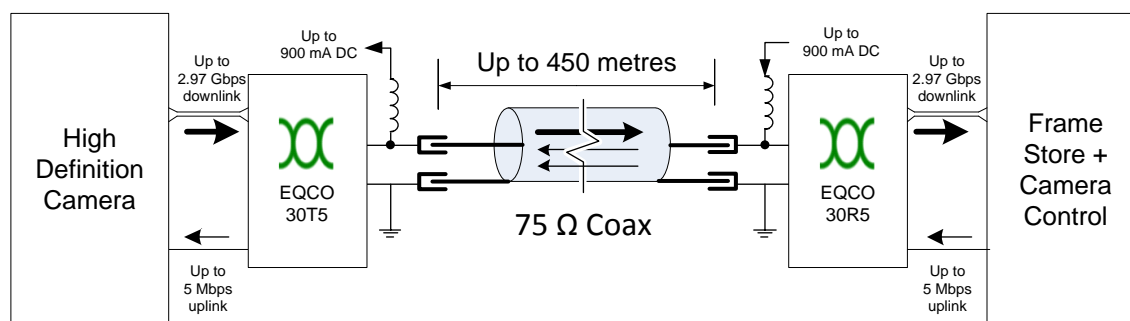


Figure 1: Typical EQCO30T5/EQCO30R5 set-up

The EQCO30T5 includes an uplink receiver for receiving digital data coming from the frame store in full duplex, giving 5Mbps of bandwidth for

- Triggering purposes, Auxiliary outputs
- Firmware upgrades,
- Audio channels
- Etc..

Figure 2 shows a block diagram of the EQCO30T5 showing electrical connections. The *input Pre-driver* brings the input signal to a digital signal, with or without the use of input trace equalisation. The level of the input signal is compared in the *Transmit Detection* part to a reference level for generating the LOS signal. The *active splitter/combiner/driver* launches the digital signal in the cable, with an amplitude determined by the external resistor connected to Rref and with an edgerate for SD or 3G/HDSDI depending on the SD/HDB signal. It also splits of the incoming signal towards the *LF receiver* for providing the *LFout* signal of 5 Mbps.

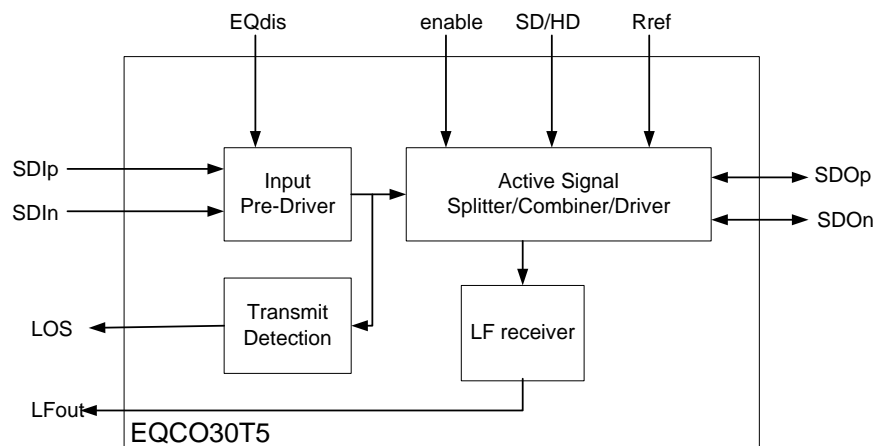


Figure 2: EQCO30T5 block diagram showing electrical connections

2.2 Package and Pinout

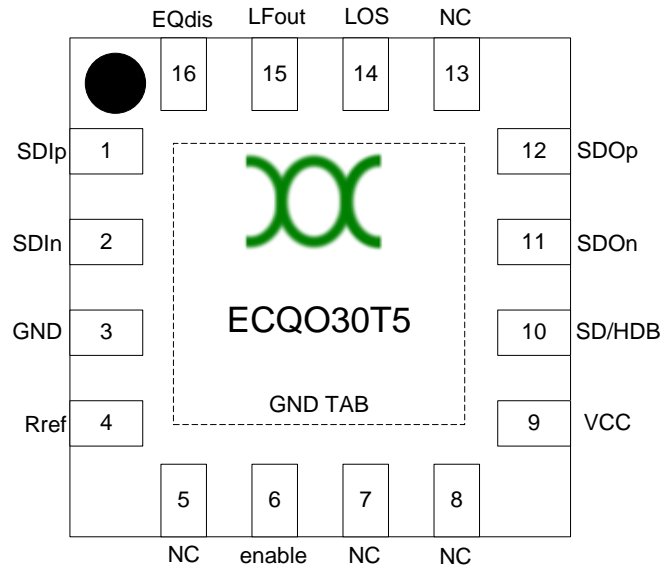


Figure 3: EQCO30T5 Pin Layout (viewed from top)

2.3 Pin Descriptions

Pin Number	Pin Name	Signal Type	Description
(TAB)	GND	Power	Use as single point Ground
1,2	SDIp,SDIn	Differential Input	Serial Input Positive/Negative Differential serial input.
3	GND	Power	Ground of power supply, connect to GND TAB
4	Rref	Analog Input	Input determining output amplitude of cable driver
9	VCC	Power	+3.3 V of power supply
6	enable	input	Enables the output driver pins
5,7,8,13	NC	input	Do not connect, leave floating. Used for internal testing.
10	SD/HDB	input	Select edge rate
11	SDOn	Driver Output	Serial Negative cable driver output. Has on chip 50 Ω serial output resistance. To be complemented with 25 Ω externally.
12	SDOp	Driver Output	Serial Positive cable driver output. Has on chip 50 Ω serial output resistance. To be complemented with 25 Ω externally.
14	LOS	output	Los of input signal
15	LFout	output	Digital output signal of the full-duplex uplink
16	EQdis	input	Disables input trace equalization

Table 1: EQCO30T5 Device Pin List



2.3.1 SDIp/SDIn

SDIp/SDIn form a differential input pair. To be AC-coupled, unless common mode is within common mode input range. When AC-coupled, the common mode gets biased to 600 mV. Internal differential 100 Ω input termination present.

2.3.2 Rref

A resistor is to be connected between Vcc and the Rref pin. A resistor of 750 Ω gives an 800 mV launch amplitude in the 75 Ω coaxial cables. A larger resistor gives a smaller amplitude.

2.3.3 Enable

When enable is floating or pulled HIGH, the output driver is enabled. When enable is LOW, the output is disabled, and the power consumption drops significantly.

2.3.4 SD/HDB

With SD/HDB set to HIGH the output rise and fall times are set for SD operation. When left floating or pulled LOW, the rise and fall times are set for 3G/HD operation.

2.3.5 SDO_n, SDO_p

The output driver is not based on a CML output stage. Both outputs operate independently, so there is very little interference between the outputs and their termination condition. There is also no LR-output network needed for achieving good return-loss. In series with the output a 25 Ω resistor is to be connected to drive a 75 Ω coax cable. The output amplitude is achieved behind this 25 Ω resistor. See application circuits at the end of the datasheet. PCBs don't require layout changes when migrating from competing cable drivers, however less components are needed. One does not need to optimize the return-loss network, since it is omitted.

2.3.6 LOS

The LOS pin indicates whether there is a valid input present at SDIp/SDIn. When HIGH, no input is detected, when LOW, input is detected.

2.3.7 LFout

LFout provides the 5 Mbps received uplink signal (LVTTTL voltage levels). It can easily drive a PCB trace of 20 pF at this speed. For longer distance communication from this pin to the next chip, the use a buffer is recommended. The output impedance is about 300 Ω .

2.3.8 EQdis

When EQdis is left Floating, or pulled LOW, the input trace equalization is turned-ON. A typical 3-dB gain at 1.5 GHz is invoked. This value is optimized for compensating the high-frequency losses of approximately 20 cm of 5-mil stripline in FR4. When pulled high, this equalization is turned-off.



3 Electrical Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under this section may cause permanent damage to the device. These are stress ratings only and are not tested. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Conditions	Min	Typ	Max	Units
Storage Temperature		-65	-	+150	°C
Ambient Temperature	Power Applied	-55	-	+125	°C
Operating Temperature	Normal Operation (VCC=1.2V±5%)	-40	-	+85	°C
Supply Voltage to Ground		-0.8	-	+3.6	V
DC Input Voltage		-0.8	-	+3.6	V
DC Voltage to Outputs		-0.8	-	+3.6	V
Current into Outputs	Outputs Low	-	-	90	mA
Electro Static Discharge (ESD) HBM	JEDEC EIA/JESD-A114A	>2.2	-	-	kV
Electro Static Discharge (ESD) contact	IEC 61000-4-2	>4	-	-	kV
Latch-Up Current		>100	-	-	mA

Table 2: Absolute Maximum Ratings

3.2 Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit
Power supply					
V _{CC}	Supply Voltage	3.15	3.3	3.45	V
I _S	Supply Current, both transmitting and receiving	-	45	-	mA
Operational bit rate					
BR _{output}	Bit rate cable driver output	0.05	-	4	Gbps
BR _{uplink}	Bit rate uplink receiver	0.5	-	5	Mbps
SDIp/SDIn Input					
ΔV _i	Input amplitude V _{SDIp,n}	2x100	-	2x900	mV
V _{CMIN}	Input common mode voltage	-	600	-	mV
R _{input}	Differential input termination	-	2x50	-	Ω
SDOp connection to Coax					
Z _{coax}	Coax Cable Characteristic Impedance	-	75	-	Ω
R _{SDOp} , R _{SDOn}	Input impedance between SDOp and VCC/GND. To get to 75, add external 25 Ω series resistor.	45	50	55	Ω
R _{loss}	Return Loss as seen on SDOp pin having 25 Ω series resistor Frequency range = 5 MHz-1.5 GHz	-	-	-15	dB
R _{loss}	Return Loss as seen on SDOp pin having 25 Ω series	-	-	-10	dB



Parameter	Description	Min	Typ	Max	Unit
	resistor Frequency range = 1.5 GHz – 3.0 GHz				
ΔV_{TX}	Transmit Amplitude with $R_{ref} = 750 \Omega$	720	800	880	mV
$t_{rise_tx_SD}$	Rise /fall time 20% to 80% of ΔV_{TX} (SD/HDB=HIGH)	400	-	800	ps
t_{rise_tx}	Rise /fall time 20% to 80% of ΔV_{TX} (SD/HDB=LOW)	-	-	65	ps
LFO Output (LVTTL like)					
t_{rise_LFO}	Rise /fall time 20% to 80% of V_{CC} for 20 pF load	-	15	-	ns

Table13: Electrical Characteristics (Over the Operating VCC and -40 to 85 °C Range)

3.3 Jitter Numbers

Parameter	Conditions	Min	Typ	Max	Units
Additive peak to peak jitter on SDOp and SDOn	Downlink signal = 3.0 Gbps	-	10	-	ps
Peak to peak jitter on LFO	0-450 m Belden1694A coax, @ low speed signal = 5 Mbps, 8B/10B, and @downlink signal= 270M, 8B/10B	-	50	-	ns

Table 14: Jitter numbers (over operating VCC range at -40 to +85 °C, and full ΔV_{TX} range)



4 Package Drawing

A 16 pin Micro Lead frame Package (MLP) also known as Quad Flat No Lead (QFN) package is used. The package outline conforms to JEDEC MO-220.

Dimensions in Figure 4 and Figure 5 are in millimeters.

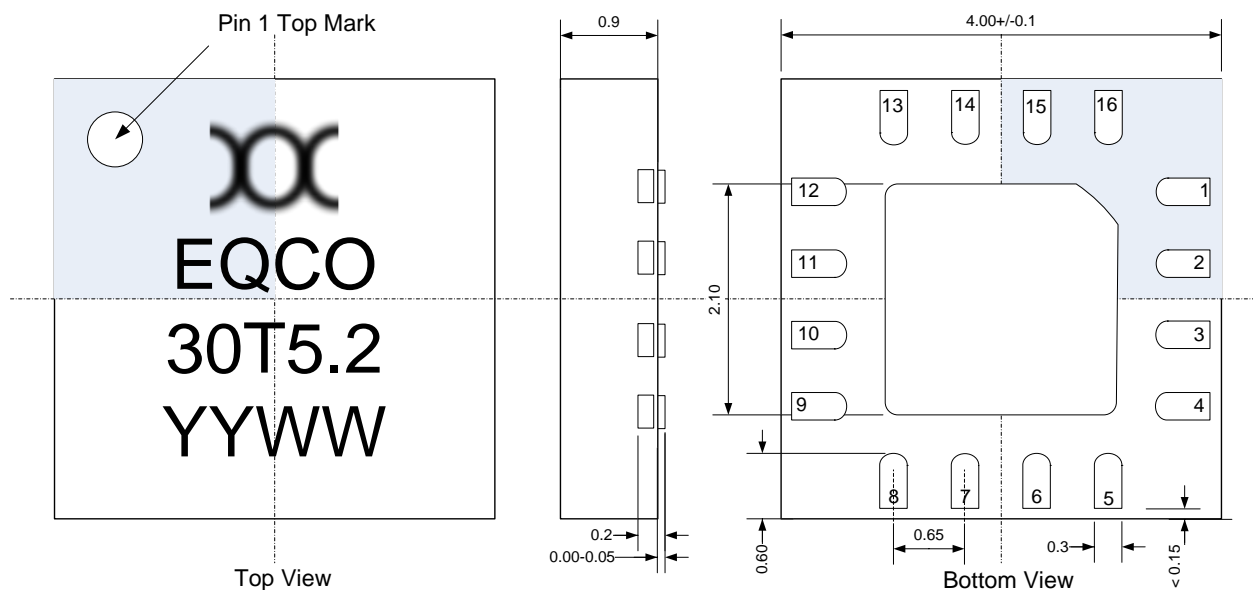


Figure 4: Package Drawing

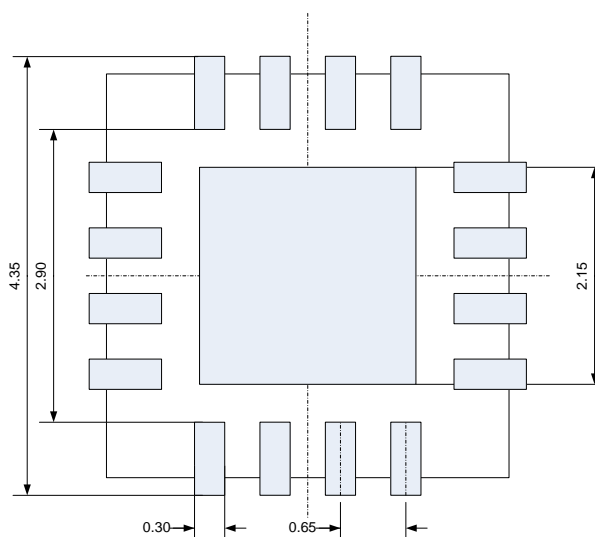


Figure 5: Recommended PCB Footprint

5 Application Information for SMPTE

5.1 Typical Application Circuit

Figure 6 illustrates a typical schematic implementation of the EQCO30T5 used as a cable driver for SMPTE video signals:

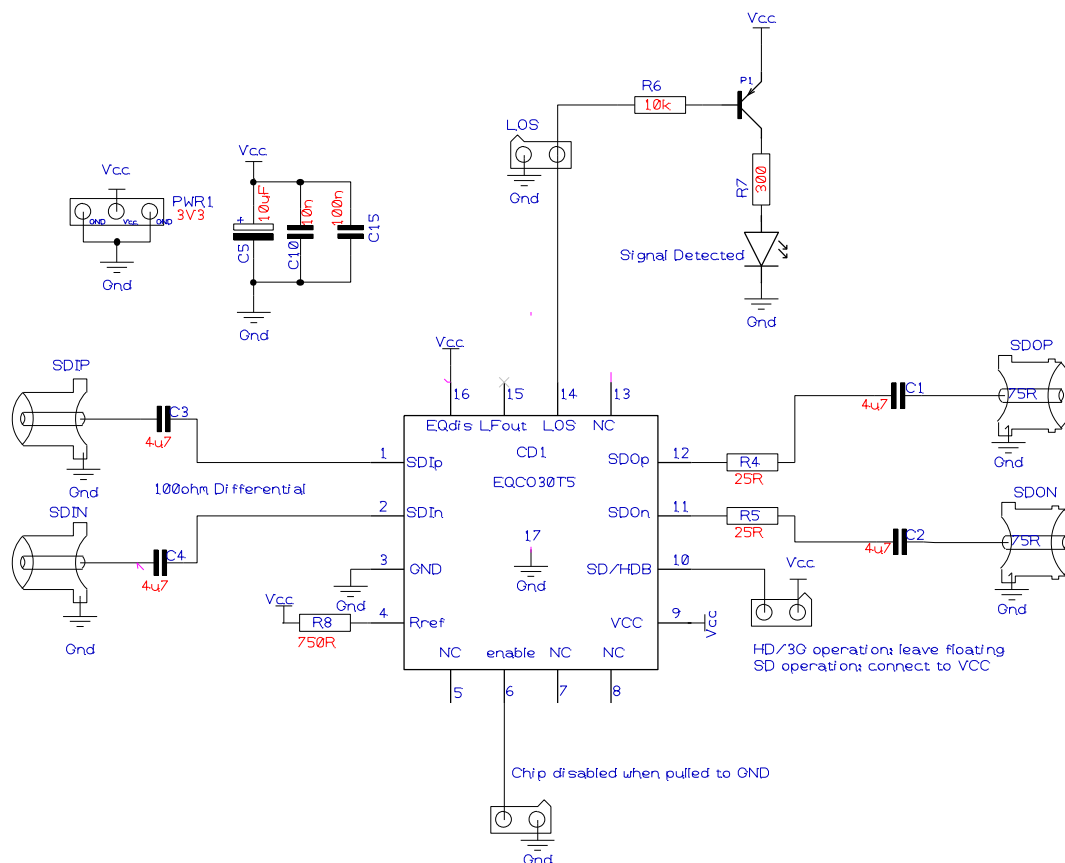


Figure 6: EQCO30T5 as SMPTE cable driver: typical application circuit

Resistors R4 and R5 are to be placed close to the pins 12 and 11 respectively. From there onwards the traces up to the coax connectors should be laid-out as 75Ω traces (including somewhere the C1 and C2 capacitors as AC-couplers).

5.1.1 Return loss network

Competing cable drivers need external RL return loss networks. The EQCO30T5 does not need these type of external networks. Figure 7 compares the output network of the EQCO30T5 with the network of competing cable drivers.

The EQCO30T5 is pin compatible with other cable drivers, but with a different component population. No termination resistor to VCC is required (do not fit =DNF). The inductor of the return loss network must not be populated and the 75 Ω resistor of this network should be replaced with a 25 Ω resistor to achieve correct operation.

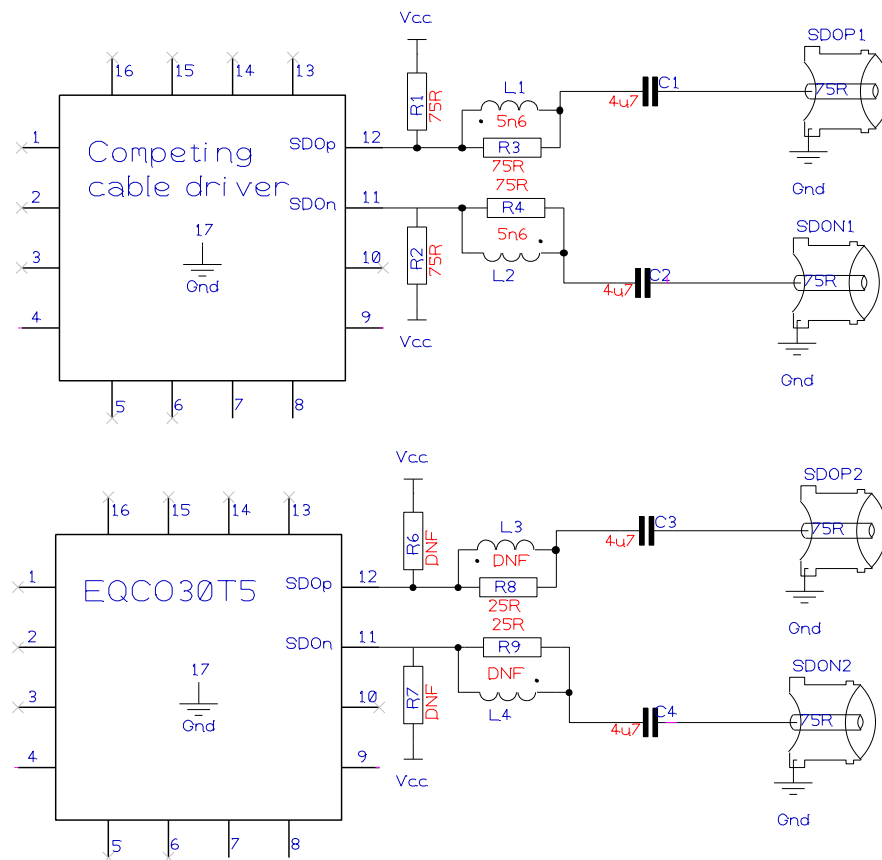


Figure 7: Comparison between EQCO30T5 and competing solutions

6 Application Information for bidirectional link

6.1 Typical Application Circuit

Figure 8 illustrates a typical schematic implementation of the EQCO30T5 [1] when used in a bidirectional link, including low speed uplink and power supply transmission over a single coax:

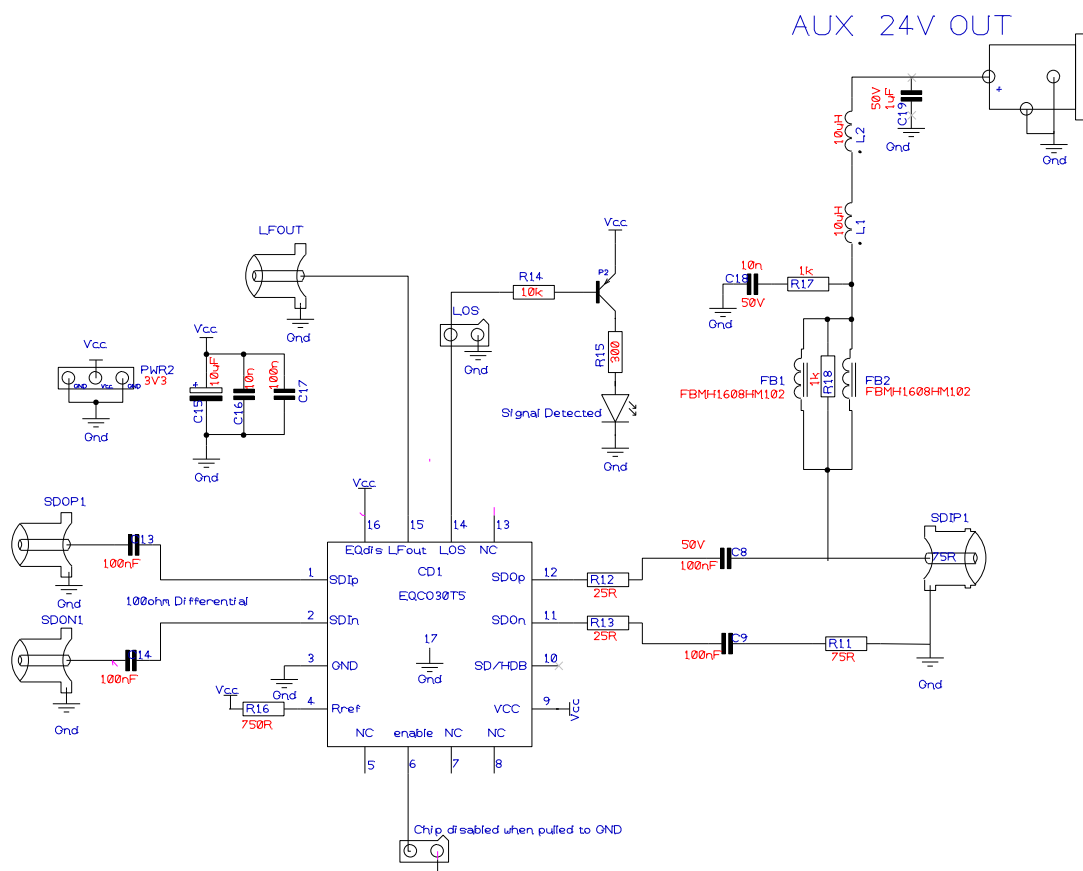


Figure 8: EQCO30T5 in bidirectional link (including power supply transmission)

Resistors R12 and R13 are to be placed close to the pins 12 and 11 respectively. From there onwards the traces up to the coax connector SDIP1 should be laid-out as 75Ω traces (including somewhere the C8 and C9 capacitors as AC-couplers). Resistor R11 has to be placed very close to this coax connector with a very short, low impedant connection between one of the shielding pins of the connector and the resistor. To get the return loss as good as in the appendix, the power and ground planes below components R12, R13, C8 and C9 should be removed (applying cut-outs).

6.1.1 Component recommendation

When using the components below, a maximum current of 900 mA can be communicated to power up the camera side. Different types of inductors may be suitable as well, allowing higher current level, however, the RF quality of the inductor has then to be checked.

Ferrite Beads Fb1, Fb2 = FBMH1608HM102 from Taiyo Yuden



Inductor L1, L2 = 1812PS_103 from Coilcraft

6.1.2 Bidirectional link in SMPTE applications

8B/10B coding is needed when the full duplex bidirectional link is used in combination with power supply transmission over the same coaxial cable.

The low speed uplink can also be used in SMPTE applications using the schematic of figure 8, however only without the inductor network (FB1, FB2, L1, L2, R18). Power supply transmission over the cable is then not longer possible. It is then also recommended to use AC coupling capacitors C8 and C9, having a value of 4.7 μ F for easy passage of pathological patterns.



7 Document Control

7.1 Version History

Version	Date	Author	Comments
2v0	27 Jan 2014	A. Peeters	Revision
1v0	13 March 2012	A. Peeters	Final Document
0v2	17 January 2012	M. Kuijk	Added Return Loss measurement
0v1	6 January 2012	B. Devuyt	New document

7.2 Document References

- [1] Patents & Patents pending: EP2247047B1, US20110103267A1, EP12153028.1, EP2648378A1 & US2013/301483A1.

7.3 Disclaimer:

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8 Appendix: Typical Return Loss Measurement

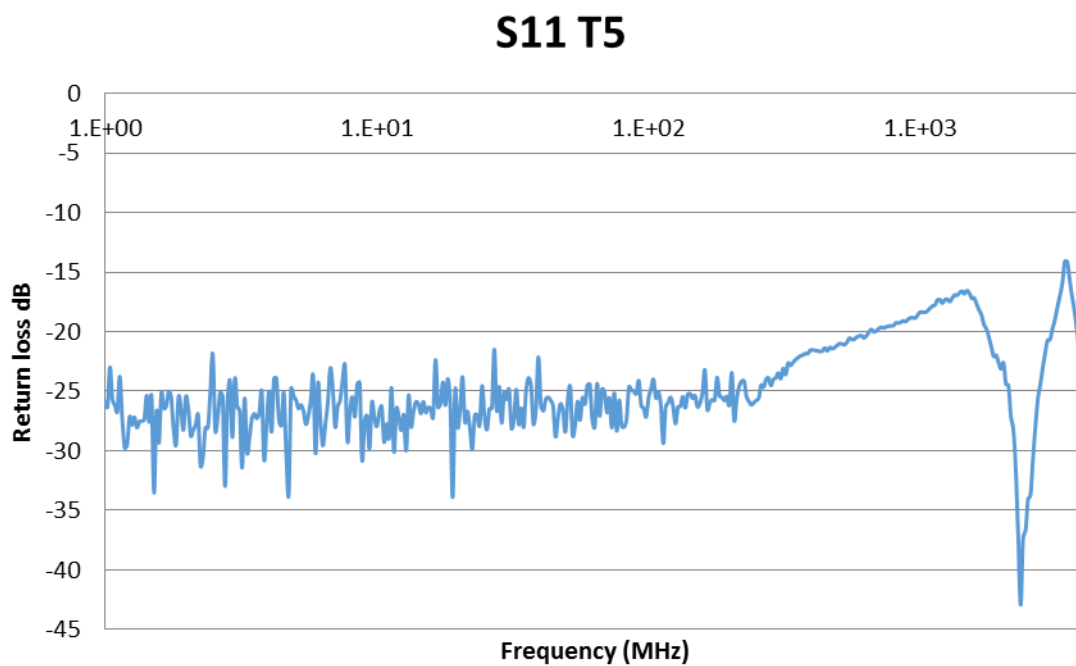


Figure 9: EQCO30T5: Typical Return Loss measurement (dB versus MHz).



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