

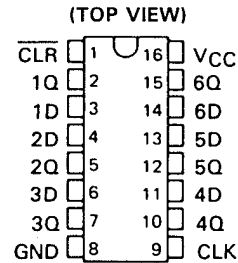
SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175, SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

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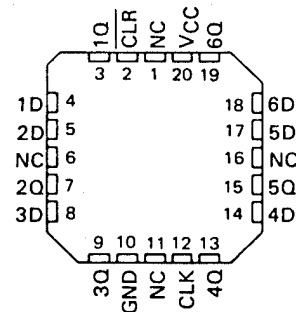
'174, 'LS174, 'S174 ... HEX D-TYPE FLIP-FLOPS
'175, 'LS175, 'S175 ... QUADRUPLE D-TYPE FLIP-FLOPS

- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators

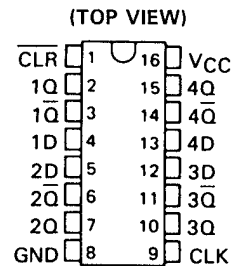
SN54174, SN54LS174, SN54S174 ... J OR W PACKAGE
SN74174 ... N PACKAGE
SN74LS174, SN74S174 ... D OR N PACKAGE



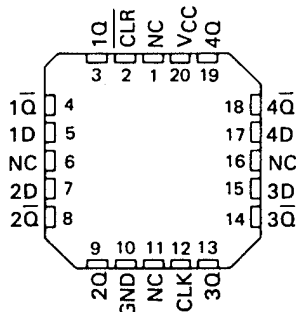
SN54LS174, SN54S174 ... FK PACKAGE
(TOP VIEW)



SN54175, SN54LS175, SN54S175 ... J OR W PACKAGE
SN74175 ... N PACKAGE
SN74LS175, SN74S175 ... D OR N PACKAGE



SN54LS175, SN54S175 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

FUNCTION TABLE
(EACH FLIP-FLOP)

| INPUTS | | | OUTPUTS | |
|--------|-------|---|----------------|-----------------|
| CLEAR | CLOCK | D | Q | Q̄† |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | Q ₀ | Q̄ ₀ |

H = high level (steady state)

L = low level (steady state)

X = irrelevant

↑ = transition from low to high level

Q₀ = the level of Q before the indicated steady-state input conditions were established.

† = '175, 'LS175, and 'S175 only

| TYPES | TYPICAL | TYPICAL |
|----------------|-----------|---------------|
| | MAXIMUM | POWER |
| | CLOCK | DISSIPATION |
| | FREQUENCY | PER FLIP-FLOP |
| '174, '175 | 35 MHz | 38 mW |
| 'LS174, 'LS175 | 40 MHz | 14 mW |
| 'S174, 'S175 | 110 MHz | 75 mW |

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

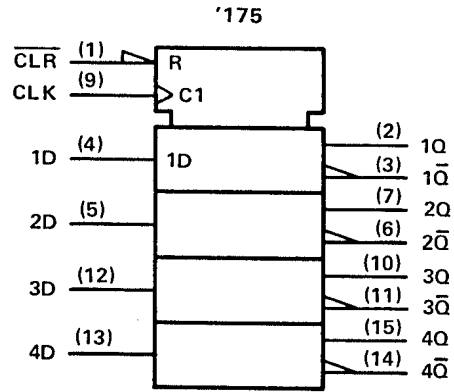
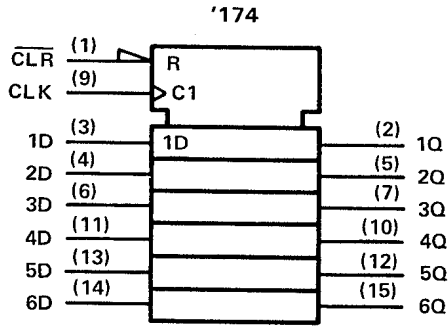
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**SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175,
SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR**

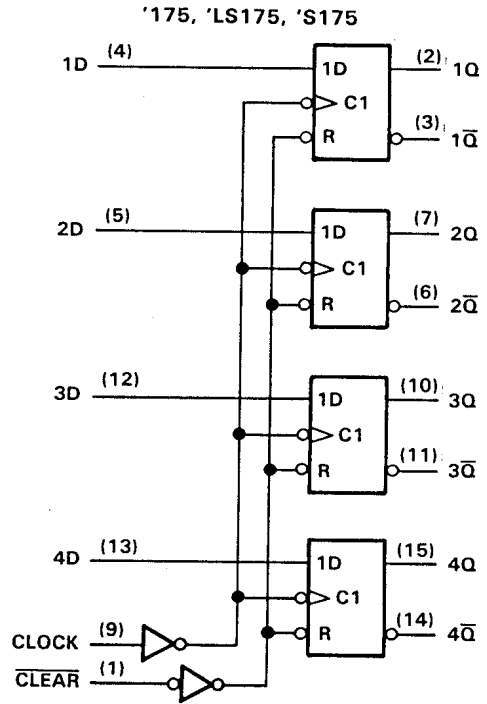
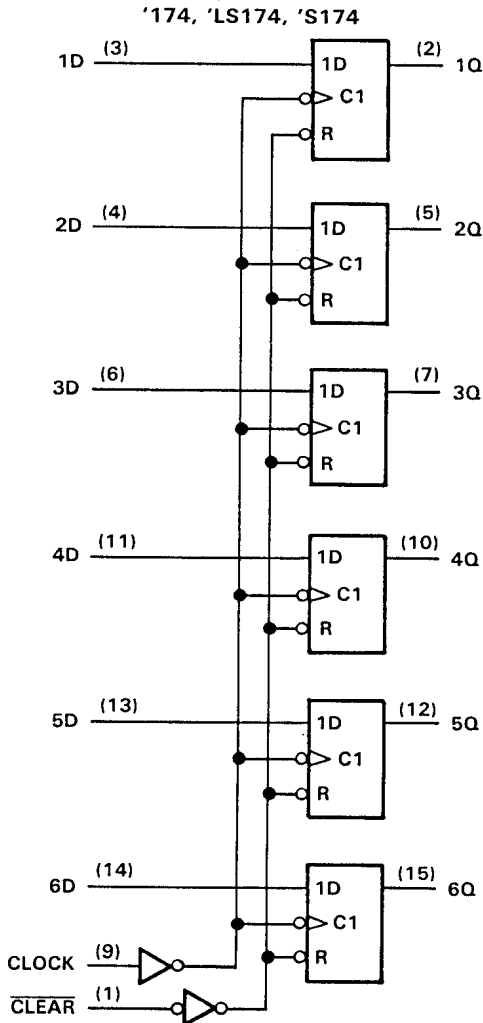
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logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

logic diagrams (positive logic)



Pin numbers shown are for D, J, N, and W packages.



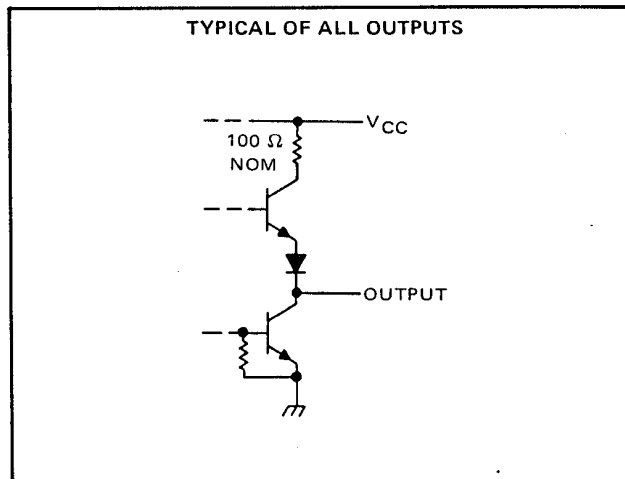
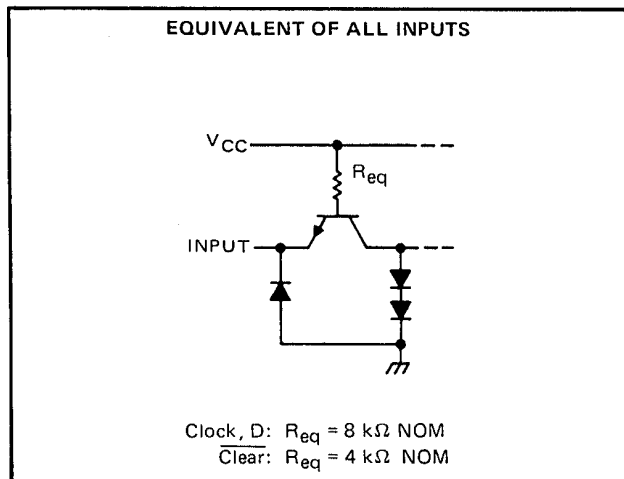
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SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175,
 SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175
 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

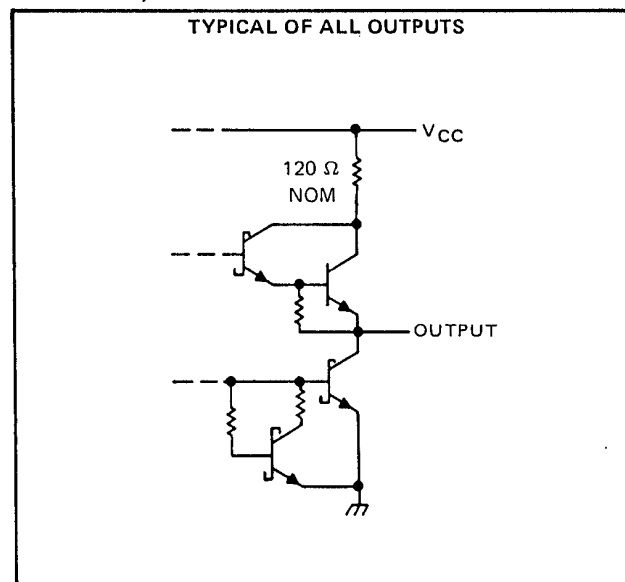
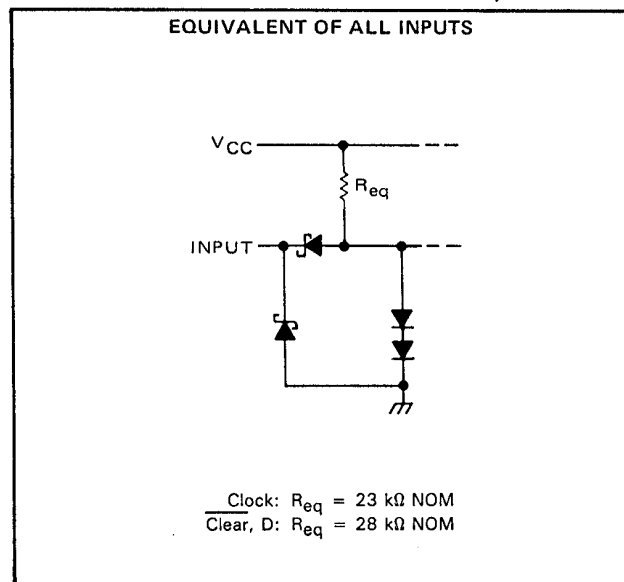
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schematics of inputs and outputs

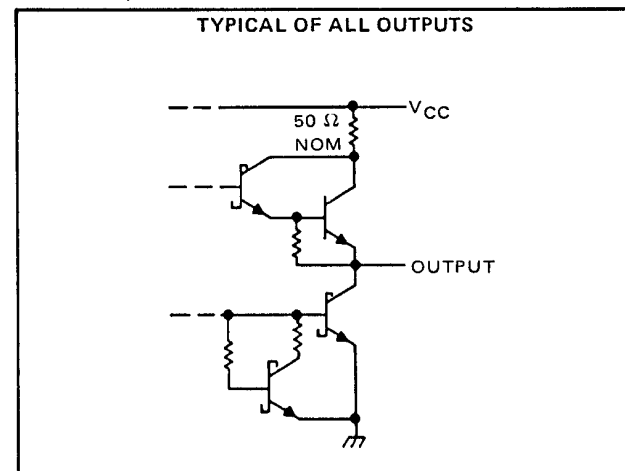
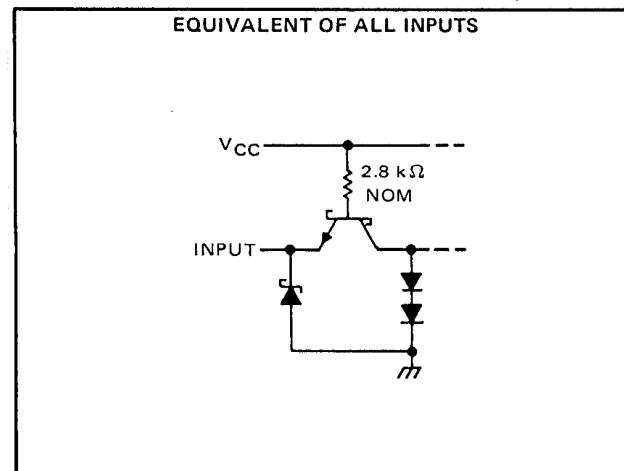
SN54174, SN54175, SN74174, SN74175



SN54LS174, SN54LS175, SN74LS174, SN74LS175



SN54S174, SN54S175, SN74S174, SN74S175



SN54174, SN54175, SN74174, SN74175 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage | 5.5 V |
| Operating free-air temperature range: SN54174, SN54175 Circuits | -55°C to 125°C |
| SN74174, SN74175 Circuits | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

| | SN54174, SN54175 | | | SN74174, SN74175 | | | UNIT | | |
|---------------------------------------|----------------------|-----|------|------------------|-----|------|---------|----|----|
| | MIN | NOM | MAX | MIN | NOM | MAX | | | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V | | |
| High-level output current, I_{OH} | | | -800 | | | -800 | μ A | | |
| Low-level output current, I_{OL} | | | 16 | | | 16 | mA | | |
| Clock frequency, f_{clock} | 0 | | 25 | 0 | | 25 | MHz | | |
| Width of clock or clear pulse, t_w | 20 | | | 20 | | | ns | | |
| Setup time, t_{su} | Data input | | | 20 | | | ns | | |
| | Clear inactive-state | | | 25 | | | ns | | |
| Data hold time, t_h | 5 | | | 5 | | | ns | | |
| Operating free-air temperature, T_A | -55 | | | 125 | | | 0 | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | MIN | TYP‡ | MAX | UNIT |
|--|--|-------|------|------|---------|
| V_{IH} High-level input voltage | | 2 | | | V |
| V_{IL} Low-level input voltage | | | | 0.8 | V |
| V_{IK} Input clamp voltage | $V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$ | | | -1.5 | V |
| V_{OH} High-level output voltage | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$ | 2.4 | 3.4 | | V |
| V_{OL} Low-level output voltage | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$ | | 0.2 | 0.4 | V |
| I_I Input current at maximum input voltage | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$ | | | 1 | mA |
| I_{IH} High-level input current | $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$ | | | 40 | μ A |
| I_{IL} Low-level input current | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$ | | | -1.6 | mA |
| I_{OS} Short-circuit output current§ | $V_{CC} = \text{MAX}$ | SN54' | -20 | -57 | mA |
| | | SN74' | -18 | -57 | |
| I_{CC} Supply current | $V_{CC} = \text{MAX},$ See Note 2 | '174 | 45 | 65 | mA |
| | | '175 | 30 | 45 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-----|-----|-----|------|
| f_{max} Maximum clock frequency | | 25 | 35 | | MHz |
| t_{PLH} Propagation delay time, low-to-high-level output from clear (SN54175, SN74175 only) | $C_L = 15 \text{ pF}, R_L = 400 \Omega,$ See Note 3 | | 16 | 25 | ns |
| t_{PHL} Propagation delay time, high-to-low-level output from clear | | | 23 | 35 | ns |
| t_{PLH} Propagation delay time, low-to-high-level output from clock | | | 20 | 30 | ns |
| t_{PHL} Propagation delay time, high-to-low-level output from clock | | | 24 | 35 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



SN54LS174, SN54LS175, SN74LS174, SN74LS175 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage | 7 V |
| Operating free-air temperature range: SN54LS174, SN54LS175 Circuits | -55°C to 125°C |
| SN74LS174, SN74LS175 Circuits | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

| | SN54LS174 SN54LS175 | | | SN74LS174 SN74LS175 | | | UNIT | | |
|---------------------------------------|------------------------|-----|------|------------------------|-----|------|---------|----|----|
| | MIN | NOM | MAX | MIN | NOM | MAX | | | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V | | |
| High-level output current, I_{OH} | | | -400 | | | -400 | μ A | | |
| Low-level output current, I_{OL} | | | 4 | | | 8 | mA | | |
| Clock frequency, f_{clock} | 0 | | 30 | 0 | | 30 | MHz | | |
| Width of clock or clear pulse, t_W | 20 | | | 20 | | | ns | | |
| Setup time, t_{su} | Data input | | | 20 | | | ns | | |
| | Clear inactive-state | | | 25 | | | ns | | |
| Data hold time, t_h | 5 | | | 5 | | | ns | | |
| Operating free-air temperature, T_A | -55 | | | 125 | | | 0 | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN54LS174 SN54LS175 | | | SN74LS174 SN74LS175 | | | UNIT | |
|--|--|-------------------------|------|-----|------------------------|------|------|---------|----|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | | |
| V_{IH} High-level input voltage | | 2 | | | 2 | | | V | |
| V_{IL} Low-level input voltage | | 0.7 | | | 0.8 | | | V | |
| V_{IK} Input clamp voltage | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$ | -1.5 | | | -1.5 | | | V | |
| V_{OH} High-level output voltage | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$ | 2.5 | 3.5 | | 2.7 | 3.5 | | V | |
| V_{OL} Low-level output voltage | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}$ | $I_{OL} = 4 \text{ mA}$ | | | 0.25 | 0.4 | 0.25 | 0.4 | V |
| | | $I_{OL} = 8 \text{ mA}$ | | | 0.35 | | | 0.5 | |
| I_I Input current at maximum input voltage | $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$ | 0.1 | | | 0.1 | | | mA | |
| I_{IH} High-level input current | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$ | 20 | | | 20 | | | μ A | |
| I_{IL} Low-level input current | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$ | -0.4 | | | -0.4 | | | mA | |
| I_{OS} Short-circuit output current § | $V_{CC} = \text{MAX}$ | -20 | -100 | | -20 | -100 | | mA | |
| I_{CC} Supply current | $V_{CC} = \text{MAX},$ See Note 2 | 'LS174 | | | 16 | 26 | 16 | 26 | mA |
| | | 'LS175 | | | 11 | 18 | 11 | 18 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | 'LS174 | | | 'LS175 | | | UNIT | |
|---|--|--------|-----|-----|--------|-----|-----|------|----|
| | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| f_{max} Maximum clock frequency | $C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega,$ See Note 3 | 30 | 40 | | 30 | 40 | | MHz | |
| t_{PLH} Propagation delay time, low-to-high-level output from clear | | | | | 20 | 30 | ns | | |
| t_{PHL} Propagation delay time, high-to-low-level output from clear | | | | | 23 | 35 | ns | | |
| t_{PLH} Propagation delay time, low-to-high-level output from clock | | | | | 20 | 30 | 13 | 25 | ns |
| t_{PHL} Propagation delay time, high-to-low-level output from clock | | | | | 21 | 30 | 16 | 25 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



SN54S174, SN54S175, SN74S174, SN74S175 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage | 5.5 V |
| Operating free-air temperature range: SN54S174, SN54S175 Circuits | -55°C to 125°C |
| SN74S174, SN74S175 Circuits | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

| | SN54S174, SN54S175 | | | SN74S174, SN74S175 | | | UNIT |
|---------------------------------------|----------------------|-----|-----|--------------------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, I_{OH} | | | -1 | | | -1 | mA |
| Low-level output current, I_{OL} | | | 20 | | | 20 | mA |
| Clock frequency, f_{clock} | 0 | | 75 | 0 | | 75 | MHz |
| Pulse width, t_w | Clock | | 7 | | | 7 | ns |
| | Clear | | 10 | | | 10 | |
| Setup time, t_{su} | Data input | | 5 | | | 5 | ns |
| | Clear inactive-state | | 5 | | | 5 | |
| Data hold time, t_h | | | 3 | | | 3 | ns |
| Operating free-air temperature, T_A | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | MIN | TYP‡ | MAX | UNIT |
|--|--|--------|------|------|------|
| V_{IH} High-level input voltage | | 2 | | | V |
| V_{IL} Low-level input voltage | | | | 0.8 | V |
| V_{IK} Input clamp voltage | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$ | | | -1.2 | V |
| V_{OH} High-level output voltage | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$ | SN54S' | 2.5 | 3.4 | V |
| | | SN74S' | 2.7 | 3.4 | |
| V_{OL} Low-level output voltage | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$ | | | 0.5 | V |
| I_I Input current at maximum input voltage | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$ | | | 1 | mA |
| I_{IH} High-level input current | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$ | | | 50 | µA |
| I_{IL} Low-level input current | $V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$ | | | -2 | mA |
| I_{OS} Short-circuit output current § | $V_{CC} = \text{MAX}$ | -40 | | -100 | mA |
| I_{CC} Supply current | $V_{CC} = \text{MAX}, \text{ See Note 2}$ | '174 | 90 | 144 | mA |
| | | '175 | 60 | 96 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----|------|-----|------|
| f_{max} Maximum clock frequency | | 75 | 110 | | MHz |
| t_{PLH} Propagation delay time, low-to-high-level \bar{Q} output from clear (SN54S175, SN74S175 only) | $C_L = 15 \text{ pF},$ $R_L = 280 \Omega,$ See Note 3 | | 10 | 15 | ns |
| t_{PHL} Propagation delay time, high-to-low-level \bar{Q} output from clear | | | 13 | 22 | ns |
| t_{PLH} Propagation delay time, low-to-high-level output from clock | | | 8 | 12 | ns |
| t_{PHL} Propagation time, high-to-low-level output from clock | | | 11.5 | 17 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| JM38510/01702BEA | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | |
| JM38510/01702BFA | OBSOLETE | CFP | W | 16 | | TBD | Call TI | Call TI | |
| JM38510/07105BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| JM38510/07105BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| JM38510/07106BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| JM38510/30106B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| JM38510/30106BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| JM38510/30106BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| JM38510/30107B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| JM38510/30107BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| JM38510/30107BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| JM38510/30107SEA | ACTIVE | CDIP | J | 16 | 25 | TBD | A42 | N / A for Pkg Type | |
| JM38510/30107SFA | ACTIVE | CFP | W | 16 | 25 | TBD | A42 | N / A for Pkg Type | |
| M38510/07105BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/07105BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/07106BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/30106B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| M38510/30106BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/30106BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/30107B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| M38510/30107BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/30107BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| M38510/30107SEA | ACTIVE | CDIP | J | 16 | 25 | TBD | A42 | N / A for Pkg Type | |
| M38510/30107SFA | ACTIVE | CFP | W | 16 | 25 | TBD | A42 | N / A for Pkg Type | |
| SN54175J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | |
| SN54LS174J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN54LS175J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN54S174J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN54S175J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN74174N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| SN74175N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | |
| SN74175N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | |
| SN74LS174D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS174DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS174DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS174DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS174DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS174DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS174J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | |
| SN74LS174N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74LS174N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | |
| SN74LS174NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74LS174NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS174NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS174NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS175D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS175DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS175DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS175DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS175DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| SN74LS175DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS175J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | |
| SN74LS175N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74LS175N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | |
| SN74LS175NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74LS175NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS175NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS175NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74S174J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | |
| SN74S174N | NRND | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74S174N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | |
| SN74S174NE4 | NRND | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74S175D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74S175DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74S175DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74S175DR | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | |
| SN74S175N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74S175N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | |
| SN74S175NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SNJ54175J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI | |
| SNJ54175W | OBSOLETE | CFP | W | 16 | | TBD | Call TI | Call TI | |
| SNJ54LS174FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54LS174J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54LS174W | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54LS175FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54LS175J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| SNJ54LS175W | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54S174FK | NRND | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54S174J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54S174W | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54S175FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54S175J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54S175W | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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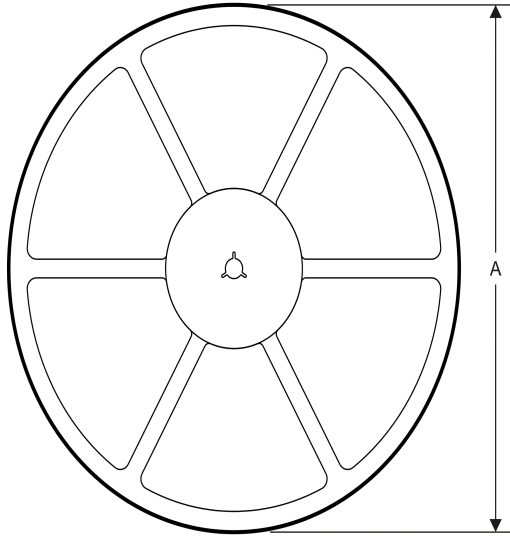
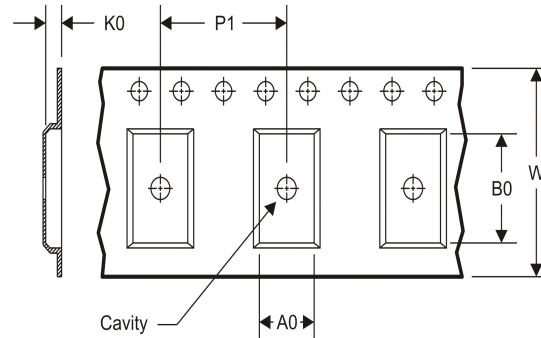
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OTHER QUALIFIED VERSIONS OF SN54175, SN54LS174, SN54LS175, SN54LS175-SP, SN54S174, SN54S175, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175 :

- Catalog: [SN74175](#), [SN74LS174](#), [SN74LS175](#), [SN54LS175](#), [SN74S174](#), [SN74S175](#)
- Military: [SN54175](#), [SN54LS174](#), [SN54LS175](#), [SN54S174](#), [SN54S175](#)
- Space: [SN54LS175-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS174DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS174NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS175DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS175NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS174DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LS174NSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LS175DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LS175NSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |

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